Transcend
Exceeding Your Expectations

TS128M~2GUSD

microSD Memory Card

Description

Transcend microSD card series are non-volatile, which means no external power is required to retain the information stored on it. Besides, it is also a solid-state device that without moving parts to skip or break down. Based on original NAND flash chip, Transcend microSD can offer an incredible combination of fast data transfer, great flexibility, excellent security and incredibly small size.

Features

- ROHS compliant product.
- Operating Voltage: 2.7 ~ 3.6V
- Operating Temperature: -25 ~ 85°C
- Durability: 10,000 insertion/removal cycles
- Fully compatible with SD card spec. v1.1
- Comply with SD Association File System Specification
- Mechanical Write Protection Switch with microSD adapter
- SD Host allows MultiMediaCard upward compatibility
- Form Factor: 11mm x 15mm x 1mm

Placement

1 2 3 4 5 6 7 8

Front   Back

Pin Definition

Pin No.	SD Mode			SPI Mode		
	Name	Type	Description	Name	Type	Description
1	DAT2	I/O/PP	Data Line [Bit2]	RSV		Reserved
2	CD/DAT3	I/O/PP	Card Detect / Data Line [Bit3]	CS	I	Chip Select
3	CMD	PP	Command / Response	DI	I	Data In
4	V_{DD}	S	Supply voltage	V_{DD}	S	Supply voltage
5	CLK	I	Clock	SCLK	I	Clock
6	V_{SS}	S	Supply voltage ground	V_{SS}	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line [Bit0]	DO	O/PP	Data out
8	DAT1	I/O/PP	Data Line [Bit1]	RSV		Reserved

S: Power Supply; I:Input; O:Output; PP:Push-Pull

Architecture
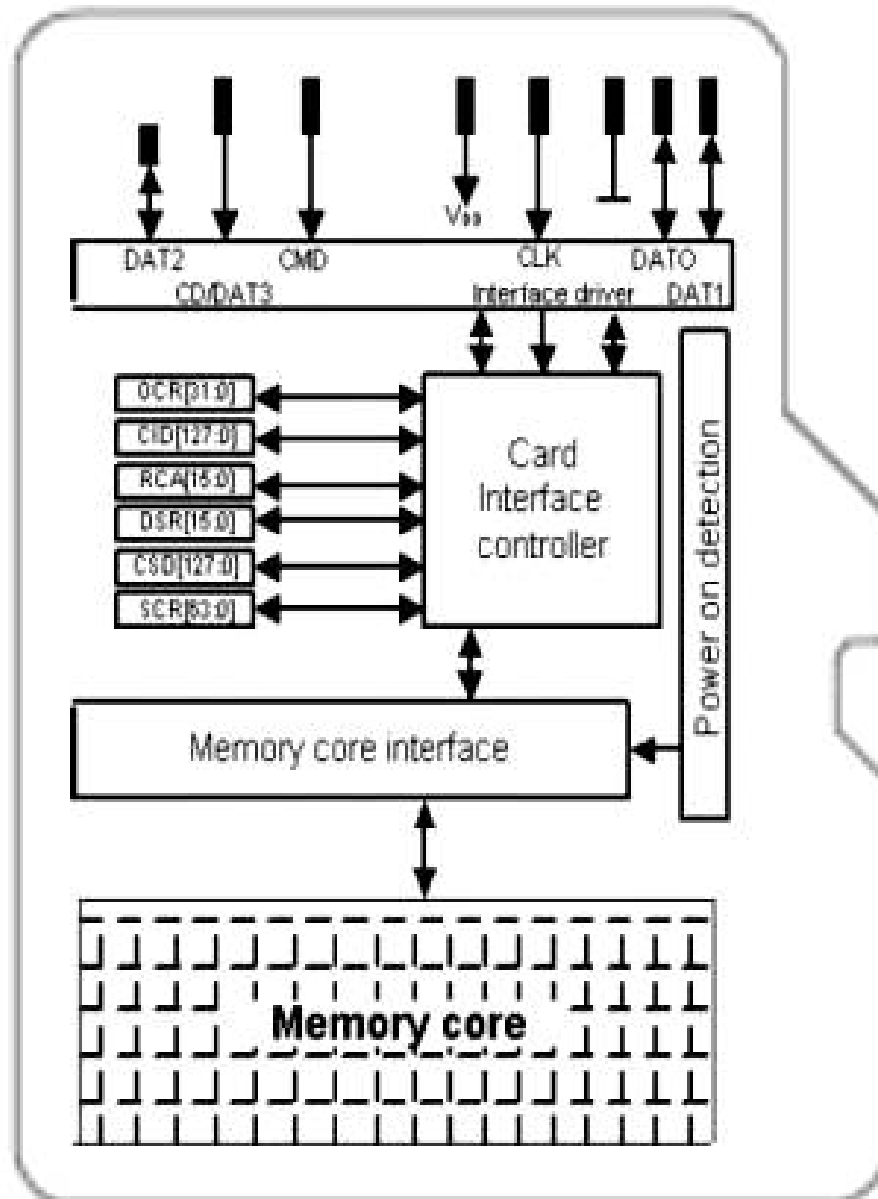
Bus Operating Conditions

• General

Parameter	Symbol	Min.	Max.	Unit	Remark
Peak voltage on all lines		-0.3	VDD+0.3	V	
All Inputs					
Input Leakage Current		-10	10	µA	
All Outputs					
Output Leakage Current		-10	10	µA	

• Power Supply Voltage

Parameter	Symbol	Min.	Max.	Unit	Remark
Supply voltage	V_{DD}	2.0	3.6	V	CMD0, 15,55,ACMD41 commands
Supply voltage specified in OCR register					Except CMD0, 15,55, ACMD41 commands
Supply voltage differentials (V_{SS1}, V_{SS2})		-0.3	0.3	V	
Power up time			250	ms	From 0v to V_{DD} Min.

Note. The current consumption of any card during the power-up procedure must not exceed 10 mA.

• Bus Signal Line Load

The total capacitance C_L the CLK line of the SD Memory Card bus is the sum of the bus master capacitance C_{HOST}, the bus capacitance C_{BUS} itself and the capacitance C_{CARD} of each card connected to this line:

$C_L = C_{HOST} + C_{BUS} + N*C_{CARD}$

Where N is the number of connected cards. Requiring the sum of the host and bus capacitances not to exceed 30 pF for up to 10 cards, and 40 pF for up to 30 cards, the following values must not be exceeded:
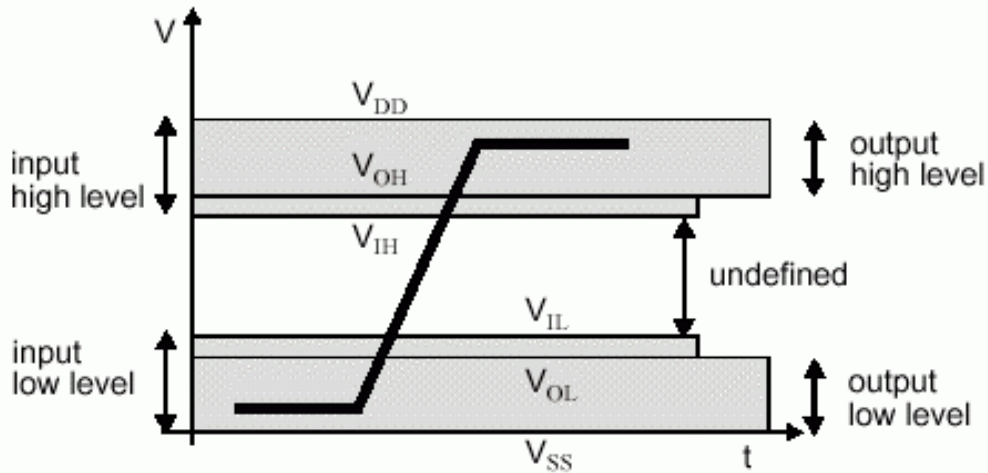
Parameter	Symbol	Min.	Max.	Unit	Remark
Bus signal line capacitance	C_L		100	pF	$f_{PP} \leq 20$ MHz, 7 cards
Single card capacitance	C_{CARD}		10	pF	
Maximum signal line inductance			16	nH	$f_{PP} \leq 20$ MHz
Pull-up resistance inside card (pin1)	R_{DAT3}	10	90	KΩ	May be used for card detection

Note that the total capacitance of CMD and DAT lines will be consist of C_{HOST}, C_{BUS} and one C_{CARD} only since they are connected separately to the SD Memory Card host.

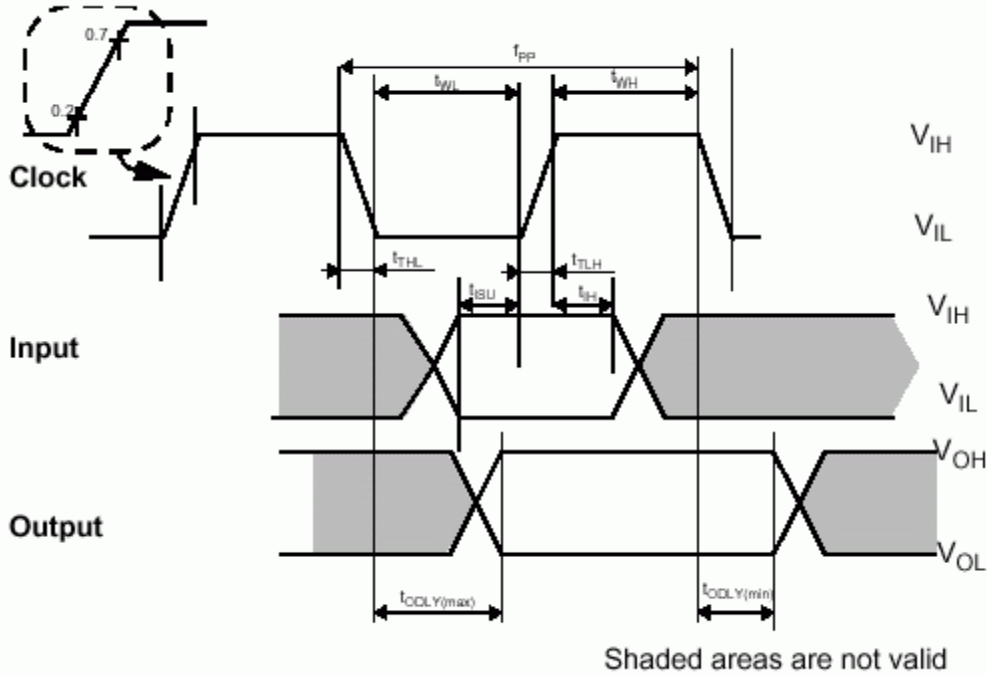| Parameter	Symbol	Min.	Max.	Unit	Remark
Pull-up resistance	R_{CMD}, R_{DAT}	10	100	KΩ	To prevent bus floating
Bus signal line capacitance	C_L		250	pF	$f_{PP} \leq 5$ MHz, 21 cards

• **Bus Signal Levels**

As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.

To meet the requirements of the JEDEC specification JESD8-1A, the card input and output voltages shall be within the following specified ranges for any V_{DD} of the allowed voltage range:

Parameter	Symbol	Min.	Max.	Unit	Remark
Output HIGH voltage	V_{OH}	$0.75* V_{DD}$		V	I_{OH} = -100 µA @V_{DD} min
Output LOW voltage	V_{OL}		$0.125* V_{DD}$	V	I_{OL} = 100 µA @V_{DD} min
Input HIGH voltage	V_{IH}	$0.625* V_{DD}$	$V_{DD} + 0.3$	V	
Input LOW voltage	V_{IL}	$V_{SS} - 0.3$	$0.25* V_{DD}$	V	

• **Bus Timing**

Shaded areas are not valid

Parameter	Symbol	Min	Max.	Unit	Remark
Clock CLK (All values are referred to min (V_{IH}) and max (V_{IL})					
Clock frequency Data Transfer Mode	f_{PP}	0	25	MHz	$C_L \le 100$ pF, (7 cards)
Clock frequency Identification Mode (The low freq. is required for MultiMediaCard compatibility.)	f_{OD}	0	400	KHz	$C_L \le 250$ pF, (21 cards)
Clock low time	t_{WL}	10		ns	$C_L \le 100$ pF, (7 cards)
		50		ns	$C_L \le 250$ pF, (21 cards)
Clock high time	t_{WH}	10		ns	$C_L \le 100$ pF, (7 cards)
		50		ns	$C_L \le 250$ pF, (21 cards)
Clock rise time	t_{TLH}		10	ns	$C_L \le 100$ pF, (7 cards)
			50	ns	$C_L \le 250$ pF, (21 cards)
Clock fall time	t_{THL}		10	ns	$C_L \le 100$ pF, (7 cards)
			50	ns	$C_L \le 250$ pF, (21 cards)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	5		ns	$C_L \le 25$ pF, (1 cards)
Input hold time	t_{IH}	5		ns	$C_L \le 25$ pF, (1 cards)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time	t_{ODLY}	0	14	ns	$C_L \le 25$ pF, (1 cards)

Reliability and Durability

Temperature	Operation: -25°C / 85°C (Target spec)
Moisture and corrosion	Operation: 25°C / 95% rel. humidity
	Storage: 40°C / 93% rel. hum./500h
	Salt Water Spray: 3% NaCl/35C; 24h acc. MIL STD Method 1009
Durability	10000 mating cycles
Bending	10N
Torque	0.10N*m , +/- 2.5deg max
Drop test	1.5m free fall
UV light exposure	UV: 254nm, 15Ws/cm² according to ISO 7816-1
Visual inspection	No warppage; no mold skin; complete form; no cavities surface smoothness <= -0.1
Shape and form	mm/cm² within contour; no cracks; no pollution (fat, oil dust, etc.)

Above technical information is based on standard data and tested to be reliable. However, Transcend makes no warranty, either expressed or implied, as to its accuracy and assumes no liability in connection with the use of this product. Transcend reserves the right to make changes in specifications at any time without prior notice.

Register Information

Within the card interface six registers are defined: OCR, CID, CSD, RCA, DSR and SCR. These can be accessed only by corresponding commands (see Chapter 4.7). The OCR, CID, CSD and SCR registers carry the card/content specific information, while the RCA and DSR registers are configuration registers storing actual configuration parameters.

1. OCR register

The 32-bit operation conditions register stores the V_{DD} voltage profile of the card. In addition, this register includes a status information bit. This status bit is set if the card power up procedure has been finished. The OCR register shall be implemented by the cards which do not support the full operating voltage range of the SD Memory Card bus, or if the card power up extends the definition in the timing diagram.

OCR bit position	VDD voltage window
0-3	reserved
4	reserved
5	reserved
6	reserved
7	reserved
8	2.0-2.1
9	2.1-2.2
10	2.2-2.3
11	2.3-2.4
12	2.4-2.5
13	2.5-2.6
14	2.6-2.7
15	2.7-2.8
16	2.8-2.9
17	2.9-3.0
18	3.0-3.1
19	3.1-3.2
20	3.2-3.3
21	3.3-3.4
22	3.4-3.5
23	3.5-3.6
24-30	reserved
31	card power up status bit (busy)1

A voltage range is not supported if the corresponding bit value is set to LOW. As long as the card is busy, the corresponding bit (31) is set to LOW.

2. CID Register

The Card IDentification (CID) register is 128 bits wide. It contains the card identification information used during the card identification phase. Every individual flash card shall have a unique identification number. The structure of the CID register is defined in the following paragraphs:

Name	Field	Width	CID-slice
Manufacturer ID	MID	8	[127:120]
OEM/Application ID	OID	16	[119:104]
Product name	PNM	40	[103:64]
Product revision	PRV	8	[63:56]
Product serial number	PSN	32	[55:24]
reserved	--	4	[23:20]
Manufacturing date	MDT	12	[19:8]
CRC7 checksum	CRC	7	[7:1]
not used, always '1'	-	1	[0:0]

• MID

An 8 bit binary number that identifies the card manufacturer. The MID number is controlled, defined and allocated to a SD Memory Card manufacturer by the SD Group. This procedure is established to ensure uniqueness of the CID register.

• OID

A 2 ASCII string characters that identifies the card OEM and/or the card contents (when used as a distribution media either on ROM or FLASH cards). The OID number is controlled, defined and allocated to a SD Memory Card manufacturer by the SD Group. This procedure is established to ensure uniqueness of the CID register.

• PNM

The product name is a string, 5 ASCII characters long.

• PRV

The product revision is composed of two Binary Coded Decimal (BCD) digits, four bits each, representing an "n.m" revision number. The "n" is the most significant nibble and "m" is the least significant nibble.
As an example, the PRV binary value field for product revision "6.2" will be: 0110 0010

• PSN

The Serial Number is 32 bits of binary number.

• MDT