



LAN8720A/LAN8720Ai

Small Footprint RMII 10/100 Ethernet Transceiver with HP Auto-MDIX Support



PRODUCT FEATURES

Datasheet

Highlights

- Single-Chip Ethernet Physical Layer Transceiver (PHY)
- Comprehensive flexPWR[®] Technology
 - Flexible Power Management Architecture
 - LVCMOS Variable I/O voltage range: +1.6V to +3.6V
 - Integrated 1.2V regulator
- HP Auto-MDIX support
- Miniature 24-pin QFN lead-free RoHS compliant package (4 x 4 x 0.85mm height).

Target Applications

- Set-Top Boxes
- Networked Printers and Servers
- Test Instrumentation
- LAN on Motherboard
- Embedded Telecom Applications
- Video Record/Playback Systems
- Cable Modems/Routers
- DSL Modems/Routers
- Digital Video Recorders
- IP and Video Phones
- Wireless Access Points
- Digital Televisions
- Digital Media Adaptors/Servers
- Gaming Consoles
- POE Applications (Refer to SMSC Application Note 17.18)

Key Benefits

- High-Performance 10/100 Ethernet Transceiver
 - Compliant with IEEE802.3/802.3u (Fast Ethernet)
 - Compliant with ISO 802-3/IEEE 802.3 (10BASE-T)
 - Loop-back modes
 - Auto-negotiation
 - Automatic polarity detection and correction
 - Link status change wake-up detection
 - Vendor specific register functions
 - Supports the reduced pin count RMII interface
- Power and I/Os
 - Various low power modes
 - Integrated power-on reset circuit
 - Two status LED outputs
 - Latch-Up Performance Exceeds 150mA per EIA/JESD 78, Class II
 - May be used with a single 3.3V supply
- Additional Features
 - Ability to use a low cost 25Mhz crystal for reduced BOM
- Packaging
 - 24-pin QFN (4x4 mm) Lead-Free RoHS Compliant package with RMII
- Environmental
 - Extended commercial temperature range (0°C to +85°C)
 - Industrial temperature range version available (-40°C to +85°C)

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Order Numbers:

LAN8720A-CP-TR for 24-pin QFN lead-free RoHS compliant package (0 to +85°C temp)

LAN8720Ai-CP-TR for 24-pin QFN lead-free RoHS compliant package (-40 to +85°C temp)

Reel size is 4,000.

This product meets the halogen maximum concentration values per IEC61249-2-21

For RoHS compliance and environmental information, please visit www.smSC.com/rohs

Please contact your SMSC sales representative for additional documentation related to this product such as application notes, anomaly sheets, and design guidelines.

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Chapter 1 Introduction

1.1 General Terms and Conventions

The following is list of the general terms used throughout this document:

BYTE	8-bits
FIFO	First In First Out buffer; often used for elasticity buffer
MAC	Media Access Controller
RMII™	Reduced Media Independent Interface™
N/A	Not Applicable
X	Indicates that a logic state is “don’t care” or undefined.
RESERVED	Refers to a reserved bit field or address. Unless otherwise noted, reserved bits must always be zero for write operations. Unless otherwise noted, values are not guaranteed when reading reserved bits. Unless otherwise noted, do not read or write to reserved addresses.
SMI	Serial Management Interface

1.2 General Description

The LAN8720A/LAN8720Ai is a low-power 10BASE-T/100BASE-TX physical layer (PHY) transceiver with variable I/O voltage that is compliant with the IEEE 802.3-2005 standards.

The LAN8720A/LAN8720Ai supports communication with an Ethernet MAC via a standard RMII interface. It contains a full-duplex 10-BASE-T/100BASE-TX transceiver and supports 10Mbps (10BASE-T) and 100Mbps (100BASE-TX) operation. The LAN8720A/LAN8720Ai implements auto-negotiation to automatically determine the best possible speed and duplex mode of operation. HP Auto-MDIX support allows the use of direct connect or cross-over LAN cables.

The LAN8720A/LAN8720Ai supports both IEEE 802.3-2005 compliant and vendor-specific register functions. However, no register access is required for operation. The initial configuration may be selected via the configuration pins as described in [Section 3.7, "Configuration Straps," on page 31](#). Register-selectable configuration options may be used to further define the functionality of the transceiver.

Per IEEE 802.3-2005 standards, all digital interface pins are tolerant to 3.6V. The device can be configured to operate on a single 3.3V supply utilizing an integrated 3.3V to 1.2V linear regulator. The linear regulator may be optionally disabled, allowing usage of a high efficiency external regulator for lower system power dissipation.

The LAN8720A/LAN8720Ai is available in both extended commercial and industrial temperature range versions. A typical system application is shown in [Figure 1.1](#).

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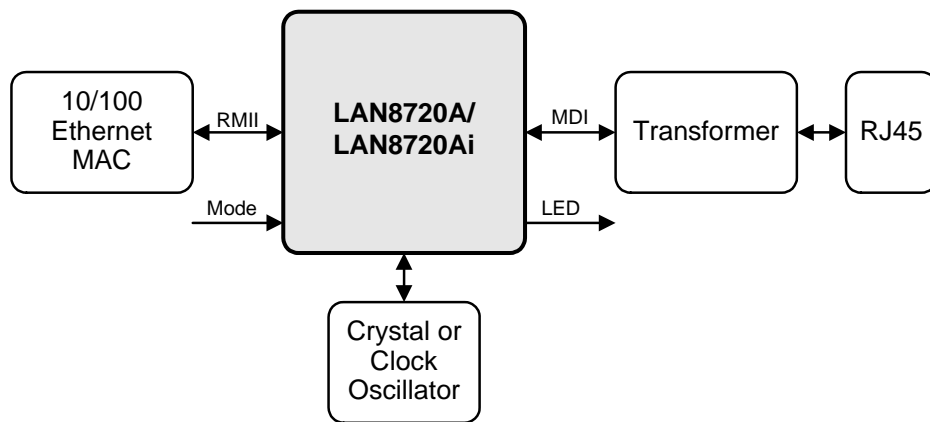


Figure 1.1 System Block Diagram

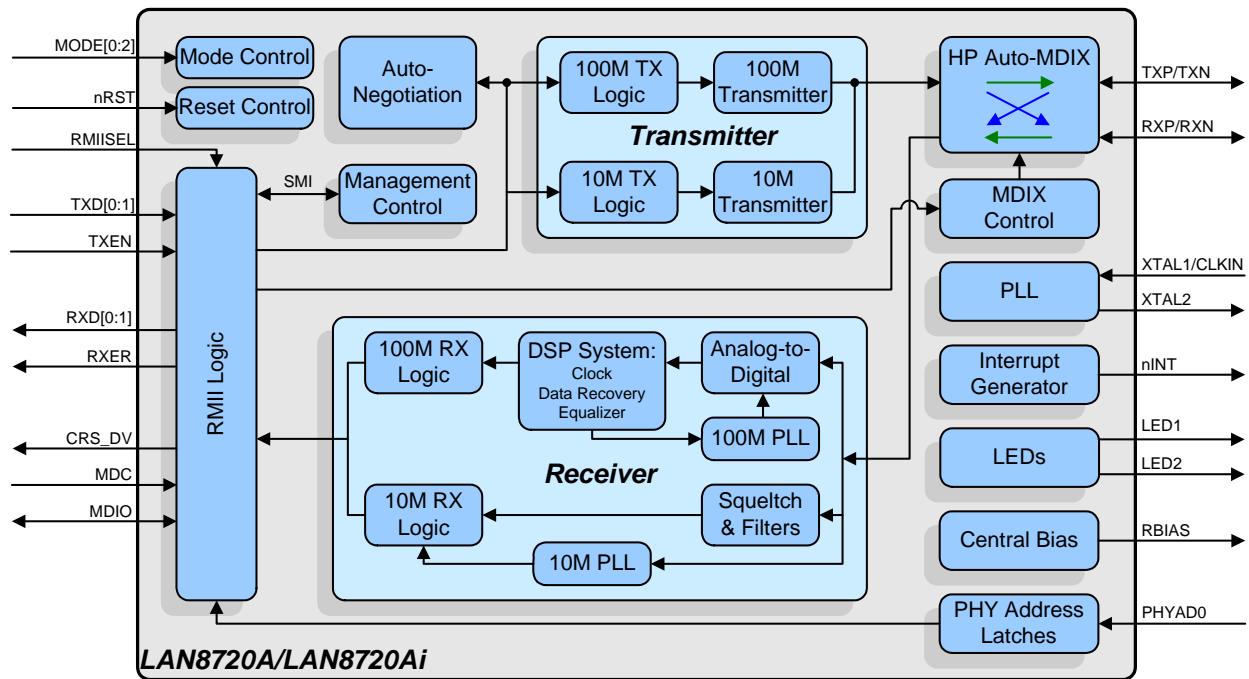
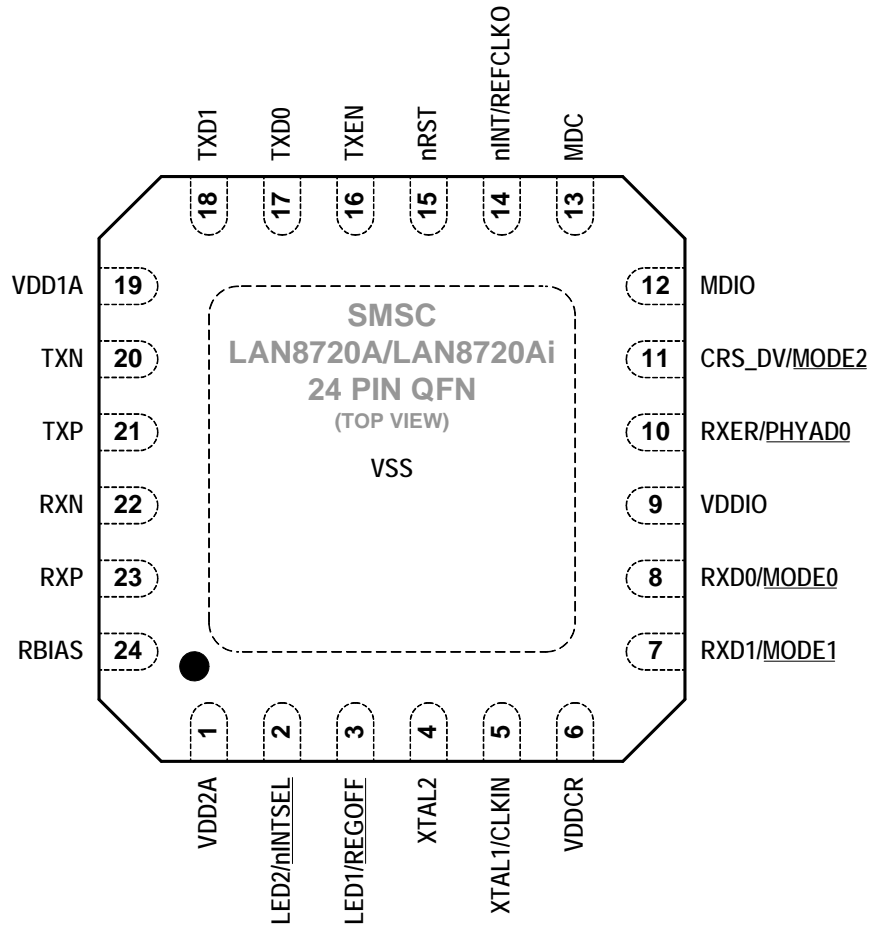


Figure 1.2 Architectural Overview

Chapter 2 Pin Description and Configuration



NOTE: Exposed pad (VSS) on bottom of package must be connected to ground

Figure 2.1 24-QFN Pin Assignments (TOP VIEW)

Note: When a lower case “n” is used at the beginning of the signal name, it indicates that the signal is active low. For example, nRST indicates that the reset signal is active low.

Note: The buffer type for each signal is indicated in the BUFFER TYPE column. A description of the buffer types is provided in [Section 2.2](#).

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Table 2.1 RMII Signals

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Transmit Data 0	TXD0	VIS	The MAC transmits data to the transceiver using this signal.
1	Transmit Data 1	TXD1	VIS	The MAC transmits data to the transceiver using this signal.
1	Transmit Enable	TXEN	VIS (PD)	Indicates that valid transmission data is present on TXD[1:0].
1	Receive Data 0	RXD0	VO8	Bit 0 of the 2 data bits that are sent by the transceiver on the receive path.
	PHY Operating Mode 0 Configuration Strap	<u>MODE0</u>	VIS (PU)	Combined with MODE1 and MODE2, this configuration strap sets the default PHY mode. See Note 2.1 for more information on configuration straps. Note: Refer to Section 3.7.2, "MODE[2:0]: Mode Configuration," on page 31 for additional details.
1	Receive Data 1	RXD1	VO8	Bit 1 of the 2 data bits that are sent by the transceiver on the receive path.
	PHY Operating Mode 1 Configuration Strap	<u>MODE1</u>	VIS (PU)	Combined with MODE0 and MODE2, this configuration strap sets the default PHY mode. See Note 2.1 for more information on configuration straps. Note: Refer to Section 3.7.2, "MODE[2:0]: Mode Configuration," on page 31 for additional details.
1	Receive Error	RXER	VO8	This signal is asserted to indicate that an error was detected somewhere in the frame presently being transferred from the transceiver.
	PHY Address 0 Configuration Strap	<u>PHYAD0</u>	VIS (PD)	This configuration strap sets the transceiver's SMI address. See Note 2.1 for more information on configuration straps. Note: Refer to Section 3.7.1, "PHYAD[0]: PHY Address Configuration," on page 31 for additional information.

Table 2.1 RMII Signals (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Carrier Sense / Receive Data Valid	CRS_DV	VO8	This signal is asserted to indicate the receive medium is non-idle. When a 10BASE-T packet is received, CRS_DV is asserted, but RXD[1:0] is held low until the SFD byte (10101011) is received. Note: Per the RMII standard, transmitted data is not looped back onto the receive data pins in 10BASE-T half-duplex mode.
	PHY Operating Mode 2 Configuration Strap	<u>MODE2</u>	VIS (PU)	Combined with MODE0 and MODE1, this configuration strap sets the default PHY mode. See Note 2.1 for more information on configuration straps. Note: Refer to Section 3.7.2, "MODE[2:0]: Mode Configuration," on page 31 for additional details.

Note 2.1 Configuration strap values are latched on power-on reset and system reset. Configuration straps are identified by an underlined symbol name. Signals that function as configuration straps must be augmented with an external resistor when connected to a load. Refer to [Section 3.7, "Configuration Straps,"](#) on page 31 for additional information.

Table 2.2 LED Pins

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	LED 1	LED1	O12	Link activity LED Indication. This pin is driven active when a valid link is detected and blinks when activity is detected. Note: Refer to Section 3.8.1, "LEDs," on page 37 for additional LED information.
	Regulator Off Configuration Strap	<u>REGOFF</u>	IS (PD)	This configuration strap is used to disable the internal 1.2V regulator. When the regulator is disabled, external 1.2V must be supplied to VDDCR. <ul style="list-style-type: none">■ When <u>REGOFF</u> is pulled high to VDD2A with an external resistor, the internal regulator is disabled.■ When <u>REGOFF</u> is floating or pulled low, the internal regulator is enabled (default). See Note 2.2 for more information on configuration straps. Note: Refer to Section 3.7.3, "REGOFF: Internal +1.2V Regulator Configuration," on page 32 for additional details.

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Table 2.2 LED Pins (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
	LED 2	LED2	O12	Link Speed LED Indication. This pin is driven active when the operating speed is 100Mbps. It is inactive when the operating speed is 10Mbps or during line isolation. Note: Refer to Section 3.8.1, "LEDs," on page 37 for additional LED information.
1	nINT/ REFCLKO Function Select Configuration Strap	<u>nINTSEL</u>	IS (PU)	This configuration strap selects the mode of the nINT/REFCLKO pin. <ul style="list-style-type: none"> ■ When <u>nINTSEL</u> is floated or pulled to VDD2A, nINT is selected for operation on the nINT/REFCLKO pin (default). ■ When <u>nINTSEL</u> is pulled low to VSS, REFCLKO is selected for operation on the nINT/REFCLKO pin. See Note 2.2 for more information on configuration straps. Note: Refer to See Section 3.8.1.2, "nINTSEL and LED2 Polarity Selection," on page 37 for additional information.

Note 2.2 Configuration strap values are latched on power-on reset and system reset. Configuration straps are identified by an underlined symbol name. Signals that function as configuration straps must be augmented with an external resistor when connected to a load. Refer to [Section 3.7, "Configuration Straps,"](#) on [page 31](#) for additional information.

Table 2.3 Serial Management Interface (SMI) Pins

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	SMI Data Input/Output	MDIO	VIS/ VOD8	Serial Management Interface data input/output
1	SMI Clock	MDC	VIS	Serial Management Interface clock

Table 2.4 Ethernet Pins

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Ethernet TX/RX Positive Channel 1	TXP	AIO	Transmit/Receive Positive Channel 1
1	Ethernet TX/RX Negative Channel 1	TXN	AIO	Transmit/Receive Negative Channel 1

Table 2.4 Ethernet Pins (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Ethernet TX/RX Positive Channel 2	RXP	AIO	Transmit/Receive Positive Channel 2
1	Ethernet TX/RX Negative Channel 2	RXN	AIO	Transmit/Receive Negative Channel 2

Table 2.5 Miscellaneous Pins

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	External Crystal Input	XTAL1	ICLK	External crystal input
	External Clock Input	CLKIN	ICLK	Single-ended clock oscillator input. Note: When using a single ended clock oscillator, XTAL2 should be left unconnected.
1	External Crystal Output	XTAL2	OCLK	External crystal output
1	External Reset	nRST	VIS (PU)	System reset. This signal is active low.
1	Interrupt Output	nINT	VOD8 (PU)	Active low interrupt output. Place an external resistor pull-up to VDDIO. Note: Refer to Section 3.6, "Interrupt Management," on page 29 for additional details on device interrupts. Note: Refer to Section 3.8.1.2, "nINTSEL and LED2 Polarity Selection," on page 37 for details on how the <u>nINTSEL</u> configuration strap is used to determine the function of this pin.
	Reference Clock Output	REFCLKO	VO8	This optional 50MHz clock output is derived from the 25MHz crystal oscillator. REFCLKO is selectable via the <u>nINTSEL</u> configuration strap. Note: Refer Section 3.7.4.2, "REF_CLK Out Mode," on page 34 for additional details. Note: Refer to Section 3.8.1.2, "nINTSEL and LED2 Polarity Selection," on page 37 for details on how the <u>nINTSEL</u> configuration strap is used to determine the function of this pin.

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Table 2.6 Analog Reference Pins

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	External 1% Bias Resistor Input	RBIAS	AI	<p>This pin requires connection of a 12.1k ohm (1%) resistor to ground.</p> <p>Refer to the LAN8720A/LAN8720Ai reference schematic for connection information.</p> <p>Note: The nominal voltage is 1.2V and the resistor will dissipate approximately 1mW of power.</p>

Table 2.7 Power Pins

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	+1.6V to +3.6V Variable I/O Power	VDDIO	P	<p>+1.6V to +3.6V variable I/O power</p> <p>Refer to the LAN8720A/LAN8720Ai reference schematic for connection information.</p>
1	+1.2V Digital Core Power Supply	VDDCR	P	<p>Supplied by the on-chip regulator unless configured for regulator off mode via the <u>REGOFF</u> configuration strap.</p> <p>Refer to the LAN8720A/LAN8720Ai reference schematic for connection information.</p> <p>Note: 1 uF and 470 pF decoupling capacitors in parallel to ground should be used on this pin.</p>
1	+3.3V Channel 1 Analog Port Power	VDD1A	P	<p>+3.3V Analog Port Power to Channel 1</p> <p>Refer to the LAN8720A/LAN8720Ai reference schematic for connection information.</p>
1	+3.3V Channel 2 Analog Port Power	VDD2A	P	<p>+3.3V Analog Port Power to Channel 2 and the internal regulator.</p> <p>Refer to the LAN8720A/LAN8720Ai reference schematic for connection information.</p>
1	Ground	VSS	P	<p>Common ground. This exposed pad must be connected to the ground plane with a via array.</p>

2.1 Pin Assignments

Table 2.8 24-QFN Package Pin Assignments

PIN NUM	PIN NAME	PIN NUM	PIN NAME
1	VDD2A	13	MDC
2	LED2/ <u>nINTSEL</u>	14	nINT/REFCLKO
3	LED1/ <u>REGOFF</u>	15	nRST
4	XTAL2	16	TXEN
5	XTAL1/CLKIN	17	TXD0
6	VDDCR	18	TXD1
7	RXD1/ <u>MODE1</u>	19	VDD1A
8	RXD0/ <u>MODE0</u>	20	TXN
9	VDDIO	21	TXP
10	RXER/ <u>PHYAD0</u>	22	RXN
11	CRS_DV/ <u>MODE2</u>	23	RXP
12	MDIO	24	RBIAS

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2.2 Buffer Types

Table 2.9 Buffer Types

BUFFER TYPE	DESCRIPTION
IS	Schmitt-triggered input
O12	Output with 12mA sink and 12mA source
VIS	Variable voltage Schmitt-triggered input
VO8	Variable voltage output with 8mA sink and 8mA source
VOD8	Variable voltage open-drain output with 8mA sink
PU	50uA (typical) internal pull-up. Unless otherwise noted in the pin description, internal pull-ups are always enabled. Note: Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added.
PD	50uA (typical) internal pull-down. Unless otherwise noted in the pin description, internal pull-downs are always enabled. Note: Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled low, an external resistor must be added.
AI	Analog input
AIO	Analog bi-directional
ICLK	Crystal oscillator input pin
OCLK	Crystal oscillator output pin
P	Power pin

Note: The digital signals are not 5V tolerant. Refer to [Section 5.1, "Absolute Maximum Ratings*,"](#) on [page 63](#) for additional buffer information.

Note 2.3 Sink and source capabilities are dependant on the VDDIO voltage. Refer to [Section 5.1, "Absolute Maximum Ratings*,"](#) on [page 63](#) for additional information.