

SN55110A, SN75110A, SN75112 DUAL LINE DRIVERS

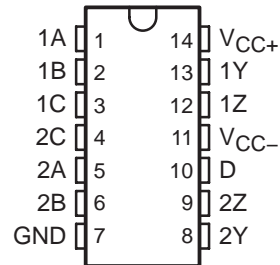
SLLS106G – DECEMBER 1975 – REVISED NOVEMBER 2004

- Improved Stability Over Supply Voltage and Temperature Ranges
- Constant-Current Outputs
- High Speed
- Standard Supply Voltages
- High Output Impedance
- High Common-Mode Output Voltage Range
... -3 V to 10 V
- TTL-Input Compatibility
- Inhibitor Available for Driver Selection
- Glitch Free During Power Up/Power Down
- SN75112 and External Circuit Meets or Exceeds the Requirements of CCITT Recommendation V.35

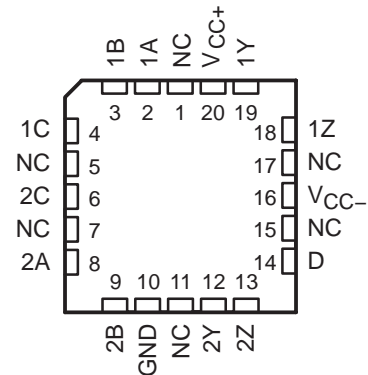
description/ordering information

The SN55110A, SN75110A, and SN75112 dual line drivers have improved output current regulation with supply-voltage and temperature variations. In addition, the higher current of the SN75112 (27 mA) allows data to be transmitted over longer lines. These drivers offer optimum performance when used with the SN55107A, SN75107A, and SN75108A line receivers.

SN55110A ... J OR W PACKAGE
SN75110A ... D, N, OR NS PACKAGE
SN75112 ... D OR N PACKAGE
(TOP VIEW)



SN55110A ... FK PACKAGE
(TOP VIEW)



NC – No internal connection

ORDERING INFORMATION

| TA | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|--------------|--------------|-----------------------|------------------|
| 0°C to 70°C | PDIP (N) | Tube of 25 | SN75110AN | SN75110AN |
| | | Tube of 50 | SN75112N | SN75112N |
| | SOIC (D) | Reel of 2500 | SN75110AD | SN75110A |
| | | Tube of 50 | SN75112D | |
| | | Reel of 2500 | SN75112DR | SN75112 |
| | | Tube of 50 | SN75110ADR | |
| SOP (NS) | Reel of 2000 | SN75110ANSR | SN75110A | |
| -55°C to 125°C | CDIP (J) | Tube of 25 | SN55110AJ | SN55110AJ |
| | | Tube of 150 | SNJ55110AJ | SNJ55110AJ |
| | CFP (W) | Tube of 150 | SNJ55110AW | SNJ55110AW |
| | LCCC (FK) | Tube of 55 | SNJ55110AFK | SNJ55110AFK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2004, Texas Instruments Incorporated
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN55110A, SN75110A, SN75112 DUAL LINE DRIVERS

SLLS106G – DECEMBER 1975 – REVISED NOVEMBER 2004

description/ordering information (continued)

These drivers feature independent channels with common voltage supply and ground terminals. The significant difference between the three drivers is in the output-current specification. The driver circuits feature a constant output current that is switched to either of two output terminals by the appropriate logic levels at the input terminals. The output current can be switched off (inhibited) by low logic levels on the enable inputs. The output current nominally is 12 mA for the '110A devices and is 27 mA for the SN75112.

The enable/inhibit feature is provided so the circuits can be used in party-line or data-bus applications. A strobe or inhibitor (enable D), common to both drivers, is included for increased driver-logic versatility. The output current in the inhibited mode, $I_{O(off)}$, is specified so that minimum line loading is induced when the driver is used in a party-line system with other drivers. The output impedance of the driver in the inhibited mode is very high. The output impedance of a transistor is biased to cutoff.

The driver outputs have a common-mode voltage range of -3 V to 10 V , allowing common-mode voltage on the line without affecting driver performance.

All inputs are diode clamped and are designed to satisfy TTL-system requirements. The inputs are tested at 2 V for high-logic-level input conditions and 0.8 V for low-logic-level input conditions. These tests ensure 400-mV noise margin when interfaced with TTL Series 54/74 devices.

The SN55110A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN75110A and SN75112 are characterized for operation from 0°C to 70°C .

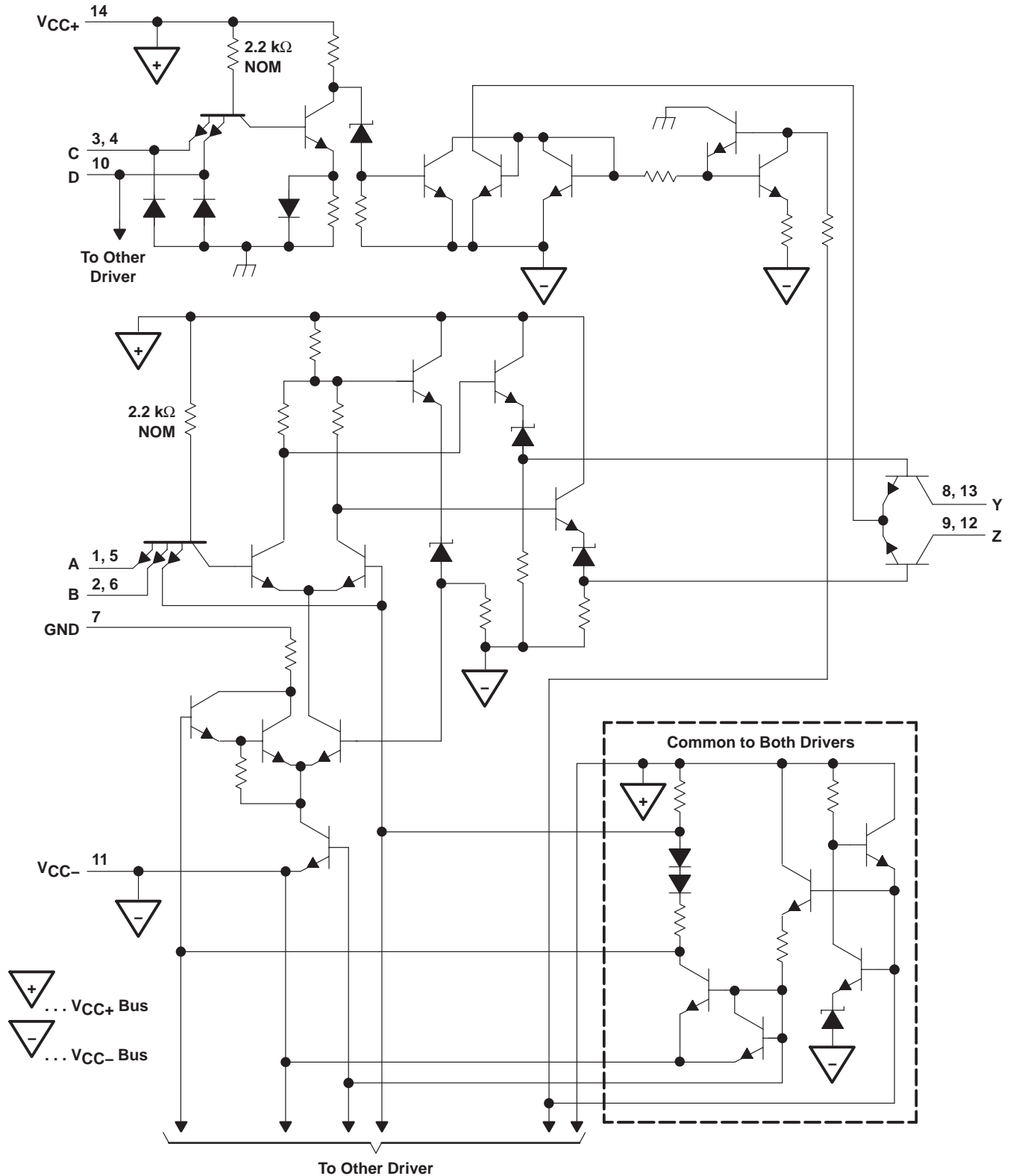
FUNCTION TABLE
(each driver)

| LOGIC INPUTS | | ENABLE INPUTS | | OUTPUTS† | |
|--------------|---|---------------|---|----------|-----|
| A | B | C | D | Y | Z |
| X | X | L | X | Off | Off |
| X | X | X | L | Off | Off |
| L | X | H | H | On | Off |
| X | L | H | H | On | Off |
| H | H | H | H | Off | On |

H = high level, L = low level, X = irrelevant

† When using only one channel of the line drivers, the other channel should be inhibited and/or have its outputs grounded.

schematic (each driver)



Pin numbers shown are for the D, J, N, NS, and W packages.

SN55110A, SN75110A, SN75112 DUAL LINE DRIVERS

SLLS106G – DECEMBER 1975 – REVISED NOVEMBER 2004

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

| | |
|--|----------------|
| Supply voltage: V_{CC+} (see Note 1) | 7 V |
| V_{CC-} (see Note 1) | -7 V |
| Input voltage, V_I | 5.5 V |
| Output voltage range, V_O | -5 V to 12 V |
| Package thermal impedance, θ_{JA} (see Notes 2 and 3): D package | 86°C/W |
| N package | 80°C/W |
| NS package | 76°C/W |
| Package thermal impedance, θ_{JC} (see Notes 4 and 5): FK package | 13.42°C/W |
| J package | 15.05°C/W |
| W package | 14.65°C/W |
| Operating virtual junction temperature | 150°C |
| Case temperature for 60 seconds: FK package | 260°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or W package | 300°C |
| Storage temperature range, T_{stg} | -65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. Voltage values are with respect to network ground terminal.
 2. Maximum power dissipation is a function of $T_J(\text{max})$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.
 4. Maximum power dissipation is a function of $T_J(\text{max})$, θ_{JC} , and T_C . The maximum allowable power dissipation at any allowable case temperature is $P_D = (T_J(\text{max}) - T_C)/\theta_{JC}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
 5. The package thermal impedance is calculated in accordance with MIL-STD-883.

recommended operating conditions (see Note 6)

| | SN55110A | | | SN75110A SN75112 | | | UNIT |
|--------------------------------------|----------|-----|------|---------------------|-----|-------|------|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| V_{CC+} Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| V_{CC-} Supply voltage | -4.5 | -5 | -5.5 | -4.75 | -5 | -5.25 | V |
| Positive common-mode output voltage | 0 | | 10 | 0 | | 10 | V |
| Negative common-mode output voltage | 0 | | -3 | 0 | | -3 | V |
| V_{IH} High-level input voltage | 2 | | | 2 | | | V |
| V_{IL} Low-level output voltage | | | 0.8 | | | 0.8 | V |
| T_A Operating free-air temperature | -55 | | 125 | 0 | | 70 | °C |

NOTE 6: When using only one channel of the line drivers, the other channel should be inhibited and/or have its outputs grounded.



SN55110A, SN75110A, SN75112 DUAL LINE DRIVERS

SLLS106G – DECEMBER 1975 – REVISED NOVEMBER 2004

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | SN55110A SN75110A | | | SN75112 | | | UNIT |
|-----------------------|---|---|--|------|-----|---------|------|-----|---------------|
| | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| V_{IK} | Input clamp voltage | $V_{CC\pm} = \text{MIN}$, $I_L = -12 \text{ mA}$ | -0.9 | -1.5 | | -0.9 | -1.5 | V | |
| $I_{O(\text{on})}$ | On-state output current | $V_{CC\pm} = \text{MAX}$, $V_O = 10 \text{ V}$ | 12 | 15 | | 27 | 40 | mA | |
| | | $V_{CC} = \text{MIN to MAX}$, $V_O = -1 \text{ V to } 1 \text{ V}$, $T_A = 25^\circ\text{C}$ | | | | 24 | 28 | | 32 |
| | | $V_{CC\pm} = \text{MIN}$, $V_O = -3 \text{ V}$ | 6.5 | 12 | | 15 | 27 | | |
| $I_{O(\text{off})}$ | Off-state output current | $V_{CC\pm} = \text{MIN}$, $V_O = 10 \text{ V}$ | | | 100 | | | 100 | μA |
| I_I | Input current at maximum input voltage | A, B, or C inputs | $V_{CC\pm} = \text{MAX}$, $V_I = 5.5 \text{ V}$ | | | 1 | | | 1 |
| | | D input | | | | | | | |
| I_{IH} | High-level input current | A, B, or C inputs | $V_{CC\pm} = \text{MAX}$, $V_I = 2.4 \text{ V}$ | | | 40 | | | 40 |
| | | D input | | | | | | | |
| I_{IL} | Low-level input current | A, B, or C inputs | $V_{CC\pm} = \text{MAX}$, $V_I = 0.4 \text{ V}$ | | | -3 | | | -3 |
| | | D input | | | | | | | |
| $I_{CC+(\text{on})}$ | Supply current from V_{CC} with driver enabled | $V_{CC\pm} = \text{MAX}$, A and B inputs at 0.4 V, C and D inputs at 2 V | 23 | 35 | | 25 | 40 | mA | |
| $I_{CC-(\text{on})}$ | Supply current from V_{CC-} with driver enabled | $V_{CC\pm} = \text{MAX}$, A and B inputs at 0.4 V, C and D inputs at 2 V | -34 | -50 | | -65 | -100 | mA | |
| $I_{CC+(\text{off})}$ | Supply current from V_{CC-} with driver inhibited | $V_{CC\pm} = \text{MAX}$, A, B, C, and D inputs at 0.4 V | 21 | | | 30 | | mA | |
| $I_{CC-(\text{off})}$ | Supply current from $V_{CC\pm}$ with driver inhibited | $V_{CC\pm} = \text{MAX}$, A, B, C, and D inputs at 0.4 V | -17 | | | -32 | | mA | |

† For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC+} = 5 \text{ V}$, $V_{CC-} = -5 \text{ V}$, $T_A = 25^\circ\text{C}$.

switching characteristics, $V_{CC\pm} = \pm 5 \text{ V}$, $T_A = 25^\circ\text{C}$ (see Figure 1)

| PARAMETERS§ | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|-------------|--------------|-------------|---|--|-----|-----|-----|------|
| t_{PLH} | A or B | Y or Z | $C_L = 40 \text{ pF}$, $R_L = 50 \Omega$, | | 9 | 15 | ns | |
| t_{PHL} | | | | | | | | |
| t_{PLH} | C or D | Y or Z | $C_L = 40 \text{ pF}$, $R_L = 50 \Omega$, | | 16 | 25 | ns | |
| t_{PHL} | | | | | | | | |

§ t_{PLH} = propagation delay time, low- to high-level output

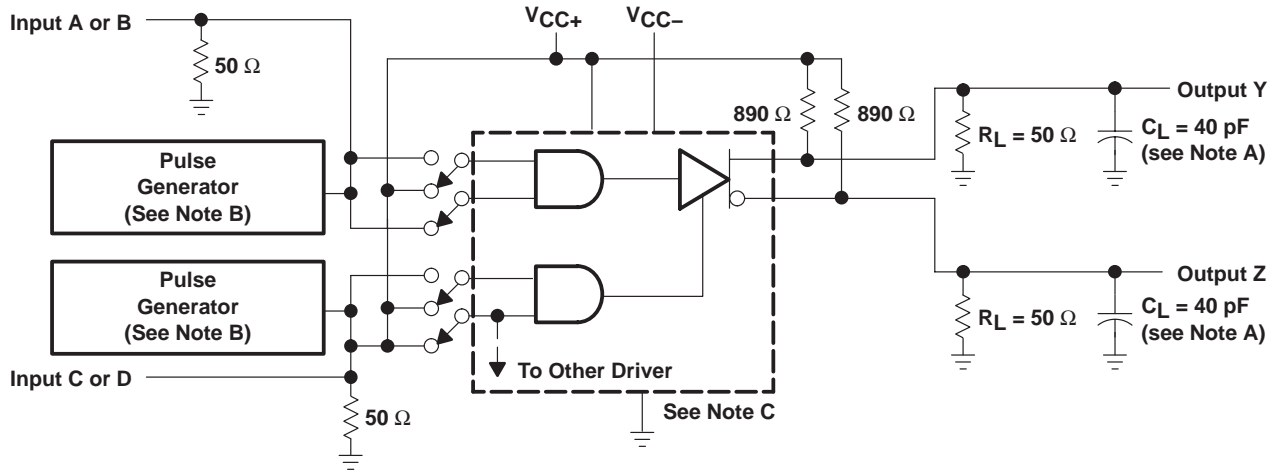
t_{PHL} = propagation delay time, high- to low-level output



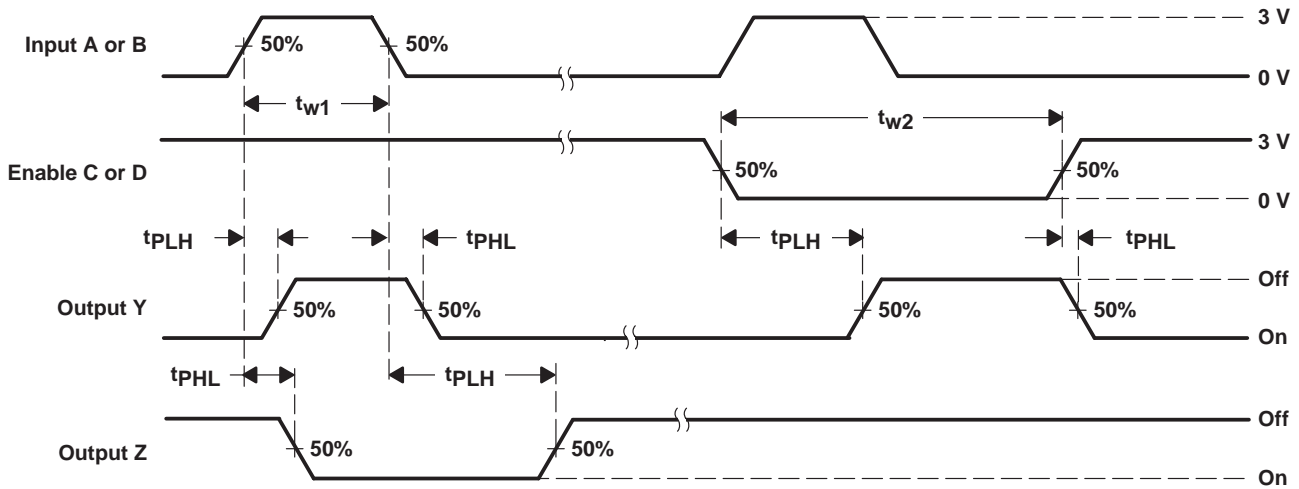
SN55110A, SN75110A, SN75112 DUAL LINE DRIVERS

SLLS106G – DECEMBER 1975 – REVISED NOVEMBER 2004

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

- NOTES: A. C_L includes probe and jig capacitance.
 B. The pulse generators have the following characteristics: $Z_O = 50 \Omega$, $t_r = t_f = 10 \pm 5 \text{ ns}$, $t_{w1} = 500 \text{ ns}$, $\text{PRR} \leq 1 \text{ MHz}$, $t_{w2} = 1 \mu\text{s}$, $\text{PRR} \leq 500 \text{ kHz}$.
 C. For simplicity, only one channel and the enable connections are shown.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

SN55110A, SN75110A
ON-STATE OUTPUT CURRENT
vs
NEGATIVE SUPPLY VOLTAGE

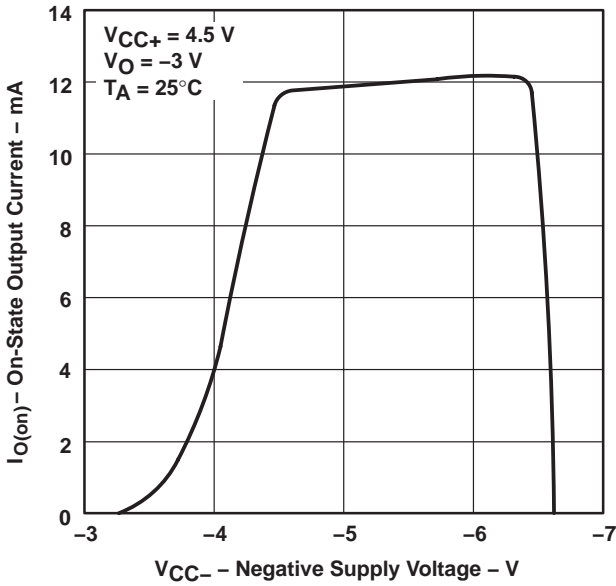


Figure 2

SN75112
ON-STATE OUTPUT CURRENT
vs
NEGATIVE SUPPLY VOLTAGE

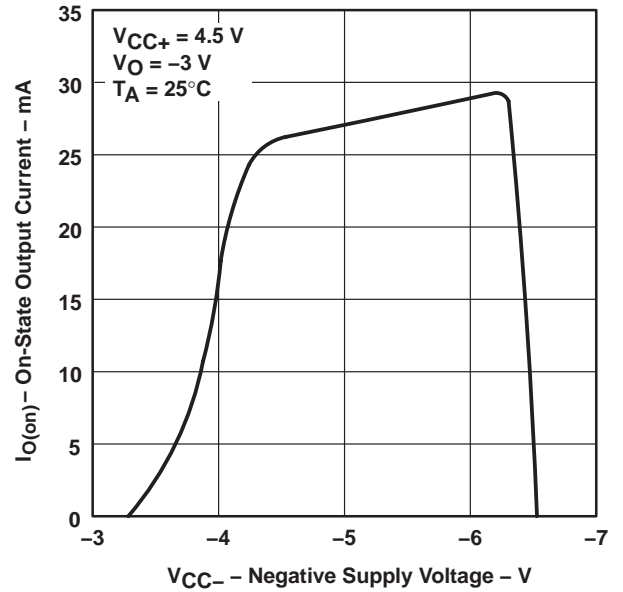


Figure 3

SN55110A, SN75110A, SN75112 DUAL LINE DRIVERS

SLLS106G – DECEMBER 1975 – REVISED NOVEMBER 2004

APPLICATION INFORMATION

special pulse-control circuit

Figure 4 shows a circuit that can be used as a pulse-generator output or in many other testing applications.

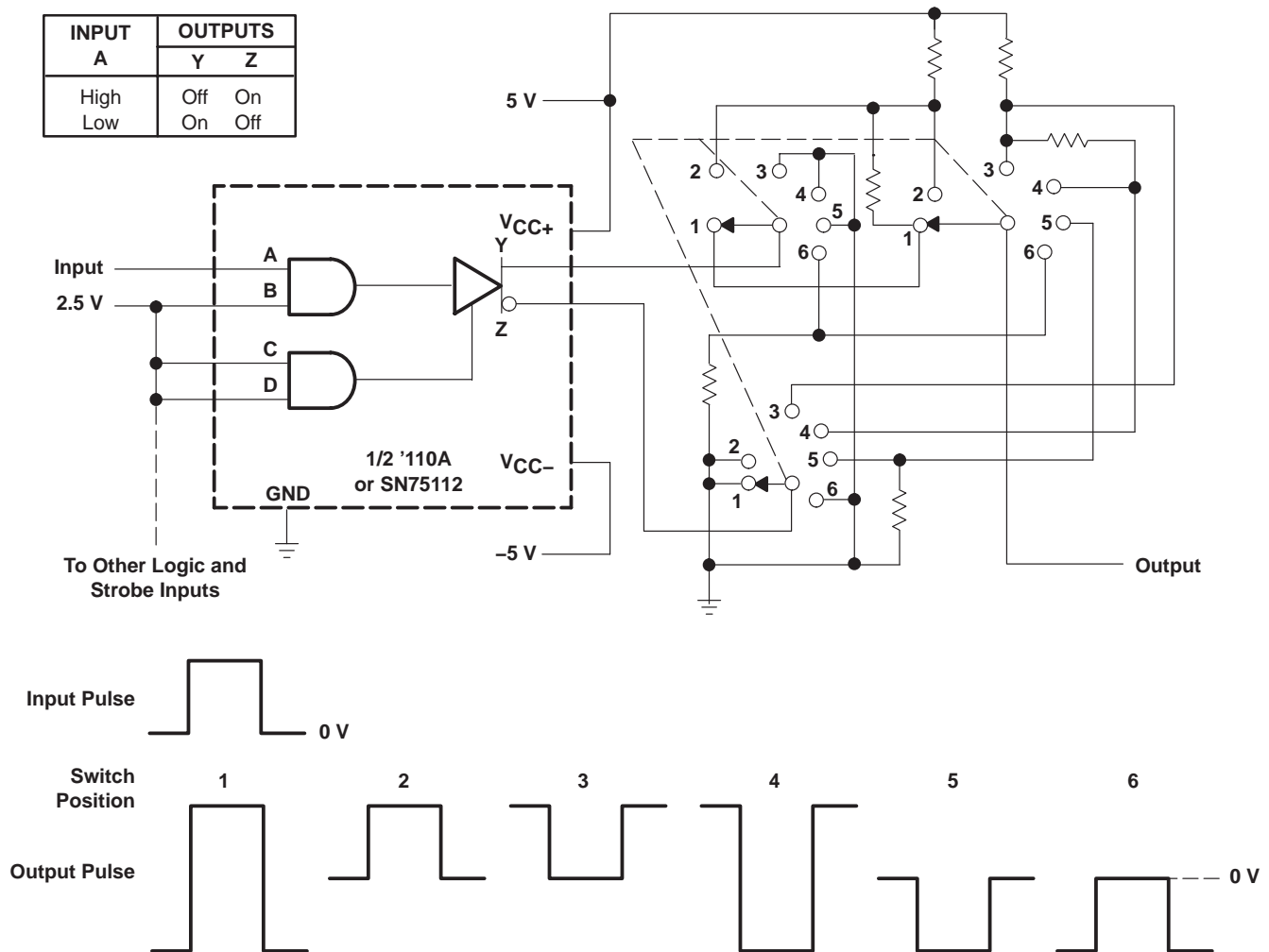


Figure 4. Pulse-Control Circuit

APPLICATION INFORMATION

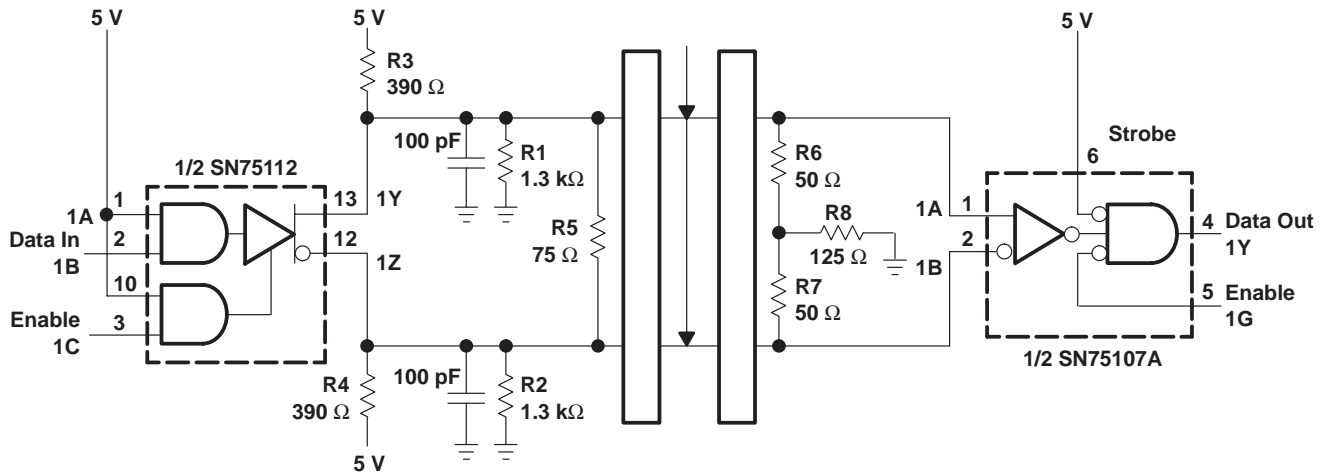
using the SN75112 as a CCITT-recommended V.35 line driver

The SN75112 dual line driver, the SN75107A dual line receiver, and some external resistors can be used to implement the data-interchange circuit of CCITT recommendation V.35 (1976) modem specification. The circuit of one channel is shown in Figure 5 and meets the requirement of the interface as specified by Appendix 11 of CCITT V.35 and is summarized in Table 1 (V.35 has been replaced by ITU V.11).

Table 1. CCITT V.35 Electrical Requirements

| GENERATOR | MIN | MAX | UNIT |
|---------------------------------------|----------------------------|-----|----------|
| Source impedance, Z_{source} | 50 | 150 | Ω |
| Resistance to ground, R | 135 | 165 | Ω |
| Differential output voltage, V_{OD} | 440 | 660 | mV |
| 10% to 90% rise time, t_r | 40 | | ns |
| or | 0.01 \times ui^\dagger | | |
| Common-mode output voltage, V_{OC} | -0.6 | 0.6 | V |
| LOAD (RECEIVER) | MIN | MAX | UNIT |
| Input impedance, Z_I | 90 | 110 | Ω |
| Resistance to ground, R | 135 | 165 | Ω |

$\dagger ui$ = unit interval or minimum signal-element pulse duration



All resistors are 5%, 1/4 W.

Figure 5. CCITT-Recommended V.35 Interface Using the SN75112 and SN75107A

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| 5962-87547012A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| 5962-8754701CA | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| 5962-8754701DA | ACTIVE | CFP | W | 14 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| SN55110AJ | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| SN75110AD | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75110ADE4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75110ADG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75110ADR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75110ADRE4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75110ADRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75110AJ | OBSOLETE | CDIP | J | 14 | | TBD | Call TI | Call TI |
| SN75110AN | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN75110ANE4 | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN75110ANSR | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75110ANSRE4 | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75110ANSRG4 | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75112D | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75112DE4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75112DG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75112DR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75112DRE4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75112DRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75112N | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN75112NE4 | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SNJ55110AFK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| SNJ55110AJ | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| SNJ55110AW | ACTIVE | CFP | W | 14 | 1 | TBD | A42 SNPB | N / A for Pkg Type |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

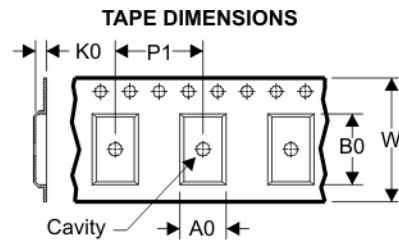
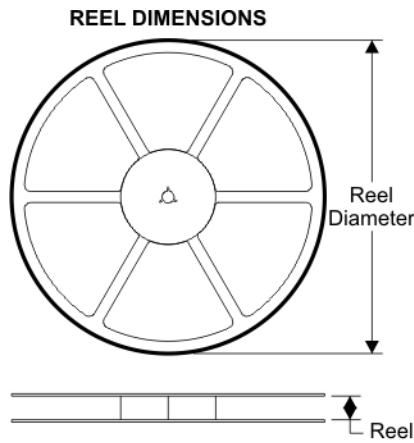
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

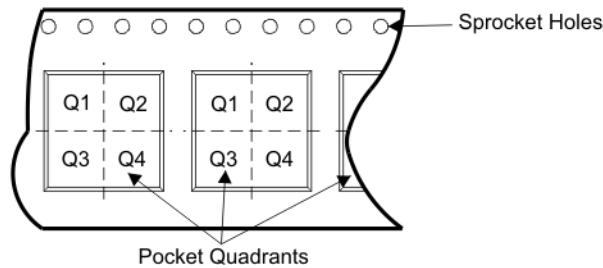
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL BOX INFORMATION



| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



| Device | Package | Pins | Site | Reel Diameter (mm) | Reel Width (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|---------|------|---------|--------------------|-----------------|---------|---------|---------|---------|--------|---------------|
| SN75110ADR | D | 14 | SITE 41 | 330 | 16 | 6.5 | 9.0 | 2.1 | 8 | 16 | Q1 |
| SN75110ANSR | NS | 14 | SITE 41 | 330 | 16 | 8.2 | 10.5 | 2.5 | 12 | 16 | Q1 |
| SN75112DR | D | 14 | SITE 41 | 330 | 16 | 6.5 | 9.0 | 2.1 | 8 | 16 | Q1 |

TAPE AND REEL BOX DIMENSIONS



| Device | Package | Pins | Site | Length (mm) | Width (mm) | Height (mm) |
|-------------|---------|------|---------|-------------|------------|-------------|
| SN75110ADR | D | 14 | SITE 41 | 346.0 | 346.0 | 33.0 |
| SN75110ANSR | NS | 14 | SITE 41 | 346.0 | 346.0 | 33.0 |
| SN75112DR | D | 14 | SITE 41 | 346.0 | 346.0 | 33.0 |

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



4040180-2/D 07/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



4040140/D 10/96

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AB.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

| Products | | Applications | |
|-----------------------|--|---------------------|--|
| Amplifiers | amplifier.ti.com | Audio | www.ti.com/audio |
| Data Converters | dataconverter.ti.com | Automotive | www.ti.com/automotive |
| DSP | dsp.ti.com | Broadband | www.ti.com/broadband |
| Interface | interface.ti.com | Digital Control | www.ti.com/digitalcontrol |
| Logic | logic.ti.com | Military | www.ti.com/military |
| Power Mgmt | power.ti.com | Optical Networking | www.ti.com/opticalnetwork |
| Microcontrollers | microcontroller.ti.com | Security | www.ti.com/security |
| RFID | www.ti-rfid.com | Telephony | www.ti.com/telephony |
| Low Power Wireless | www.ti.com/lpw | Video & Imaging | www.ti.com/video |
| | | Wireless | www.ti.com/wireless |

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2007, Texas Instruments Incorporated