

# TLP754

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## 1. Applications

- Intelligent Power Module Signal Isolation
- Factory Automation (FA)
- Industrial Inverters

## 2. General

The TLP754 is a photocoupler in a DIP8 package that consists of a GaAs infrared light-emitting diode (LED) optically coupled to an integrated high-gain, high-speed photodetector IC chip. It provides guaranteed performance and specifications at temperatures up to 125 °C. An internal noise shield provides a guaranteed common mode transient immunity of  $\pm 20$  kV/ $\mu$ s. The TLP754 guarantees minimum and maximum of propagation delay time, pulse width distortion. Therefore it is suitable for isolation interface between IPM and control IC circuits in motor control application.

## 3. Features

- (1) Inverter logic type (open collector output)
- (2) Package: DIP8
- (3) Operating temperature: -40 to 125 °C
- (4) Supply voltage: -0.5 to 30 V
- (5) Threshold input current: 5.0 mA (max)
- (6) Supply current: 1.3 mA (max)
- (7) Propagation delay time:  $t_{pHL} = 400$  ns (max),  $t_{pLH} = 550$  ns (max)
- (8) Pulse width distortion: 400 ns (max)
- (9) Common-mode transient immunity:  $\pm 20$  kV/ $\mu$ s (min)
- (10) Isolation voltage: 5000 Vrms (min)
- (11) Safety standards

UL-approved: UL1577, File No.E67349

cUL-approved: CSA Component Acceptance Service No.5A File No.E67349

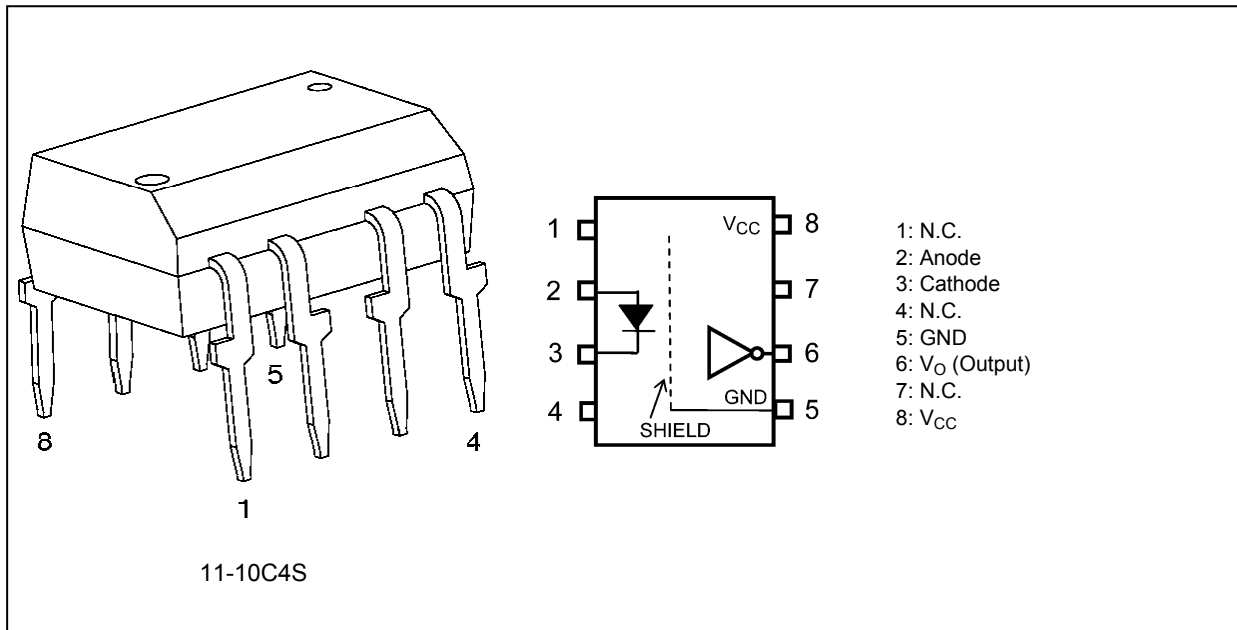
VDE-approved: EN60747-5-5, EN60065 or EN60950-1 (**Note 1**)

Note 1: When a VDE approved type is needed, please designate the **Option (D4)**.

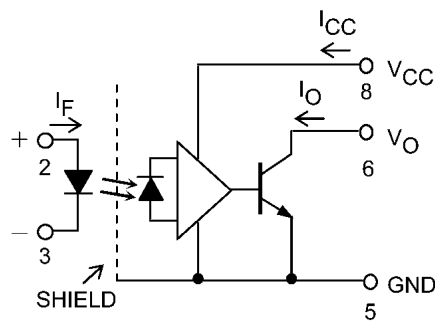
Start of commercial production

2012-01

**4. Packaging and Pin Configuration**



**5. Internal Circuit**



**6. Principle of Operation**

**6.1. Truth Table**

Input	LED	Output
H	ON	L
L	OFF	H

**6.2. Mechanical Parameters**

Characteristics	7.62-mm Pitch TLP754	10.16-mm Pitch TLP754F	Unit
Creepage distances	7.0 (min)	8.0 (min)	mm
Clearance distances	7.0 (min)	8.0 (min)	
Internal isolation thickness	0.4 (min)	0.4 (min)	

**7. Absolute Maximum Ratings (Note) (Unless otherwise specified, T<sub>a</sub> = 25 °C)**

	Characteristics	Symbol	Note	Rating	Unit
LED	Input forward current	I <sub>F</sub>		20	mA
	Input forward current derating (T <sub>a</sub> ≥ 116 °C)	ΔI <sub>F</sub> /ΔT <sub>a</sub>		-0.6	mA/°C
	Input forward current (pulsed)	I <sub>FP</sub>	(Note 1)	50	mA
	Input forward current derating (pulsed) (T <sub>a</sub> ≥ 110 °C)	ΔI <sub>FP</sub> /ΔT <sub>a</sub>		-1.25	mA/°C
	Input power dissipation	P <sub>D</sub>		40	mW
	Input power dissipation derating (T <sub>a</sub> ≥ 110 °C)	ΔP <sub>D</sub> /ΔT <sub>a</sub>		-1.0	mW/°C
	Input reverse voltage	V <sub>R</sub>		5	V
Detector	Output current	I <sub>O</sub>		15	mA
	Output voltage	V <sub>O</sub>		-0.5 to 30	V
	Supply voltage	V <sub>CC</sub>		-0.5 to 30	
	Output power dissipation	P <sub>O</sub>		80	mW
	Output power dissipation derating (T <sub>a</sub> ≥ 110 °C)	ΔP <sub>O</sub> /ΔT <sub>a</sub>		-2.0	mW/°C
Common	Operating temperature	T <sub>opr</sub>		-40 to 125	°C
	Storage temperature	T <sub>stg</sub>		-55 to 150	
	Lead soldering temperature (10 s)	T <sub>sol</sub>		260	
	Isolation voltage AC, 60 s, R.H. ≤ 60 %	BV <sub>S</sub>	(Note 2)	5000	Vrms

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Pulse width (PW) ≤ 1 ms, duty = 50 %

Note 2: This device is considered as a two-terminal device: Pins 1, 2, 3 and 4 are shorted together, and pins 5, 6, 7 and 8 are shorted together.

**8. Recommended Operating Conditions (Note)**

Characteristics	Symbol	Note	Min	Typ.	Max	Unit
Input on-state current	I <sub>F(ON)</sub>	(Note 1)	7.5	—	15	mA
Input off-state voltage	V <sub>F(OFF)</sub>		0	—	0.8	V
Supply voltage	V <sub>CC</sub>	(Note 2)	4.5	—	30	
Operating temperature	T <sub>opr</sub>	(Note 2)	-40	—	125	°C

Note: The recommended operating conditions are given as a design guide necessary to obtain the intended performance of the device. Each parameter is an independent value. When creating a system design using this device, the electrical characteristics specified in this datasheet should also be considered.

Note: A ceramic capacitor (0.1 μF) should be connected between pin 8 and pin 5 to stabilize the operation of a high-gain linear amplifier. Otherwise, this photocoupler may not switch properly. The bypass capacitor should be placed within 1 cm of each pin.

Note 1: The rise and fall times of the input on-current should be less than 0.5 μs.

Note 2: Denotes the operating range, not the recommended operating condition.

**9. Electrical Characteristics (Note)**  
(Unless otherwise specified,  $T_a = -40$  to  $125$  °C,  $V_{CC} = 4.5$  to  $30$  V)

Characteristics	Symbol	Note	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input forward voltage	$V_F$		—	$I_F = 10$ mA, $T_a = 25$ °C	1.45	1.55	1.7	V
Input forward voltage temperature coefficient	$\Delta V_F / \Delta T_a$		—	$I_F = 10$ mA	—	-2.0	—	mV/°C
Input reverse current	$I_R$		—	$V_R = 5$ V, $T_a = 25$ °C	—	—	10	$\mu$ A
Input capacitance	$C_t$		—	$V = 0$ V, $f = 1$ MHz	—	60	—	pF
High-level output current	$I_{OH}$		Fig. 12.1.1	$V_F = 0.8$ V, $V_O < V_{CC}$	—	—	50	$\mu$ A
Low-level output voltage	$V_{OL}$		Fig. 12.1.2	$I_F = 10$ mA, $I_O = 2.4$ mA	—	0.2	0.6	V
High-level supply current	$I_{CCH}$		Fig. 12.1.3	$I_F = 0$ mA	—	1.0	1.3	mA
Low-level supply current	$I_{CCL}$		Fig. 12.1.4	$I_F = 10$ mA	—	1.0	1.3	
Output current	$I_O$		Fig. 12.1.5	$I_F = 10$ mA, $V_O = 0.6$ V	4.0	—	—	
Threshold input current (H/L)	$I_{FHL}$		—	$I_O = 0.75$ mA, $V_O < 0.8$ V	—	1.5	5.0	
Threshold input voltage (L/H)	$V_{FLH}$		—	$I_O = 0.75$ mA, $V_O > 2.0$ V	0.8	—	—	V

Note: All typical values are at  $T_a = 25$  °C.

**10. Isolation Characteristics (Unless otherwise specified,  $T_a = 25$  °C)**

Characteristics	Symbol	Note	Test Conditions	Min	Typ.	Max	Unit
Total capacitance (input to output)	$C_S$	(Note 1)	$V_S = 0$ V, $f = 1$ MHz	—	1.0	—	pF
Isolation resistance	$R_S$	(Note 1)	$V_S = 500$ V, R.H. $\leq 60$ %	$1 \times 10^{12}$	$10^{14}$	—	$\Omega$
Isolation voltage	$BV_S$	(Note 1)	AC, 60 s	5000	—	—	$V_{rms}$
			AC, 1 s in oil	—	10000	—	
			DC, 60 s in oil	—	10000	—	Vdc

Note 1: This device is considered as a two-terminal device: Pins 1, 2, 3 and 4 are shorted together, and pins 5, 6, 7 and 8 are shorted together.

**11. Switching Characteristics (Note)**  
(Unless otherwise specified,  $T_a = -40$  to  $125$  °C,  $V_{CC} = 15$  V)

Characteristics	Symbol	Note	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Propagation delay time (H/L)	$t_{pHL}$	(Note 1)	Fig. 12.1.6	$I_F = 0 \rightarrow 10$ mA, $R_L = 20$ k $\Omega$ , $C_L = 100$ pF	30	150	400	ns
				$I_F = 0 \rightarrow 10$ mA, $R_L = 20$ k $\Omega$ , $C_L = 10$ pF	—	70	—	
Propagation delay time (L/H)	$t_{pLH}$	(Note 1)	Fig. 12.1.6	$I_F = 10 \rightarrow 0$ mA, $R_L = 20$ k $\Omega$ , $C_L = 100$ pF	150	350	550	ns
				$I_F = 10 \rightarrow 0$ mA, $R_L = 20$ k $\Omega$ , $C_L = 10$ pF	—	110	—	
Pulse width distortion	$ \dot{t}_{pHL} - \dot{t}_{pLH} $	(Note 1)	Fig. 12.1.6	$I_F = 10$ mA, $R_L = 20$ k $\Omega$ , $C_L = 100$ pF	—	—	400	ns
Propagation delay skew (device to device)	$t_{psk}$	(Note 1), (Note 2)	Fig. 12.1.6	$I_F = 10$ mA, $R_L = 20$ k $\Omega$ , $C_L = 100$ pF	-50	—	450	
Common-mode transient immunity at output high	$CM_H$		Fig. 12.1.7	$V_{CM} = 1500$ V <sub>p-p</sub> , $I_F = 0$ mA, $R_L = 20$ k $\Omega$ , $T_a = 25$ °C, $C_L = 10$ pF or 100 pF	$\pm 20$	$\pm 25$	—	kV/ $\mu$ s
Common-mode transient immunity at output low	$CM_L$			$V_{CM} = 1500$ V <sub>p-p</sub> , $I_F = 10$ mA, $R_L = 20$ k $\Omega$ , $T_a = 25$ °C, $C_L = 10$ pF or 100 pF	$\pm 20$	$\pm 25$	—	

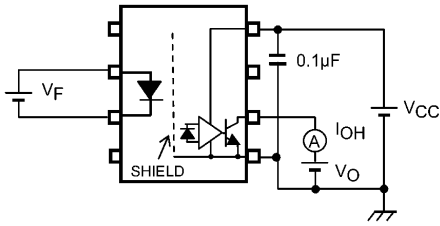
Note: All typical values are at  $T_a = 25$  °C.

Note 1: Input signal ( $f = 10$  kHz, duty = 10 %, input current  $t_r = t_f = 5$  ns or less )

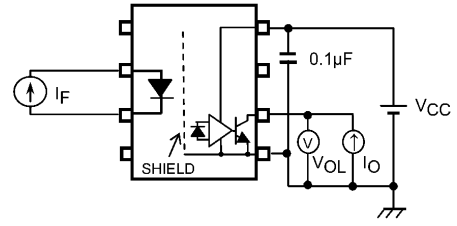
Note 2: The propagation delay skew,  $t_{psk}$ , is defined as the propagation delay time of the largest or smallest  $t_{pLH}$  minus the largest or smallest  $t_{pHL}$  of multiple samples. Evaluations of these samples are conducted under identical test conditions (supply voltage, input current, temperature, etc).

**12. Test Circuits and Characteristics Curves**

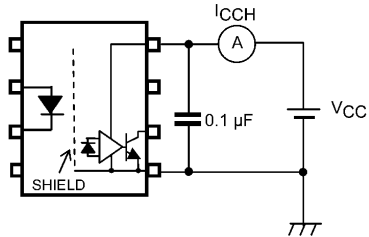
**12.1. Test Circuits**



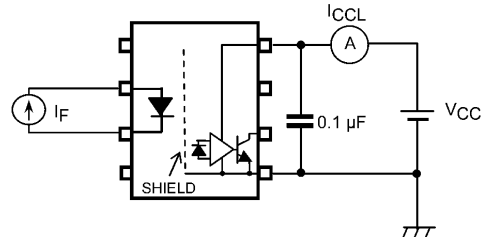
**Fig. 12.1.1 IOH Test Circuit**



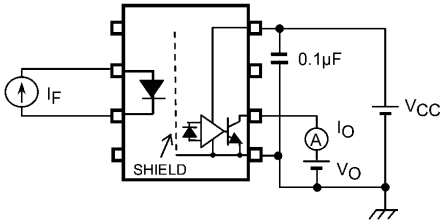
**Fig. 12.1.2 VOL Test Circuit**



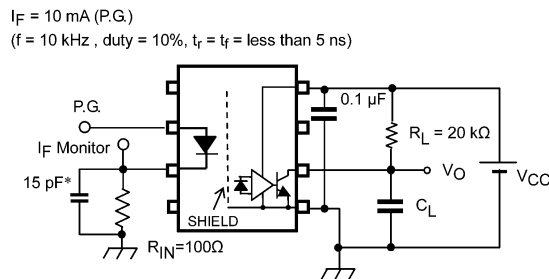
**Fig. 12.1.3 ICCH Test Circuit**



**Fig. 12.1.4 ICCL Test Circuit**



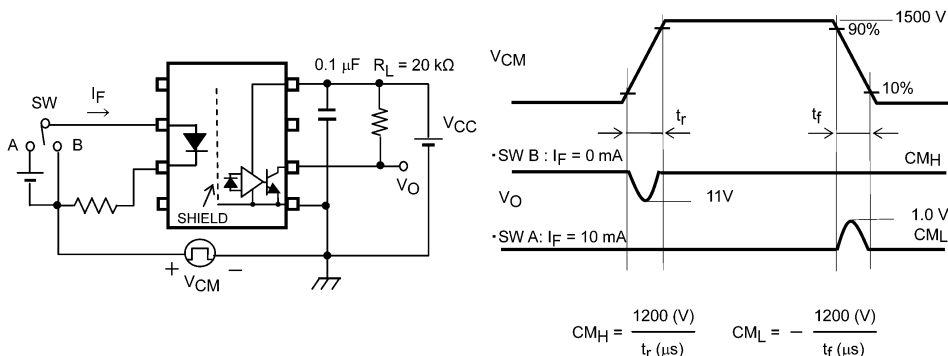
**Fig. 12.1.5 IO Test Circuit**



$I_F = 10 \text{ mA (P.G.)}$   
 $(f = 10 \text{ kHz, duty} = 10\%, t_r = t_f = \text{less than } 5 \text{ ns})$

\* Includes probe and stray capacitance.  
 P.G.: Pulse generator

**Fig. 12.1.6 Switching Time Test Circuit and Waveform**



$$CM_H = \frac{1200 \text{ (V)}}{t_r \text{ (}\mu\text{s)}} \quad CM_L = - \frac{1200 \text{ (V)}}{t_f \text{ (}\mu\text{s)}}$$

**Fig. 12.1.7 Common-Mode Transient Immunity and waveform**

12.2. Characteristics Curves (Note)

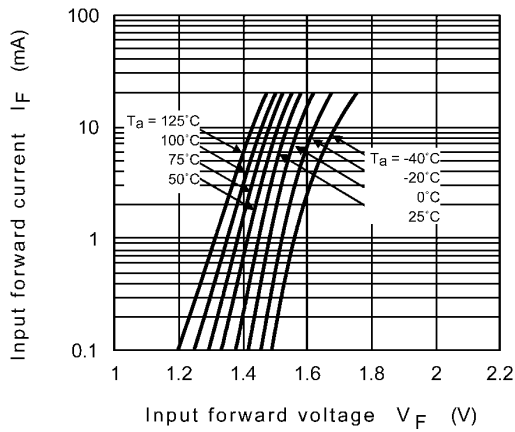


Fig. 12.2.1  $I_F - V_F$

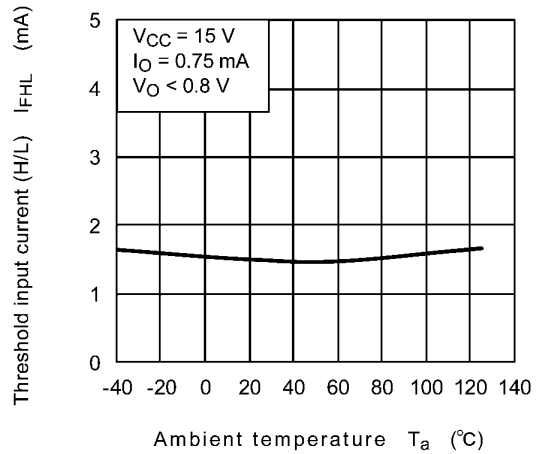


Fig. 12.2.2  $I_{FHL} - T_a$

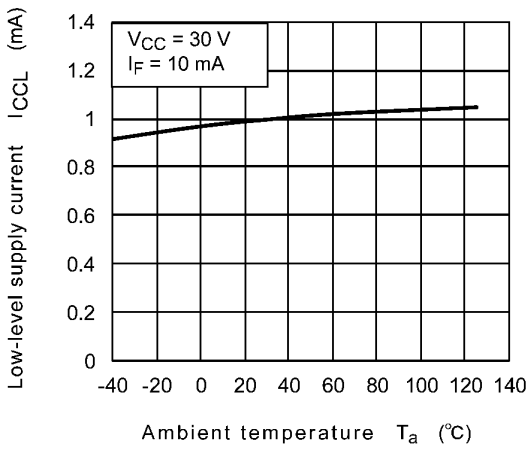


Fig. 12.2.3  $I_{CCL} - T_a$

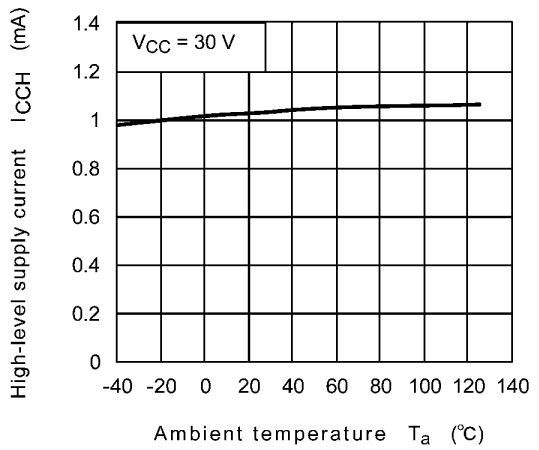


Fig. 12.2.4  $I_{CCH} - T_a$

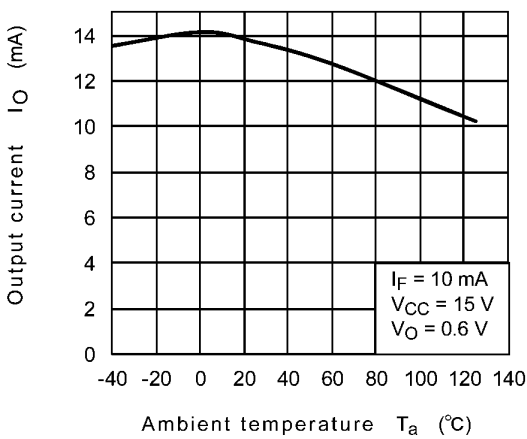


Fig. 12.2.5  $I_O - T_a$

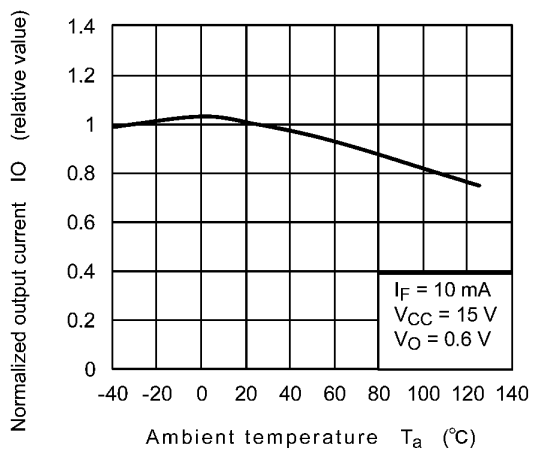


Fig. 12.2.6 Normalized  $I_O - T_a$

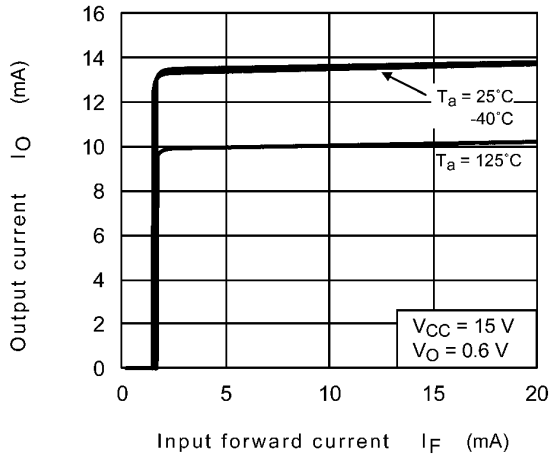


Fig. 12.2.7  $I_O - I_F$

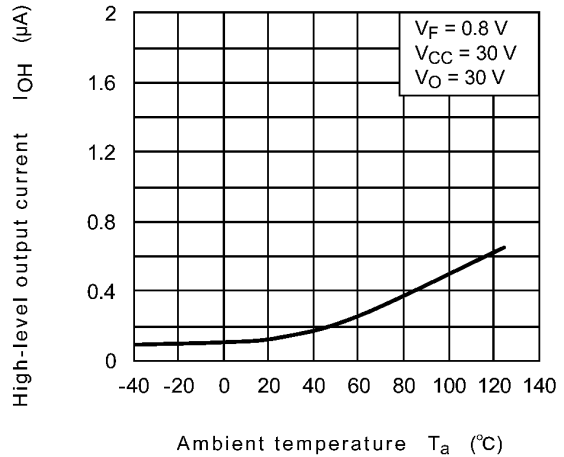


Fig. 12.2.8  $I_{OH} - T_a$

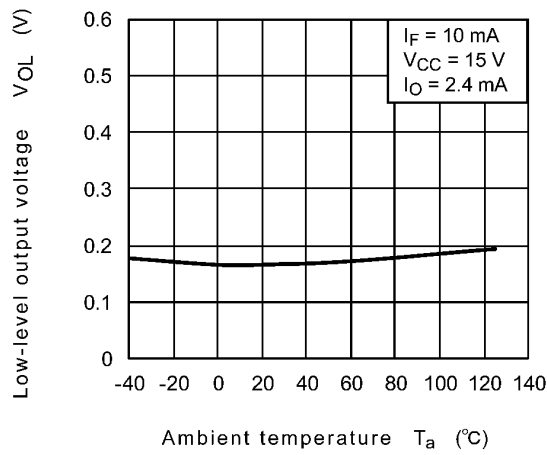


Fig. 12.2.9  $V_{OL} - T_a$

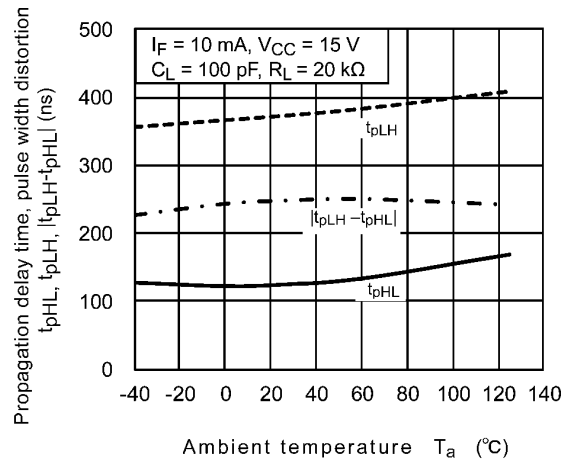


Fig. 12.2.10  $t_{pHL}, t_{pLH}, |t_{pLH}-t_{pHL}| - T_a$

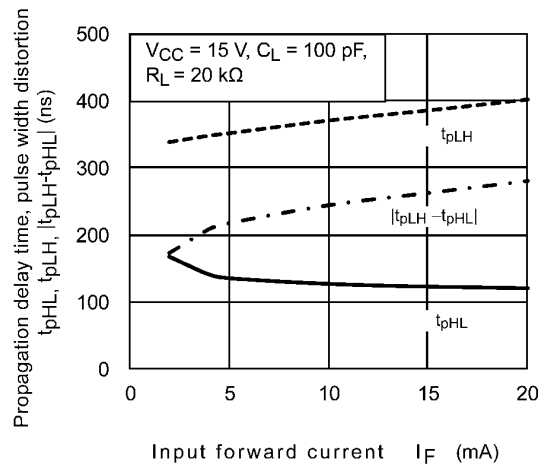


Fig. 12.2.11  $t_{pHL}, t_{pLH}, |t_{pLH}-t_{pHL}| - I_F$

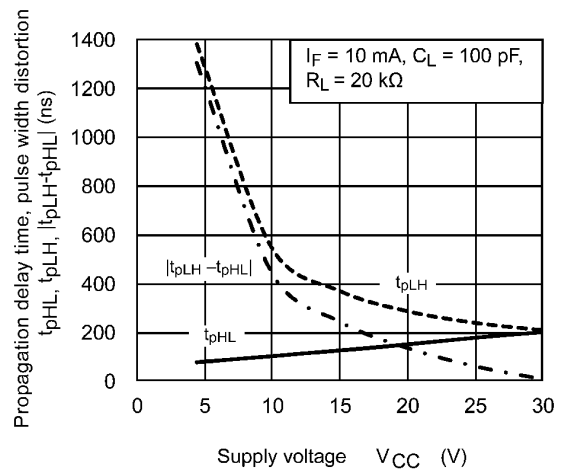


Fig. 12.2.12  $t_{pHL}, t_{pLH}, |t_{pLH}-t_{pHL}| - V_{CC}$

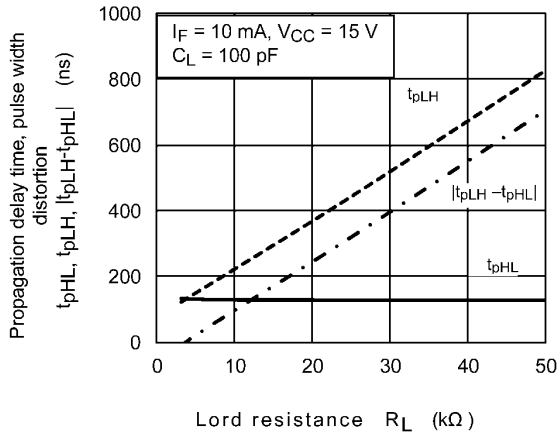


Fig. 12.2.13  $t_{pHL}$ ,  $t_{pLH}$ ,  $|t_{pLH} - t_{pHL}| - R_L$

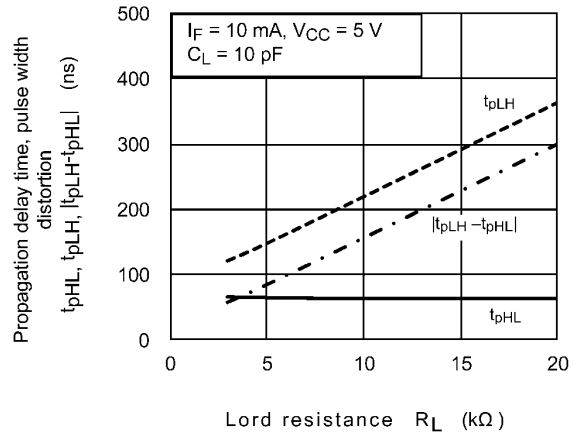


Fig. 12.2.14  $t_{pHL}$ ,  $t_{pLH}$ ,  $|t_{pLH} - t_{pHL}| - R_L$

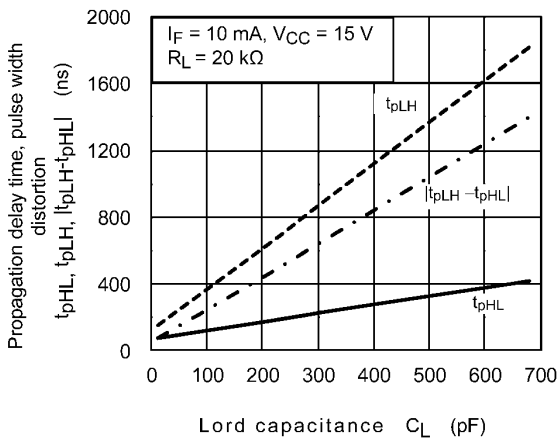


Fig. 12.2.15  $t_{pHL}$ ,  $t_{pLH}$ ,  $|t_{pLH} - t_{pHL}| - C_L$

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



## 13. Soldering and Storage

### 13.1. Precautions for Soldering

The soldering temperature should be controlled as closely as possible to the conditions shown below, irrespective of whether a soldering iron or a reflow soldering method is used.

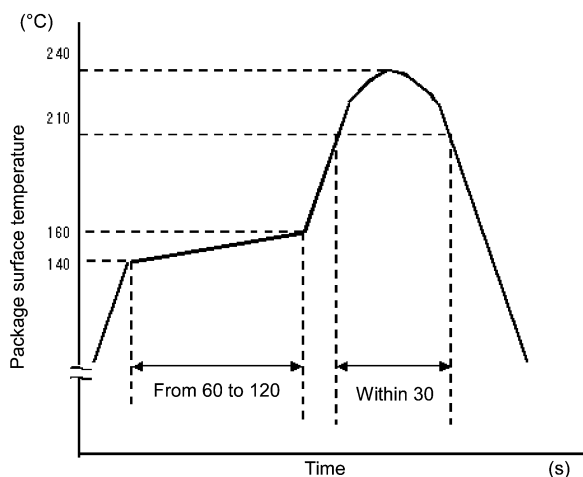
- When using soldering reflow.

The soldering temperature profile is based on the package surface temperature.

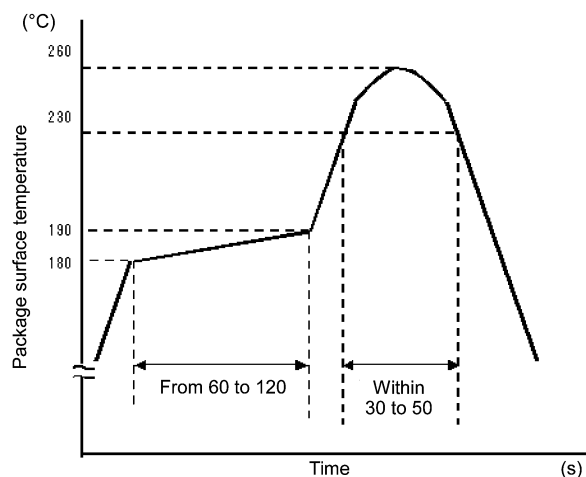
(See the figure shown below, which is based on the package surface temperature.)

Reflow soldering must be performed once or twice.

The mounting should be completed with the interval from the first to the last mountings being 2 weeks.



**Fig. 13.1.1** An example of a temperature profile when Sn-Pb eutectic solder is used



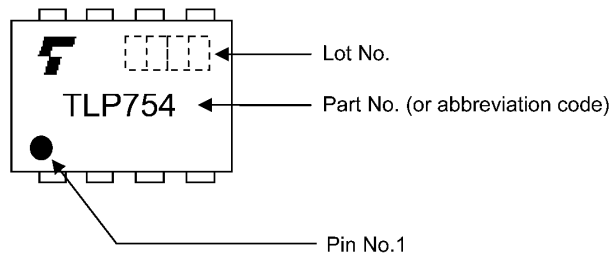
**Fig. 13.1.2** An example of a temperature profile when lead(Pb)-free solder is used

- When using soldering flow (Applicable to both eutectic solder and Lead(Pb)-Free solder)  
Preheat the device at a temperature of 150 °C (package surface temperature) for 60 to 120 seconds.  
Mounting condition of 260 °C within 10 seconds is recommended.  
Flow soldering must be performed once.
- When using soldering Iron  
Complete soldering within 10 seconds for lead temperature not exceeding 260 °C or within 3 seconds not exceeding 350 °C  
Heating by soldering iron must be done only once per lead.

### 13.2. Precautions for General Storage

- Avoid storage locations where devices may be exposed to moisture or direct sunlight.
- Follow the precautions printed on the packing label of the device for transportation and storage.
- Keep the storage location temperature and humidity within a range of 5 °C to 35 °C and 45 % to 75 %, respectively.
- Do not store the products in locations with poisonous gases (especially corrosive gases) or in dusty conditions.
- Store the products in locations with minimal temperature fluctuations. Rapid temperature changes during storage can cause condensation, resulting in lead oxidation or corrosion, which will deteriorate the solderability of the leads.
- When restoring devices after removal from their packing, use anti-static containers.
- Do not allow loads to be applied directly to devices while they are in storage.
- If devices have been stored for more than two years under normal storage conditions, it is recommended that you check the leads for ease of soldering prior to use.

14. Marking



**15. EN60747-5-5 Option (D4) Specification**

- Part number: TLP754, TLP754F (**Note 1**)
- The following part naming conventions are used for the devices that have been qualified according to option (D4) of EN60747.

Example: TLP754(D4-TP1, F)

D4 : EN60747 option

TP1: Tape type

F : [[G]]/RoHS COMPATIBLE (**Note 2**)

Note 1: Use TOSHIBA standard type number for safety standard application.



e.g., TLP754(D4-TP1,F) → TLP754

Note 2: Please contact your Toshiba sales representative for details on environmental information such as the product's RoHS compatibility.

RoHS is the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronics equipment.

Description		Symbol	Rating	Unit
Application classification				
for rated mains voltage ≤ 300 Vrms			I-IV	—
for rated mains voltage ≤ 600 Vrms			I-III	—
Climatic classification			40 / 125 / 21	—
Pollution degree			2	—
Maximum operating insulation voltage	TLPxxx type	V <sub>IORM</sub>	890	V <sub>peak</sub>
	TLPxxxF type		1140	
Input to output test voltage, Method A V <sub>pr</sub> = 1.6 × V <sub>IORM</sub> , type and sample test t <sub>p</sub> = 10 s, partial discharge < 5 pC	TLPxxx type	V <sub>pr</sub>	1424	V <sub>peak</sub>
	TLPxxxF type		1824	
Input to output test voltage, Method B V <sub>pr</sub> = 1.875 × V <sub>IORM</sub> , 100 % production test t <sub>p</sub> = 1 s, partial discharge < 5 pC	TLPxxx type	V <sub>pr</sub>	1670	V <sub>peak</sub>
	TLPxxxF type		2140	
Highest permissible overvoltage (transient overvoltage, t <sub>pr</sub> = 60 s)		V <sub>TR</sub>	8000	V <sub>peak</sub>
Safety limiting values (max. permissible ratings in case of fault, also refer to thermal derating curve)				
current (input current I <sub>F</sub> , P <sub>so</sub> = 0)		I <sub>si</sub>	100	mA
power (output or total power dissipation)		P <sub>so</sub>	800	mW
temperature		T <sub>s</sub>	150	°C
Insulation resistance	V <sub>IO</sub> = 500 V, T <sub>a</sub> = 25 °C V <sub>IO</sub> = 500 V, T <sub>a</sub> = 100 °C V <sub>IO</sub> = 500 V, T <sub>a</sub> = T <sub>s</sub>	R <sub>si</sub>	≥ 10 <sup>12</sup> ≥ 10 <sup>11</sup> ≥ 10 <sup>9</sup>	Ω

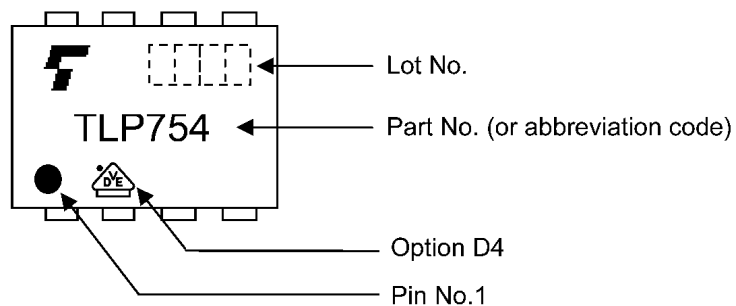
**Fig. 15.1 EN60747 Isolation Characteristics**

		 7.62 mm pitch TLPxxx type	 10.16 mm pitch TLPxxxF type
Minimum creepage distance	Cr	7.0 mm	8.0 mm
Minimum clearance	Cl	7.0 mm	8.0 mm
Minimum insulation thickness	ti	0.4 mm	
Comparative tracking index	CTI	175	

**Fig. 15.2 Insulation Related Specifications (Note)**

Note: If a printed circuit is incorporated, the creepage distance and clearance may be reduced below this value. (e. g., at a standard distance between soldering eye centers of 7.5 mm). If this is not permissible, the user shall take suitable measures.

Note: This photocoupler is suitable for **safe electrical isolation** only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits.



**Fig. 15.3 Marking Example (Note)**

Note: The above marking is applied to the photocouplers that have been qualified according to option (D4) of EN60747.(Fig15.3)

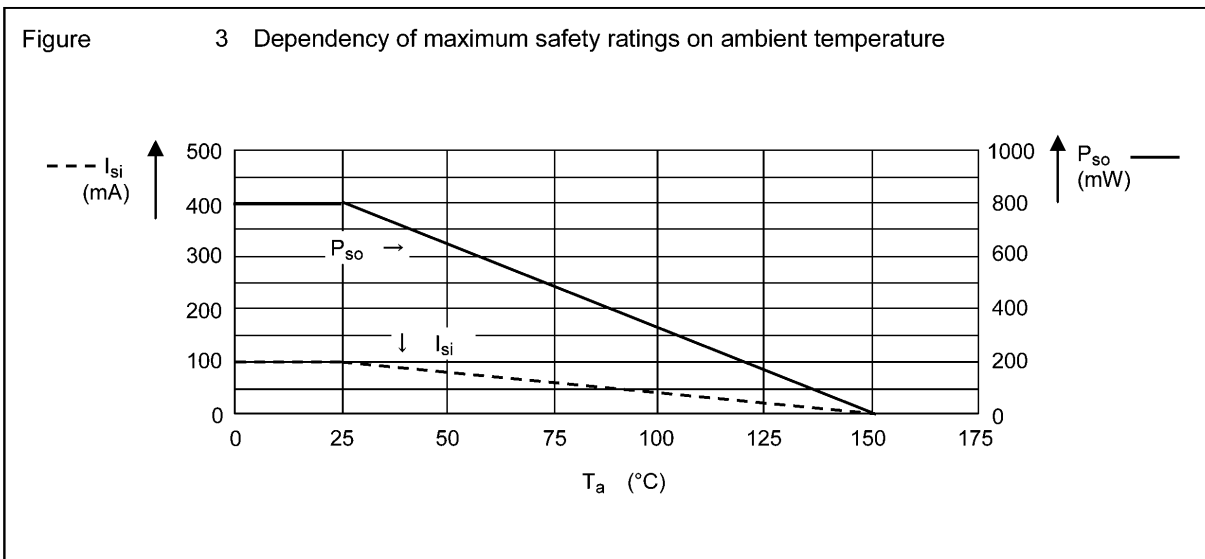
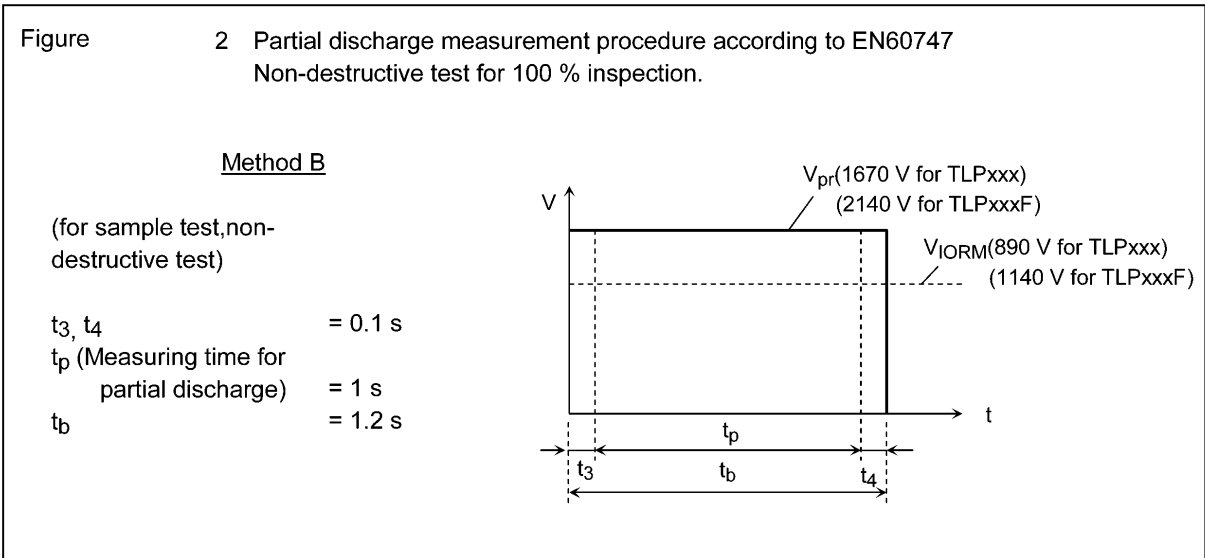
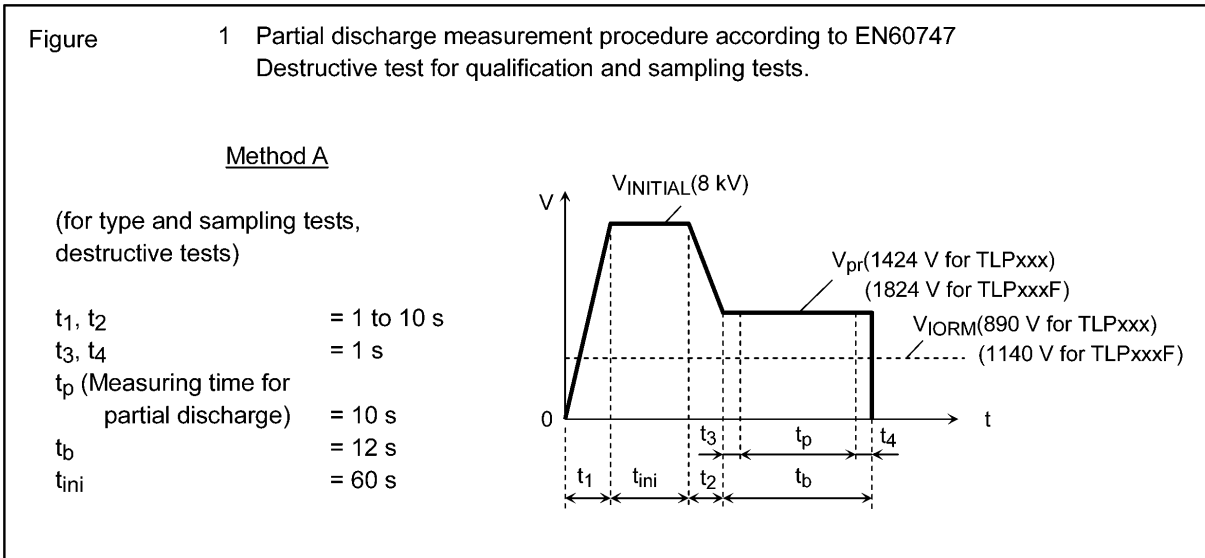
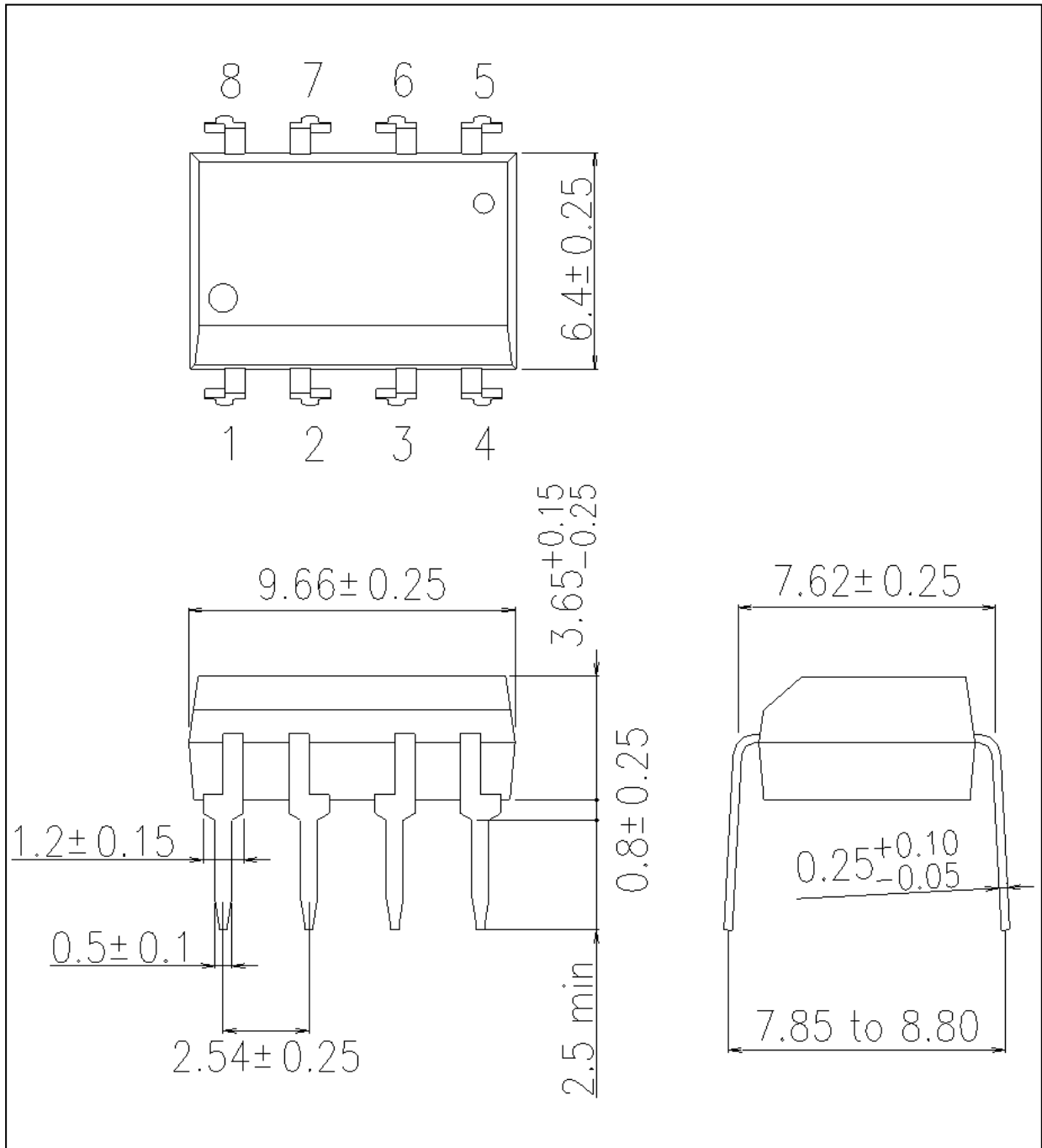


Fig. 15.4 Measurement Procedure

**Package Dimensions**

Unit: mm



Weight: 0.54 g (typ.)

Package Name(s)
TOSHIBA: 11-10C4S

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