

DS34LV86T 3V Enhanced CMOS Quad Differential Line Receiver

 Check for Samples: [DS34LV86T](#)

FEATURES

- Low Power CMOS Design (30 mW Typical)
- Interoperable With Existing 5V RS-422 Networks
- Industrial Temperature Range
- Meets TIA/EIA-422-B (RS-422) and ITU-T V.11 Recommendation
- 3.3V Operation
- $\pm 7V$ Common Mode Range @ $V_{ID} = 3V$
- $\pm 10V$ Common Mode Range @ $V_{ID} = 0.2V$
- Receiver OPEN Input Failsafe Feature
- Ensured AC Parameter:
 - Maximum Receiver Skew: 4 ns
 - Transition Time: 10 ns
- Pin Compatible With DS34C86T
- 32 MHz Toggle Frequency
- >6.5k ESD Tolerance (HBM)
- Available in SOIC Packaging

DESCRIPTION

The DS34LV86T is a high speed quad differential CMOS receiver that meets the requirements of both TIA/EIA-422-B and ITU-T V.11. The CMOS DS34LV86T features typical low static I_{CC} of 9 mA which makes it ideal for battery powered and power conscious applications. The Tri-State enables, EN, allow the device to be disabled when not in use to minimize power consumption. The dual enable scheme allows for flexibility in turning receivers on and off.

The receiver output (RO) is ensured to be High when the inputs are left open. The receiver can detect signals as low as ± 200 mV over the common mode range of $\pm 10V$. The receiver outputs (RO) are compatible with TTL and LVCMOS levels.

Connection Diagram

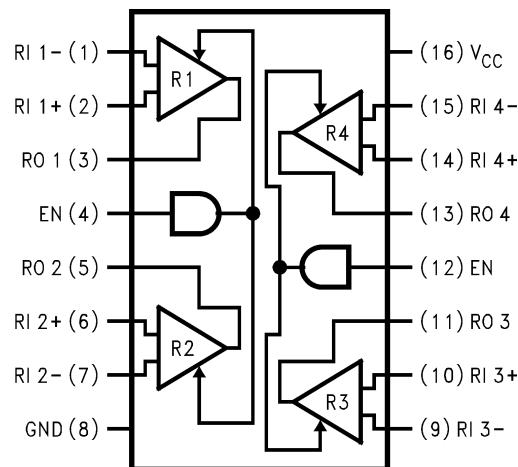


Figure 1. SOIC (Top View)
See Package Number D



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TRUTH TABLE⁽¹⁾

Enable EN	Inputs RI+–RI–	Output RO
L	X	Z
H	$V_{ID} \geq +0.2V$	H
H	$V_{ID} \leq -0.2V$	L
H	Open†	H

- (1) L = Logic Low
 H = Logic High
 X = Irrelevant
 Z = Tri-State
 † = Open, Not Terminated



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾⁽²⁾

Supply Voltage (V_{CC})		+7V
Enable Input Voltage (EN)		+7V
Receiver Input Voltage	(V_{ID} : RI+, RI–)	±14V
Receiver Input Voltage	(V_{CM} : RI+, RI–)	±14V
Receiver Output Voltage (RO)		–0.5V to $V_{CC} + 0.5V$
Receiver Output Current (RO)		±25 mA
Maximum Package Power Dissipation @ +25°C	D Package	1190 mW
Derate D Package		9.8 mW/°C above +25°C
Storage Temperature Range		–65°C to +150°C
Lead Temperature Range	Soldering (4 Seconds)	+260°C
ESD Ratings (HBM, 1.5k, 100 pF)	Receiver Inputs and Enables	≥6.5 kV
	Other Pins	≥2 kV

- (1) Absolute Maximum Ratings are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the devices should be operated at these limits. The table of [Electrical Characteristics](#) specifies conditions of device operation.
 (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

RECOMMENDED OPERATING CONDITIONS

	Min	Typ	Max	Units	
Supply Voltage (V_{CC})	3.0	3.3	3.6	V	
Operating Free Air	Temperature (T_A)	–40	+25	+85	°C

ELECTRICAL CHARACTERISTICS⁽¹⁾⁽²⁾

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified.

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units
V_{TH}	Differential Input Threshold	$V_{OUT} = V_{OH}$ or V_{OL} $-7V < V_{CM} < +7V$	RI+, RI-	-200	±17.5	+200	mV
V_{HY}	Hysteresis	$V_{CM} = 1.5V$			35		mV
V_{IH}	Minimum High Level Input Voltage		EN	2.0			V
V_{IL}	Minimum Low Level Input Voltage					0.8	V
R_{IN}	Input Resistance	$V_{IN} = -7V, +7V$ (Other Input = GND)	RI+, RI-	5.0	8.5		kΩ
I_{IN}	Input Current (Other Input = 0V, Power On or $V_{CC} = 0V$)	$V_{IN} = +10V$		0	1.1	1.8	mA
		$V_{IN} = +3V$		0	0.27		mA
		$V_{IN} = 0.5V$			-0.02		mA
		$V_{IN} = -3V$		0	-0.43		mA
		$V_{IN} = -10V$		0	-1.26	-2.2	mA
I_{EN}		$V_{IN} = 0V$ to V_{CC}	EN			±1	μA
V_{OH}	High Level Output Voltage	$I_{OH} = -6$ mA, $V_{ID} = +1V$ $I_{OH} = -6$ mA, $V_{ID} = OPEN$	RO	2.4	3		V
V_{OH}	High Level Output Voltage	$I_{OH} = -100$ μA, $V_{ID} = +1V$ $I_{OH} = -100$ μA, $V_{ID} = OPEN$			$V_{CC} - 0.1$		V
V_{OL}	Low Level Output Voltage	$I_{OL} = +6$ mA, $V_{ID} = -1V$			0.13	0.5	V
I_{OZ}	Output Tri-State Leakage Current	$V_{IN} = V_{CC}$ or GND EN = V_{IL}				±50	μA
I_{SC}	Output Short Circuit Current	$V_O = 0V$, $V_{ID} \geq 200$ mV See ⁽³⁾			-10	-35	-70
I_{CC}	Power Supply Current	No Load, All RI+, RI- = Open, EN = V_{CC} or GND	V_{CC}		9	15	mA

- (1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{ID} .
- (2) All typicals are given for: $V_{CC} = +3.3V$, $T_A = +25^\circ C$.
- (3) Short one output at a time to ground. Do not exceed package power dissipation ratings.

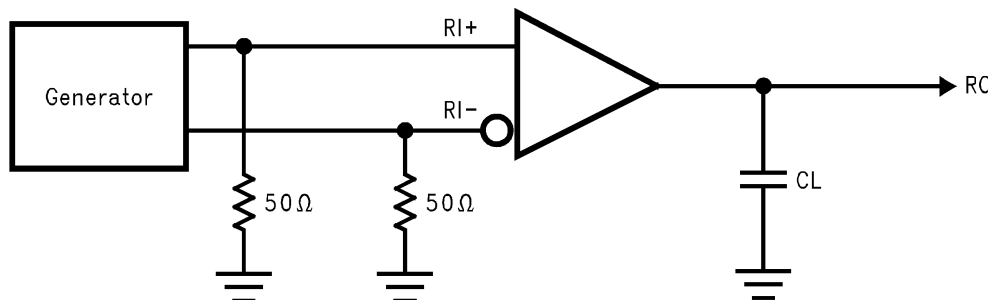
SWITCHING CHARACTERISTICS⁽¹⁾⁽²⁾⁽³⁾

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}	Propagation Delay High to Low	$C_L = 15\text{ pF}$ See (Figure 2 and Figure 3)	6	17.5	35	ns
t_{PLH}	Propagation Delay Low to High		6	17.8	35	ns
t_r	Rise Time (20% to 80%)			4.1	10	ns
t_f	Fall Time (80% to 20%)			3.3	10	ns
t_{PHZ}	Disable Time	$C_L = 50\text{ pF}$ See (Figure 4 and Figure 5)			40	ns
t_{PLZ}	Disable Time				40	ns
t_{PZH}	Enable Time				40	ns
t_{PZL}	Enable Time				40	ns
t_{SK1}	Skew, $ t_{PHL} - t_{PLH} $ See ⁽⁴⁾	$C_L = 15\text{ pF}$		0.3	4	ns
t_{SK2}	Skew, Pin to Pin See ⁽⁵⁾			0.6	4	ns
t_{SK3}	Skew, Part to Part See ⁽⁶⁾			7	17	ns
f_{MAX}	Maximum Operating Frequency See ⁽⁷⁾	$C_L = 15\text{ pF}$	32			MHz

- (1) All typicals are given for: $V_{CC} = +3.3\text{V}$, $T_A = +25^\circ\text{C}$.
- (2) Generator waveform for all tests unless otherwise specified: $f = 1\text{ MHz}$, Duty Cycle = 50%, $Z_O = 50\Omega$, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.
- (3) C_L includes probe and jig capacitance.
- (4) t_{SK1} is the $|t_{PHL} - t_{PLH}|$ of a channel.
- (5) t_{SK2} is the maximum skew between any two channels within a device, on either edge.
- (6) t_{SK3} is the difference in propagation delay times between any channels of any devices. This specification (maximum limit) applies to devices within $V_{CC} \pm 0.1\text{V}$ of one another, and a Delta $T_A = \pm 5^\circ\text{C}$ (between devices) within the operating temperature range. This parameter is specified by design and characterization.
- (7) All channels switching, output duty cycle criteria is 40%/60% measured at 50% Input = 1V to 2V, 50% Duty Cycle, $t_r/t_f \leq 5$. This parameter is ensured by design and characterization.

PARAMETER MEASUREMENT INFORMATION

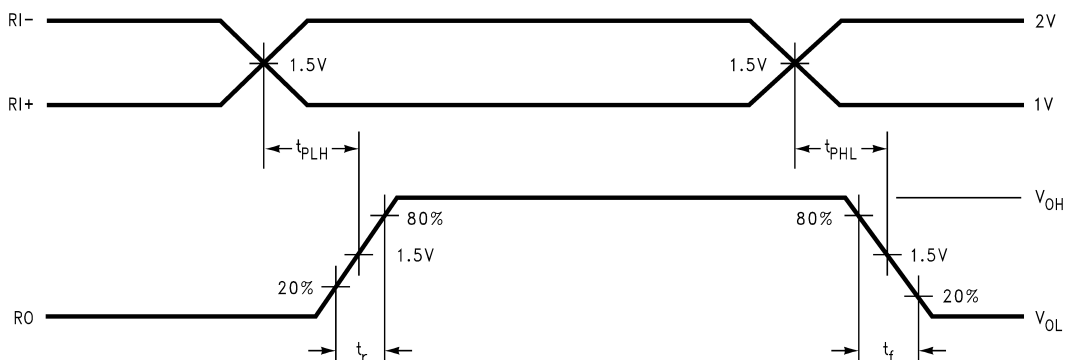


Generator waveform for all tests unless otherwise specified: $f = 1\text{ MHz}$, Duty Cycle = 50%, $Z_O = 50\Omega$, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

C_L includes probe and jig capacitance.

Figure 2. Receiver Propagation Delay and Transition Time Test Circuit

PARAMETER MEASUREMENT INFORMATION (continued)



Generator waveform for all tests unless otherwise specified: $f = 1 \text{ MHz}$, Duty Cycle = 50%, $Z_O = 50\Omega$, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$.

C_L includes probe and jig capacitance.

Figure 3. Receiver Propagation Delay and Transition Time Waveform

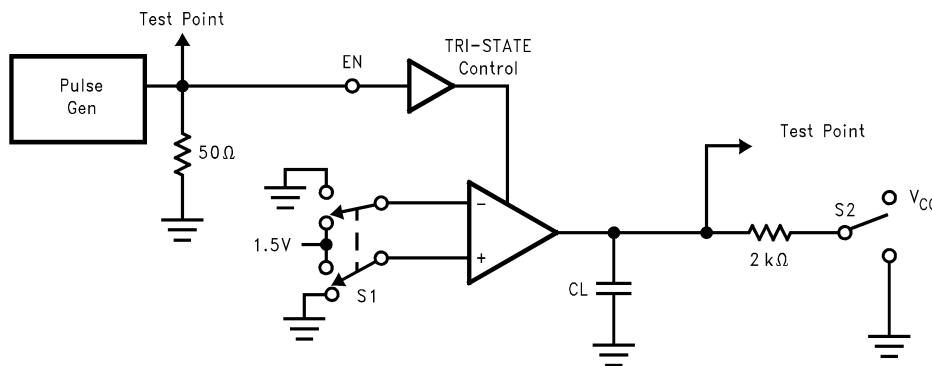
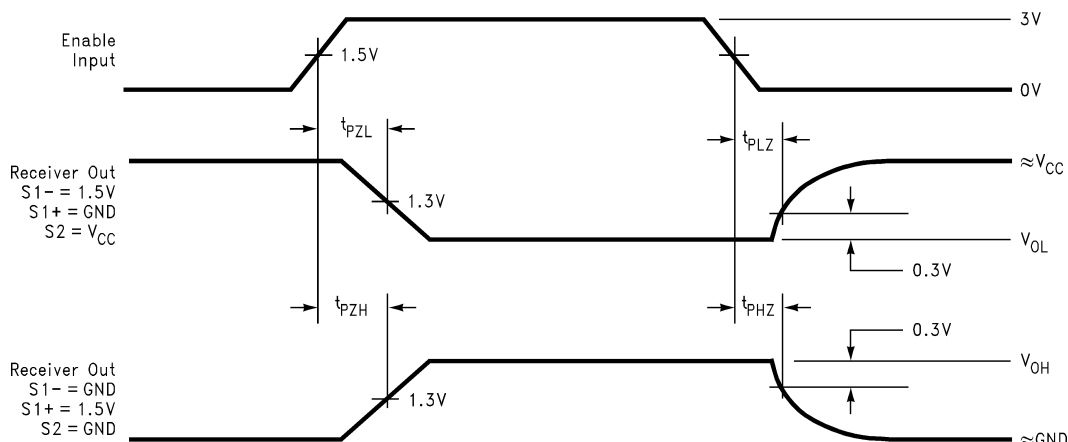


Figure 4. Receiver Tri-State Test Circuit



Generator waveform for all tests unless otherwise specified: $f = 1 \text{ MHz}$, Duty Cycle = 50%, $Z_O = 50\Omega$, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$.

C_L includes probe and jig capacitance.

Figure 5. Receiver Tri-State Output Enable and Disable Waveforms

TYPICAL APPLICATION INFORMATION

General application guidelines and hints for differential drivers receivers may be found in the following application notes:

AN-214 (SNLA137), AN-457 (SNLA148), AN-805 (SNOA233), AN-847 (SNLA031), AN-903 (SNLA034), AN-912 (SNLA036), AN-916 (SNLA219)

Power Decoupling Recommendations: Bypass caps must be used on power pins. High frequency ceramic (surface mount is recommended) 0.1 μ F in parallel with 0.01 μ F at the power supply pin. A 10 μ F or greater solid tantalum or electrolytic should be connected at the power entry point on the printed circuit board.

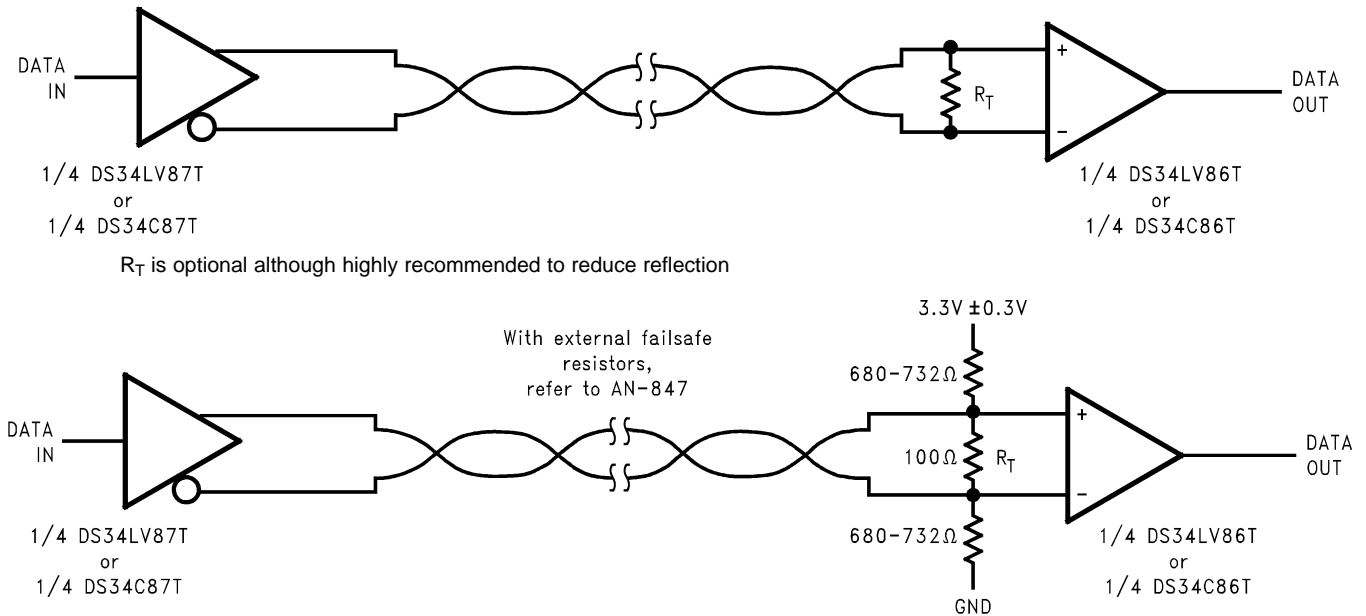


Figure 6. Typical Receiver Connections

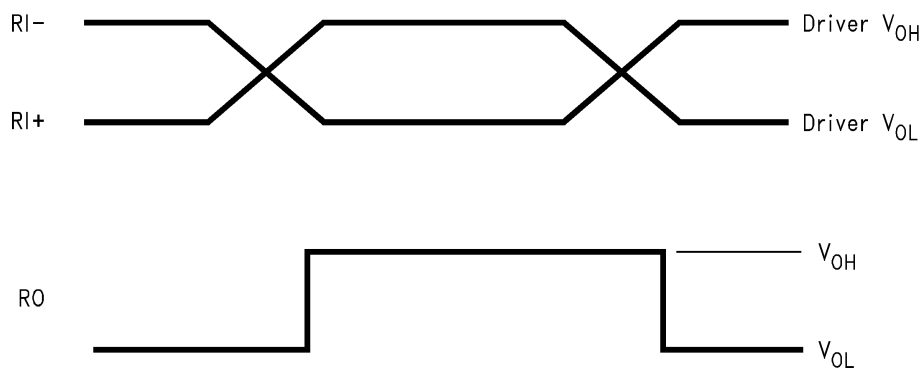


Figure 7. Typical Receiver Output Waveforms

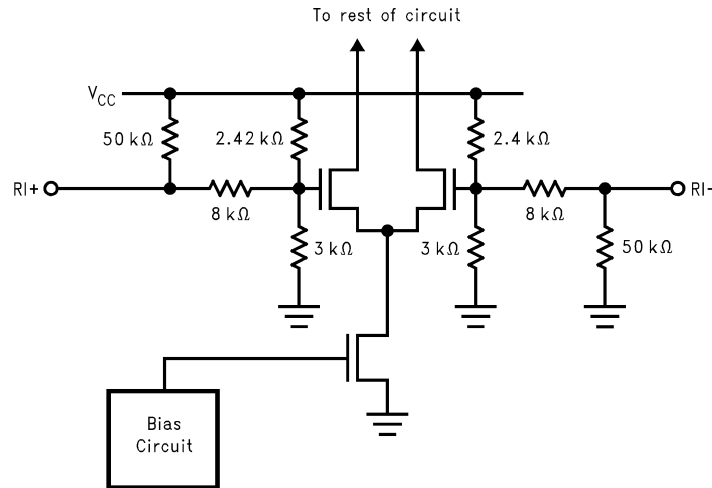


Figure 8. Typical Receiver Input Circuit

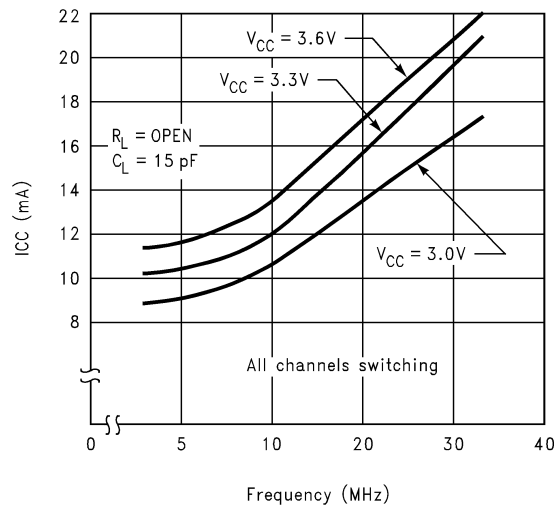


Figure 9. Typical ICC vs Frequency

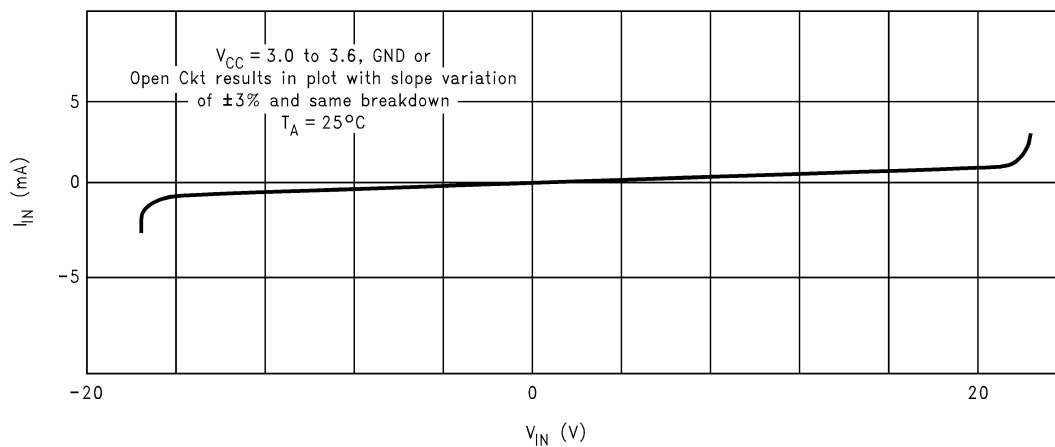


Figure 10. I_{IN} vs V_{IN} (Power On, Power Off)

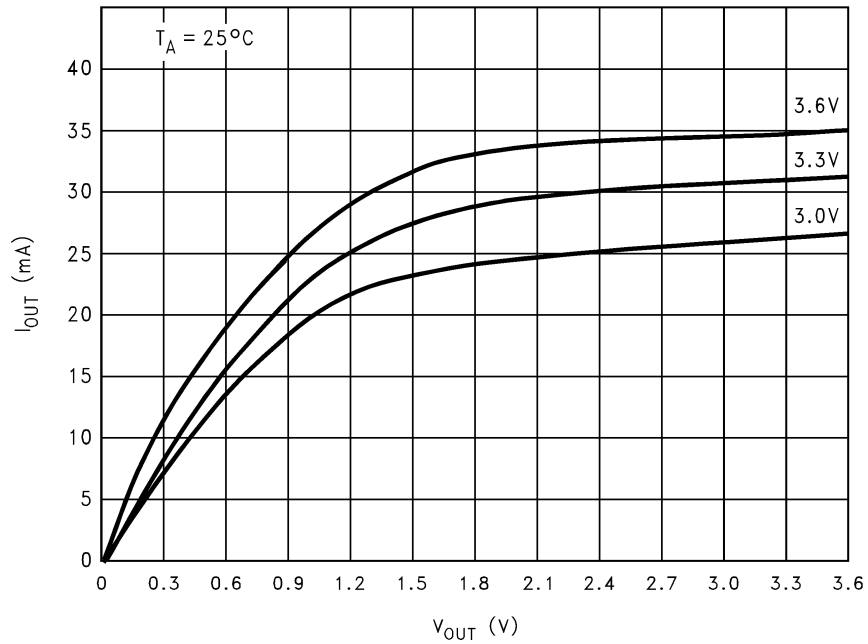


Figure 11. I_{OL} vs V_{OL}

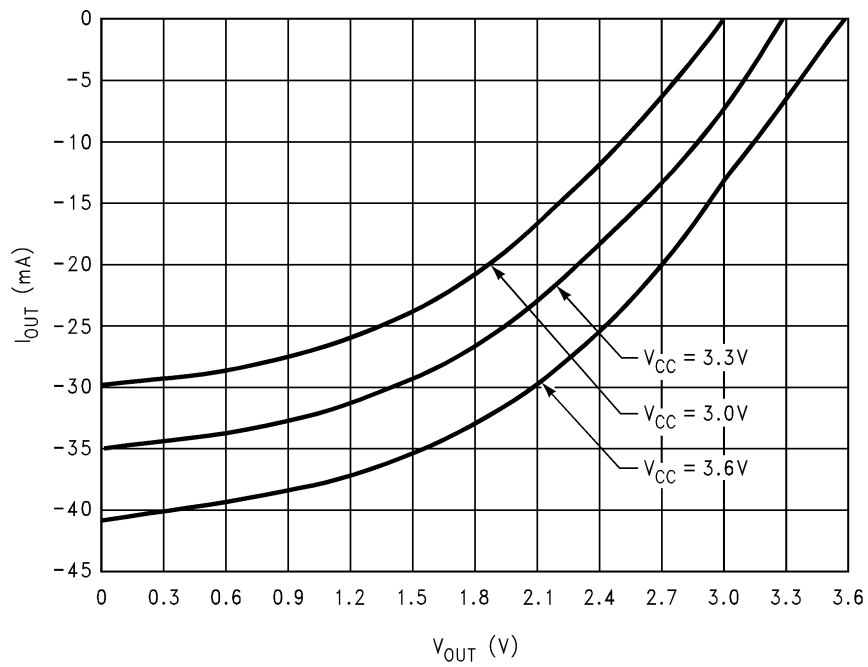


Figure 12. I_{OH} vs V_{OH}

REVISION HISTORY

Changes from Revision C (April 2013) to Revision D	Page
<hr/> <ul style="list-style-type: none">• Changed layout of National Data Sheet to TI format <hr/>	<hr/> 8 <hr/>

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS34LV86TM	NRND	SOIC	D	16	48	TBD	Call TI	Call TI	-40 to 85	DS34LV86 TM	
DS34LV86TM/NOPB	ACTIVE	SOIC	D	16	48	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS34LV86 TM	Samples
DS34LV86TMX	NRND	SOIC	D	16	2500	TBD	Call TI	Call TI	-40 to 85	DS34LV86 TM	
DS34LV86TMX/NOPB	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS34LV86 TM	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS34LV86TMX	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1
DS34LV86TMX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS34LV86TMX	SOIC	D	16	2500	367.0	367.0	35.0
DS34LV86TMX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com