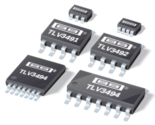
**Burr-Brown Products**
**from Texas Instruments**



# TLV3491
# TLV3492
# TLV3494

SBOS262D – DECEMBER 2002 – REVISED APRIL 2005

# 1.8V, Nanopower, PUSH-PULL OUTPUT COMPARATOR

## FEATURES

- **VERY LOW SUPPLY CURRENT: 0.8µA (typ)**
- **INPUT COMMON-MODE RANGE 200mV BEYOND SUPPLY RAILS**
- **SUPPLY VOLTAGE: +1.8V to +5.5V**
- **HIGH SPEED: 6µs**
- **PUSH-PULL CMOS OUTPUT STAGE**
- **SMALL PACKAGES:**
  **SOT23-5 (Single)**
  **SOT23-8 (Dual)**

## APPLICATIONS

- **PORTABLE MEDICAL EQUIPMENT**
- **WIRELESS SECURITY SYSTEMS**
- **REMOTE CONTROL SYSTEMS**
- **HANDHELD INSTRUMENTS**
- **ULTRA-LOW POWER SYSTEMS**

## DESCRIPTION

The TLV349x family of push-pull output comparators features a fast 6µs response time and < 1.2µA (max) nanopower capability, allowing operation from 1.8V – 5.5V. Input common-mode range beyond supply rails make the TLV349x an ideal choice for low-voltage applications.

Micro-sized packages provide options for portable and space-restricted applications. The single (TLV3491) is available in SOT23-5 and SO-8. The dual (TLV3492) comes in SOT23-8 and SO-8. The quad (TLV3494) is available in TSSOP-14 and SO-14.

The TLV349x is excellent for power-sensitive, low-voltage (2-cell) applications.

### TLV349x RELATED PRODUCTS

| PRODUCT | FEATURES |
|---|---|
| TLV370x | 560nA, 2.5V to 16V, Push-Pull CMOS Output Stage Comparator |
| TLV340x | 550nA, 2.5V to 16V, Open Drain Output Stage Comparator |

## ABSOLUTE MAXIMUM RATINGS(1)

| | |
|---|---|
| Supply Voltage | +5.5V |
| Signal Input Terminals, Voltage(2) | (V–) – 0.5V to (V+) + 0.5V |
| Current(2) | ±10mA |
| Output Short-Circuit(3) | Continuous |
| Operating Temperature | –40°C to +125°C |
| Storage Temperature | –65°C to +150°C |
| Junction Temperature | +150°C |
| Lead Temperature (soldering, 10s) | +300°C |
| ESD Rating (Human Body Model) | 3000V |

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied. (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less. (3) Short-circuit to ground, one amplifier per package.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

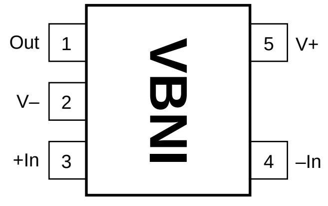
## PACKAGE/ORDERING INFORMATION(1)

| PRODUCT | PACKAGE-LEAD | PACKAGE DESIGNATOR | SPECIFIED TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER | TRANSPORT MEDIA, QUANTITY |
|---|---|---|---|---|---|---|
| TLV3491 | SOT23-5 | DBV | –40°C to +125°C | VBNI | TLV3491AIDBVT | Tube, 250 |
| " | " | " | " | " | TLV3491AIDBVR | Tape and Reel, 3000 |
| TLV3491 | SO-8 | D | –40°C to +125°C | TLV3491 | TLV3491AID | Tube, 100 |
| " | " | " | " | " | TLV3491AIDR | Tube, 2500 |
| TLV3492 | SOT23-8 | DCN | –40°C to +125°C | VBO1 | TLV3492AIDCNT | Tube, 250 |
| " | " | " | " | " | TLV3492AIDCNR | Tape and Reel, 3000 |
| TLV3492 | SO-8 | D | –40°C to +125°C | TLV3492 | TLV3492AID | Tube, 100 |
| " | " | " | " | " | TLV3492AIDR | Tape and Reel, 2500 |
| TLV3494 | TSSOP-14 | PW | –40°C to +125°C | TLV3494 | TLV3494AIPWT | Tape and Reel, 94 |
| " | " | " | " | " | TLV3494AIPWR | Tape and Reel, 2500 |
| TLV3494 | SO-14 | D | –40°C to +125°C | TLV3494 | TLV3494AID | Tape and Reel, 58 |
| " | " | " | " | " | TLV3494AIDR | Tape and Reel, 2500 |

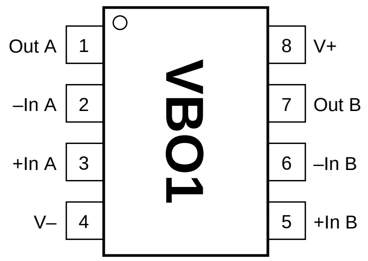
NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

## PIN CONFIGURATIONS

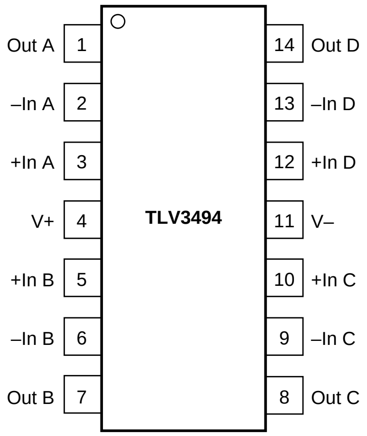
**Top View**



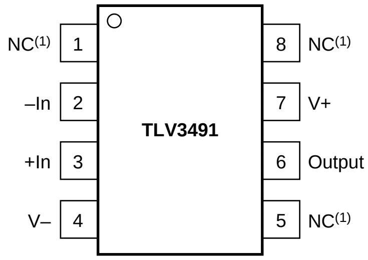
SOT23-5



SOT23-8
SO-8



TSSOP-14
SO-14



SO-8

**NOTES: (1) NC means no internal connection.**

# ELECTRICAL CHARACTERISTICS: $V_S$ = +1.8V to +5.5V

## **Boldface** limits apply over the specified temperature range, **$T_A$ = –40°C to +125°C.**

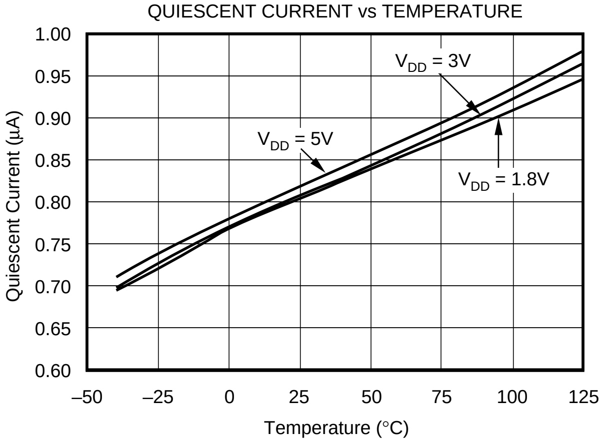
At $T_A$ = +25°C, and $V_S$ = +1.8V to +5.5V, unless otherwise noted.

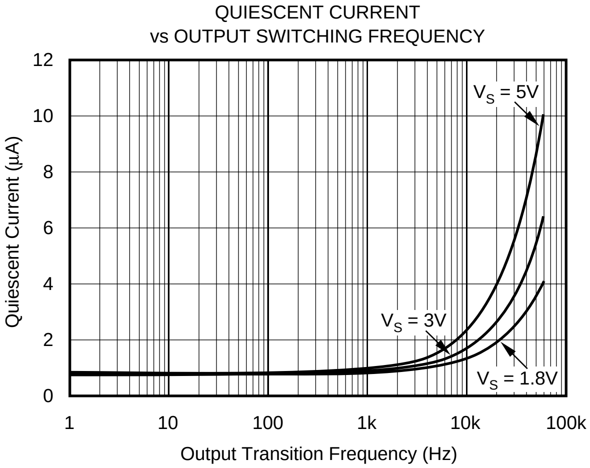
| PARAMETER | | CONDITION | TLV3491, TLV3492, TLV3494 | | | UNITS |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| **OFFSET VOLTAGE** | $V_{OS}$ | | | | | |
| Input Offset Voltage | | $V_{CM}$ = 0V, $I_O$ = 0V | | ±3 | ±15 | mV |
| **vs Temperature** | **$dV_{OS}/dT$** | **$T_A$ = –40°C to +125°C** | | **±12** | | **μV/°C** |
| vs Power Supply | PSRR | $V_S$ = 1.8V to 5.5V | | 350 | 1000 | μV/V |
| **INPUT BIAS CURRENT** | | | | | | |
| Input Bias Current | $I_B$ | $V_{CM} = V_{CC}/2$ | | ±1 | ±10 | pA |
| Input Offset Current | $I_{OS}$ | $V_{CM} = V_{CC}/2$ | | ±1 | ±10 | pA |
| **INPUT VOLTAGE RANGE** | | | | | | |
| Common-Mode Voltage Range | $V_{CM}$ | | (V–) – 0.2V | | (V+) + 0.2V | V |
| Common-Mode Rejection Ratio | CMRR | $V_{CM}$ = –0.2V to (V+) – 1.5V | 60 | 74 | | dB |
| | | $V_{CM}$ = –0.2V to (V+) + 0.2V | 54 | 62 | | dB |
| **INPUT CAPACITANCE** | | | | | | |
| Common-Mode | | | | 2 | | pF |
| Differential | | | | 4 | | pF |
| **SWITCHING CHARACTERISTICS** | | f = 10kHz, $V_{STEP}$ = 1V | | | | |
| Propagation Delay Time, Low-to-High | $t_{(PLH)}$ | Input Overdrive = 10mV | | 12 | | μs |
| | | Input Overdrive = 100mV | | 6 | | μs |
| Propagation Delay Time, High-to-Low | $t_{(PHL)}$ | Input Overdrive = 10mV | | 13.5 | | μs |
| | | Input Overdrive = 100mV | | 6.5 | | μs |
| Rise Time | $t_R$ | $C_L$ = 10pF | | 100 | | ns |
| Fall Time | $t_F$ | $C_L$ = 10pF | | 100 | | ns |
| **OUTPUT** | | $V_S$ = 5V | | | | |
| Voltage Output High from Rail | $V_{OH}$ | $I_{OUT}$ = 5mA | | 90 | 200 | mV |
| Voltage Output Low from Rail | $V_{OL}$ | $I_{OUT}$ = 5mA | | 160 | 200 | mV |
| Short-Circuit Current | $I_{SC}$ | | | See Typical Characteristics | | |
| **POWER SUPPLY** | | | | | | |
| Specified Voltage | $V_S$ | | 1.8 | | 5.5 | V |
| Operating Voltage Range | | | 1.8 | | 5.5 | V |
| Quiescent Current(1) | $I_Q$ | $V_O$ = 5V, $V_O$ = High | | 0.85 | 1.2 | μA |
| **TEMPERATURE RANGE** | | | | | | |
| Specified Range | | | –40 | | +125 | °C |
| Operating Range | | | –40 | | +125 | °C |
| Storage Range | | | –65 | | +150 | °C |
| Thermal Resistance, $\theta_{JA}$ | | | | | | |
| SOT23-5, SOT23-8 | | | | 200 | | °C/W |
| SO-8 | | | | 150 | | °C/W |
| SO-14, TSSOP-14 | | | | 100 | | °C/W |

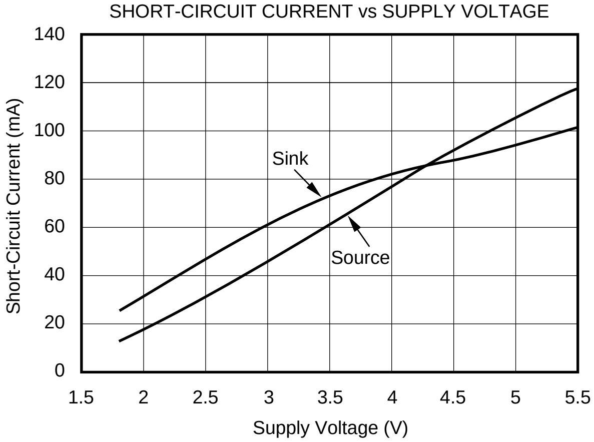
NOTE: (1) $I_Q$ per channel.

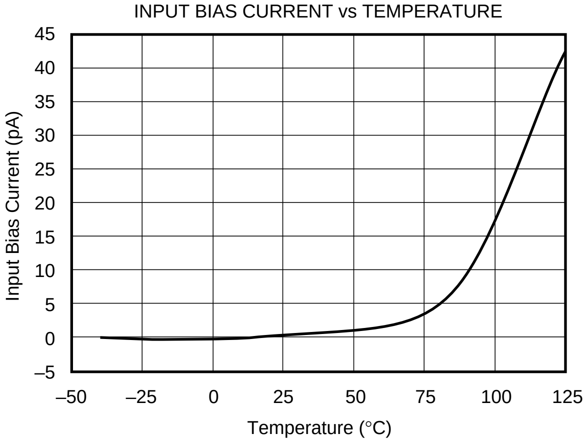
# TYPICAL CHARACTERISTICS

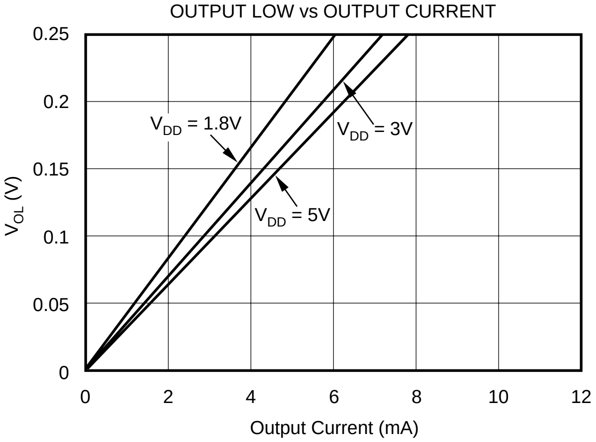
At $T_A$ = +25°C, $V_S$ = +1.8V to +5.5V, and Input Overdrive = 100mV, unless otherwise noted.

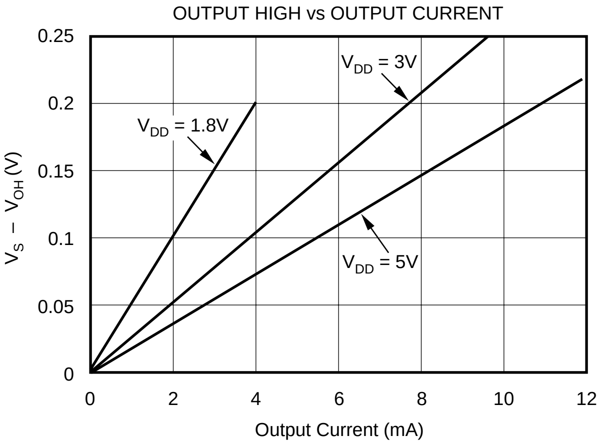






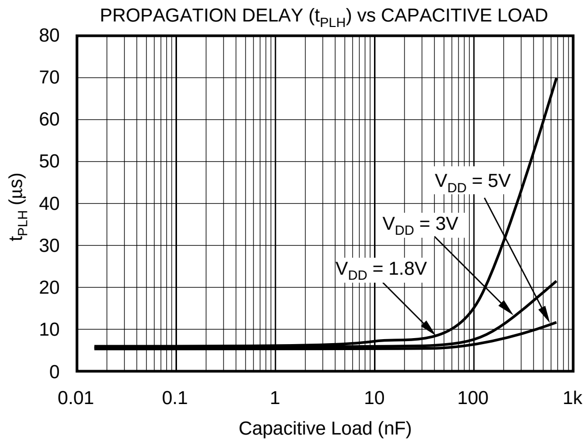


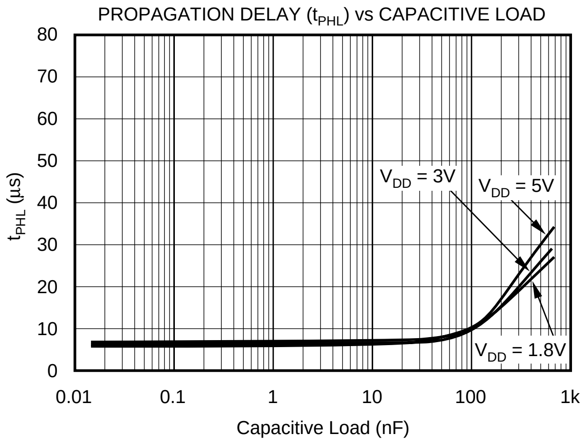


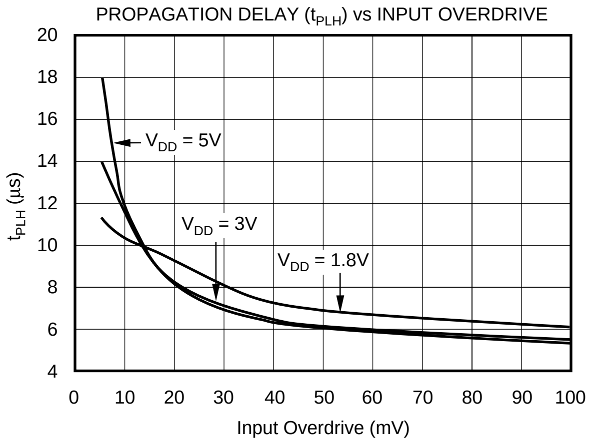


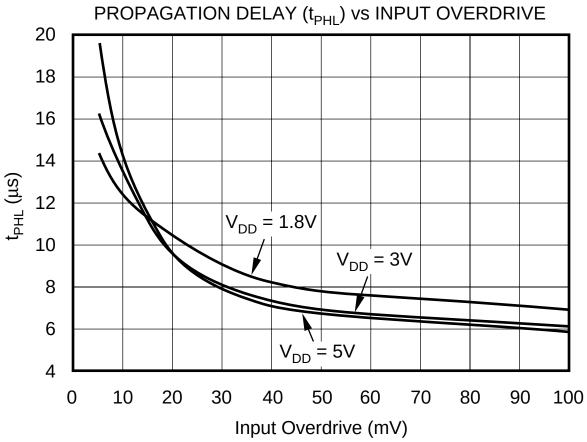
# TYPICAL CHARACTERISTICS (Cont.)

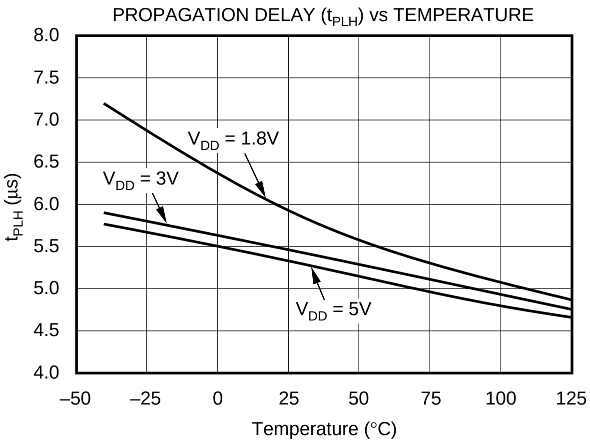
At $T_A$ = +25°C, $V_S$ = +1.8V to +5.5V, and Input Overdrive = 100mV, unless otherwise noted.

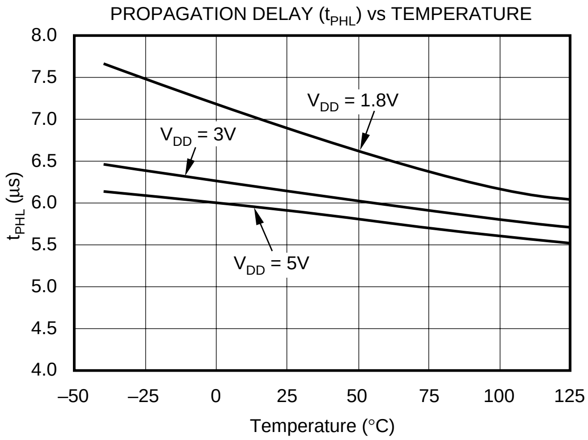








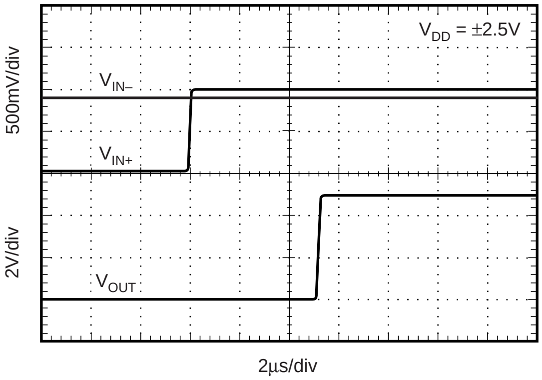




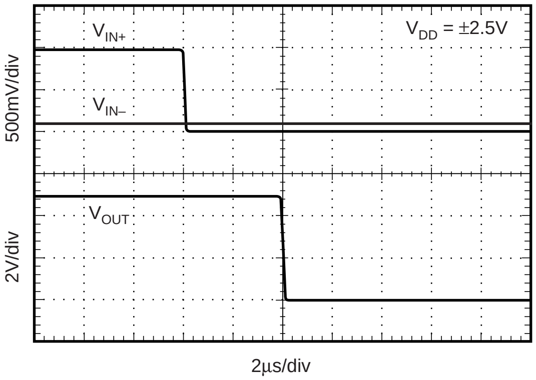
# TYPICAL CHARACTERISTICS (Cont.)

At $T_A$ = +25°C, $V_S$ = +1.8V to +5.5V, and Input Overdrive = 100mV, unless otherwise noted.

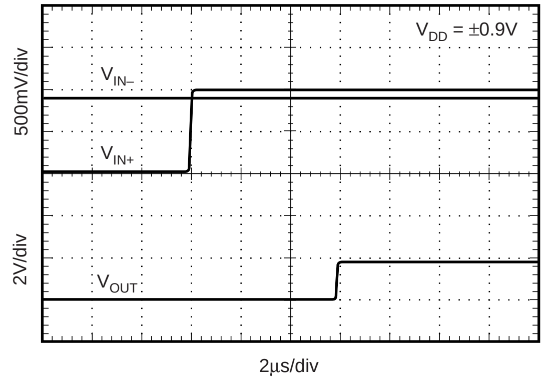
PROPAGATION DELAY ($t_{PLH}$)



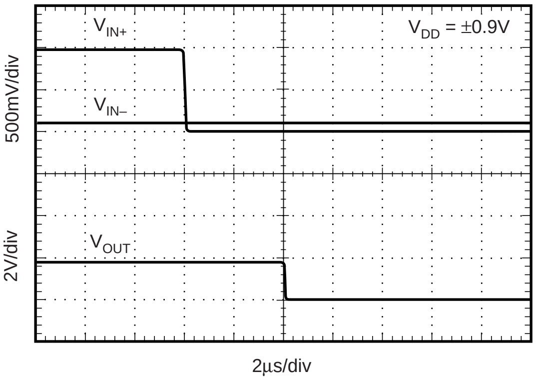
PROPAGATION DELAY ($t_{PHL}$)



PROPAGATION DELAY ($t_{PLH}$)



PROPAGATION DELAY ($t_{PHL}$)



# APPLICATIONS INFORMATION

The TLV349x family of comparators features rail-to-rail input and output on supply voltages as low as 1.8V. The push-pull output stage is optimal for reduced power budget applications and features no shoot-through current. Low supply voltages, common-mode input range beyond supply rails, and a typical supply current of 0.8µA make the TLV349x family an excellent candidate for battery-powered applications with single-cell operation.

## BOARD LAYOUT

Figure 1 shows the typical connections for the TLV349x. To minimize supply noise, power supplies should be capacitively decoupled by a 0.01µF ceramic capacitor in parallel with a 10µF electrolytic capacitor. Comparators are very sensitive to input noise. Proper grounding (use of ground plane) will help maintain specified performance of the TLV349x family.

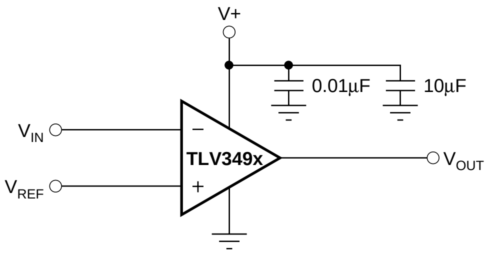


FIGURE 1. Basic Connections of the TLV349x.

## SETTING REFERENCE VOLTAGE

It is important to use a stable reference when setting the transition point for the TLV349x. The REF1004 provides a 1.25V reference voltage with low drift and only 8µA of quiescent current.

## EXTERNAL HYSTERESIS

Comparator inputs have no noise immunity within the range of specified offset voltage (±15mV). For noisy input signals, the comparator output may display multiple switching as input signals move through the switching threshold. The typical comparator threshold of the TLV349x is ±15mV. To prevent multiple switching within the comparator threshold of the TLV349x, external hysteresis may be added by connecting a small amount of feedback to the positive input. Figure 2 shows a typical topology used to introduce hysteresis, described by the equation:

$$V_{HYST} = \frac{V^{+} \times R_1}{R_1 + R_2}$$

$V_{HYST}$ will set the value of the transition voltage required to switch the comparator output by increasing the threshold region, thereby reducing sensitivity to noise.

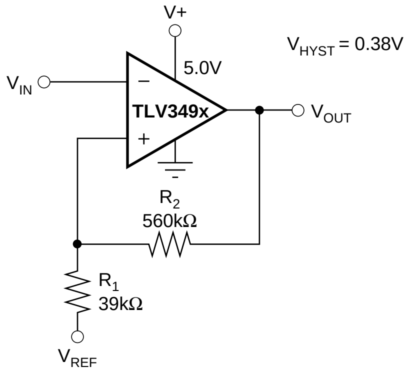


FIGURE 2. Adding Hysteresis to the TLV349x.

# APPLICATIONS

## RELAXATION OSCILLATOR

The TLV349x can be configured as a relaxation oscillator to provide a simple and inexpensive clock output (see Figure 3.) The capacitor is charged at a rate of 0.69RC. It also discharges at a rate of 0.69RC. Therefore, the period is 1.38RC. $R_1$ may be a different value than $R_2$.

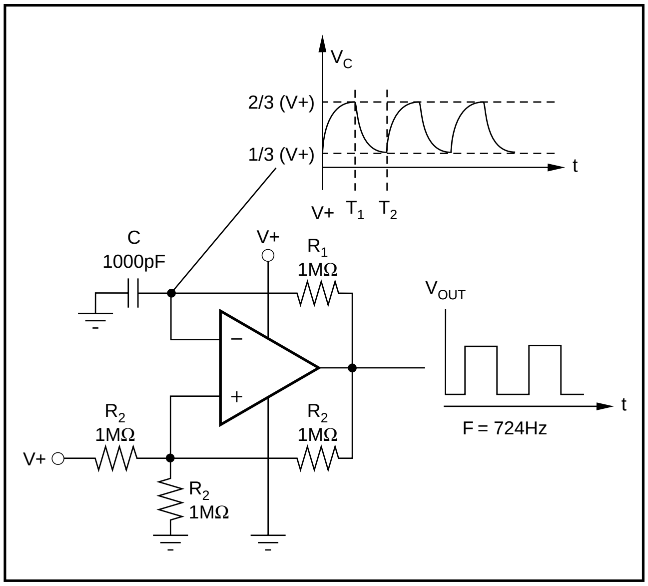


FIGURE 3. TLV349x Configured as a Relaxation Oscillator.

## POWER-ON RESET

The reset circuit shown in Figure 4 provides a time delayed release of reset to the MSP430 microcontroller. Operation of the circuit is based on a stabilization time constant of the supply voltage, rather than on a predetermined voltage value. The negative input is a reference voltage created by a simple resistor divider. These resistor values should be relatively high to reduce the current consumption of the circuit. The positive input is an RC circuit that provides a power-up delay. When power is applied, the output of the comparator is low, holding the processor in the reset condition. Only after allowing time for the supply voltage to stabilize does the positive input of the comparator become higher than the negative input, resulting in a high output state and releasing the processor for operation. The stabilization time required for the supply voltage is adjustable by the selection of the RC component values. Use of a lower-valued resistor in this portion of the circuit will not increase current consumption because no current flows through the RC circuit after the supply has stabilized. The reset delay time needed depends on the power-up characteristics of the system power supply. $R_1$ and $C_1$ are selected to allow enough time for the power supply to stabilize. D1 provides rapid reset if power is lost. In this example, the $R_1 \cdot C_1$ time constant is 10ms.

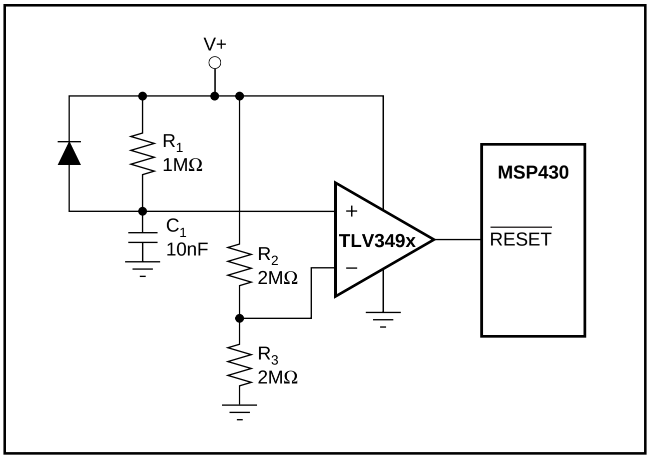


FIGURE 4. The TLV349x Configured as a Reset Circuit for the MSP430.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV3491AID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TLV<br>3491 | Samples |
| TLV3491AIDBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | VBNI | Samples |
| TLV3491AIDBVRG4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | VBNI | Samples |
| TLV3491AIDBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | VBNI | Samples |
| TLV3491AIDBVTG4 | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | VBNI | Samples |
| TLV3491AIDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TLV<br>3491 | Samples |
| TLV3491AIDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TLV<br>3491 | Samples |
| TLV3491AIDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TLV<br>3491 | Samples |
| TLV3492AID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TLV<br>3492 | Samples |
| TLV3492AIDCNR | ACTIVE | SOT-23 | DCN | 8 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VBO1 | Samples |
| TLV3492AIDCNRG4 | ACTIVE | SOT-23 | DCN | 8 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VBO1 | Samples |
| TLV3492AIDCNT | ACTIVE | SOT-23 | DCN | 8 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VBO1 | Samples |
| TLV3492AIDCNTG4 | ACTIVE | SOT-23 | DCN | 8 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VBO1 | Samples |
| TLV3492AIDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TLV<br>3492 | Samples |
| TLV3492AIDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TLV<br>3492 | Samples |
| TLV3492AIDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TLV<br>3492 | Samples |
| TLV3494AID | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TLV3494 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV3494AIDG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TLV3494 | Samples |
| TLV3494AIPWR | ACTIVE | TSSOP | PW | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TLV<br>3494 | Samples |
| TLV3494AIPWRG4 | ACTIVE | TSSOP | PW | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TLV<br>3494 | Samples |
| TLV3494AIPWT | ACTIVE | TSSOP | PW | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TLV<br>3494 | Samples |
| TLV3494AIPWTG4 | ACTIVE | TSSOP | PW | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TLV<br>3494 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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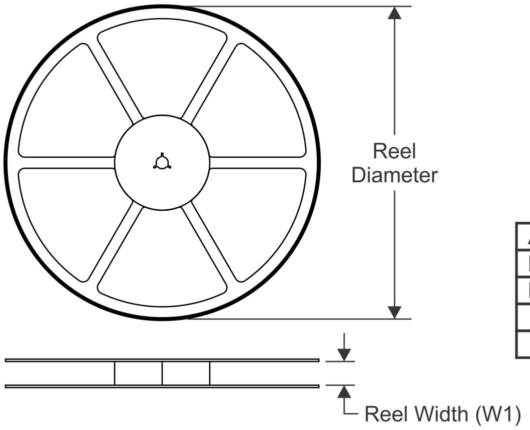
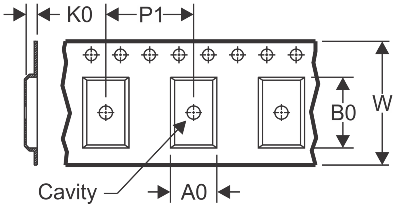
## TAPE AND REEL INFORMATION

REEL DIMENSIONS

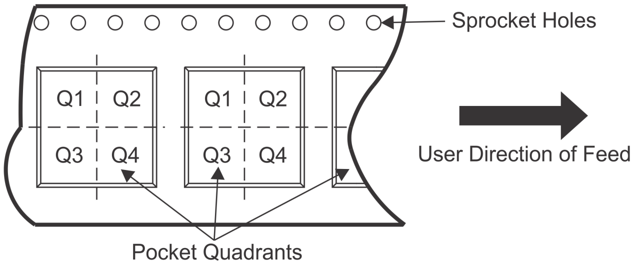


TAPE DIMENSIONS



| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

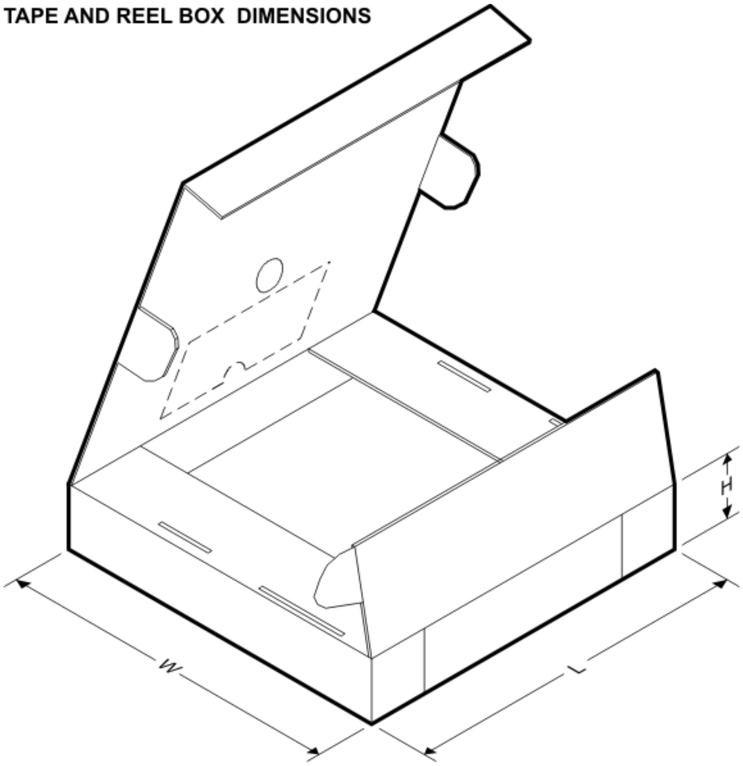
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV3491AIDBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV3491AIDBVT | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV3491AIDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV3492AIDCNR | SOT-23 | DCN | 8 | 3000 | 180.0 | 8.4 | 3.2 | 3.1 | 1.39 | 4.0 | 8.0 | Q3 |
| TLV3492AIDCNT | SOT-23 | DCN | 8 | 250 | 180.0 | 8.4 | 3.2 | 3.1 | 1.39 | 4.0 | 8.0 | Q3 |
| TLV3492AIDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV3494AIPWR | TSSOP | PW | 14 | 2500 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TLV3494AIPWT | TSSOP | PW | 14 | 250 | 180.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

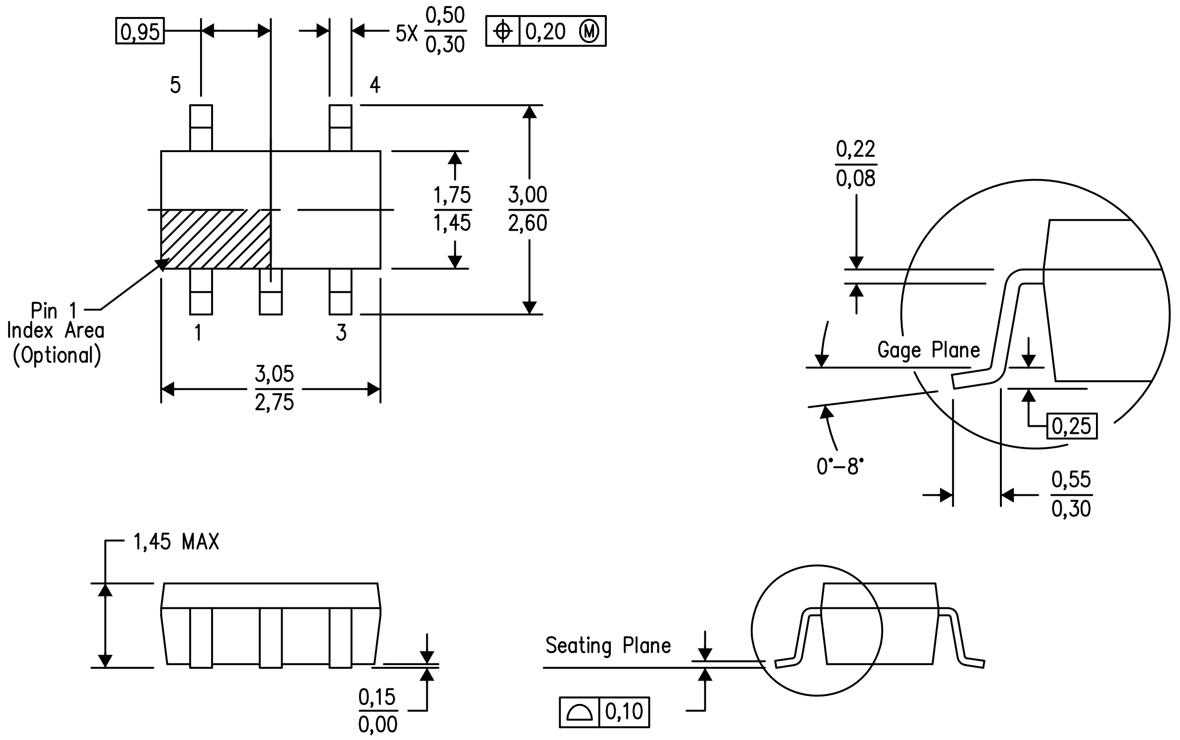
## TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TLV3491AIDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TLV3491AIDBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TLV3491AIDR | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| TLV3492AIDCNR | SOT-23 | DCN | 8 | 3000 | 210.0 | 185.0 | 35.0 |
| TLV3492AIDCNT | SOT-23 | DCN | 8 | 250 | 210.0 | 185.0 | 35.0 |
| TLV3492AIDR | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| TLV3494AIPWR | TSSOP | PW | 14 | 2500 | 367.0 | 367.0 | 35.0 |
| TLV3494AIPWT | TSSOP | PW | 14 | 250 | 210.0 | 185.0 | 35.0 |

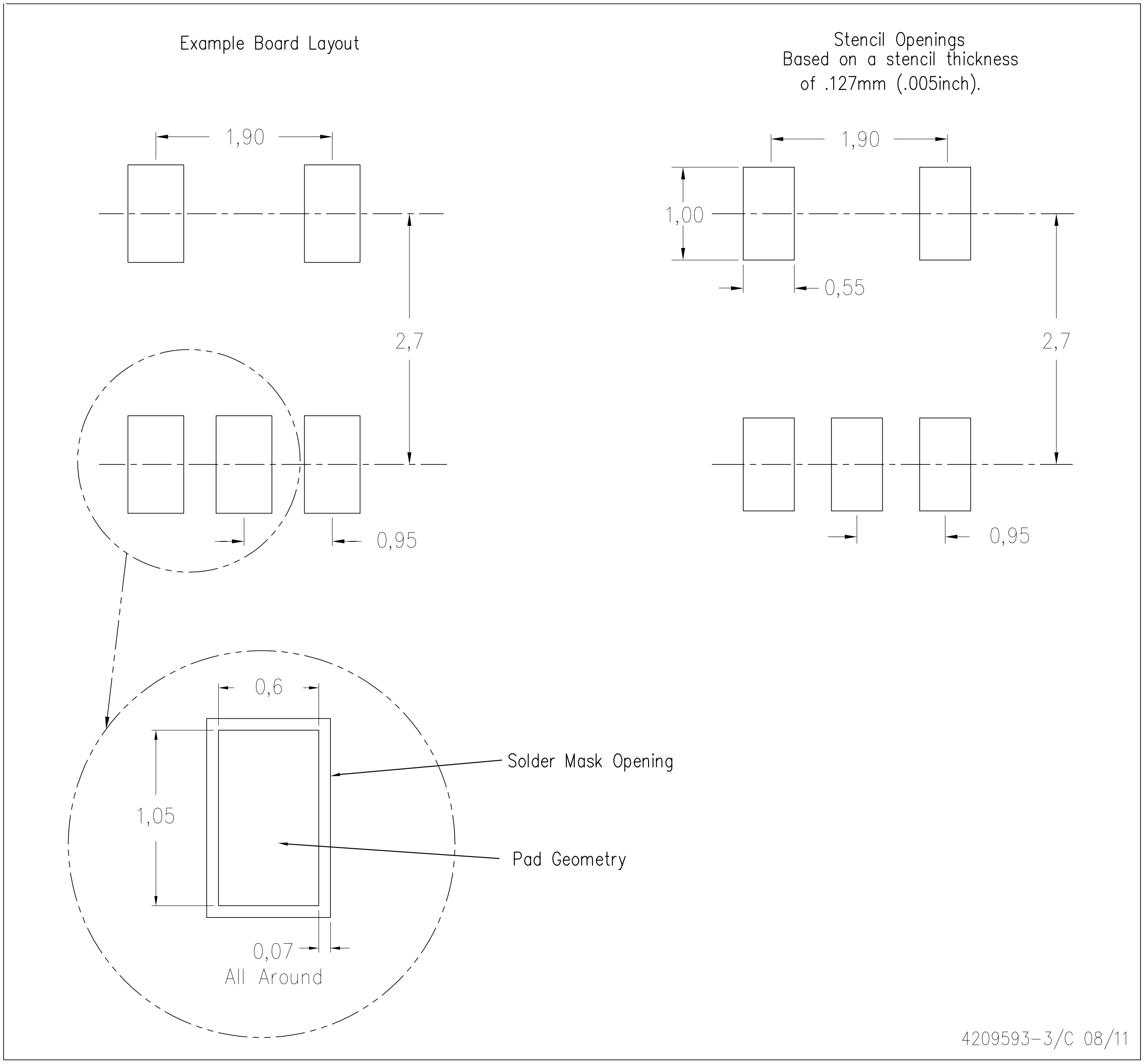
DBV (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



4073253-4/L 08/2013

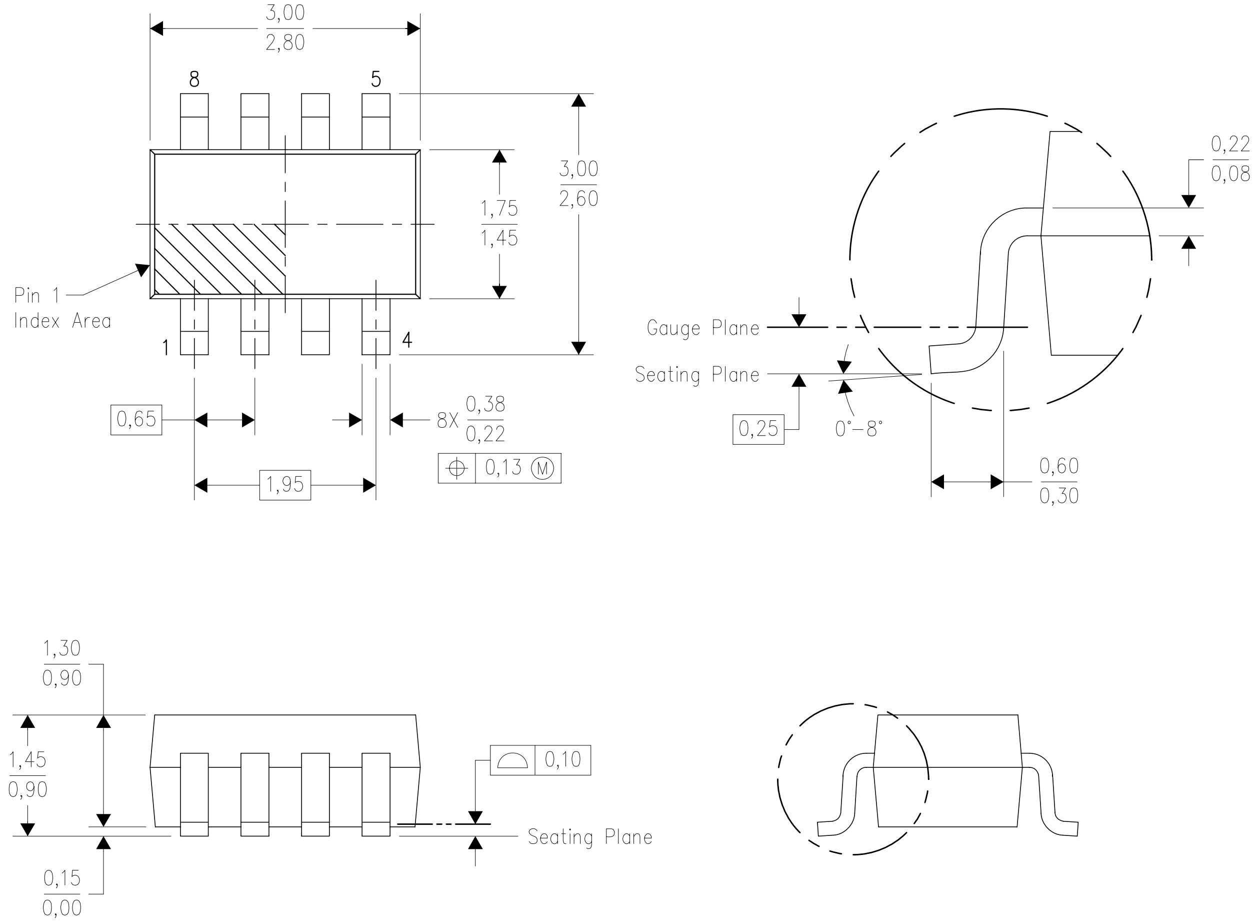
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-178 Variation AA.

DBV (R–PDSO–G5)　　PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC–7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

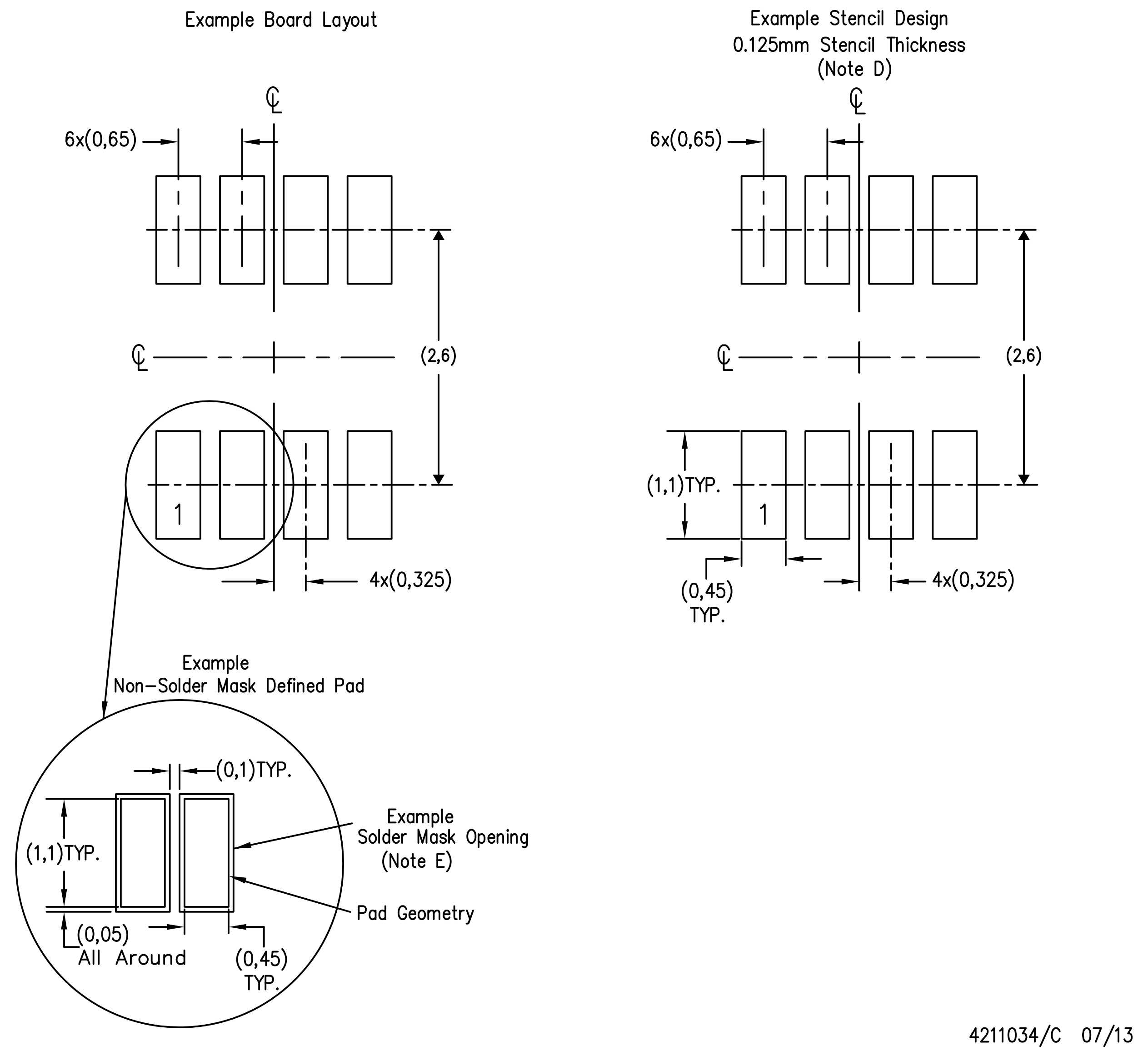
## DCN (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



4202106/D 11/2009

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Package outline exclusive of metal burr & dambar protrusion/intrusion.
- D. Package outline inclusive of solder plating.
- E. A visual index feature must be located within the Pin 1 index area.
- F. Falls within JEDEC MO–178 Variation BA.
- G. Body dimensions do not include flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

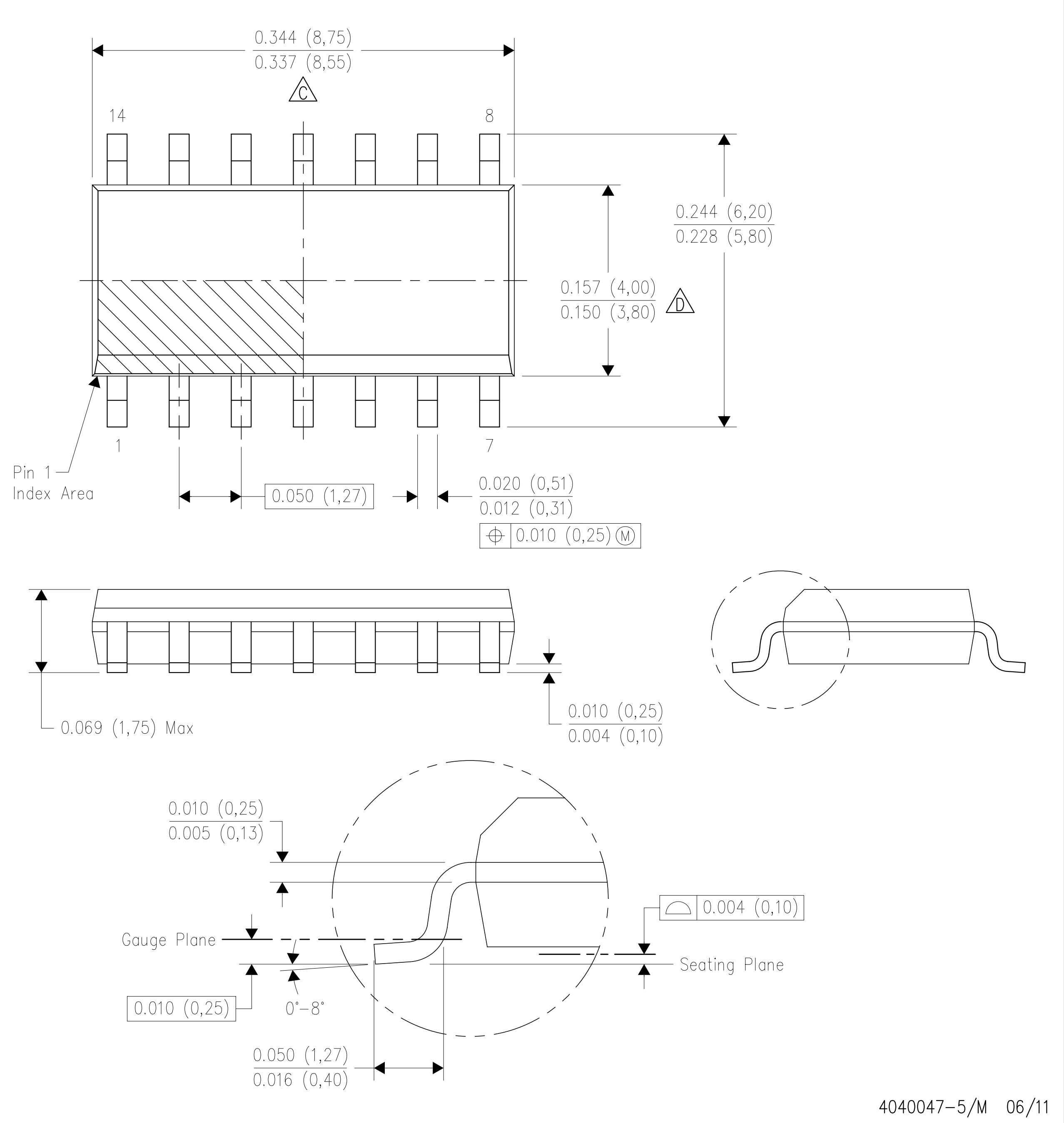
## DCN (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



4211034/C 07/13

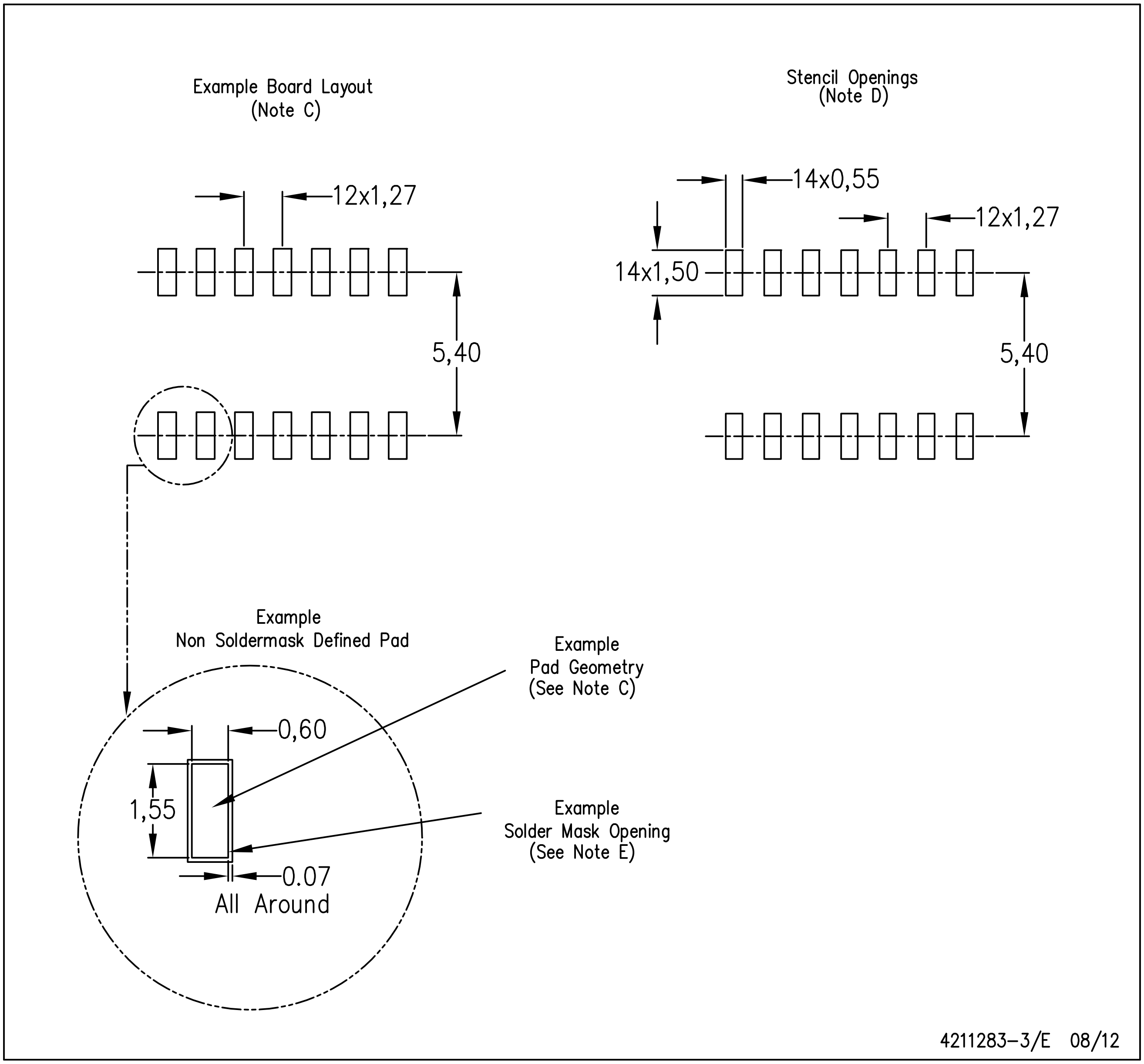
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



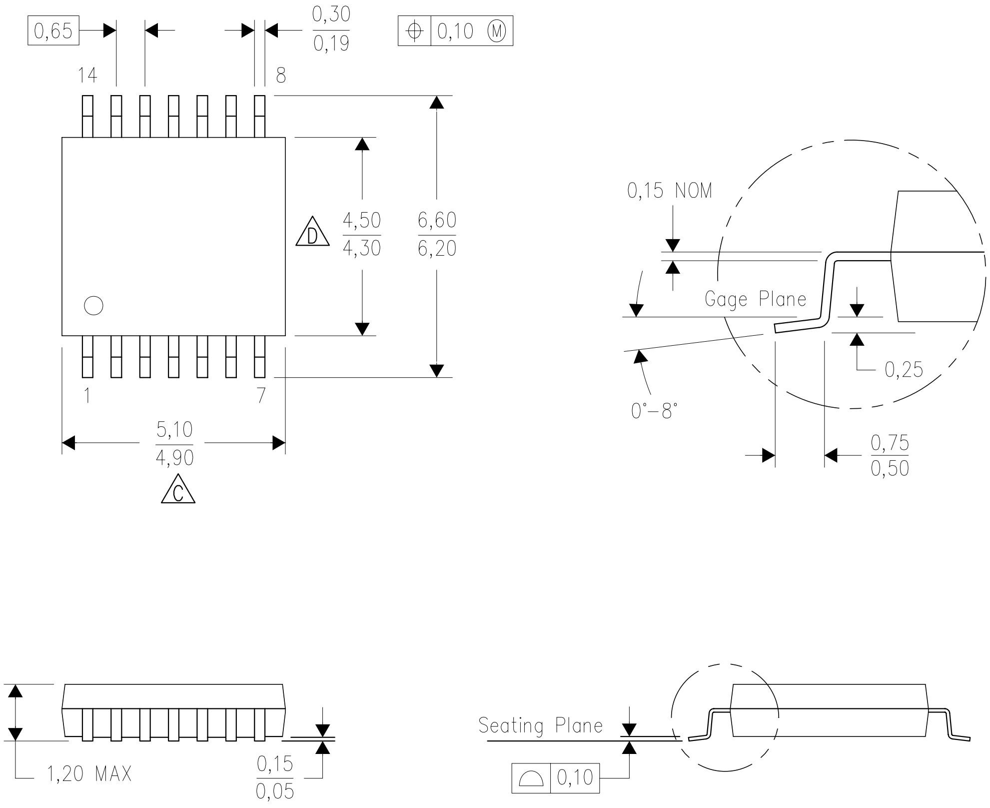
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- △C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- △D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS–012 variation AB.

D (R-PDSO-G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

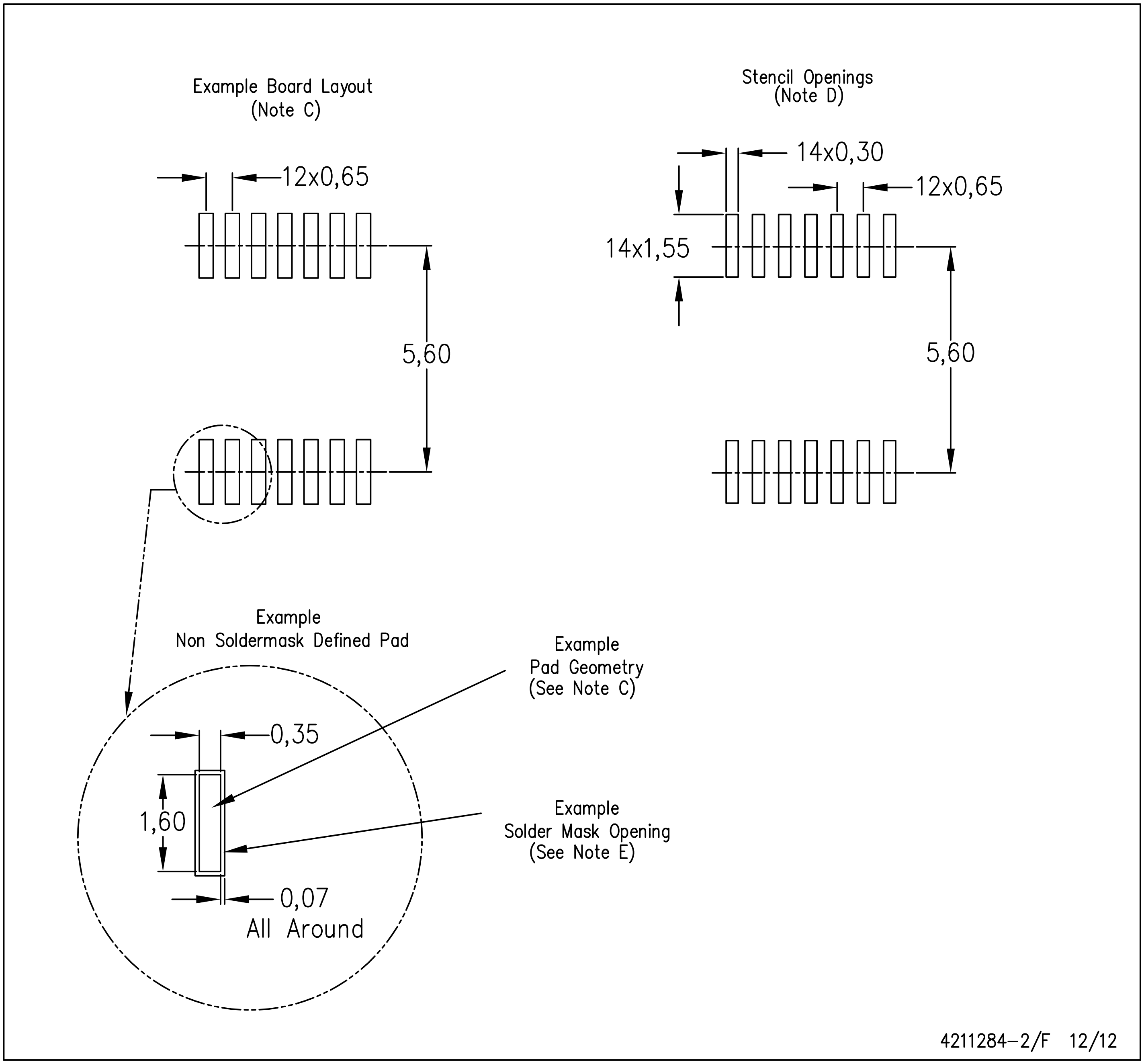
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

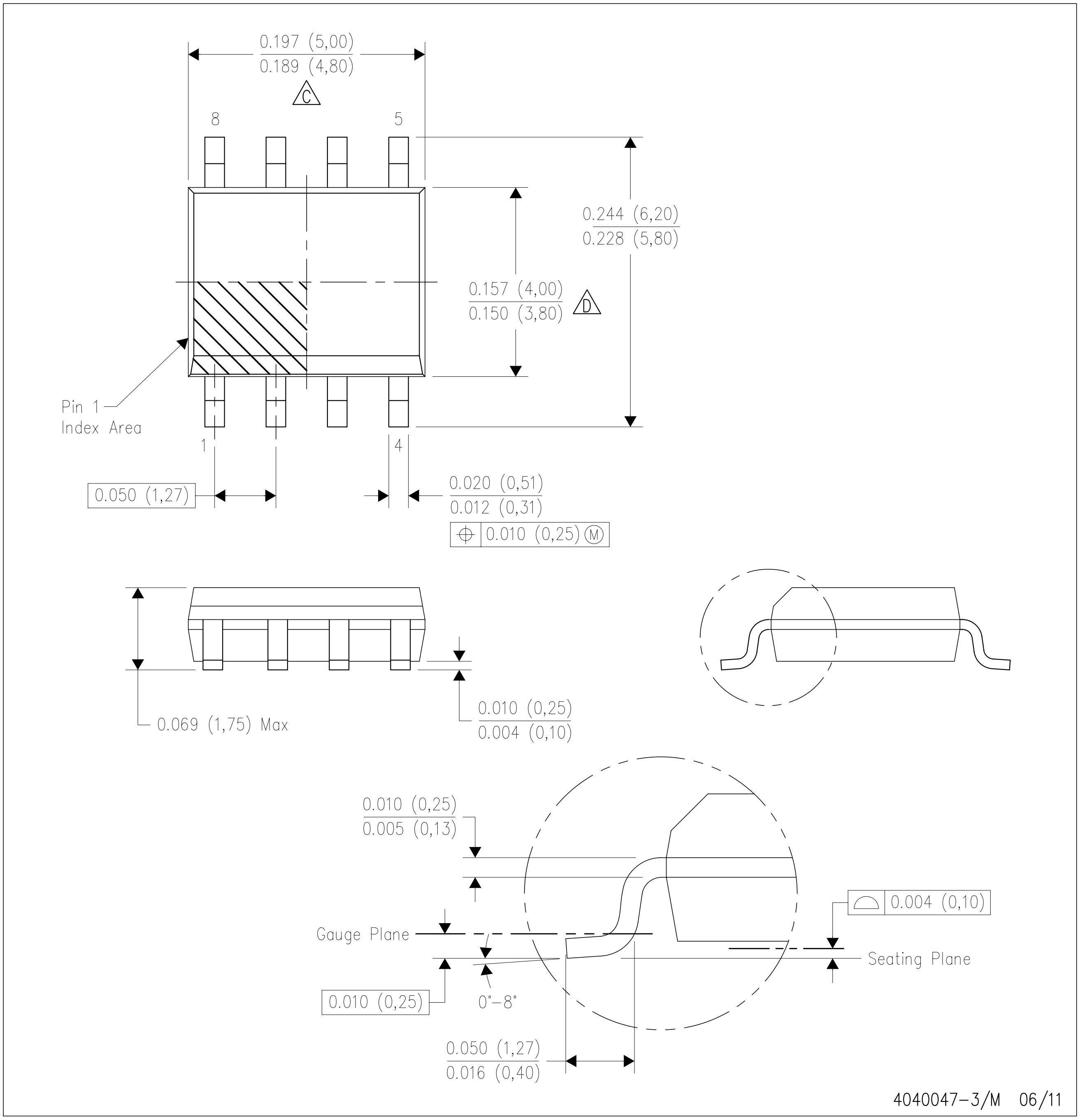
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



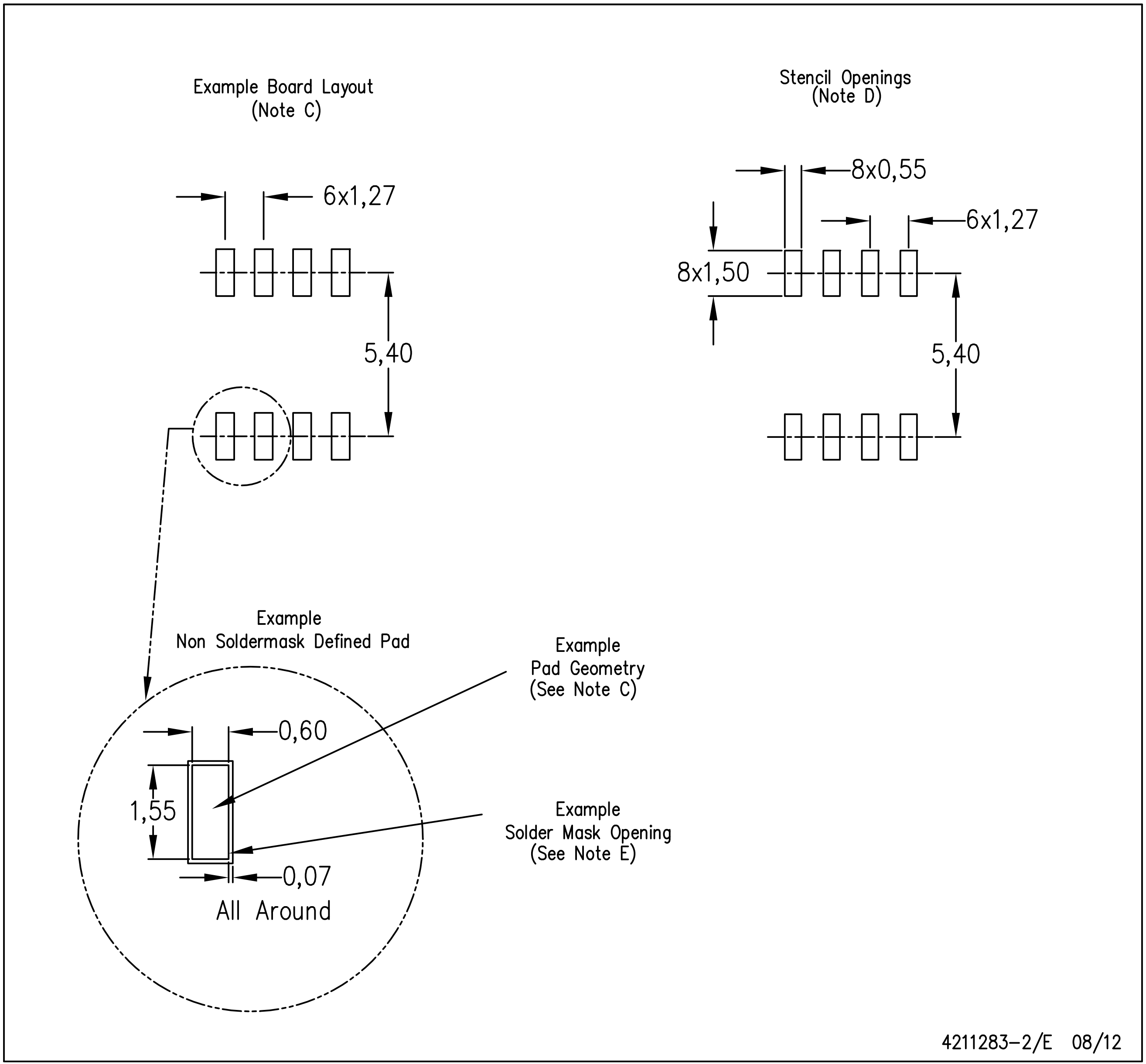
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AA.

## D (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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