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# NTE4501
# Integrated Circuit
# CMOS, Dual 4–Input NAND Gate, 2–Input NOR/OR Gate, 8–Input AND/NAND Gate

**Description:**

The NTE4501 is a “triple gate” device in a 16–Lead DIP type package constructed with MOS P–Channel and N–Channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

**Features:**

- Quiescent Current = 0.5nA/package Typ at 5Vdc
- Noise Immunity = 45% of $V_{DD}$ Typ
- Diode Protection on All Inputs
- Supply Voltage Range: 3Vdc to 18Vdc
- Single Supply Operation – Positive or Negative
- High Fanout > 50
- Logic Swing Independent of fanout
- Capable of Driving Two Low–Power TTL Loads, One Low–Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

**Absolute Maximum Ratings:** (Voltages referenced to $V_{SS}$, Note 1)

DC Supply Voltage, $V_{DD}$ . . . . . –0.5 to +18.0V
Input Voltage (All Inputs), $V_{in}$ . . . . . –0.5 to $V_{DD}$ to +0.5V
DC Current Drain (Per Pin), I . . . . . 10mA
Operating Temperature Range, $T_A$ . . . . . –55° to +125°C
Storage Temperature Range, $T_{stg}$ . . . . . –65° to +150°C

Note 1. Maximum Ratings are those values beyond which damage to the device may occur.

## Electrical Characteristics:

| Parameter | | Symbol | $V_{DD}$ Vdc | −55°C | | +25°C | | | +125°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Typ | Max | Min | Max | |
| Output Voltage | "0" Level | $V_{OL}$ | 5.0 | – | 0.05 | – | 0 | 0.05 | – | 0.05 | Vdc |
| $V_{in}$ = $V_{DD}$ or 0 | | | 10 | – | 0.05 | – | 0 | 0.05 | – | 0.05 | Vdc |
| | | | 15 | – | 0.05 | – | 0 | 0.05 | – | 0.05 | Vdc |
| | "1" Level | $V_{OH}$ | 5.0 | 4.95 | – | 4.95 | 5.0 | – | 4.95 | – | Vdc |
| $V_{in}$ = 0 or $V_{DD}$ | | | 10 | 9.95 | – | 9.95 | 10 | – | 9.95 | – | Vdc |
| | | | 15 | 14.95 | – | 14.95 | 15 | – | 14.95 | – | Vdc |
| Input Voltage (Note 2) | "0" Level | $V_{IL}$ | | | | | | | | | |
| ($V_O$ = 3.6 or 1.4Vdc) | | | 5.0 | – | 1.5 | – | 2.25 | 1.5 | – | 1.4 | Vdc |
| ($V_O$ = 7.2 or 2.8Vdc) | | | 10 | – | 3.0 | – | 4.50 | 3.0 | – | 2.9 | Vdc |
| ($V_O$ = 11.5 or 3.5Vdc) | | | 15 | – | 3.75 | – | 6.75 | 3.75 | – | 3.6 | Vdc |
| | "1" Level | $V_{IH}$ | | | | | | | | | |
| ($V_O$ = 1.4 or 3.6Vdc) | | | 5.0 | 3.6 | – | 3.5 | 2.75 | – | 3.5 | – | Vdc |
| ($V_O$ = 12.8 or 7.2Vdc) | | | 10 | 7.1 | – | 7.0 | 5.50 | – | 7.0 | – | Vdc |
| ($V_O$ = 3.5 or 11.5Vdc) | | | 15 | 11.4 | – | 11.25 | 8.25 | – | 11.0 | – | Vdc |
| Output Drive Current | | $I_{OH}$ | | | | | | | | | |
| ($V_{OH}$ = 2.5Vdc) | Source | | 5.0 | −1.2 | – | −1.0 | −1.7 | – | −0.7 | – | mAdc |
| ($V_{OH}$ = 4.6Vdc) | | | 5.0 | −0.25 | – | −0.2 | −0.36 | – | −0.14 | – | mAdc |
| ($V_{OH}$ = 9.5Vdc) | NAND | | 10 | −0.62 | – | −0.5 | −0.9 | – | −0.35 | – | mAdc |
| ($V_{OH}$ = 13.5Vdc) | | | 15 | −1.8 | – | −1.5 | −3.5 | – | −1.1 | – | mAdc |
| ($V_{OH}$ = 2.5Vdc) | NOR | | 5.0 | −2.1 | – | −1.75 | −3.0 | – | −1.22 | – | mAdc |
| ($V_{OH}$ = 4.6Vdc) | | | 5.0 | −0.42 | – | −0.36 | −0.63 | – | −0.24 | – | mAdc |
| ($V_{OH}$ = 9.5Vdc) | | | 10 | −1.06 | – | −0.88 | −1.58 | – | −0.62 | – | mAdc |
| ($V_{OH}$ = 13.5Vdc) | | | 15 | −3.1 | – | −3.0 | −5.1 | – | −2.1 | – | mAdc |
| ($V_{OH}$ = 2.5Vdc) | NOR | | 5.0 | −3.6 | – | −1.75 | −3.0 | – | −1.22 | – | mAdc |
| ($V_{OH}$ = 4.6Vdc) | | | 5.0 | −0.72 | – | −0.6 | −1.08 | – | −0.42 | – | mAdc |
| ($V_{OH}$ = 9.5Vdc) | Inverter | | 10 | −1.8 | – | −1.5 | −2.7 | – | −1.05 | – | mAdc |
| ($V_{OH}$ = 13.5Vdc) | | | 15 | −5.4 | – | −4.5 | −10.5 | – | −3.15 | – | mAdc |
| ($V_{OL}$ = 0.4Vdc) | Sink | $I_{OL}$ | 5.0 | 0.64 | – | 0.51 | 0.88 | – | 0.36 | – | mAdc |
| ($V_{OL}$ = 0.5Vdc) | NAND | | 10 | 1.6 | – | 1.3 | 2.25 | – | 0.9 | – | mAdc |
| ($V_{OL}$ = 1.5Vdc) | | | 15 | 4.2 | – | 3.4 | 8.8 | – | 2.4 | – | mAdc |
| ($V_{OL}$ = 0.4Vdc) | NOR | | 5.0 | 0.92 | – | 0.77 | 1.32 | – | 0.54 | – | mAdc |
| ($V_{OL}$ = 0.5Vdc) | | | 10 | 2.34 | – | 1.95 | 3.37 | – | 1.36 | – | mAdc |
| ($V_{OL}$ = 1.5Vdc) | | | 15 | 6.12 | – | 5.1 | 13.2 | – | 3.57 | – | mAdc |
| ($V_{OL}$ = 0.4Vdc) | NOR | | 5.0 | 1.54 | – | 1.28 | 2.2 | – | 0.9 | – | mAdc |
| ($V_{OL}$ = 0.5Vdc) | Inverter | | 10 | 3.9 | – | 3.25 | 5.63 | – | 2.27 | – | mAdc |
| ($V_{OL}$ = 1.5Vdc) | | | 15 | 10.2 | – | 8.5 | 22 | – | 5.95 | – | mAdc |

Note 2. Noise immunity specified for worse case input combination.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Note 4. To calculate total supply current at loads other than 50pF:

$$I_T(C_L) = I_T(50pF) + 4 \times 10^{-3}(C_L - 50)\ V_{DD}/f$$

where: $I_T$ is in μA (per package), $C_L$ in pF, $V_{DD}$ in Vdc, f in kHz is input frequency.

**Electrical Characteristics (Cont'd):**

| Parameter | Symbol | $V_{DD}$ Vdc | −55°C | | +25°C | | | +125°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Typ | Max | Min | Max | |
| Input Current | $I_{in}$ | 15 | – | ±0.1 | – | ±0.00001 | ±0.1 | – | ±0.1 | μAdc |
| Input Capacitance ($V_{IN}$ = 0) | $C_{in}$ | – | – | – | – | 5.0 | 7.5 | – | – | pF |
| Quiescent Current (Per Package) | $I_{DD}$ | 5.0 | – | 0.05 | – | 0.0005 | 0.5 | – | 1.5 | μAdc |
| | | 10 | – | 0.10 | – | 0.0010 | 0.10 | – | 3.0 | μAdc |
| | | 15 | – | 0.20 | – | 0.0015 | 0.20 | – | 6.0 | μAdc |
| Total Supply Current (Dynamic plus Quiescent, Per Package, $C_L$ = 50pF on all outputs, all buffers switching, Note 3, Note 4) | $I_T$ | 5.0 | $I_T$ = (1.2μA/kHz) f + $I_{DD}$ | | | | | | | μAdc |
| | | 10 | $I_T$ = (2.4μA/kHz) f + $I_{DD}$ | | | | | | | μAdc |
| | | 15 | $I_T$ = (3.6μA/kHz) f + $I_{DD}$ | | | | | | | μAdc |

Note 2. Noise immunity specified for worse case input combination.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Note 4. To calculate total supply current at loads other than 50pF:

$$I_T(C_L) = I_T(50pF) + 4 \times 10^{-3}(C_L - 50)\ V_{DD}/f$$

where: $I_T$ is in μA (per package), $C_L$ in pF, $V_{DD}$ in Vdc, f in kHz is input frequency.

**Switching Characteristics:** ($C_L$ = 50pF, $T_A$ = +25°C, Note 2, Note 3)

| Parameter | Symbol | $V_{DD}$ Vdc | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Rise Time NAND, NOR | $t_{TLH}$ | | | | | |
| $t_{TLH}$ = (3.0ns/pf) $C_L$ + 30ns | | 5.0 | – | 180 | 360 | ns |
| $t_{TLH}$ = (1.5ns/pf) $C_L$ + 15ns | | 10 | – | 90 | 180 | ns |
| $t_{TLH}$ = (1.1ns/pf) $C_L$ + 10ns | | 15 | – | 65 | 130 | ns |
| Output Fall Time NAND, NOR | $t_{THL}$ | | | | | |
| $t_{THL}$ = (1.5ns/pf) $C_L$ + 25ns | | 5.0 | – | 100 | 200 | ns |
| $t_{THL}$ = (0.75ns/pf) $C_L$ + 12.5ns | | 10 | – | 50 | 100 | ns |
| $t_{THL}$ = (0.55ns/pf) $C_L$ + 9.5ns | | 15 | – | 40 | 80 | ns |
| Output Rise Time NOR−Inverter | $t_{TLH}$ | | | | | |
| $t_{TLH}$ = (1.35ns/pf) $C_L$ + 32.5ns | | 5.0 | – | 100 | 200 | ns |
| $t_{TLH}$ = (0.60ns/pf) $C_L$ + 20ns | | 10 | – | 50 | 100 | ns |
| $t_{TLH}$ = (0.40ns/pf) $C_L$ + 17ns | | 15 | – | 40 | 80 | ns |
| Output Fall Time NOR−Inverter | $t_{THL}$ | | | | | |
| $t_{THL}$ = (0.67ns/pf) $C_L$ + 26.5ns | | 5.0 | – | 60 | 120 | ns |
| $t_{THL}$ = (0.45ns/pf) $C_L$ + 17.5ns | | 10 | – | 40 | 80 | ns |
| $t_{THL}$ = (0.37ns/pf) $C_L$ + 11.5ns | | 15 | – | 30 | 60 | ns |

Note 2. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the device's potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

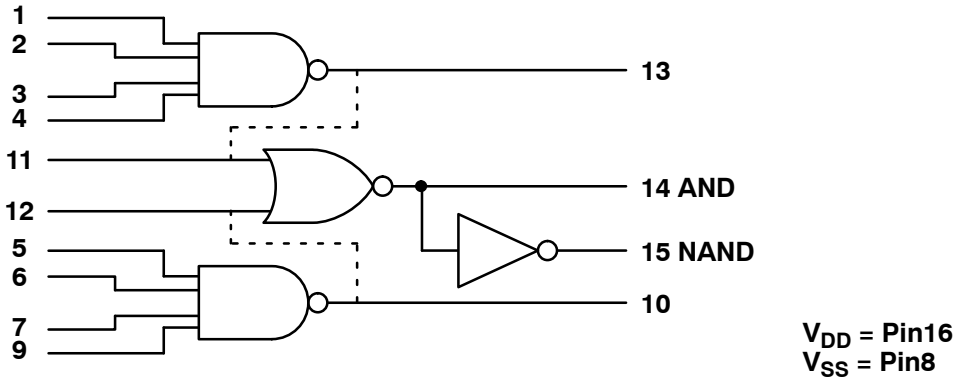
**Switching Characteristics (Cont'd):** ($C_L$ = 50pF, $T_A$ = +25°C, Note 2, Note 3)

| Parameter | | Symbol | $V_{DD}$ Vdc | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Propagation Delay Time | | | | | | | |
| $t_{PLH}$, $t_{PHL}$ = (1.7ns/pf) $C_L$ + 45ns | NAND | $t_{PLH}$, $t_{PHL}$ | 5.0 | – | 130 | 260 | ns |
| $t_{PLH}$, $t_{PHL}$ = (0.66ns/pf) $C_L$ + 37ns | | | 10 | – | 70 | 140 | ns |
| $t_{PLH}$, $t_{PHL}$ = (0.5ns/pf) $C_L$ + 25ns | | | 15 | – | 50 | 100 | ns |
| $t_{PLH}$, $t_{PHL}$ = (1.7ns/pf) $C_L$ + 30ns | NOR | $t_{PLH}$, $t_{PHL}$ | 5.0 | – | 115 | 230 | ns |
| $t_{PLH}$, $t_{PHL}$ = (0.66ns/pf) $C_L$ + 32ns | | | 10 | – | 65 | 130 | ns |
| $t_{PLH}$, $t_{PHL}$ = (0.5ns/pf) $C_L$ + 20ns | | | 15 | – | 45 | 90 | ns |
| $t_{PLH}$, $t_{PHL}$ = (1.7ns/pf) $C_L$ + 45ns | NOR–Inverter | $t_{PLH}$, $t_{PHL}$ | 5.0 | – | 130 | 260 | ns |
| $t_{PLH}$, $t_{PHL}$ = (0.66ns/pf) $C_L$ + 37ns | | | 10 | – | 70 | 140 | ns |
| $t_{PLH}$, $t_{PHL}$ = (0.5ns/pf) $C_L$ + 25ns | | | 15 | – | 50 | 100 | ns |

Note 2. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the device's potential performance.

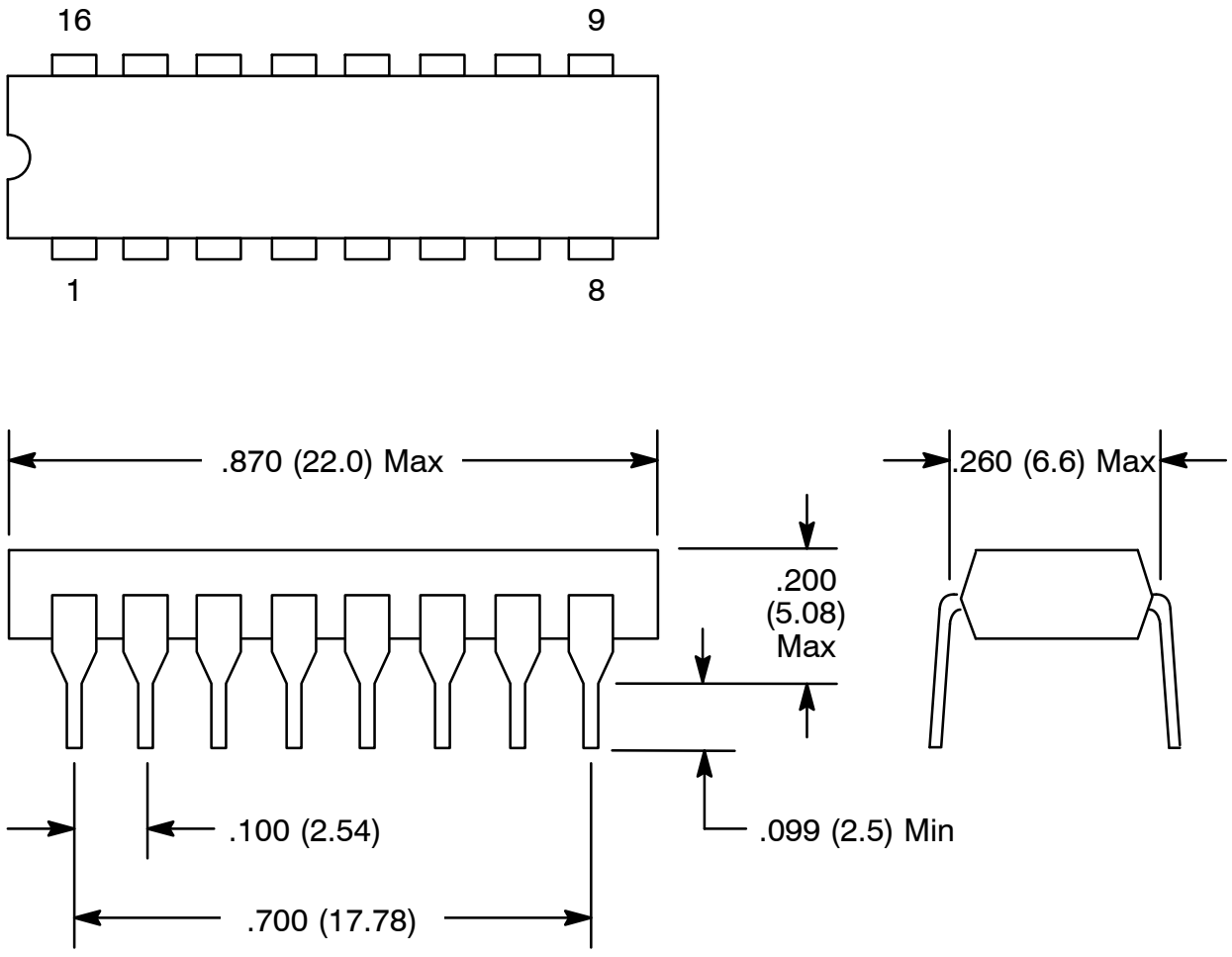
Note 3. The formulas given are for the typical characteristics only at +25°C.

**Logic Diagram**




**Use Dotted–Connection Externally to Obtain 8–Input AND/NAND**

**Note: Pin14 must not be used as an input to the inverter.**


16
9
1
8
.870 (22.0) Max
.260 (6.6) Max
.200
(5.08)
Max
.100 (2.54)
.099 (2.5) Min
.700 (17.78)