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NTE7496
Integrated Circuit
TTL – 5–Bit Shift Register

Description:

The NTE7496 is a 5–bit shift register in a 16–Lead plastic DIP type package that consists of five R–S master–slave flip–flops connected to perform parallel–to–serial or serial–to–parallel conversion of binary data. Since both inputs and outputs for all flip–flops are accessible, parallel–in/parallel–out or serial–in/serial–out operation may be performed.

All flip–flops are simultaneously set to a low output level by applying a low–level voltage to the clear input while the preset is inactive (low). Clearing is independent of the level of the clock input.

The register may be parallel loaded by using the clear input in conjunction with the preset inputs. After clearing all stages to low output levels, data to be loaded is applied to the individual preset inputs (A, B, C, D, and E) and a high–level load pulse is applied to the preset enable input. Presetting, like clearing, is independent of the level of the clock input.

Transfer of information to the outputs occurs on the positive–going edge of the clock pulse. The proper information must be set up at the R–S inputs of each flip–flop prior to the rising edge of the clock input waveform. The serial input provides this information to the first flip–flop, while the outputs of the subsequent flip–flops provide information for the remaining R–S inputs. The clear input must be high and the preset or preset enable inputs must be low when clocking occurs.

Applications:

- N–Bit Serial–to–Parallel Converter
- N–Bit Parallel–to–Serial Converter
- N–Bit Storage Register

Absolute Maximum Ratings: (Note 1)

Supply Voltage, V_{CC} 7V
Input Voltage (Note 2), V_{IN} 5.5V
Power Dissipation 240mW
Operating Temperature Range, T_A . . . . . 0°C to +70°C
Storage Temperature Range, T_{stg} . . . . . –65°C to +150°C

Note 1. Voltage values are with respect to network ground terminal.
Note 2. Input voltages must be zero or positive with respect to network ground terminal.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
High−Level Output Current	I_{OH}	–	–	−400	μA
Low−Level Output Current	I_{OL}	–	–	16	mA
Clock Frequency	f_{clock}	0	–	10	MHz
Width of Clock Input Pulse	$t_{w(clock)}$	35	–	–	ns
Width of Clear and Input Pulse	t_w	30	–	–	ns
Serial Input Setup Time	t_{su}	30	–	–	ns
Serial Input Hold Time	t_h	0	–	–	ns
Operating Temperature Range	T_A	0	–	+70	°C

Electrical Characteristics: (Note 3, Note 4)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2	–	–	V
Low Level Input Voltage	V_{IL}		–	–	0.8	V
High Level Output Voltage	V_{OH}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −400μA	2.4	3.4	–	V
Low Level Output Voltage	V_{OL}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16mA	–	0.2	0.4	V
Input Current	I_I	V_{CC} = MAX, V_I = 5.5V	–	–	1	mA
High Level Input Current Preset Enable Input	I_{IH}	V_{CC} = MAX, V_I = 2.4V	–	–	200	μA
All Other Inputs			–	–	40	μA
Low Level Input Current Preset Enable Input	I_{IL}	V_{CC} = MAX, V_I = 0.4V	–	–	−8.0	mA
All Other Inputs			–	–	−1.6	mA
Short−Circuit Output Current	I_{OS}	V_{CC} = MAX, Note 5	−18	–	−57	mA
Supply Current	I_{CC}	V_{CC} = MAX, Note 6	–	48	79	mA

Note 3. .For conditions shown as MIN or MAX, use the appropriate value specified under “Recommended Operation Conditions”.

Note 4. All typical values are at V_{CC} = 5V, T_A = +25°C.

Note 5. Not more than one output should be shorted at a time.

Note 6. I_{CC} is measured with the clear input grounded and all other inputs and outputs open.

Switching Characteristics: (V_{CC} = 5V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Propagation Delay Time (From Clock)	t_{PLH}	R_L = 400Ω, C_L = 15pF	–	25	40	ns
	t_{PHL}		–	25	40	ns
Propagation Delay Time (From Preset or Preset Enble)	t_{PLH}		–	28	35	ns
Propagation Delay Time (From Clear)	t_{PHL}		–	–	55	ns

Function Table:

Inputs									Outputs				
		Preset											
$\overline{\text{Clear}}$	Preset Enable	A	B	C	D	E	Clock	Serial	Q_A	Q_B	Q_C	Q_D	Q_E
L	L	X	X	X	X	X	X	X	L	L	L	L	L
L	X	L	L	L	L	L	X	X	L	L	L	L	L
H	H	H	H	H	H	H	X	X	H	H	H	H	H
H	H	L	L	L	L	L	L	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}
H	H	H	L	H	L	H	L	X	H	Q_{B0}	H	Q_{D0}	H
H	L	X	X	X	X	X	L	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}
H	L	X	X	X	X	X	↑	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}
H	L	X	X	X	X	X	↑	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}

H = HIGH Level (Steady State), L = Low Level (Steady State)

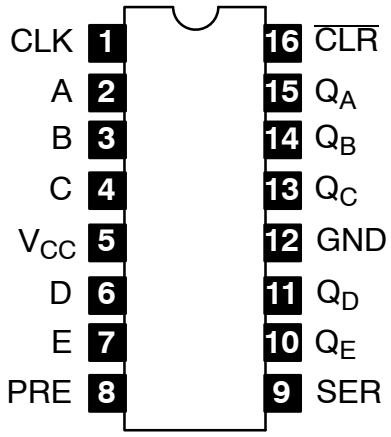
X = Irrelevant (Any input, including transitions)

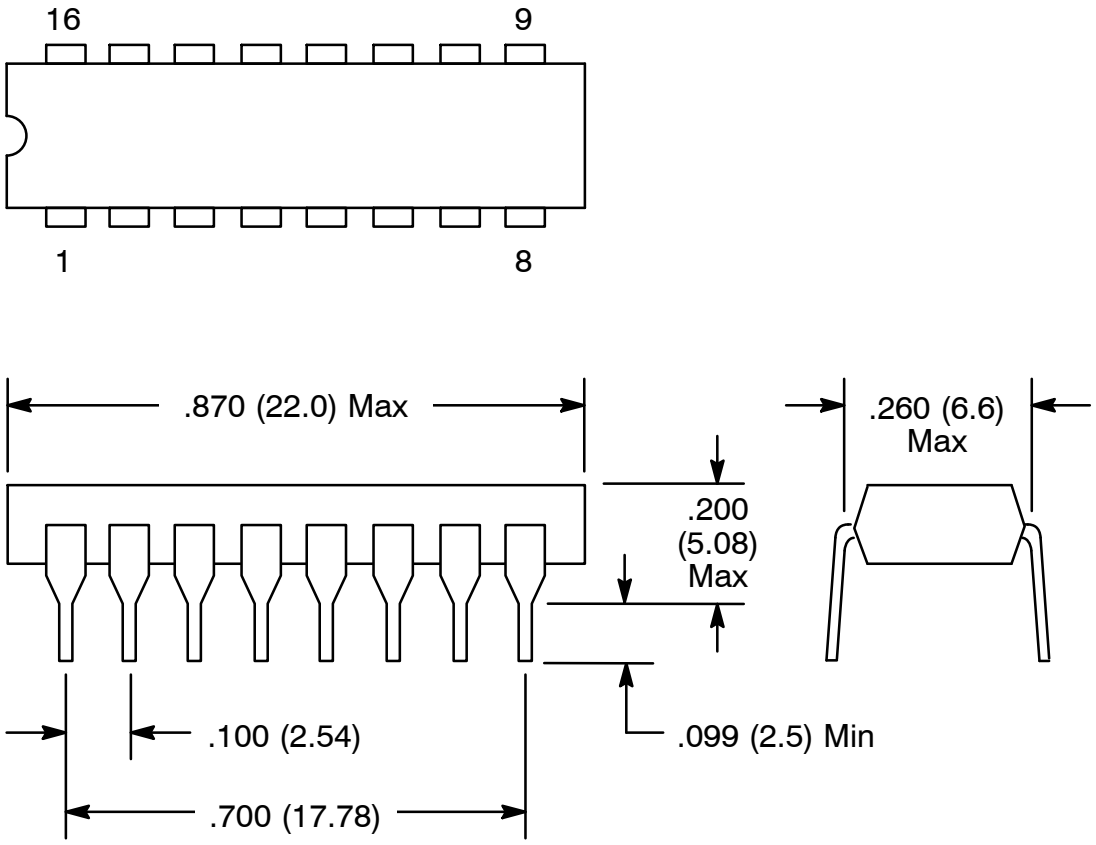
↑ = Transition from Low to High Level

Q_{A0}, Q_{B0}, etc. = The level of Q_A, Q_B, etc., respectively before the indicated steady−state input conditions were established.

Q_{An}, Q_{Bn}, etc. = The level of Q_A, Q_B, etc., respectively before the most recent ↑ transition of the clock.

Pin Connection Diagram




16
9
1
8
.870 (22.0) Max
.260 (6.6)
Max
.200
(5.08)
Max
.100 (2.54)
.099 (2.5) Min
.700 (17.78)