LRA/ERM Haptic Driver with Multiple I²C Addresses, Integrated Waveform Memory, and Wideband Support

General Description

DA7281 is a linear resonant actuator (LRA) and eccentric rotating mass (ERM) haptic driver offering automatic closed-loop LRA resonant frequency tracking. The feature guarantees consistency across LRA production tolerances, operating temperature, aging, and mechanical coupling. DA7281 offers wideband operation that fully utilizes the capabilities of newer wideband and multi-directional LRAs.

The differential output drive architecture and continuous actuator motion sensing enable efficient, calibration-free playback and minimize software complexity, unlike many existing solutions that require repeated manually triggered calibration to track LRA parameters. Featuring wake-up on General Purpose Input (GPI) sequence trigger and/or I²C activity, DA7281 automatically returns to a low quiescent current state (typically 0.36 µA) between playbacks. At only 20 % of the idle current of the nearest alternative solution, DA7281 significantly extends battery life in mobile systems.

To reduce system complexity, an integrated Waveform Memory allows haptic sequences to be pre-loaded to DA7281. Independent sequences can be triggered, with low-latency (0.75 ms), by up to three separate input pins without host interaction. Haptic sequences can also be streamed to DA7281 from an external source via I²C or pulse width modulated (PWM) signal.

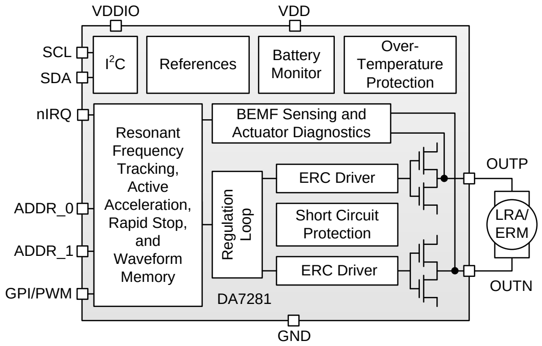
DA7281 actively monitors the back electromotive force (BEMF) while continuously driving and applies closed-loop Active Acceleration and Rapid Stopping for sharper clicks and a higher fidelity user experience. This offers significant advantages over existing solutions that need to move into a high-impedance state during drive to measure the BEMF, which adds a considerable amount of inactive time to the sequence and lowers the effective click strength for a given LRA.

Key Features

- LRA or ERM drive capability
- Automatic LRA resonant frequency tracking
- Wideband LRA support
- I²C and PWM input streaming
- Low latency (0.75 ms) I²C/GPI wake-up from IDLE state, I_Q = 0.36 µA
- Ultra-low latency (0.15 ms) in STANDBY state, I_Q = 0.8 mA
- GPI pin for triggering of up to two independent haptic sequences
- On-board Waveform Memory with amplitude, time, and frequency control
- Active Acceleration and Rapid Stop technology for high-fidelity haptic feedback
- Actuator diagnostics and fault handling
- Up to four I²C addresses via two address pins
- No software requirements with embedded operation
- Differential PWM output drive
- Current driven system to deliver constant actuator power
- Configurable EMI suppression
- Automatic short circuit protection
- Ultra-low power consumption, I_Q = 0.36 µA, with state retention in IDLE state
- Supply monitoring, reporting, and automatic output limiting
- Open- and closed-loop modes
- Custom wave drive support
- Small solution footprint WLCSP or QFN

Applications

- Mobiles
- Wearables and hearables
- Computer peripherals
- Gaming
- Automotive and industrial
- Virtual and augmented reality controllers



LRA/ERM Haptic Driver with Multiple I²C Addresses, Integrated Waveform Memory, and Wideband Support

System Diagrams

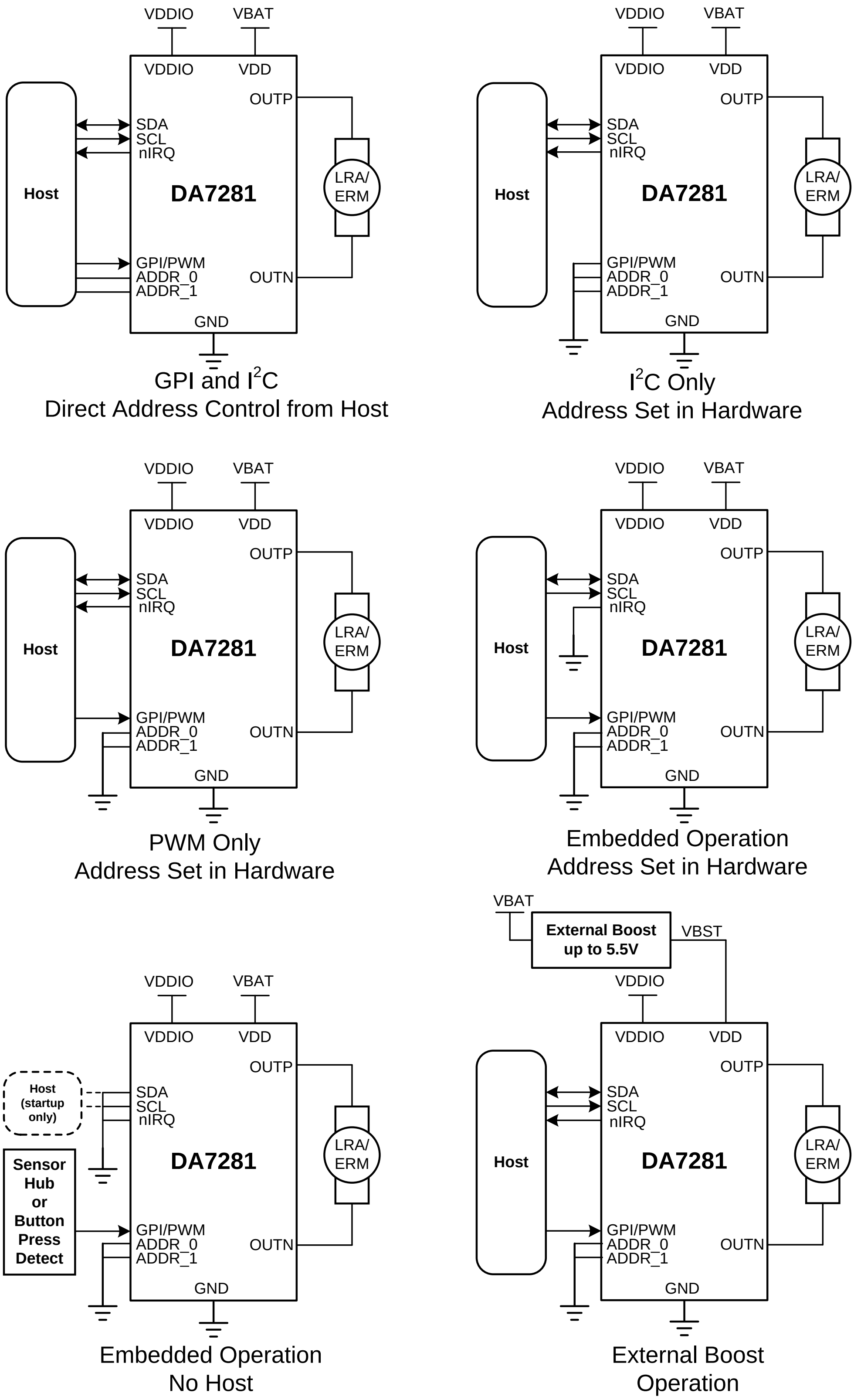


Figure 1: System Diagrams

Contents

General Description **1**
Key Features **1**
Applications **1**
System Diagrams **2**
Legal **6**
Product Family **6**
1 Terms and Definitions **7**
2 Block Diagram **8**
3 Pinout **9**
3.1 WLCSP Package 9
3.2 QFN Package 9
4 Characteristics **11**
4.1 Absolute Maximum Ratings 11
4.2 Recommended Operating Conditions 11
4.3 Electrical Characteristics 12
4.4 Timing Characteristics 13
4.5 Thermal Characteristics 14
5 Functional Description **15**
5.1 Features Description 15
5.2 Functional Modes 20
5.3 Resonant Frequency Tracking 24
5.4 Active Acceleration and Rapid Stop 24
5.5 Wideband Frequency Control 26
5.6 Device Configuration and Playback 26
5.7 Advanced Operation 35
5.8 Waveform Memory 43
5.9 General Data Format 48
5.10 I²C Control Interface 51
6 Register Overview **55**
6.1 Register Map 55
6.2 Register Descriptions 57
7 Package Information **71**
7.1 WLCSP Package Outline 71
7.2 QFN Package Outline 72
7.3 Moisture Sensitivity Level 73
7.4 WLCSP Handling 73
7.5 Soldering Information 73
8 Ordering Information **74**
9 Application Information **74**
10 Layout Guidelines **75**

Figures

Figure 1: System Diagrams ... 2
Figure 2: DA7281 Block Diagram ... 8
Figure 3: DA7281 WLCSP Pinout Diagram (Top View) ... 9
Figure 4: DA7281 QFN Pinout Diagram (Top View) ... 9
Figure 5: I²C Interface Timing ... 13
Figure 6: LRA Output Acceleration Swept in Frequency with Constant Power Input Signal ... 15
Figure 7: Narrowband and Wideband LRA Response across Frequency ... 16
Figure 8: Dual Mode LRA Response across Frequency ... 16
Figure 9: System State Diagram ... 20
Figure 10: Example PWM Inputs with ACCELERATION_EN = 0 ... 22
Figure 11: LRA Single Step Drive without Acceleration and Rapid Stop ... 25
Figure 12: LRA Single Step with Acceleration and Rapid Stop ... 25
Figure 13: Simple Drive (Top) versus Active Acceleration and Rapid Stop Enabled (Bottom) ... 25
Figure 14: Operation in DRO Mode ... 29
Figure 15: Operation in PWM Mode ... 30
Figure 16: Operation in RTWM Mode ... 31
Figure 17: Operation in ETWM Mode ... 33
Figure 18: Output Voltage and Current for Different AMP_PID_EN Values ... 36
Figure 19: Custom Wave Point Numbering ... 37
Figure 20: Half-Period Control in DRO Mode ... 38
Figure 21: Polarity Timing Relationship ... 39
Figure 22: Equivalent Electrical Model of an Actuator ... 39
Figure 23: Automatic Output Limiting ... 41
Figure 24: Coin ERM Physical and Electrical Summary ... 42
Figure 25: Waveform Memory Structure ... 43
Figure 26: Snippet Ramp and Step with ACCELERATION_EN = 1 ... 44
Figure 27: Snippet Example ... 45
Figure 28: Command Structure for a Single Frame ... 45
Figure 29: Sequence Structure ... 47
Figure 30: Waveform Memory Example ... 47
Figure 31: Overview of Data Formats with Acceleration Disabled ... 48
Figure 32: Overview of Data Formats with Acceleration Enabled ... 49
Figure 33: Instantiating More than Four DA7281s in the Same System ... 51
Figure 34: Schematic of the I²C Control Interface Bus ... 52
Figure 35: I²C START and STOP Conditions ... 52
Figure 36: I²C Byte Write (SDA line) ... 53
Figure 37: Examples of the I²C Byte Read (SDA line) ... 53
Figure 38: Examples of I2C Page Read (SDA line) ... 53
Figure 39: I²C Page Write (SDA line) ... 54
Figure 40: I²C Repeated Write (SDA line) ... 54
Figure 41: WLCSP Package Outline Drawing ... 71
Figure 42: QFN Package Outline Drawing ... 72
Figure 43: External Components Diagram ... 74
Figure 44: WLCSP Example PCB Layout ... 75
Figure 45: QFN Example PCB Layout ... 75

Tables

Table 1: DA728x Feature Comparison ... 6
Table 2: WLCSP Pin Description ... 10
Table 3: QFN Pin Description ... 10
Table 4: Pin Type Definition ... 10
Table 5: Absolute Maximum Ratings ... 11
Table 6: Recommended Operating Conditions ... 11

Table 7: Current Consumption ... 12
Table 8: Electrical Characteristics ... 12
Table 9: Timing Characteristics ... 13
Table 10: I²C Interface Timing Requirements ... 13
Table 11: WLCSP Thermal Ratings ... 14
Table 12: QFN Thermal Ratings ... 14
Table 13: Operating Modes ... 21
Table 14: Haptics Event Flag Descriptions ... 34
Table 15: Default CUSTOM_WAVE_GEN_COEFFx Settings ... 37
Table 16: LOOP_FILT_CAP_TRIM Register Trim Settings ... 39
Table 17: LOOP_FILT_RES_TRIM Register Trim Settings ... 40
Table 18: PWL Byte Structure ... 44
Table 19: Bit Definitions for Frame Parameters ... 46
Table 20: Relationship between ADDR_x Pins and I²C Base and Effective Addresses ... 51
Table 21: Register Map ... 55
Table 22: CHIP_REV (0x0000) ... 57
Table 23: IRQ_EVENT1 (0x0003) ... 57
Table 24: IRQ_EVENT_WARNING_DIAG (0x0004) ... 57
Table 25: IRQ_EVENT_SEQ_DIAG (0x0005) ... 58
Table 26: IRQ_STATUS1 (0x0006) ... 58
Table 27: IRQ_MASK1 (0x0007) ... 58
Table 28: CIF_I2C1 (0x0008) ... 59
Table 29: CIF_I2C2 (0x0009) ... 59
Table 30: FRQ_LRA_PER_H (0x000A) ... 59
Table 31: FRQ_LRA_PER_L (0x000B) ... 60
Table 32: ACTUATOR1 (0x000C) ... 60
Table 33: ACTUATOR2 (0x000D) ... 60
Table 34: ACTUATOR3 (0x000E) ... 60
Table 35: CALIB_V2I_H (0x000F) ... 61
Table 36: CALIB_V2I_L (0x0010) ... 61
Table 37: CALIB_IMP_H (0x0011) ... 61
Table 38: CALIB_IMP_L (0x0012) ... 62
Table 39: TOP_CFG1 (0x0013) ... 62
Table 40: TOP_CFG2 (0x0014) ... 62
Table 41: TOP_CFG3 (0x0015) ... 63
Table 42: TOP_CFG4 (0x0016) ... 63
Table 43: TOP_INT_CFG1 (0x0017) ... 63
Table 44: TOP_INT_CFG6_H (0x001C) ... 63
Table 45: TOP_INT_CFG6_L (0x001D) ... 64
Table 46: TOP_INT_CFG7_H (0x001E) ... 64
Table 47: TOP_INT_CFG7_L (0x001F) ... 64
Table 48: TOP_INT_CFG8 (0x0020) ... 64
Table 49: TOP_CTL1 (0x0022) ... 64
Table 50: TOP_CTL2 (0x0023) ... 65
Table 51: SEQ_CTL1 (0x0024) ... 65
Table 52: SWG_C1 (0x0025) ... 65
Table 53: SWG_C2 (0x0026) ... 66
Table 54: SWG_C3 (0x0027) ... 66
Table 55: SEQ_CTL2 (0x0028) ... 66
Table 56: GPI_CTL (0x002B) ... 66
Table 57: MEM_CTL1 (0x002C) ... 67
Table 58: MEM_CTL2 (0x002D) ... 67
Table 59: ADC_DATA_H1 (0x002E) ... 67
Table 60: ADC_DATA_L1 (0x002F) ... 67
Table 61: POLARITY (0x0043) ... 67
Table 62: LRA_AVR_H (0x0044) ... 67
Table 63: LRA_AVR_L (0x0045) ... 68
Table 64: FRQ_LRA_PER_ACT_H (0x0046) ... 68
Table 65: FRQ_LRA_PER_ACT_L (0x0047) ... 68

Table 66: FRQ_PHASE_H (0x0048) 68
Table 67: FRQ_PHASE_L (0x0049) 68
Table 68: FRQ_CTL (0x004C) 69
Table 69: TRIM3 (0x005F) 69
Table 70: TRIM4 (0x0060) 69
Table 71: TRIM6 0x(0062) 69
Table 72: D2602_TOP_CFG5 (0x006E) 70
Table 73: IRQ_EVENT_ACTUATOR_FAULT (0x0081) 70
Table 74: IRQ_STATUS2 (0x0082) 70
Table 75: IRQ_MASK2 (0x0083) 70
Table 76: SNP_MEM_xx (0x0084 to 0x00E7) 70
Table 77: MSL Classification 73
Table 78: Ordering Information 74

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Product Family

Table 1: DA728x Feature Comparison

Feature	DA7280	DA7281	DA7282
OFF state via EN pin	No	No	Yes
OFF state current	N/A	N/A	5 nA
IDLE state current	360 nA	360 nA	680 nA
Number of GPI sequence trigger pins	3	1	3
Multiple I²C addressing	No	Yes	No

1 Terms and Definitions

BEMF	Back electromotive force
CDM	Charged device model
DMA	Dual mode actuator
DRO	Direct register override
EMI	Electromagnetic interference
ERC	Edge rate control
ERM	Eccentric rotating mass
ESD	Electrostatic discharge
ETWM	Edge triggered Waveform Memory
FET	Field-effect transistor
GND	Ground
GPI	General purpose input
Half-period	One half of the LRA resonant frequency period. For example, if f_{LRA} = 200 Hz, one half-period is 2.5 ms.
HBM	Human body model
IRQs	Interrupt requests
LRA	Linear resonant actuator
OTP	One time programmable
PCB	Printed circuit board
PID	Proportional-Integral-Derivative
PoR	Power-on reset
PWL	Piecewise linear
PWM	Pulse width modulated
QFN	Quad flat no leads
RC	Resistor-capacitor
RTWM	Register triggered Waveform Memory
WLCSP	Wafer level chip scale package

2 Block Diagram

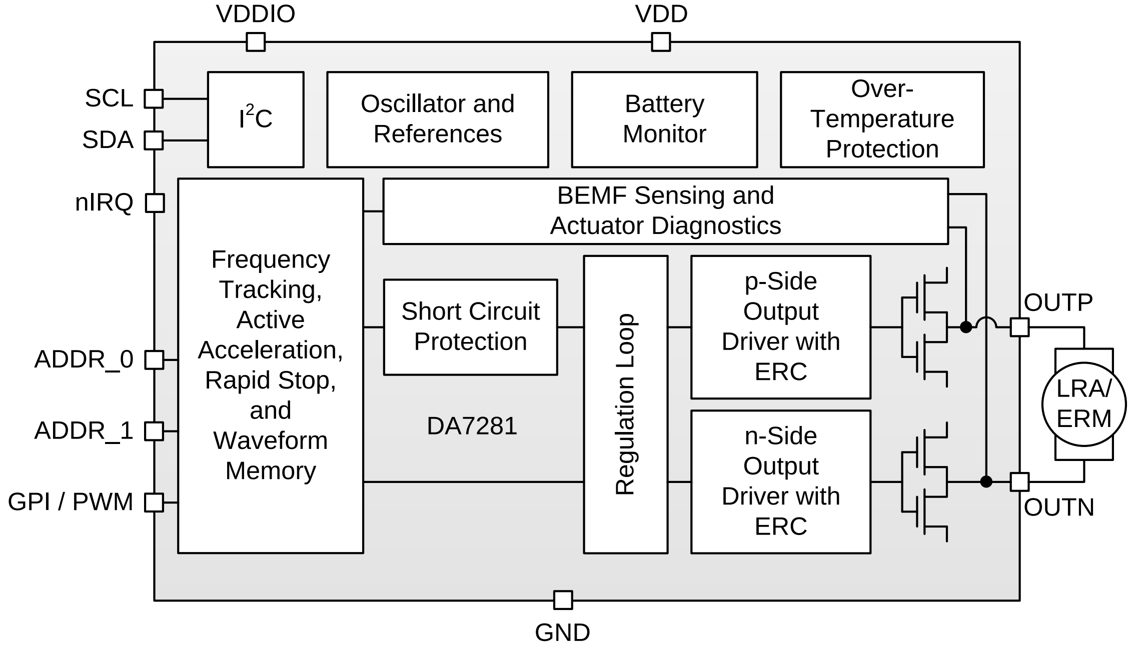


Figure 2: DA7281 Block Diagram

3 Pinout

3.1 WLCSP Package

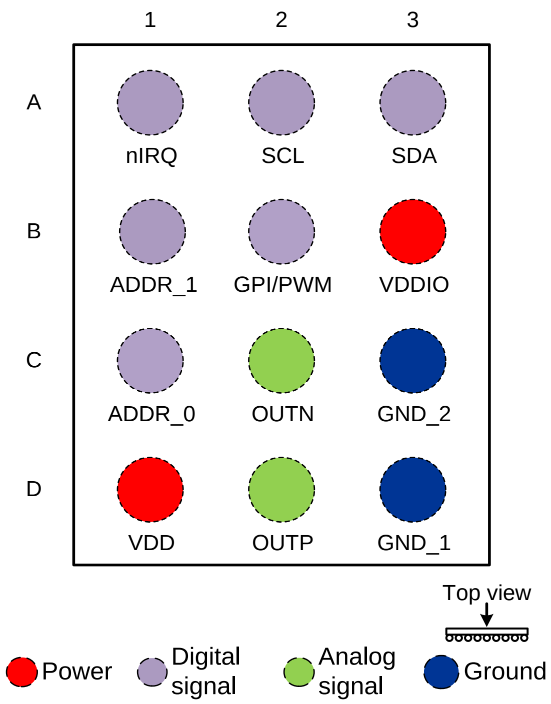


Figure 3: DA7281 WLCSP Pinout Diagram (Top View)

3.2 QFN Package

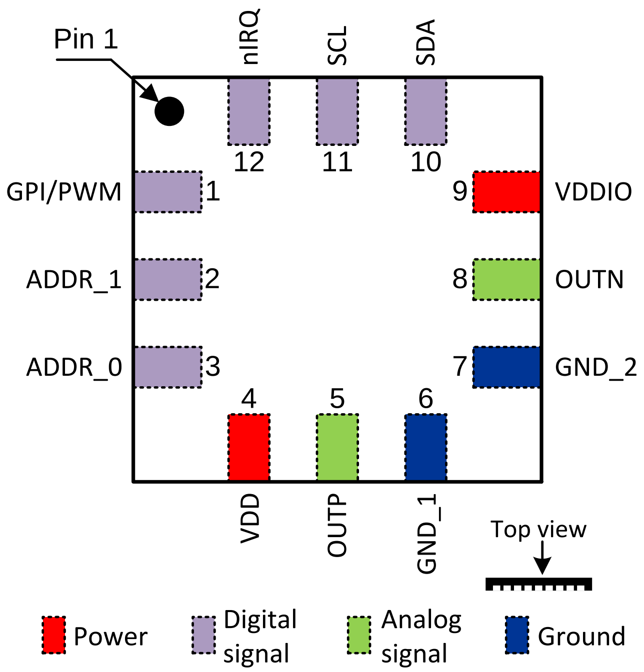


Figure 4: DA7281 QFN Pinout Diagram (Top View)

Table 2: WLCSP Pin Description

Pin No.	Pin Name	Type (Table 4)	Description
A1	nIRQ	DO	Interrupt request line to host, open-drain, active low, connect to VDDIO via external pull-up resistor
A2	SCL	DI	I^2C clock input
A3	SDA	DIO	I^2C data input/output, open-drain, connect to VDDIO via external pull-up resistor
B1	ADDR_1	DI	I^2C address 1
B2	GPI/PWM	DI	GPI sequence trigger, or PWM input
B3	VDDIO	PWR	Supply for digital I/O interfaces
C1	ADDR_0	DI	I^2C address 0
C2	OUTN	AO	Haptic driver negative output
C3	GND_2	GND	Ground
D1	VDD	PWR	Haptics power supply; decouple to GND_1
D2	OUTP	AO	Haptic driver positive output
D3	GND_1	GND	Ground

Table 3: QFN Pin Description

Pin No.	Pin Name	Type (Table 4)	Description
1	GPI/PWM	DI	GPI sequence trigger or PWM input
2	ADDR_1	DI	I^2C address 1
3	ADDR_0	DI	I^2C address 0
4	VDD	PWR	Haptics power supply; decouple to GND_1
5	OUTP	AO	Haptic driver positive output
6	GND_1	GND	Ground
7	GND_2	GND	Ground
8	OUTN	AO	Haptic driver negative output
9	VDDIO	PWR	Supply for digital I/O interfaces
10	SDA	DIO	I^2C data input/output, open-drain, connect to VDDIO via external pull-up resistor
11	SCL	DI	I^2C clock input
12	nIRQ	DO	Interrupt request line to host, open-drain, active low, connect to VDDIO via external pull-up resistor

Table 4: Pin Type Definition

Pin Type	Description
DI	Digital input
DO	Digital output
DIO	Digital input/output
AO	Analog output
PWR	Power
GND	Ground

4 Characteristics

4.1 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 5: Absolute Maximum Ratings

Parameter	Description	Conditions	Min	Max	Unit
V_{DD}	Haptics power supply	Referenced to GND	-0.3	6	V
V_{DDIO}	Haptics IO supply		-0.3	6	V
V_{OUTN}	Haptic driver negative output		-0.3	6	V
V_{OUTP}	Haptic driver positive output		-0.3	6	V
V_{nIRQ}	Interrupt request line to host		-0.3	6	V
V_{SCL}	I^{2}C clock input		-0.3	6	V
V_{SDA}	I^{2}C data input/output		-0.3	6	V
V_{GPI}	General purpose input		-0.3	6	V
V_{ADDR_x}	I^{2}C address pins		-0.3	6	V
T_A	Operating ambient temperature		-40	85	°C
T_J	Operating junction temperature		-40	125	°C
T_{STG}	Storage temperature		-65	150	°C
ESD_{HBM}	ESD protection	Human Body Model (HBM) All non-exposed pins	4		kV
ESD_{CDM}	ESD protection	Charged Device Model (CDM)	1		kV

4.2 Recommended Operating Conditions

Unless otherwise noted, the parameters listed in Table 6 are valid for T_A = 25 ºC, V_{DD} = 3.8 V, and V_{DDIO} = 1.8 V.

Table 6: Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DD}	Haptics power supply (battery or regulated rail)		2.8	3.8	5.5	V
V_{DDIO}	Haptics IO supply (Note 1)		1.35	1.8	5.5	V
Z_{LD}	Load impedance		4		50	Ω
C_{LD}	Capacitance to ground on OUTP and OUTN				1	nF
f_{LRA}	LRA resonant frequency	Frequency tracking enabled	50		300	Hz
f_{LRA_OL}	LRA resonant frequency, open-loop	Frequency tracking disabled	25		1000	Hz

Note 1 During device operation V_{DDIO} must be ≤ V_{DD} if ADDR_0, ADDR_1, and GPI are not grounded.

4.3 Electrical Characteristics

Unless otherwise noted, the parameters listed in Table 7 are valid for T_A = 25 ºC, V_{DD} = 3.8 V, and V_{DDIO} = 1.8 V.

Table 7: Current Consumption

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{Q_IDLE}	System VDD current in IDLE state	System waiting for playback request		0.36	1	µA
I_{Q_VDDIO}	VDDIO pin current	No I/O or nIRQ activity		0.13	0.5	µA
$I_{Q\_STANDBY}$	System VDD current in STANDBY state	System waiting for playback request		0.8	1	mA
$I_{Q\_NO\_LD}$	System VDD current with no load	High-impedance load > 10 MΩ, H-bridge switching		1.35	1.5	mA

Unless otherwise noted, the parameters listed in Table 8 are valid for T_A = 25 ºC, V_{DD} = 3.8 V, and V_{DDIO} = 1.8 V.

Table 8: Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{SHRT}	Short circuit protection threshold	Short to GND or VDD	400	500	600	mA
I_{OUT_MAX}	Maximum drive current			250	500 (Note 1)	mA
f_{TRCK_LRA}	LRA frequency tracking range	Automatic tracking limits	50		300 (Note 2)	Hz
$f_{TRCK\_ACC\_LRA}$	LRA frequency tracking accuracy	Frequency tracking accuracy during playback		0.5		Hz
$f_{WIDEBAND}$	Wideband frequency range	User defined drive frequency	25		1000	Hz
f_{OUT_PWM}	PWM output frequency	Differential OUTP and OUTN switching frequency	183	187.5	192	kHz
ERC	Programming range of output switching pins edge rate control	OUTP and OUTN slope	25	100	100	mV/ns
f_{IN_PWM}	PWM data input frequency		10		250	kHz
R_{DS_ON}	H-bridge drain to source resistance when on	High side plus low side FETs		2		Ω
Z_{FLT_UZ}	Actuator under-impedance threshold	Not applicable for coin ERM		4		Ω
Z_{FTL_OZ}	Over-impedance threshold	Not applicable for coin ERM		50		Ω
Z_{OUT_OFF}	Output impedance when H-bridge not switching	Pull-down enabled		15		kΩ

Note 1 For operation up to 500 mA (instead of 250 mA), see Section 5.7.12.

Note 2 For operation outside this range, see Section 5.7.1.

4.4 Timing Characteristics

Unless otherwise noted, the parameters listed in Table 9 are valid for T_A = 25 ºC, V_{DD} = 3.8 V, and V_{DDIO} = 1.8 V.

Table 9: Timing Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
t_{ON}	Cold boot to IDLE state time	V_{DD} present and PoR released		1.2	1.5	ms
t_{OUT_IDLE}	Time to output from IDLE state	From GPI or I^{2}C trigger to output drive		0.75		ms
$t_{OUT\_STANDBY}$	Time to output from STANDBY state	From GPI or I^{2}C trigger to output drive		0.15		ms

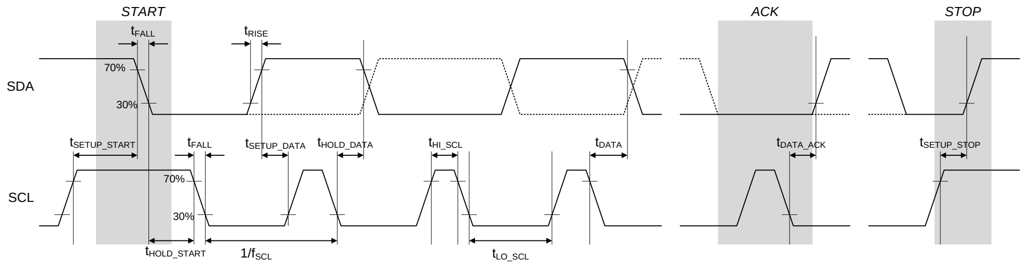


Figure 5: I^{2}C Interface Timing

Table 10: I^{2}C Interface Timing Requirements

Parameter	Description	Conditions	Min	Max	Unit
t_{BUF}	Bus free time from STOP to START condition		0.5		µs
Standard, Fast, and Fast-Plus Modes					
C_{BUS}	Bus line capacitive load			520	pF
f_{SCL}	SCL clock frequency		0	1000 (Note 1)	kHz
t_{SETUP_START}	Start condition setup time		0.26		µs
t_{HOLD_START}	Start condition hold time		0.26		µs
t_{LO_SCL}	SCL low time		0.5		µs
t_{HI_SCL}	SCL high time		0.26		µs
t_{RISE}	SCL and SDA rise time			120	ns
t_{FALL}	SCL and SDA fall time			120	ns
t_{SETUP_DATA}	Data setup time		50		ns
t_{HOLD_DATA}	Data hold-time		0		ns
t_{SETUP_STOP}	Stop condition setup time		0.26		µs
t_{DATA}	Data valid time			0.45	µs
t_{DATA_ACK}	Data valid acknowledge time			0.45	µs
t_{SPIKE}	Spike suppression (SCL, SDA)	Fast/Fast+ mode		50	ns

Note 1 f_{SCL} maximum is 400 kHz at V_{DDIO} ≤ 1.65 V and 1000 kHz at V_{DDIO} > 1.65 V.

4.5 Thermal Characteristics

Table 11: WLCSP Thermal Ratings

Parameter	Description (Note 1)	Min	Typ	Max	Unit
$R_{\Theta JA}$	Junction-to-ambient thermal resistance		90.3		°C/W
$R_{\Theta JC\_TOP}$	Junction-to-case (top) thermal resistance		43.6		°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance		49.0		°C/W
Ψ_{JT}	Junction-to-top characterization parameter		6.4		°C/W
Ψ_{JB}	Junction-to-board characterization parameter		45.8		°C/W

Note 1 Multilayer JEDEC standard, still air, ambient temperature 25 °C, simulated value.

Table 12: QFN Thermal Ratings

Parameter	Description (Note 1)	Min	Typ	Max	Unit
$R_{\Theta JA}$	Junction-to-ambient thermal resistance		88.2		°C/W
$R_{\Theta JC\_TOP}$	Junction-to-case (top) thermal resistance		54.6		°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance		39.3		°C/W
Ψ_{JT}	Junction-to-top characterization parameter		3.4		°C/W
Ψ_{JB}	Junction-to-board characterization parameter		50.0		°C/W
$R_{\Theta JC\_BOTTOM}$	Junction-to-case (bottom) thermal resistance		4.4		°C/W

Note 1 Multilayer JEDEC standard, still air, ambient temperature 25 °C, simulated value.

5 Functional Description

DA7281 is a haptic driver capable of driving both LRA and ERM actuators. The power-optimized architecture and advanced closed-loop digital algorithms achieve a very high-fidelity haptic drive. It features two I^2C address pins, frequency control within an onboard Waveform Memory and a GPI input, for triggering up to two distinct sequences. This helps with emulating button pressing in many applications including gaming, mobile, and wearable devices.

The device controls the level of drive across the load and senses the movement of the actuator. The driven waveform is generated by a current regulated loop using a high-frequency PWM modulation. The differential output drive features a switching regulator architecture with H-bridge differential drive across the load at a frequency of 187.5 kHz. The drive level is based on the sequence from the data source selected by I^2C interface, input PWM signal, or Waveform Memory.

DA7281 is capable of closed-loop actuator monitoring while driving to enable calibration-free playback, frequency tracking (LRA only), Active Acceleration, Rapid Stop, and actuator diagnostics.

Continuous resonant frequency tracking can be enabled while driving an LRA to track the mechanical resonance of the actuator through closed-loop control. This maximizes electrical to mechanical energy conversion efficiency for narrowband actuators and is especially useful in applications such as operating system notifications and alarms.

Resonant frequency tracking can be disabled to operate DA7281 in open-loop wideband frequency operation while driving LRAs with a wider bandwidth frequency response.

Active Acceleration and Rapid Stop features enable automated driving of both ERM and LRA loads (when frequency tracking is enabled). This reduces the time to reach the target acceleration level and the time for the actuator to come to a complete stop.

5.1 Features Description

Driving LRA and ERM Actuators

DA7281 can drive both ERMs and LRAs depending on the register configuration, see Section 5.6.2.

Automatic LRA Resonant Frequency Tracking

LRA resonant frequency shifts over time due to changing operating conditions, such as temperature or position, and manufacturing spread. Narrowband LRAs that dominate the existing market are high-Q systems. If driven at a fixed frequency, the consequences are loss of electrical to mechanical energy conversion efficiency, weaker than nominal actuator acceleration output, and significant part-to-part variation in the end-product haptic feel. Figure 6 illustrates that if the drive frequency is fixed, for example at 200 Hz, frequency variation in the resonant peak of only 10 Hz can result in a loss of 50 % of the output acceleration.

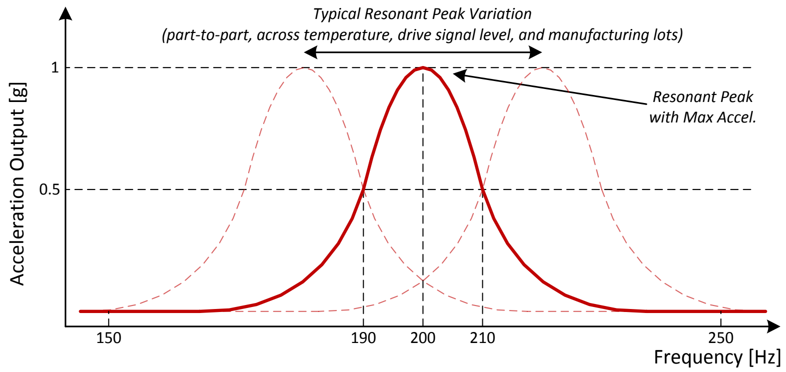


Figure 6: LRA Output Acceleration Swept in Frequency with Constant Power Input Signal

For a consistent user experience, DA7281 automatically locks onto and tracks the resonant frequency of the LRA through active BEMF sensing and closed-loop digital control. This ensures optimal output acceleration on every individual LRA throughout its lifetime and consistent part-to-part haptic feedback in the end product, see Section 5.3.

Wideband LRA Support

Wideband LRAs respond across a frequency range typically several times wider than narrowband ones, as demonstrated in Figure 7, and can be used in combination with DA7281 to a create richer haptic feedback experience by utilizing the increased vibrational frequency range, see Section 5.5.

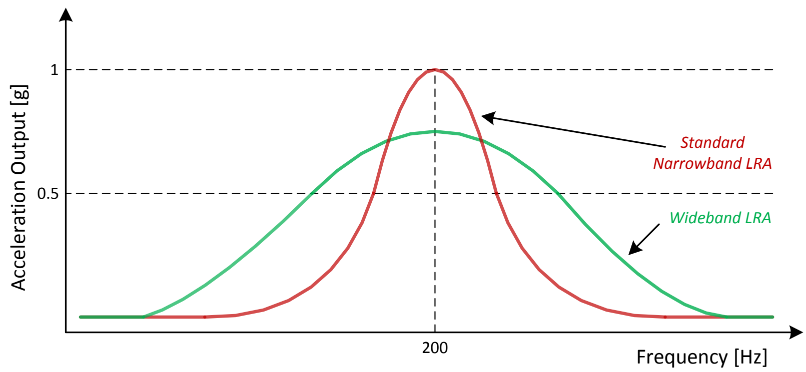


Figure 7: Narrowband and Wideband LRA Response across Frequency

Dual mode actuators (DMA) consist of two modes of vibration in different axes around different resonance points, depending on actuator construction. The two resonant points, wide response frequency, and different direction of vibration allow immersive gaming experience with multiple unique feedback effects. Figure 8 shows a typical DMA response, vibration in the y-axis occurs if the DMA is driven at 100 Hz and vibration in the x-axis occurs if the DMA is driven at 200 Hz.

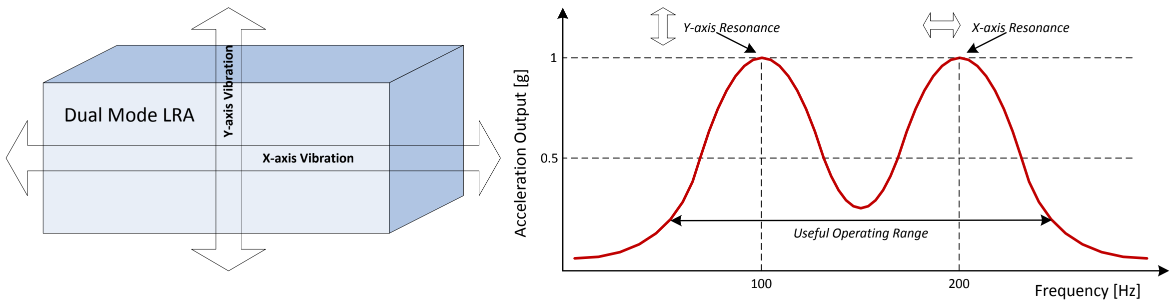


Figure 8: Dual Mode LRA Response across Frequency

The ability of DA7281 to control the frequency (25 Hz to 1000 Hz) and amplitude of the drive over time as well as the type of output wave allows the use of wideband sequences fully utilizing the capabilities of wideband and dual mode actuators for creating a richer user experience, see Section 5.7.5. Example use cases in DMAs are excitation of both resonant peaks simultaneously for maximum perceptible vibration or distinct single-frequency event-signaling clicks at different resonant frequencies and physical directions. Both DMAs and wideband LRAs can also be used to augment user audio experience by playing audio-derived haptic sequences over their useful frequency operating range.

DA7281 supports all of the above use cases and drives wideband LRAs via I²C or wideband Waveform Memory sequences triggered by I²C or GPI. The output drive can be configured as either square wave, sine wave, or custom wave to create different end effects, see Section 5.7.6.

Usually, LRA resonant frequency tracking is disabled during wideband operation. However, it can be enabled to either locate the resonant peak of wideband actuators, or to operate at a selected DMA resonance point and achieve the maximum possible actuator acceleration for a set input power, see Section 5.3 and Section 5.7.1.

I²C and PWM Input Streaming

Haptic playback data can be streamed externally either via I²C direct register override or from a PWM data source, see Section 5.2.2. The external input data PWM frequency is independent of the output PWM signal frequency driven to the actuator. The input PWM signal is low-pass filtered to create a varying DC level that is the envelope for the drive across the actuator.

Up to Four I²C Addresses via Two Address Pins

DA7281 has two dedicated address pins for setting the I²C base address. This allows up to four devices to work with the same I²C master by having different tie high and tie low settings on the pins. The I²C base address is also visible, which allows even more devices to be instantiated if the address pins are dynamically controlled, see Section 5.10.

Low Latency I²C/GPI Wake-Up from IDLE State

The device supports low latency (0.75 ms) wake-up from IDLE state, which is the lowest power state (typically 0.36 µA from V_{DD}). Wake-up is triggered by either GPI or I²C activity. I²C is fully functional in all modes including IDLE state and DA7281 retains register settings in all modes, see Section 5.2.1.

GPI Sequence Trigger for up to Two Independent Haptic Responses

The GPI input of DA7281 is used to trigger low-latency playback of up to two distinct sequences from IDLE state, see Section 5.2.7. Triggering is activated on events caused by rising or falling edges, or both. The sequence playback is configurable with odd events trigger one sequence, and even events another.

On-Board Waveform Memory with Amplitude, Time, and Frequency Control

DA7281 contains 100 bytes of highly optimized on-board Waveform Memory for user programmable haptic sequences, see Section 5.8. The Dialog Semiconductor specific format allows control of not only amplitude and time, but also frequency during the playback of a haptic sequence. This is specifically intended for use with wideband and dual mode actuators to create a richer user experience.

Active Acceleration and Rapid Stop for High-Fidelity Haptic Feedback

By measuring and responding to the BEMF of the actuator, DA7281 supports Active Acceleration which improves actuator response both when increasing and decreasing drive amplitude by overdriving or underdriving relative to the desired drive level. Similarly, Rapid Stop minimizes the time needed for the actuator to come to a complete stop by driving against the direction of actuator movement. These two features enable a high-fidelity haptic response of the actuator and improve on its inherent physical performance and mechanical time constant, see Section 5.4.

Continuous Actuator Diagnostics and Fault Handling

DA7281 monitors the actuator impedance at the start of each haptic sequence. The value of the impedance can be read back from a dedicated register, see Section 5.7.3. In addition, impedance, BEMF, and resonant frequency faults are flagged with automatic shutdown and notification via the nIRQ pin, see Section 5.6.6.

No Software Requirements with Embedded Operation

The device can function in a stand-alone embedded operation where no host action is needed to clear generated faults and the device will attempt to drive on each request. This also allows operation in GPI trigger mode without the need for a host device or host communication, see Section 5.7.7. Note that initial download of sequences to the device is still required. Once loaded, the Waveform Memory is retained in all states as long as the supply does not drop below the PoR threshold.

Differential Output Drive

DA7281 includes a full H-bridge differential output PWM drive that has the advantage of maximizing the power delivered to the LRA from a given supply and allows braking of DC motors by reversing voltage polarity. This doubles the voltage swing across the actuator and significantly increases system efficiency relative to a single transistor/LDO solution in legacy ERM or LRA applications.

Current Driven System

The device outputs regulated current, rather than voltage, which allows BEMF tracking without the need to stop driving to sense the BEMF. This maximizes power delivery to the actuator per unit time when compared to voltage driven solutions, resulting in shorter and sharper haptic clicks. In addition, constant current drive provides constant force into an actuator independently of the BEMF amplitude.

Configurable EMI Suppression

Switching node edge rate control (ERC) on the OUTP and OUTN pins reduces electromagnetic interference (EMI) and electrical interference via capacitive coupling in the end application, see Section 5.7.11. This eliminates any need for resistor-capacitor (RC) or ferrite bead filtering of the outputs, which offers a lower-cost bill of materials when using DA7281. Programmability of the ERC also gives DA7281 a distinct advantage over competing solutions as it helps fine-tune a system without any PCB modifications.

Automatic Short Circuit Protection

Automatic low-latency short circuit protection detects shorts on the OUTP and OUTN pins to supply, ground, or between OUTP and OUTN, and protects DA7281 by forcing the H-bridge into a high-impedance state, see Section 5.6.6.

Ultra-Low Power Consumption with State Retention

In IDLE state, DA7281 has an ultra-low current consumption from the power supply at typically 0.36 µA with a time to output of 0.75 ms. DA7281 returns automatically to IDLE after completing playback, keeps its register setup, and is available for I^{2}C communications, see Section 5.2.1.

Ultra-Low Latency in STANDBY State

In STANDBY state, the time to output is 0.15 ms with current consumption of typically 0.8 mA, see Section 5.2.1.

Supply Monitoring, Reporting, and Automatic Output Limiting

DA7281 monitors the power supply voltage level and adjusts the drive voltage accordingly, so that the output does not clip to the supply voltage. This feature guarantees controlled output allowing continued resonant frequency tracking and Active Acceleration/Rapid Stop functionality even when the device is operating under low power supply conditions or heavy battery load. Supply voltage can be read back by the host from a dedicated register, see Section 5.7.13.

Open- and Closed-Loop Modes

DA7281 can be configured in either open- or closed-loop mode. In open-loop mode any actuator BEMF monitoring is disabled and the device works as a simple current based drive without any auto-adjustment on the drive period or amplitude. This is useful in wideband LRA playback. In closed-loop mode, the user can optionally turn on the frequency tracking, Active Acceleration, Rapid Stop, and amplitude control features, see Section 5.7.5 and Section 5.7.6.

Open-Loop Sine/Custom Wave Drive Support

In open-loop operation DA7281 can be configured to drive the actuator with a non-square wave signal. This improves the electrical efficiency, reduces audibility in some actuators, and allows simultaneous drive of multiple resonant points in DMAs. The exact shape of the output waveform can be configured via dedicated registers with the default set to a sine wave, see Section 5.7.6.

Small Solution Footprint

Available in an ultra-small 1.35 mm x 1.75 mm, 0.4 mm pitch, 0.545 mm height, 3 x 4 WLCSP, or a 3.0 mm x 3.0 mm, 0.65 mm pitch, 0.78 mm height, 12 lead QFN package, DA7281 minimizes the required PCB size and overall solution cost. In the typical application case, only a single 100 nF decoupling capacitor is required. See Section 9 and Section 10.

Additional Features

DA7281 also features:

- A temperature and supply stable (±1.5 %) internal oscillator which guarantees consistent haptic playback in the frequency domain over a wide range of operating conditions.
- Automatic over-temperature warning and shutdown capability.
- Low pad leakage current (typ. < 50 nA, for all pads combined).
- Low idle current from VDDIO (typ. 130 nA at 1.8 V).
- I^2C operation down to V_{DDIO} = 1.35 V with V_{DD} PoR falling threshold at approx. 2.55 V.
- Output PWM frequency, at 187.5 kHz, is 167.5 kHz away from the audio band and at a non-audio sample rate multiple. This prevents audible fold back via supply disturbance common in near-audio-band switching haptic drivers.
- Easy to use Dialog SmartCanvas™ GUI with a user tab for fast device setup without the need to directly interact with registers and an intuitive graphical environment for Waveform Memory editing and visualization.

5.2 Functional Modes

5.2.1 System States

DA7281 features IDLE and STANDBY states ensuring lowest power consumption and lowest start-up latency in different operating conditions. In addition, when any fault is detected, the device returns directly to the IDLE state. Figure 9 shows the device states and the transitions into and out of each state.

When a power supply is applied, DA7281 loads the register default settings. Once BOOT is complete, DA7281 remains in the IDLE state and awaits further I^2C communication.

DA7281 enters the DRIVE state when playback of a haptic sequence begins. There are several different operating modes for playback, see Section 5.2.2.

On completion of playback, DA7281 leaves DRIVE state and returns either to IDLE state (for low power consumption) or STANDBY state (for low latency-to-drive). This is configured using STANDBY_EN.

If a fault condition occurs, DA7281 returns to the IDLE state, see Section 5.6.6 .

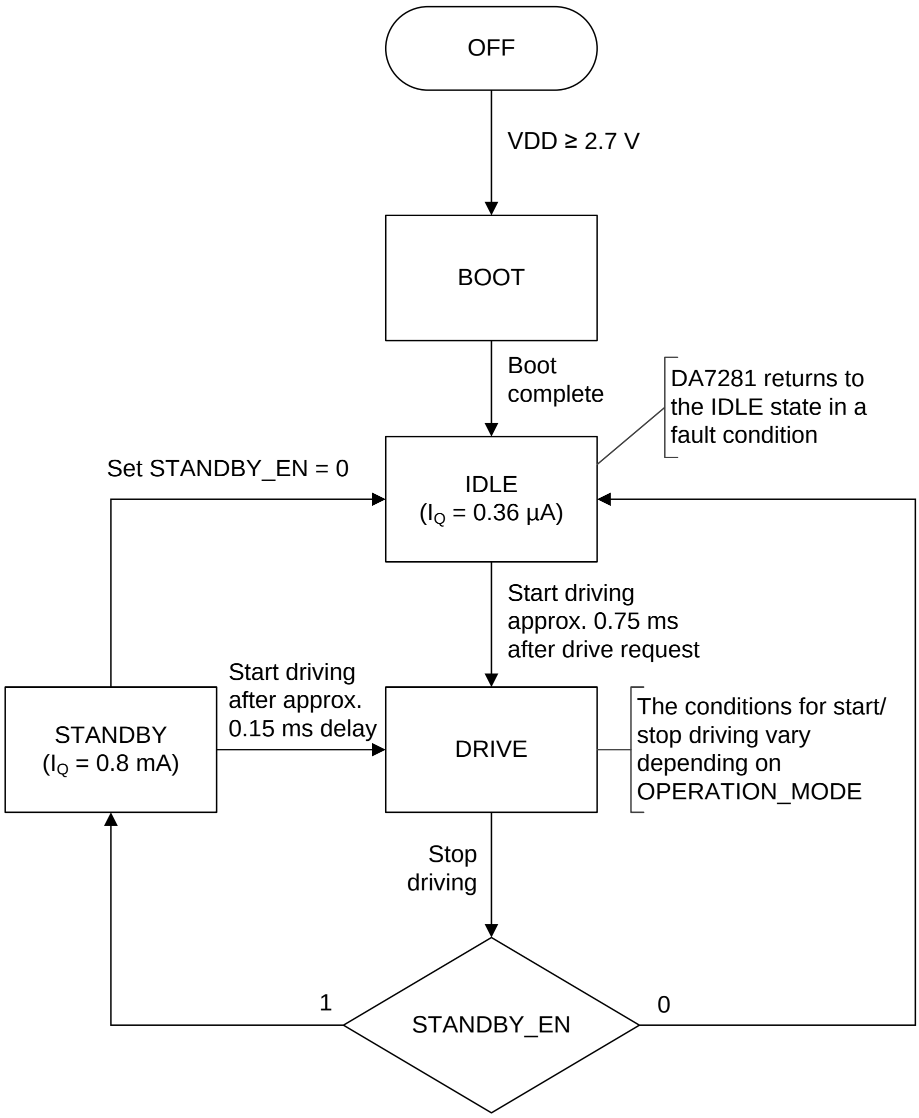


Figure 9: System State Diagram

5.2.2 Operating Modes

DA7281 offers multiple operating modes for use in different applications and to minimize power consumption, see Table 13.

Table 13: Operating Modes

Operating Mode	Description	OPERATION_MODE
Inactive	System waits in IDLE or STANDBY state based on STANDBY_EN setting	0
Direct register override (DRO)	Playback streaming via I^2C; input written to OVERRIDE_VAL	1
Pulse width modulated (PWM)	Playback streaming from PWM data input source on pin GPI/PWM	2
Register triggered waveform memory (RTWM)	Playback from Waveform Memory triggered only by I^2C write to SEQ_START	3
Edge triggered waveform memory (ETWM)	Playback from Waveform Memory triggered by rising/falling edge on pin GPI/PWM or via I^2C write to SEQ_START	4

5.2.3 Inactive Mode

DA7281 can be configured to automatically return to IDLE (for lower I_Q) or STANDBY (for minimized latency) state after completion of playback, see Section 5.2.1. In both states the register contents are retained. DA7281 remains in Inactive mode until it receives a playback request via either the GPI/PWM pin or I^2C (providing any faults in the fault registers have been cleared, see Section 5.6.6).

In the event of a fault the system will automatically return to the IDLE state, see Section 5.6.6.

5.2.4 Direct Register Override Mode

In DRO mode haptic sequences are streamed to DA7281 via I^2C input. The drive level of the output is set via OVERRIDE_VAL. For optimal start-up timing, update OVERRIDE_VAL before setting OPERATION_MODE = 1. OVERRIDE_VAL is treated as a two's complement proportional value where:

If ACCELERATION_EN = 1, the output drive level is equal to the value in OVERRIDE_VAL multiplied by the voltage stored in ACTUATOR_NOMMAX. OVERRIDE_VAL is interpreted as a proportion between 0 % (0x00) and 100 % (0x7F). The range from 0xFF to 0x80 is not used, see Figure 31. If enabled, the automatic Active Acceleration and Rapid Stop features will take the output up to the voltage in ACTUATOR_ABSMAX and/or reverse the drive level to be negative during level transitions, but in steady state the value will always scale to the voltage in ACTUATOR_NOMMAX.

If ACCELERATION_EN = 0, the output drive level is equal to the value in OVERRIDE_VAL multiplied by the voltage stored in ACTUATOR_ABSMAX. In this case OVERRIDE_VAL is interpreted as a proportion between -100% (0x80) and 100% (0x7F), see Figure 32. When DA7281 is set up to drive an ERM, the negative value represents a change in drive voltage polarity, while for an LRA it represents a phase shift of 180° in the drive signal. Negative drive can be used to speed up output acceleration level changes without the use of the Active Acceleration and Rapid Stop. Note that in the ACCELERATION_EN = 0 case Rapid Stop can still be enabled if an automatic stop to zero actuator acceleration is required.

Note: The output amplitude updates at twice the LRA frequency (when the differential voltage across the LRA crosses zero), therefore input changes more frequent than this are not required as sampling occurs only around a zero cross. Since the I^2C is asynchronous to the output drive, updates to OVERRIDE_VAL will have a one LRA half-period of uncertainty before propagating to the output. Synchronization of OVERRIDE_VAL updates to the half period is possible via software by looking at the POLARITY register and updating the output drive level, see Section 5.7.8.

When driving a wideband LRA in DRO mode, resonant frequency tracking can be turned off. This enables wideband operation and two-dimensional effects using DMAs, see Sections 5.7.5 and 5.7.6.

During playback, if a value written to OVERRIDE_VAL results in the output driving strength being maintained at 0 %, DA7281 will disable its output stage to save power. Drive is re-enabled automatically, with one LRA half-period delay, when a non-zero OVERRIDE_VAL value I²C input is received.

5.2.5 Pulse Width Modulation Mode

PWM mode is used to stream haptic sequences to DA7281 via the GPI/PWM input pin where the output drive level is determined by the duty cycle of the PWM signal. For optimal start-up timing, the PWM input signal needs to be provided before setting OPERATION_MODE = 2. The PWM duty cycle can be interpreted in two ways as follows:

If ACCELERATION_EN = 1, the output drive level is equal to the input signal duty cycle multiplied by the voltage stored in ACTUATOR_NOMMAX. In this case the duty cycle is interpreted as a proportion between 0 % and 100 %, see Figure 31. The automatic Active Acceleration and Rapid Stop (if enabled) features will take the output up to the voltage in ACTUATOR_ABSMAX and/or reverse the drive level to be negative during level transitions, but in steady state the final value will always scale to the voltage in ACTUATOR_NOMMAX.

If ACCELERATION_EN = 0, the output drive level is equal to the input signal duty cycle multiplied by the voltage stored in ACTUATOR_ABSMAX. In this case the duty cycle is interpreted as a proportion between -100 % and 100 % where 50 % duty cycle is 0 %, see Figure 32. When DA7281 is set up to drive an ERM, the negative value represents a change in drive voltage polarity, while for an LRA it represents a phase shift of 180° in the drive signal. Negative drive can be used to speed up output acceleration level changes without the use of the Active Acceleration and Rapid Stop. Note that in the ACCELERATION_EN = 0 case Rapid Stop can still be enabled if an automatic stop to zero actuator acceleration is required.

Note: The output PWM frequency is always independent of the PWM input frequency regardless of whether frequency tracking is enabled or disabled. To maximize accuracy and minimize power consumption and noise, it is best to keep the input PWM frequency as low as possible.

The PWM demodulator is rising edge sensitive. The minimum duty cycle that can be used to create the drive level can be configured in FULL_BRAKE_THR; any duty cycle below that value will produce a 0 % drive level.

During playback streaming in PWM mode, if a 0 % drive level is maintained by applying a 0 % (or 50 % if Active Acceleration is disabled) duty cycle PWM input, the DA7281 output stage is disabled to save power. Drive is re-enabled automatically, with one LRA half-period delay, when the duty cycle forces the drive level to be greater than 0 %.

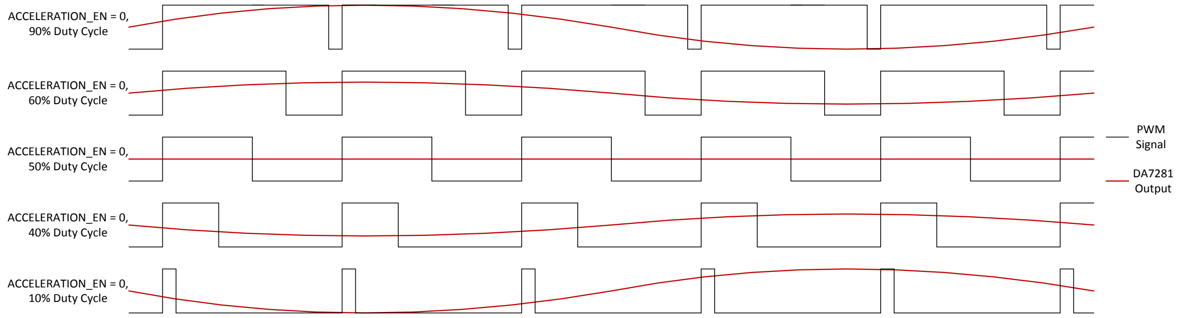


Figure 10: Example PWM Inputs with ACCELERATION_EN = 0

Note the 180° phase difference between driving > 50 % and < 50 %.

5.2.6 Register Triggered Waveform Memory Mode

If sequence consistency or I^{2}C bus availability is a concern, register triggered waveform memory mode (RTWM) mode can be used to play back previously defined sequences from the Waveform Memory, see Section 5.8, via I^{2}C register trigger only. Enter this mode by setting OPERATION_MODE = 3.

5.2.6.1 I^{2}C Triggering and Sequence Looping

Sequence selection is done via PS_SEQ_ID with the additional option to loop the sequence up to 16 times using PS_SEQ_LOOP. To trigger a sequence, set SEQ_START = 1. Once a sequence completes, the event is reported by dropping the nIRQ pin low and signaling via SEQ_DONE_M.

To repeat a sequence immediately following completion of playback, set SEQ_CONTINUE = 1.

5.2.7 Edge Triggered Waveform Memory Mode

If there is no host available, or for minimal host interaction, edge triggered waveform memory mode (ETWM) mode can be used to play back a previously defined sequences from the Waveform Memory, see Section 5.8, via external GPI edge trigger or also via I^{2}C trigger, as in RTWM mode. The ETWM is also useful if deterministic timing is required without reliance on the I^{2}C bus.

The GPI/PWM pin can be configured and will react according to the setting in GPI_POLARITY as follows:

- Rising edge trigger, GPI_POLARITY = 0: only a rising GPI edge creates an event that triggers a pre-programmed sequence.
- Falling edge trigger, GPI_POLARITY = 1: only a falling GPI edge creates an event that triggers a pre-programmed sequence.
- Rising and falling edge trigger, GPI_POLARITY = 2: both edges create events that trigger a pre-programmed sequence.

Any event received during playback from pin GPI/PWM after the initial GPI trigger event will result in a sequence stop.

- There are two ways of reacting to a GPI event based on GPI_MODE:
- Single sequence, GPI_MODE = 0: no matter how many times the GPI is triggered, it will play the sequence located at GPI_SEQUENCE_ID.
- Multi-sequence, GPI_MODE = 1: odd GPI events trigger the sequence at GPI_SEQUENCE_ID, while even GPI events trigger the sequence located at the value of GPI_SEQUENCE_ID + 1 bit.

In ETWM mode, a maximum of two different sequences can be configured when multi-sequence mode is enabled. The desired haptic sequence for the GPI must be set by programming GPI_SEQUENCE_ID.

Once a sequence has finished playing, a signal is sent via the nIRQ pin and DA7281 automatically returns to IDLE state, assuming STANDBY_EN = 0, to await the next trigger event.

Sequence looping operates in the same way as RTWM mode, see Section 5.2.6.1.

5.3 Resonant Frequency Tracking

LRAs are high-Q systems that have to be driven exactly at resonance to achieve maximum possible output acceleration. DA7281 supports continuous resonant frequency tracking via BEMF sensing during playback to achieve optimum LRA acceleration output across manufacturing spread, operating temperature range, external damping, and actuator aging.

When the FREQ_TRACK_EN is high, a digital resonant frequency tracking loop locks onto the LRA resonant frequency in real time by adjusting the drive period. This ensures that the actuator is always driven at the optimum frequency for the highest efficiency electrical to mechanical energy conversion. The loop range of 50 Hz to 300 Hz covers existing narrowband LRAs; typical resonant frequency lock accuracy is 0.5 Hz.

To increase absolute accuracy of the lock during playback, DA7281 supports automatic scaling of the frequency tracking controller gain. The feature is enabled via FREQ_TRACKING_AUTO_ADJ and becomes active after the device has achieved initial lock, see Section 5.7.1.

The resonant frequency tracking algorithm is designed to converge to the correct value from up to 25 % offset between the initial nominal datasheet value and the actual resonant frequency. This range is conservative in order to prevent unwanted behavior. A fault will trigger if the actuator resonant frequency is outside the 50 Hz to 300 Hz range. To block these two features, set FREQ_TRACKING_FORCE_ON = 1, see Section 5.7.1.

5.4 Active Acceleration and Rapid Stop

Mechanical systems such as LRAs and ERMs accelerate and decelerate exponentially and the time between transitions (for example from stopping of the drive signal to the actuator coming to a complete rest) can be perceptibly slow for the user. DA7281 features Active Acceleration and Rapid Stop to overcome this latency, which enables stronger clicks and a higher fidelity playback in both LRAs and ERMs. This capability offers a distinct advantage over legacy systems, which do not sense BEMF, because it allows the use of cheaper, slower response time actuators while keeping haptic effects crisp.

Active Acceleration employs relative drive architecture based on BEMF sensing, which enables temporary overdrive on all level changes reducing the time required to achieve a target drive level. The DA7281 Active Acceleration algorithm does not require dedicated calibration procedures and enables accurate overdrive and underdrive throughout the lifetime of an actuator. The feature removes the need for a separate calibration sequence to determine the correct overdrive duration, see Figure 11 and Figure 12.

Enabling Active Acceleration typically reduces the time to achieve the target drive level by a factor of two on sequence level changes. The Rapid Stop feature typically reduces the time to achieve a zero drive level by a factor of three when enabled. Figure 11 shows a drive sequence without the features enabled and Figure 12 illustrates the reduced time to target when Active Acceleration and Rapid Stop are enabled.

Note: The Active Acceleration and Rapid Stop features require frequency tracking to be enabled.

Figure 13 demonstrates the system with an actual LRA for an equivalent duration sequence without and with the Active Acceleration and Rapid Stop features. The nominal actuator acceleration is achieved faster and the stopping time is reduced by a factor of approximately eight.

Active Acceleration and Rapid Stop are enabled using ACCELERATION_EN and RAPID_STOP_EN.

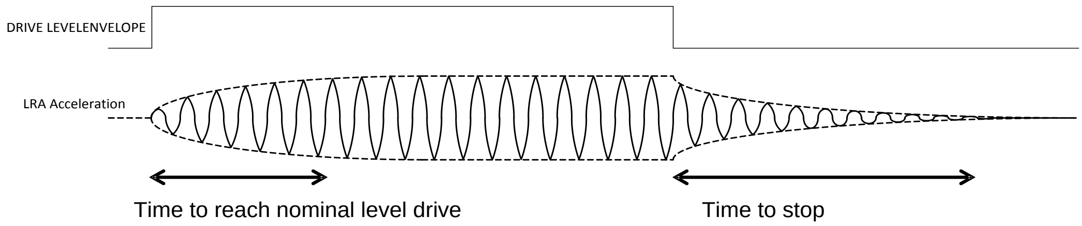


Figure 11: LRA Single Step Drive without Acceleration and Rapid Stop

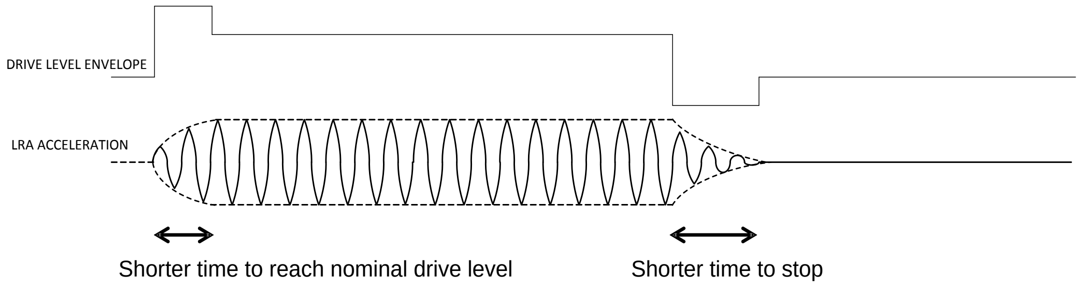


Figure 12: LRA Single Step with Acceleration and Rapid Stop

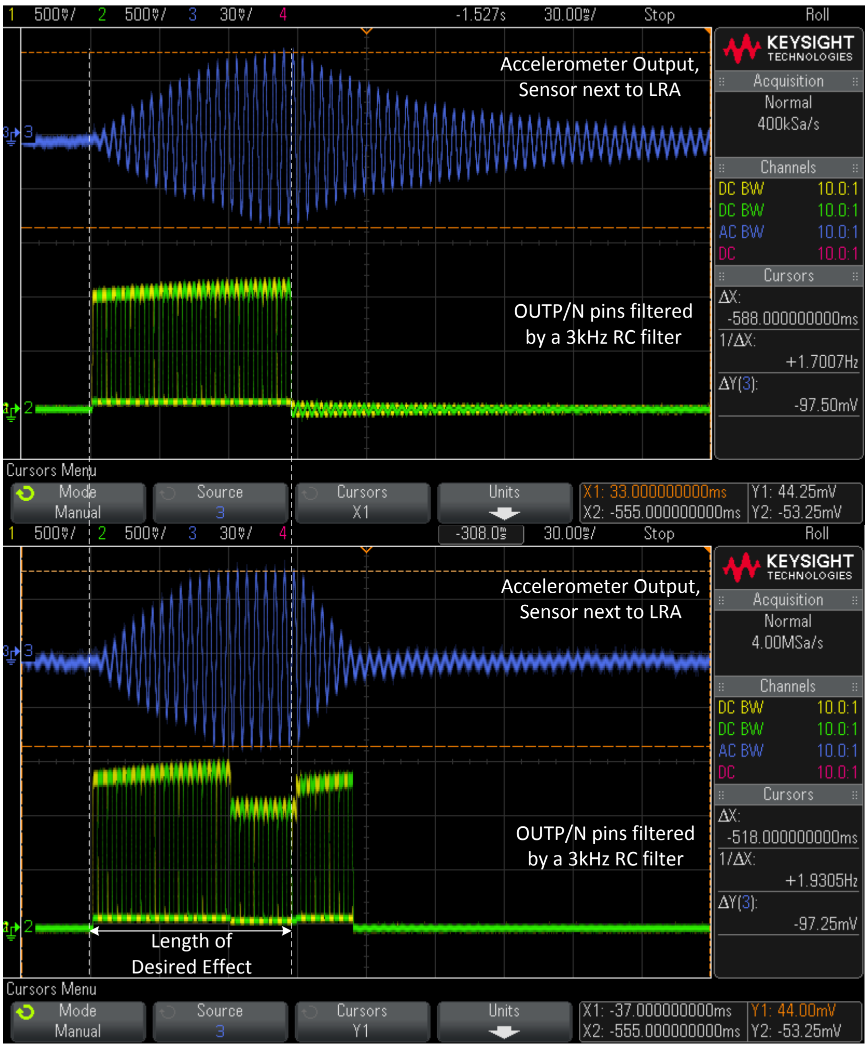


Figure 13: Simple Drive (Top) versus Active Acceleration and Rapid Stop Enabled (Bottom)

5.5 Wideband Frequency Control

DA7281 can be configured for wideband LRA support in DRO, RTWM, and ETWM modes. This allows an actuator to be driven outside of resonance to create a richer user experience. In this mode frequency tracking, Active Acceleration, and Rapid Stop features should be disabled. The accessible frequency range becomes 25 Hz to 1000 Hz. After configuring the device, see Section 5.6, the following applies:

In DRO mode, streaming is as described in Section 5.2.4. To change output frequency, a new value is uploaded to LRA_PER_H and LRA_PER_L.

In RTWM or ETWM modes, the frequency information is encoded into the frames of a sequence, see Section 5.8.3. For information on sequence playback, see Section 5.6. If a repeatable frequency is required at the start of a sequence, the first frame of a sequence must contain frequency information.

5.6 Device Configuration and Playback

Minimal one-time setup is required to drive any given actuator. This consists of setting the chosen actuator type with its key parameters and selecting the drive mode. The Dialog GUI automatically calculates the values required and sets the registers based on the entered actuator datasheet parameters. If the Dialog GUI is not used, follow the steps outlined in this section.

5.6.1 Boot

DA7281 comes out of reset when a power supply is provided to the device and boots for 1.5 ms. This is followed by entry to the Inactive mode where the device is kept in its lowest power state.

5.6.2 Actuator Setup

The following setup procedure needs to be observed to program DA7281 to work with a specific actuator:

1. Choose the correct actuator type using ACTUATOR_TYPE, 0 = LRA and 1 = ERM.
2. Choose the correct nominal maximum voltage across the actuator by checking the actuator datasheet for the maximum allowed RMS voltage and writing the value to ACTUATOR_NOMMAX. The allowable range is between 0 V and 6 V in 23.4 mV steps. The ACTUATOR_NOMMAX setting can be calculated using the following formula:

$$ACTUATOR\_NOMMAX[7:0] = \frac{V_{actuator\_nommax}}{23.4 \times 10^{-3}} \quad (1)$$

3. Choose the correct absolute maximum peak voltage across the actuator by checking the actuator datasheet and writing the value to ACTUATOR_ABSMAX. The allowable range is between 0 V and 6 V in 23.4 mV steps. The ACTUATOR_ABSMAX value can be calculated using the following formula:

$$ACTUATOR\_ABSMAX[7:0] = \frac{V_{actuator\_absmax}}{23.4 \times 10^{-3}} \quad (2)$$

4. Program the IMAX value (in units of mA) for the actuator using the following formula:

$$IMAX[4:0] = \frac{I_{\max\_actuator\_mA} - 28.6}{7.2} \quad (3)$$

   – where $I_{max\_actuator\_mA}$ is the actuator max rated current in mA, as listed in its datasheet. Note that in general this should slightly exceed the ACTUATOR_ABSMAX voltage divided by the actuator impedance.

5. Program the impedance of the actuator by checking the actuator datasheet and calculating the values for V2I_FACTOR_H and V2I_FACTOR_L using the following formulae:

$$V2I\_FACTOR[15:0] = \frac{Z \times (IMAX[4:0] + 4)}{1.6104} \quad (4)$$

$$V2I\_FACTOR\_H[7:0] = \frac{V2I\_FACTOR[15:0] - V2I\_FACTOR\_L[7:0]}{256} \quad (5)$$

$$V2I\_FACTOR\_L[7:0] = V2I\_FACTOR[15:0] - 256 \times V2I\_FACTOR\_H[7:0] \quad (6)$$

– Where V2I_FACTOR[15:0] is the 16-bit concatenation of V2I_FACTOR_H[7:0] and V2I_FACTOR_L[7:0], Z is the impedance of the actuator in Ω (as read from its datasheet), and IMAX[4:0] is the 5-bit value of IMAX.

6. Program the LRA resonant frequency in terms of period by updating LRA_PER_H and LRA_PER_L based on the following formula:

$$LRA\_PER[14:0] = \frac{1}{LRA_{freq} \times 1333.32 \times 10^{-9}} \quad (7)$$

$$LRA\_PER\_H[7:0] = \frac{LRA\_PER[14:0] - LRA\_PER\_L[6:0]}{128} \quad (8)$$

$$LRA\_PER\_L[6:0] = LRA\_PER[14:0] - 128 \times LRA\_PER\_H[7:0] \quad (9)$$

– Where LRA_{freq} represents the LRA resonant frequency in Hz, as listed in the actuator datasheet.

Note: For ERM this value will signify the frequency of BEMF sensing; if more frequent updates are required, the value can be increased up to 300 Hz.

For driving coin ERMs, see Section 5.7.18.

5.6.3 Automatic Output Control

DA7281 has several automatic control loops and mechanisms to ensure excellent playback fidelity and easy actuator setup:

- Automatic frequency tracking - this feature allows resonant frequency tracking during playback and is enabled via FREQ_TRACK_EN. Frequency tracking must be enabled to use the Active Acceleration and Rapid Stop features. For fine-tuning the frequency tracking loop, see Section 5.7.1.
- Active Acceleration - this feature improves playback fidelity by overdriving and underdriving the actuator to allow faster transitions between acceleration levels. This improves on the inherent actuator mechanical time constant. To enable Active acceleration set ACCELERATION_EN = 1. Note that the input data is interpreted as either unsigned (ACCELERATION_EN = 0) or signed (ACCELERATION_EN = 1). For more detail on data formatting, see Section 5.9.
- Rapid Stop - this is a mechanism to allow the fastest possible stop to zero acceleration output for the actuator. DA7281 achieves this by driving in full reverse the actuator by applying a 180° phase shift in the case of an LRA or inverting the voltage across the actuator in the case of an ERM actuator. For fine-tuning the Rapid Stop feature, see Section 5.7.2.

5.6.4 Waveform Memory Setup

The Waveform Memory is initially empty. The user can create any set of haptic sequences by following the Waveform Memory format described in Section 5.8. For ease of use, the Dialog GUI also provides a graphical tool to create sequences. The sequences can then be uploaded to the DA7281 Waveform Memory by going through the following steps:

1. Ensure that DA7281 is in Inactive mode (no playback ongoing and at least 1.5 ms have passed since cold boot).
2. Ensure the Waveform Memory is unlocked, set WAV_MEM_LOCK = 1.

3. Read back the location of SNP_MEM_0 by checking WAV_MEM_BASE_ADDR.
4. Write the new contents of the Waveform Memory by starting from SNP_MEM_0.
5. If desired, re-lock the Waveform Memory, set WAV_MEM_LOCK = 0.

Once the DA7281 Waveform Memory is configured, it is retained until a power-on reset event. The host can update the Waveform Memory as many times as needed during the lifetime of the device.

5.6.5 Mode Configuration

Set OPERATION_MODE according to the operating mode to be used. The device configuration flow is different for each operating mode. Sections 5.6.5.1 to 5.6.5.5 explain how to set up and operate the device in each of the operating modes.

5.6.5.1 Inactive Mode

- In Inactive mode, DA7281 waits in a low-power state in between playback events. For more details on power and latency trade-offs see Sections 5.2.1 and 5.2.3.

1. Set OPERATION_MODE = 0 for DA7281 to go to Inactive mode.
2. Configure STANDBY_EN to return to IDLE or STANDBY state after playback has finished.

5.6.5.2 Direct Register Override (DRO) Mode

Figure 14 shows how to operate the device in DRO mode.

1. Starting from either the IDLE or STANDBY state, write the initial drive amplitude of the haptic sequence to OVERRIDE_VAL.
2. When ready to begin playback, set OPERATION_MODE = 1. The output will begin switching after approximately 0.75 ms.
3. While in the DRIVE state, write to OVERRIDE_VAL to drive a new amplitude and create the desired envelope of the haptic sequence. If OVERRIDE_VAL = 0 during the DRIVE state, DA7281 will disable its output stage, but remain in a low latency-to-drive state and wait for further updates to OVERRIDE_VAL.
4. To stop driving set OPERATION_MODE = 0. DA7281 returns to either the IDLE or STANDBY state, depending on the value of STANDBY_EN.

Note: The allowable range of values written to OVERRIDE_VAL depends on whether ACCELERATION_EN is set to 1 or 0. If ACCELERATION_EN = 1 then the usable range for OVERRIDE_VAL is 0x00 to 0x7F. If ACCELERATION_EN = 0 then the usable range for OVERRIDE_VAL is 0x00 to 0xFF in two's complement. For further explanation, see Figure 31 and Figure 32.

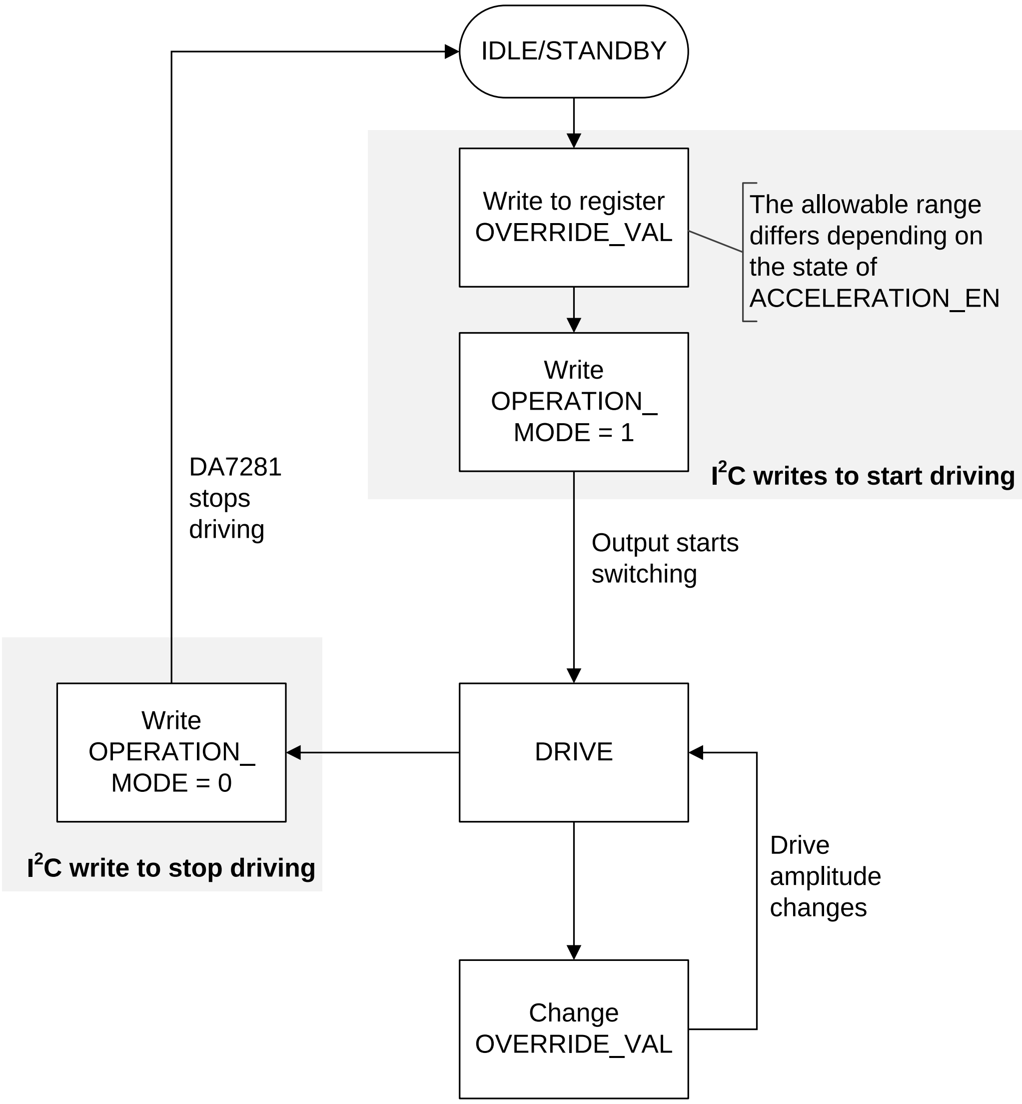


Figure 14: Operation in DRO Mode

5.6.5.3 PWM Mode

Figure 15 shows how to operate the device in PWM mode.

1. Starting from either the IDLE or STANDBY state, apply a PWM signal to the GPI/PWM pin.
2. When ready to begin playback, set OPERATION_MODE = 2. The output will begin switching after approximately 0.75 ms with a drive amplitude proportional to the duty cycle of the incoming PWM signal.
3. While in the DRIVE state, update the duty cycle of the PWM signal to drive a new amplitude level and create the desired envelope of the haptic sequence. If the duty cycle of the PWM signal falls below the threshold set by FULL_BRAKE_THR, it is interpreted as a zero output drive level.
4. In order to stop driving, set OPERATION_MODE = 0. DA7281 will return to either the IDLE or STANDBY state depending on the value of STANDBY_EN.

Note: The duty cycle of the PWM signal is interpreted differently depending on the value of ACCELERATION_EN. If ACCELERATION_EN = 1, then zero drive corresponds to 50 % duty cycle ± FULL_BRAKE_THR. If ACCELERATION_EN = 0, then zero drive corresponds to 0 % duty cycle + FULL_BRAKE_THR. For further explanation, see Figure 31 and Figure 32.

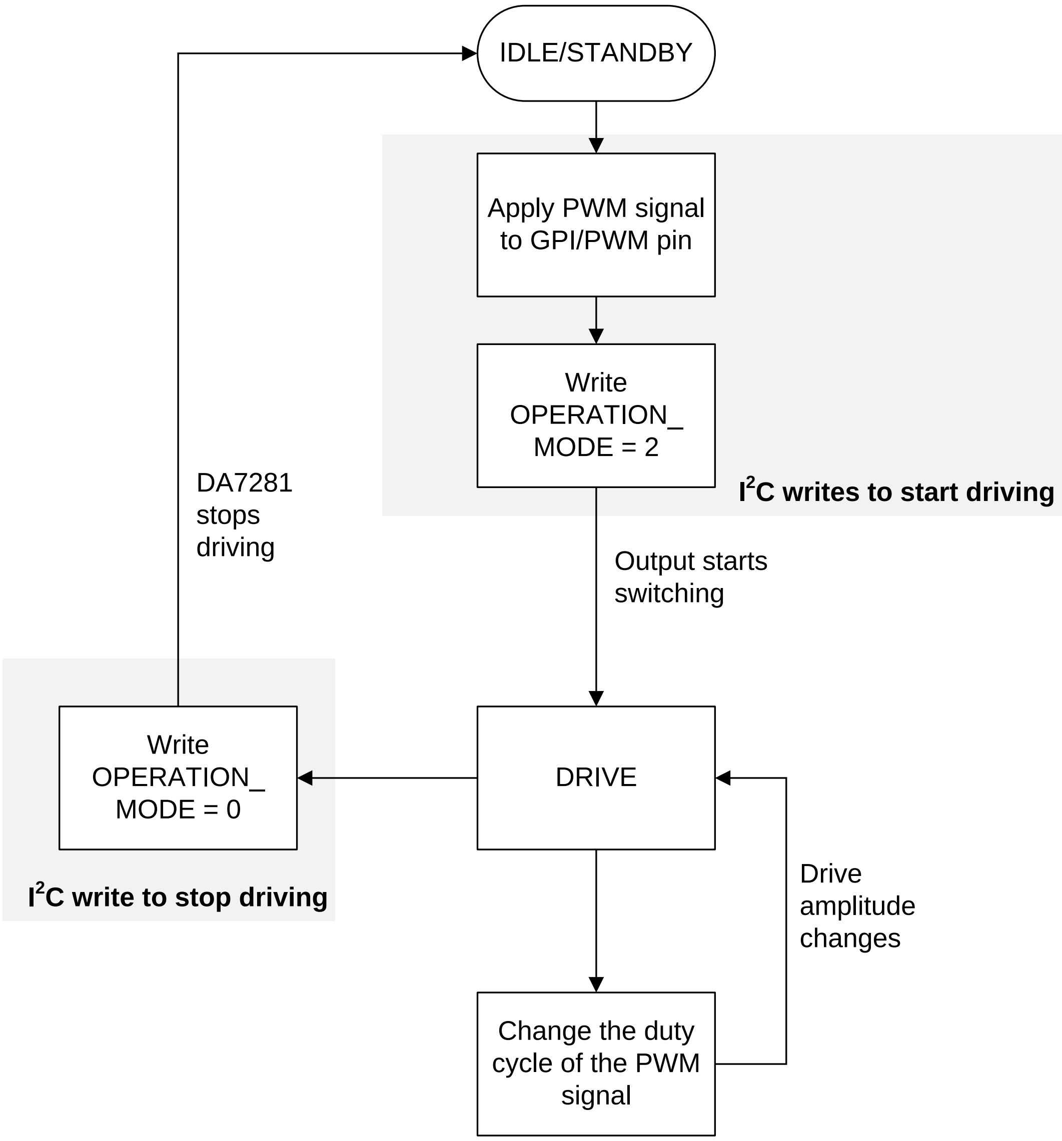


Figure 15: Operation in PWM Mode

5.6.5.4 Register Triggered Waveform Memory (RTWM) Mode

The following registers should be set up prior to operation in RTWM mode:

- Set FREQ_WAVEFORM_TIMEBASE according to the minimum or maximum sequence timebase required.
- Set SNP_MEM_x (where x = 0 to 99), see Section 5.8.
- If custom waveform sequences are required, see Section 5.7.5.
- Set WAV_MEM_LOCK = 0 to prohibit access to the waveform memory if required.

Figure 16 shows how to operate the device in RTWM mode.

1. While in the IDLE or STANDBY state, configure PS_SEQ_ID and PS_SEQ_LOOP to select the desired sequence from Waveform Memory.
2. For first-time playback, set OPERATION_MODE = 3. On subsequent sequence playbacks, this step can be skipped (if OPERATION_MODE = 3). The haptic sequence will not begin playing until a start event is created by setting SEQ_START = 1.
3. While in the DRIVE state, set SEQ_CONTINUE = 1 to repeat the sequence.
4. When the haptic sequence is completed, DA7281 will signal this by setting nIRQ = 0 and setting SEQ_DONE_M = 1. DA7281 will then return to IDLE or STANDBY state, depending on the value of STANDBY_EN.
5. Clear the nIRQ and SEQ_DONE_M signals, set SEQ_DONE_M =1.

At any time during operation in RTWM mode, set OPERATION_MODE or SEQ_START = 0 to return to the IDLE or STANDBY state.

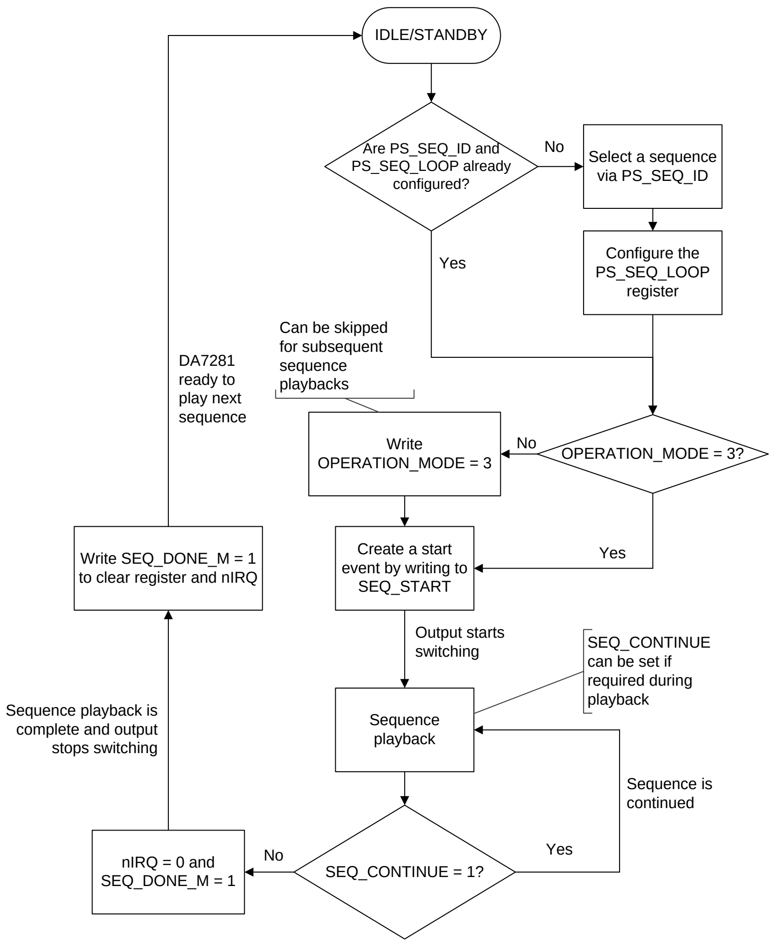


Figure 16: Operation in RTWM Mode

5.6.5.5 Edge Triggered Waveform Memory (ETWM) Mode

The following registers should be set up prior to operation in ETWM mode:

- Set SNP_MEM_x (where x = 0 to 99), see Section 5.8.
- Set FREQ_WAVEFORM_TIMEBASE according to the minimum or maximum sequence timebase required.
- If custom waveform sequences are required, see Section 5.7.5.
- Set WAV_MEM_LOCK = 0 to prohibit access to the waveform memory if required.

Figure 17 shows how to operate the device in ETWM mode.

1. Before first-time playback, set GPI_SEQUENCE_ID, GPI_MODE, and GPI_POLARITY, see Section 5.2.7. These bits determine which sequence the GPI/PWM pin points to, whether it triggers single or multiple sequences, and whether it reacts to rising, falling, or both edges.
2. Set PS_SEQ_ID and PS_SEQ_LOOP to select the sequence to play from Waveform Memory when a start event is created via writing to I^2C (SEQ_START). **Note:** If this has already been done, then this step can be skipped.
3. Set OPERATION_MODE = 4. On subsequent sequence playbacks, this step can be skipped (if OPERATION_MODE = 4). Haptic sequences will not begin playing until a start event is detected either by an edge on the GPI/PWM pin, or by setting SEQ_START = 1 via I^2C.
4. While in the DRIVE state, set SEQ_CONTINUE = 1 to repeat the sequence.
5. When the haptic sequence is completed, DA7281 will signal this by setting nIRQ = 0 and setting SEQ_DONE = 1. DA7281 will then return to IDLE or STANDBY state, depending on the value of the STANDBY_EN.
6. Clear the nIRQ and SEQ_DONE_M signals by setting SEQ_DONE_M = 0 via I^2C.

At any time during operation in ETWM mode, set OPERATION_MODE or SEQ_START = 0 to return to IDLE or STANDBY state.

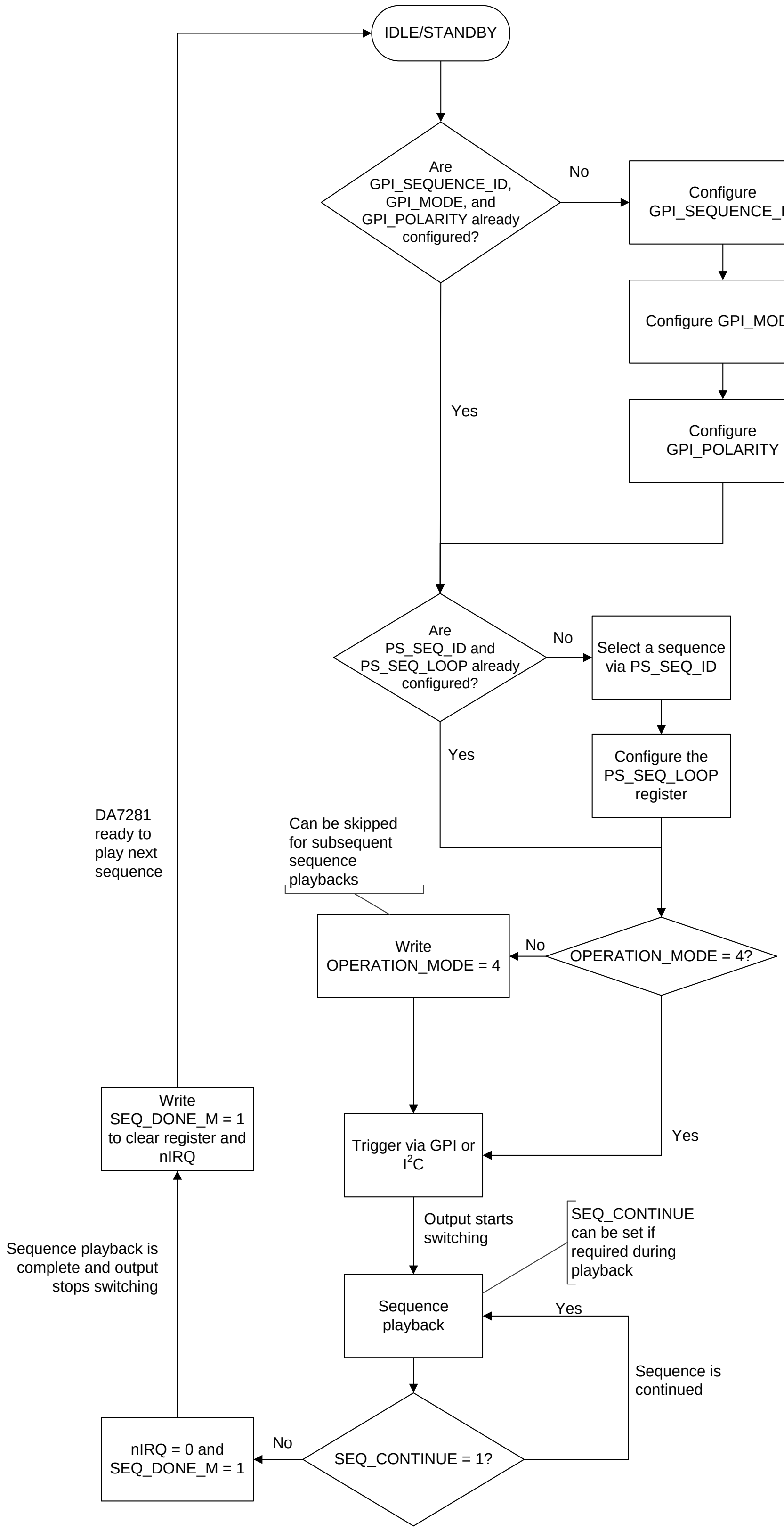


Figure 17: Operation in ETWM Mode

5.6.6 Events and Diagnostics

DA7281 supports a comprehensive system for device, supply, and actuator diagnostics based on faults, warnings, and notifications. Faults return DA7281 to IDLE state and hold the system in IDLE until cleared, while warnings and notifications are used for host information only. If events are generated, the host is notified by the open-drain nIRQ pin pulling low.

A single IRQ_EVENT1 byte containing all faults is presented to the host for simplified signaling. Warnings are reported via IRQ_EVENT_WARNING_DIAG and input data faults via IRQ_EVENT_SEQ_DIAG. Table 14 provides a summary of the full array of faults:

Table 14: Haptics Event Flag Descriptions

Event Name	Description	Required Action
Faults		
E_OC_FAULT	Short circuit / over-current fault	Write 1 to clear
E_ACTUATOR_FAULT	An issue detected with the actuator impedance, BEMF amplitude, or resonant frequency	Write 1 to clear
E_SEQ_FAULT	Sequence ID, Waveform Memory, or PWM fault has occurred	Read IRQ_EVENT_SEQ_DIAG for diagnostic information
E_OVERTEMP_CRIT	Over-temperature event	Write 1 to clear
E_UVLO	Under-voltage fault	Write 1 to clear
Notifications		
E_SEQ_DONE	Memory sequence playback is complete	Write 1 to clear
E_SEQ_CONTINUE	Playback of a new sequence has started by the host setting SEQ_CONTINUE	Write 1 to clear
E_WARNING	A system warning is in effect	Read warnings in IRQ_EVENT_WARNING_DIAG
E_ADC_SAT	The input to the voltage sense ADC has saturated	Check if V2I_FACTOR_H/L is set correctly for the driven actuator
Warnings		
E_LIM_DRIVE	Playback is limited due to battery lower than sequence target	Reduce drive level if needed
E_LIM_DRIVE_ACC	Acceleration is limited due battery lower than overdrive level	Reduce drive level if needed
E_MEM_TYPE	Input memory data type does not match acceleration configuration	Check data format
Input Data Faults		
E_SEQ_ID_FAULT	Requested sequence ID does not exist	Reload PS_SEQ_ID and Waveform Memory
E_MEM_FAULT	Waveform Memory corruption (empty bytes, non-existent snippet ID, wrong frame parameter)	Reload Waveform Memory
E_PWM_FAULT	PWM timeout	Restart PWM interface and write 1 to E_SEQ_FAULT to clear

All events are write 1 to clear and can be masked using IRQ_MASK1 and IRQ_MASK2. Some of the sources generating E_ACTUATOR_FAULT can be disabled, for frequency tracking see Section 5.7.1 and for BEMF voltage amplitude see Section 5.7.14. For self-clearing of faults once in IDLE state, see Section 5.7.7.

5.7 Advanced Operation

DA7281 features several advanced modes of operation to fine-tune actuator haptic performance.

5.7.1 Frequency Tracking

The closed-loop frequency tracking on DA7281 is implemented via a proportional-integral (PI) controller. The proportional coefficient (Kp) is stored in FRQ_PID_Kp_H/L and the integral coefficient (Ki) in FRQ_PID_Ki_H/L. The default values of the coefficients are optimized to cover a wide range of actuators with typical settling times of approximately 40 ms from a 20 % frequency offset. If further optimization is required to target a specific actuator the coefficients can be updated. The LRA tuning tool in the DA7281 SmartCanvas GUI provides an intuitive and graphical way to easily adjust the Kp and Ki coefficients.

To increase absolute accuracy of the lock during playback, DA7281 supports automatic scaling of the frequency tracking controller proportional coefficient. This feature is enabled via FREQ_TRACKING_AUTO_ADJ and becomes active after the device has achieved initial frequency lock. The FRQ_LOCKED_LIM value is used to determine the threshold for the initial lock and can be scaled up or down depending on system requirements.

The resonant frequency tracking algorithm converges to the correct value from up to 25 % offset between the initial nominal datasheet value and the actual resonant frequency. This range is conservative to prevent unwanted behavior. A fault triggers if the actuator resonant frequency is outside the 50 Hz to 300 Hz range. To block these checks, set FREQ_TRACKING_FORCE_ON = 1.

FRQ_TRACK_BEMF_LIM disables the frequency tracking if the BEMF signal becomes too low. It should always be set lower than the value in RAPID_STOP_LIM.

The instantaneous value of the resonant frequency period is updated every half-period and written to LRA_PER_ACTUAL_H/L. The values can be converted to period using the following formula:

$$LRA\ period\ (ms) = 1333.32 \times 10^{-9} \times (128 \times LRA\_PER\_ACTUAL\_H + LRA\_PER\_ACTUAL\_L) \quad (10)$$

If more accurate information is required (for example if a frequency tracking enabled sequence is played to determine the resonant frequency before entering wideband operation), the average resonant frequency information over the last four half-periods is written to LRA_PER_AVERAGE_H/L. The values can be converted to period using the following formula:

$$LRA\ period\ (ms) = 1333.32 \times 10^{-9} \times (128 \times LRA\_PER\_AVERAGE\_H + LRA\_PER\_AVERAGE\_L) \quad (11)$$

5.7.2 Rapid Stop

The Rapid Stop algorithm relies on actuator BEMF sensing to detect actuator motion during a stop-to-zero LRA acceleration. The algorithm provides a stopping signal to the LRA until the actuator crosses the point of no acceleration. Since drive updates happen only at the zero cross point, this introduces latency that may cause the actuator to overshoot the stop position. Due to this, the Rapid Stop will also trigger at a pre-determined threshold set by RAPID_STOP_LIM. The default setup covers most actuators, but if Rapid Stop is too short (actuator not fully stopped), the register value should be decreased; and if Rapid Stop overshoots (actuator stopped and then reversed), the register value should be increased.

Note: The Rapid Stop algorithm can be triggered only for sequences longer than three half-periods.

5.7.3 Initial Impedance Update

DA7281 performs an impedance measurement at the very first half-period of drive at the start of playback. This allows a one-shot update of V2I_FACTOR_H/L to take into account specific actuator variation for increased voltage accuracy of the drive. The result is reported to IMPEDANCE_H/L, which can be read by the host and converted to impedance using the following formula:

$$Actuator\ Impedance(R_{series}) = (IMPEDANCE\_H \times 4 + IMPEDANCE\_L) \times 0.0625\Omega \quad (12)$$

To disable this feature, set V2I_FACTOR_FREEZE and CALIB_IMPEDANCE_DIS = 1.

5.7.4 Amplitude PID

Some cylinder based ERMs generate excessively large-amplitude BEMF voltages. DA7281 can compensate for this by reducing the drive current level, set AMP_PID_EN = 1. The result is an improved haptic response. Figure 18 describes how the actuator voltage and current differs when AMP_PID_EN enabled or disabled.

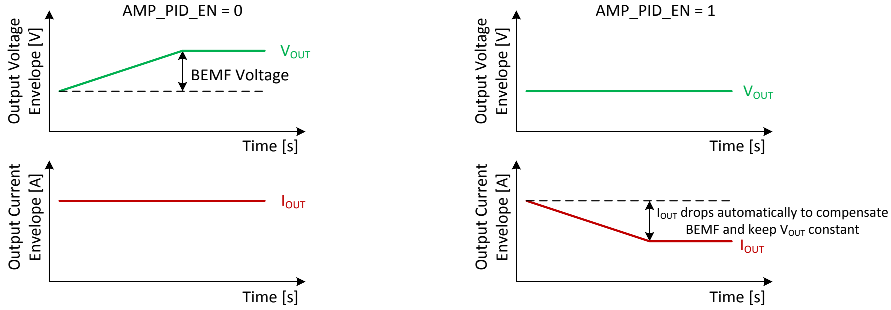


Figure 18: Output Voltage and Current for Different AMP_PID_EN Values

Note: This is not usually required for LRAs as the amplitude of the BEMF is typically very low.

5.7.5 Wideband Operation

DA7281 natively supports wideband LRAs and allows continuous frequency updates to the output signal while driving. Amplitude and frequency data use parallel data paths, for configuration see Section 5.6.5. This section describes how to use the frequency component only.

For wideband operation, frequency tracking must be disabled, by setting FREQ_TRACK_EN = 0, because drive at frequencies different from the actuator resonant frequency is required. Rapid Stop and Active Acceleration also rely on frequency tracking so must be deactivated by setting ACCELERATION_EN = 0 and RAPID_STOP_EN = 0. There are two ways to operate DA7281 during wideband operation:

- In the limited frequency range of 25 Hz to 300 Hz:
  - No further settings are required in RTWM and ETWM modes if the frequency information is already stored in the Waveform Memory frame data as described in Section 5.8.3. If the Waveform Memory does not contain frequency information, then each sequence can be played at a different frequency by setting LRA_PER_H and LRA_PER_L to the desired value via the formulae in Section 5.6.2 before triggering playback using the method described in Sections 5.6.5.4 and 5.6.5.5.
  - In the DRO and PWM modes, the frequency information can be updated via the LRA_PER_H and LRA_PER_L using the formulae in Section 5.6.2 either before triggering playback of each sequence, see Sections 5.6.5.2 and 5.6.5.3, or during the playback itself. As with amplitude, the one half-period uncertainty on the output frequency update also applies.
- In the full range of 25 Hz to 1024 Hz, the same procedures apply for all modes, but the following registers need to be set:
  - BEMF_SENSE_EN = 0
  - DELAY_H = 0
  - DELAY_SHIFT_L = 0
  - DELAY_FREEZE = 1

5.7.6 Custom Waveform Operation

With frequency tracking, Active Acceleration, and Rapid Stop disabled, and with the additional setup for wideband operation described in Section 5.7.5, DA7281 can be configured to drive a custom waveform to an LRA actuator. It is important to note that here the custom waveform denotes the actual output during a single LRA resonant period and not the overall amplitude envelope during drive events, which is controlled as previously described in Section 5.6.5. Amplitude and frequency data can be streamed as usual in DRO, PWM, RTWM, or ETWM modes.

The waveform output during a single resonant period comprises of 16 distinct points, see Figure 19, where points 0 to 4 are mirrored and repeated to create, by default, a sine wave (for example, point 3 and point 5, and point 2 and point 6 have the same amplitude).

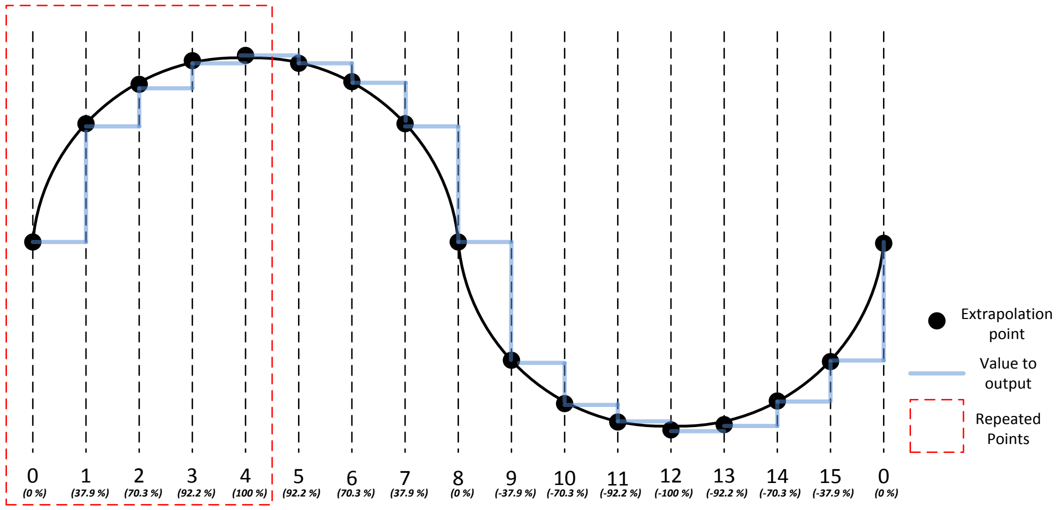


Figure 19: Custom Wave Point Numbering

Point 0 is corresponds to an amplitude of 0 % of the value of IMAX, point 4 corresponds to an amplitude of 100 %, and points 1, 2, and 3 are scaled to the IMAX value by the unsigned CUSTOM_WAVE_GEN_COEFF1, CUSTOM_WAVE_GEN_COEFF2, and CUSTOM_WAVE_GEN_COEFF3 coefficient values. The default coefficients are set to correspond to a sine wave but can be updated to recreate any required waveform that is built of four symmetrical sections, see Figure 19.

Table 15 contains a summary of the default coefficients and their settings.

Table 15: Default CUSTOM_WAVE_GEN_COEFFx Settings

Point	% of IMAX[4:0]	Corresponding Bits
0	0	-
1	37.9	CUSTOM_WAVE_GEN_COEFF1
2	70.3	CUSTOM_WAVE_GEN_COEFF2
3	92.2	CUSTOM_WAVE_GEN_COEFF3
4	100	-

Configure the following bits to enable custom waveform operation:

- BEMF_SENSE_EN = 0
- WAVEGEN_MODE = 1
- V2I_FACTOR_FREEZE = 1
- DELAY_H = 0
- DELAY_SHIFT_L = 0
- DELAY_FREEZE = 1
- ACCELERATION_EN = 0
- RAPID_STOP_EN = 0
- AMP_PID_EN = 0

After the above setup is executed, amplitude data can be streamed in any mode, see Section 5.6.5, and output frequency can be updated, see Section 5.7.6.

5.7.7 Embedded Operation

Should DA7281 be required to operate in a setup where no host is present or due to software limitations unable to communicate with the device during its required operation, DA7281 can operate in embedded operation by setting EMBEDDED_MODE = 1. In this case DA7281 is configured to clear all system faults as it enters inactive mode when playback is finished or if a fault has been detected, see Section 5.6.6.

For example, if a short circuit occurs, the system will react in its usual way: stop driving, disable the current loop, and go to Inactive mode. Once in Inactive mode, the generated interrupt is automatically cleared and DA7281 will attempt to drive again on the next playback request without the host having to come in and clear faults.

5.7.8 Polarity Change Reporting for Half-Period Control in DRO Mode

For advanced sequence playback in DRO mode, the host may require DA7281 to update the output drive amplitude every half period. Since the I^2C clock is asynchronous to the DA7281 internal clock and the exact timing of the half-period will change dynamically based on the frequency tracking loop, this is not a trivial operation.

To overcome this limitation, the register POLARITY provides feedback. POLARITY toggles at the start of every half-period (so at a rate of 400 Hz for a 200 Hz resonant frequency actuator). This allows software synchronization of the updates to the OVERRIDE_VAL, see Figure 20.

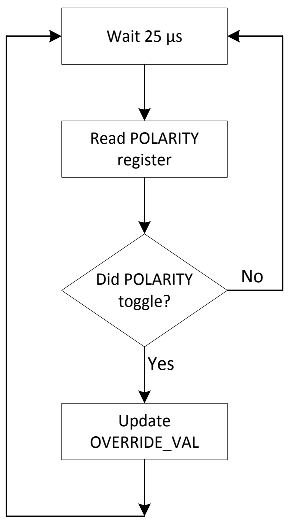


Figure 20: Half-Period Control in DRO Mode

The timing of the sequence can be described as follows in Figure 21 where Amplitude X denotes consecutive different output drive values:

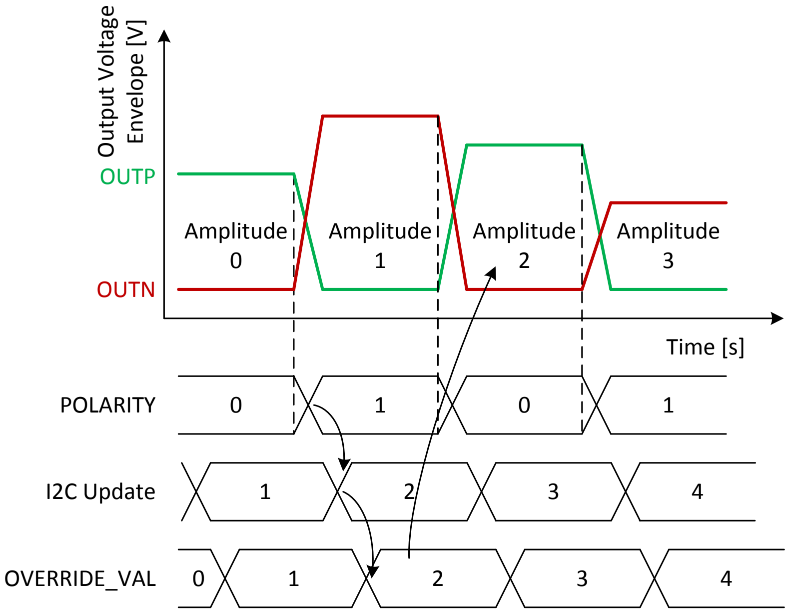


Figure 21: Polarity Timing Relationship

5.7.9 Loop Filter Configuration

Haptic actuators (both ERM and LRA) can be modelled as a series combination of a resistor (Series R) and inductor (Series L) followed by a BEMF voltage source, see Figure 22.

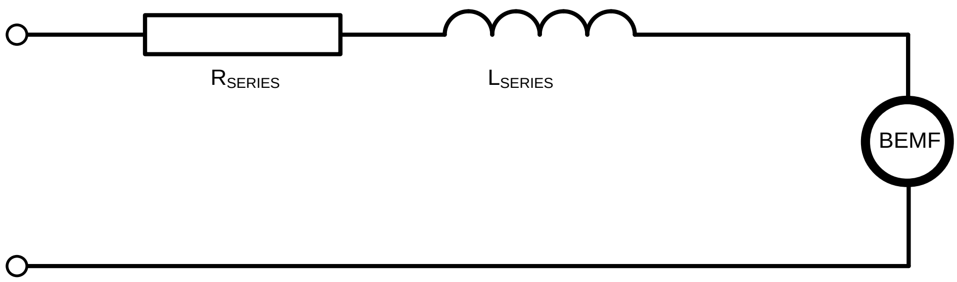


Figure 22: Equivalent Electrical Model of an Actuator

The usual variation of R_{SERIES} is from 8 Ω to 50 Ω and L_{SERIES} is from 20 µH to either 2 mH or 3 mH. The current regulation loop in the output drive must be kept stable by applying the correct setting in the loop's filter. While the defaults cover the vast majority of available LRAs and ERMs further tuning is possible by adjusting LOOP_FILT_CAP_TRIM, LOOP_FILT_RES_TRIM, and LOOP_FILT_LOW_BW.

For LOOP_FILT_CAP_TRIM apply the settings in Table 16.

Table 16: LOOP_FILT_CAP_TRIM Register Trim Settings

	Actuator Series Resistance (Ω)			
Register	**< 18**	**18 to 28**	**28 to 41**	**> 41**
LOOP_FILT_CAP_TRIM	3	2	1	0

For LOOP_FILT_RES_TRIM apply the settings in Table 17.

Table 17: LOOP_FILT_RES_TRIM Register Trim Settings

	L_{series} (µH)									
R_{series} (Ω)	25 or lower	50	75	100	125	150	175	200	225	250 or higher
4	2	2	3	3	3	3	3	3	3	3
6	1	2	2	3	3	3	3	3	3	3
8	1	2	2	2	3	3	3	3	3	3
10	0	1	2	2	2	3	3	3	3	3
12	0	1	2	2	2	2	3	3	3	3
14	0	1	1	2	2	2	2	3	3	3
16	0	1	1	2	2	2	2	2	3	3
18	0	0	1	1	2	2	2	2	2	3
20	0	1	1	2	2	2	3	3	3	3
22	0	1	1	2	2	2	2	3	3	3
24	0	1	1	2	2	2	2	3	3	3
26	0	1	1	2	2	2	2	2	3	3
28	0	1	2	2	2	3	3	3	3	3
30	0	1	2	2	2	3	3	3	3	3
32	0	1	2	2	2	2	3	3	3	3
34	0	1	1	2	2	2	3	3	3	3
36 to 40	0	1	1	2	2	2	2	3	3	3
42	0	1	2	2	3	3	3	3	3	3
44	0	1	2	2	3	3	3	3	3	3
46 to 50	0	1	2	2	2	3	3	3	3	3

Set LOOP_FILT_LOW_BW high if the actuator inductance exceeds 1 mH.

5.7.10 UVLO Threshold

The DA7281 UVLO has a default fall threshold of 2.8 V. This is adjustable in 100 mV steps via REF_UVLO_THRES. The full range is 2.7 V to 3.0 V.

5.7.11 Edge Rate Control

DA7281 contains an advanced switching node ERC to minimize EMI and board disturbances. The slope of the ERC can be adjusted by changing the values of the HBRIDGE_ERC_LS_TRIM (for low-side FET ERC) and HBRIDGE_ERC_HS_TRIM (for high-side FET ERC). Default value is 100 mVn/s and the adjustable range is 25 mV/ns to 100 mV/ns in 25 mV/ns steps.

5.7.12 Double Output Current Range

The nominal current rating for the DA7281 current regulation output is 250 mA. This range covers existing LRAs, however some LRA manufacturers allow significant actuator overdrive over short periods of time. DA7281 supports this by enabling LOOP_IDAC_DOUBLE_RANGE, which doubles the maximum output current. When this is enabled, the following setup changes apply:

- IMAX now corresponds to twice the value computed by the formula in Section 5.6.2.
- When setting the impedance in V2I_FACTOR_H and V2I_FACTOR_L via the formula in Section 5.6.2, use $Z_{formula} = 2*Z_{real}$.
- When reading back from IMPEDANCE_H and IMPEDANCE_L, use an LSB of 0.03125 Ω.

5.7.13 Supply Monitoring, Reporting, and Automatic Output Limiting

DA7281 monitors the level of the supply during playback and reports it via ADC_VDD_H and ADC_VDD_L. The two should be concatenated and read using the following formula:

$$VDD\ Supply\ Voltage = (ADC\_VDD\_H \times 128 + ADC\_VDD\_L) \times 0.1831\ mV \qquad (13)$$

DA7281 uses this information to prevent the device from clipping to supply by limiting the drive to a value determined by the VDD_MARGIN register in 187.5 mV steps where 0x0 corresponds to no margin, see Figure 23.

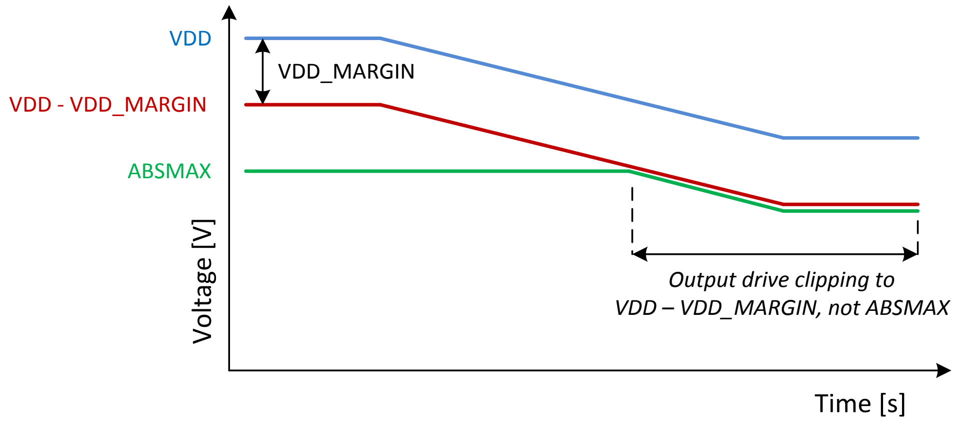


Figure 23: Automatic Output Limiting

The functionality is needed as DA7281 regulates current and if supply clipping occurs, the regulation stops and the BEMF information is lost. Furthermore, the VDD_MARGIN register allows limiting of the power across the actuator for low supply values to prevent the battery from discharging too fast.

5.7.14 BEMF Fault Limit

To detect malfunctioning actuators that have stopped moving due to a mechanical fault, DA7281 can be configured to trigger an actuator fault if the BEMF voltage level falls below a threshold for long drive durations. The threshold for detection is set in BEMF_FAULT_LIM; a zero value of the register disables the fault checking.

5.7.15 Increasing Impedance Detection Accuracy

To increase the accuracy of the impedance reading in IMPEDANCE_H and IMPEDANCE_L, the register V2I_FACTOR_OFFSET_EN could be set to 0. This removes an algorithmic offset utilized by the acceleration algorithm. Should V2I_FACTOR_OFFSET_EN be equal to 0, ACCELERATION_EN is recommended to be set to 0.

5.7.16 Frequency Pause during Rapid Stop

To address low mechanical time constant LRAs (start/stop times less than 20 ms) and improve the braking behavior, DA7281 has the option to pause frequency tracking during the execution of the Rapid Stop algorithm by setting FRQ_PAUSE_ON_POLARITY_CHANGE to 1.

5.7.17 Frequency Pause during Rapid Stop

If DA7281 is used with LRAs that have significant BEMF voltage amplitude that can transiently exceed the IR drop across an actuator when reversing the phase of the drive signal, it is recommended to set DELAY_BYPASS to 0.

5.7.18 Coin ERM Operation

The term coin ERM is used to describe an eccentric rotating mass actuator that is flat and has coin-like external appearance. The eccentric rotating mass is circular and contains two coil windings that are used for commutation, see Figure 24.

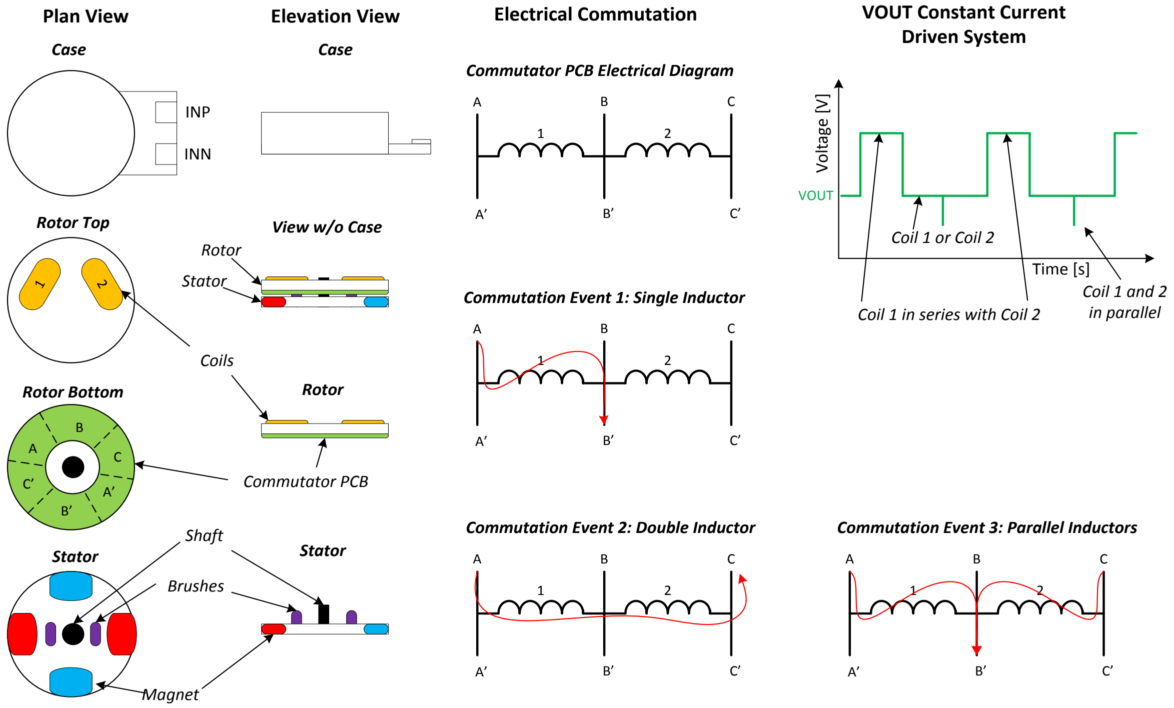


Figure 24: Coin ERM Physical and Electrical Summary

Due to the commutation of the motor, the impedance varies between one coil, two coils in series, and for very short periods two coils in parallel. Due to this behavior, DA7281 cannot extract the BEMF and actuator motion is not detectable for coin ERM actuators. Therefore, Active Acceleration and Rapid Stop features are not available. Manual overdrive or underdrive of the coin ERM to speed up the transition between two levels of acceleration is possible and recommended for better user experience. Note that due to the varying impedance and the constant current drive of DA7281, the output voltage will vary, with no effect on the performance of the DA7281, see Figure 24.

Recommended setup specific for a coin ERM, in addition to generic ERM setup described in Section 5.6.2:

- ACCELERATION_EN = 0
- RAPID_STOP_EN = 0
- AMP_PID_EN = 0
- V2I_FACTOR_FREEZE = 1
- CALIB_IMPEDANCE_DIS = 1
- BEMF_FAULT_LIM = 0
- Set the V2I factor using the single winding impedance, see Section 5.6.2
- Set IMAX using the maximum start-up current, see Section 5.6.2

5.8 Waveform Memory

The Waveform Memory stores haptic drive sequences. A single haptic effect is called a sequence and each sequence is formed by one or more frames that address one or more snippets stored in memory. The overall Waveform Memory structure is described in detail in Section 5.8.1; Sections 5.8.2 to 5.8.4 provide definitions for snippets, frames, and sequences.

Alternatively, the Dialog GUI can be used to easily construct sequences and upload them to the Waveform Memory. The GUI provides intuitive visualization of the sequences in the Waveform Memory and requires only basic knowledge of the overall memory format.

5.8.1 Waveform Memory Structure

The waveform memory structure has a 100-byte capacity for storing snippets, frames, and sequences. Sequences reference the snippets using frames to allow complex haptic sequences to be created in a memory efficient manner. The overall structure of the Waveform Memory can be seen in Figure 25. For Waveform Memory programming, see Section 5.6.4.

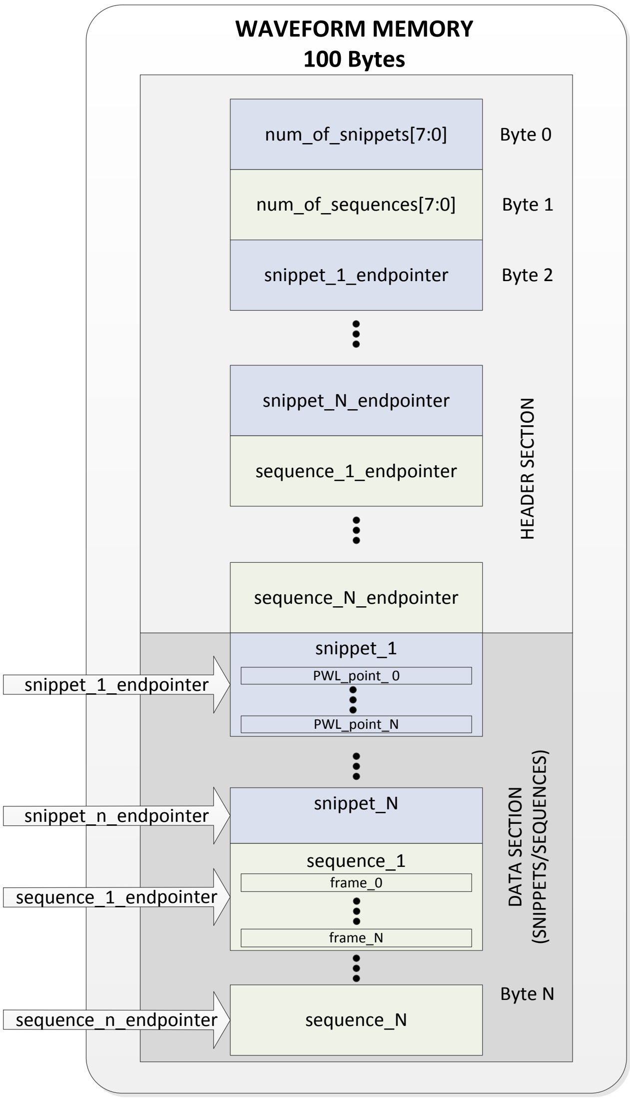


Figure 25: Waveform Memory Structure

5.8.1.1 Header Section

The three sections constituting the header for the Waveform Memory are:

- Byte 0: Defines the number of snippets stored.
- Byte 1: Defines the number of sequences stored.
- Byte 2 and onwards: The snippet(s), frames, and sequence(s) end address pointer(s) are stored. Each pointer address occupies one byte. Up to 15 snippets can be addressed in addition to snippet 0, which is the silence snippet. Up to 16 sequences can be addressed.

5.8.1.2 Data Section

The upper memory section contains the PWL data describing the snippets, see Table 18. The lower part of the memory contains the pre-stored sequences.

The set of snippet IDs must be consecutive numbers starting from SNP_ID = 1. For example, for a set containing three snippet IDs, {SNP_ID = 1, SNP_ID = 2, SNP_ID = 3} is allowed but {SNP_ID = 1, SNP_ID = 3, SNP_ID = 4} is not allowed.

5.8.2 Snippet Definition

Snippets are formed by storing a series of one or more piecewise linear (PWL) amplitude and time pairs. Snippets represent the basic building blocks used in the Waveform Memory.

Table 18: PWL Byte Structure

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Description	RMP	TIME[6:4]			AMP[3:0]			

A byte is allocated for each amplitude and time pair in the Waveform Memory, see Table 18. A snippet consists of one or more bytes containing RMP, TIME and AMP data.

- RMP defines whether a ramp (RMP = 1) or a step (RMP = 0) is required between consecutive time and amplitude pairs.
- TIME contain the unitless time information (number of timebases).
- AMP contains the amplitude information of the snippet.

For example, the snippet shown in Figure 26 will create a waveform that ramps from zero to an amplitude of 1111 over a period of two timebases, then step from 1111 to 1000, and remain there for four timebases. The length (in milliseconds) of a timebase is specified using the TIMEBASE frame bits, see Section 5.8.3.

Description	**RMP**	**TIME[6:4]**			**AMP[3:0]**			
Ramp	1	0	1	0	1	1	1	1
Step	0	1	0	0	1	0	0	0

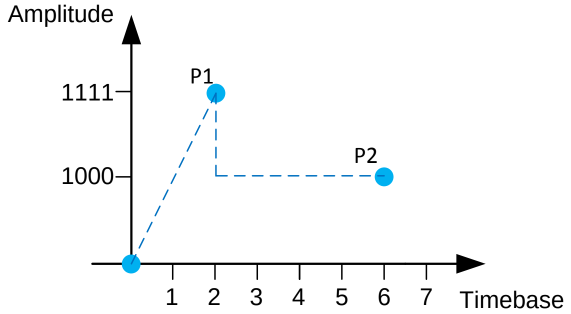


Figure 26: Snippet Ramp and Step with ACCELERATION_EN = 1

If a constant drive level is required for longer than 15 timebases, set RMP = 0 for consecutive PWL points.

Figure 27 shows a generic example of a snippet, where Pn represents the PWL pair located at amplitude An and with time step Tn, where n represents the PWL pair number.

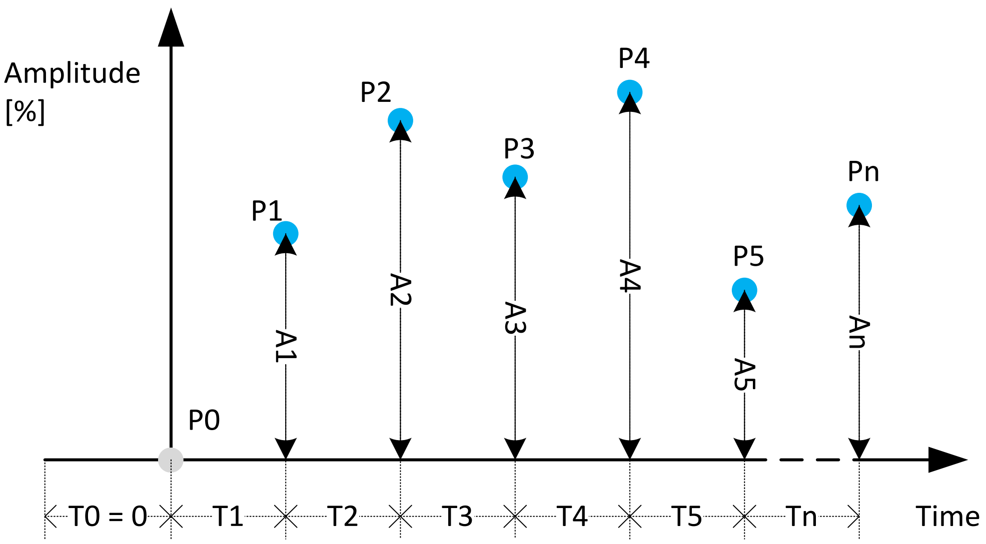


Figure 27: Snippet Example

5.8.3 Frame Definition

A frame consists of a collection of parameters used to define the playback of a snippet with differing gain, time base, carrier frequency, and number of repetitions. A frame consists of up to three bytes, its structure is shown in Figure 28. The frame parameters can be easily set up using the Dialog GUI.

- Byte 1 is mandatory, if COMMAND_TYPE = 0 then only Byte 1 exists. If COMMAND_TYPE = 1 in Byte 1 then Byte 2 (at least) exists.
- Byte 2 is optional.When used, set COMMAND_TYPE = 1 in both Byte 1 and Byte 2.
- Byte 3 is optional, for use in wideband sequences only and contains the frame frequency eight LSBs.

If COMMAND_TYPE of frame Byte 2 is set to 1 and FREQ_CMD = 1, then the Byte 3 contains drive frequency data to enable wideband LRA support.

All frame parameters except COMMAND_TYPE, SNP_ID_L, GAIN, and TIMEBASE are optional. For a full description, see Table 19.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 1 =>	COMMAND_ TYPE = 0	GAIN [1:0]		TIMEBASE[1:0]		SNP_ID_L[2:0]		
Byte 2 =>	COMMAND_ TYPE = 1	SNP_ID_LOOP[3:0]				FREQ_CMD	FREQ[8]	SNP_ID_H
Byte 3 =>	FREQ[7:0]							

Figure 28: Command Structure for a Single Frame

Table 19: Bit Definitions for Frame Parameters

Byte Number	Register Bit Definitions	Description
1 and/or 2	COMMAND_TYPE	COMMAND_TYPE labels the byte and tells the system how to interpret the following seven LSBs. COMMAND_TYPE = 0 signifies Byte 1 only is used COMMAND_TYPE = 1 signifies Byte 2 is present
1	GAIN[1:0]	Gain applied to the snippet identified by SNP_ID_L/H: 00 = 0 dB 01 = -6 dB 10 = -12 dB 11 = -18 dB
1	TIMEBASE[1:0]	The timebase length of the snippet pointed to by the snippet ID. This register is interpreted differently depending on FREQ_WAVEFORM_TIMEBASE: If FREQ_WAVEFORM_TIMEBASE = 0 (**default**): 00 = 5.44 ms 01 = 21.76 ms 10 = 43.52 ms 11 = 87.04 ms If FREQ_WAVEFORM_TIMEBASE = 1: 00 = 1.36 ms 01 = 5.44 ms 10 = 21.76 ms 11 = 43.52 ms
1	SNP_ID_L[2:0]	SNP_ID_L is mandatory and contains the LSBs of the snippet ID (SNP_ID). Up to eight snippets can be addressed.
2	SNP_ID_LOOP[3:0]	SNP_ID_LOOP is the loop multiplier of the snippet identified by SNP_ID_L/H and shows how many times a snippet is looped. If not present, the loop multiplier is 1. Possible values are 1 to 16. When the loop multiplier is > 1, playback begins from P1 instead of P0, see Figure 27, after the first snippet loop is complete.
2	FREQ_CMD	If FREQ_CMD = 1, the frame is a 3-byte command with frequency information. The frequency information is stored in FREQ[7:0].
2	FREQ[8]	Drive frequency MSB. The total frequency range is represented by the 9-bit concatenation of FREQ[8] and FREQ[7:0] (possible values: 0 to 511), which corresponds to the range 1 Hz to 1024 Hz. The LSB step size is 2 Hz and values below 25 Hz are interpreted as 25 Hz. The result is also converted from frequency to period and stored in the FRQ_LRA_PER_ACT_x registers for read-back.
2	SNP_ID_H	SNP_ID_H is the MSB of the snippet ID (SNP_ID). This can be used to increase the range of addressable snippets from 8 to 16. This bit is optional and if not present SNP_ID_H = 0.
3	FREQ[7:0]	Drive frequency LSBs. The total frequency range is represented by the nine bit concatenation of FREQ[8] and FREQ[7:0] (possible values: 0 to 511), which corresponds to the range 1 Hz to 1024 Hz. The LSB step size is 2 Hz and values below 25 Hz are interpreted as 25 Hz. The result is also converted from frequency to period and stored in the FRQ_LRA_PER_ACT_x registers for read-back.

5.8.4 Sequence Definition

A sequence is built up of one or more frames, see Figure 29, and written to memory using the format described in Section 5.8.1.

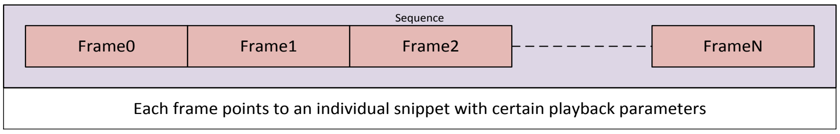


Figure 29: Sequence Structure

Note: Only sequences can be played. It is not possible to point directly to a snippet (although a sequence can be created which contains only one snippet).

A built-in snippet containing a single, silent PWL point (amplitude = 0) is available by setting SNP_ID = 0. The duration is set to two timebases.

5.8.4.1 Pre-Stored Waveform Memory Example

Figure 30 shows an example of a typical Waveform Memory operation with all features enabled.

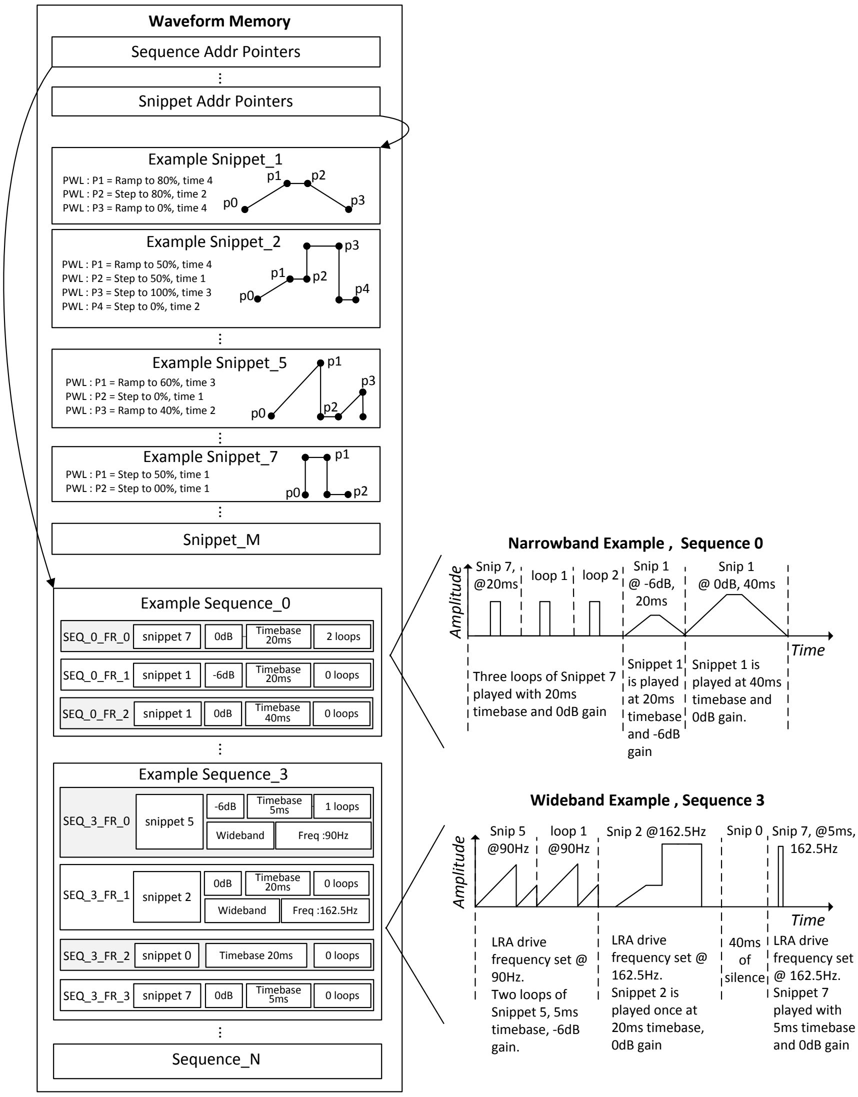


Figure 30: Waveform Memory Example

5.9 General Data Format

This section describes the data format used by the three different data input sources (DRO, PWM, and Waveform Memory). Four bits are used for storing the envelope value of snippets in Waveform Memory. Interpretation of the data is different depending on ACCELERATION_EN. For an overview of the data interpretation with and without Active Acceleration enabled, see Figure 31 and Figure 32.

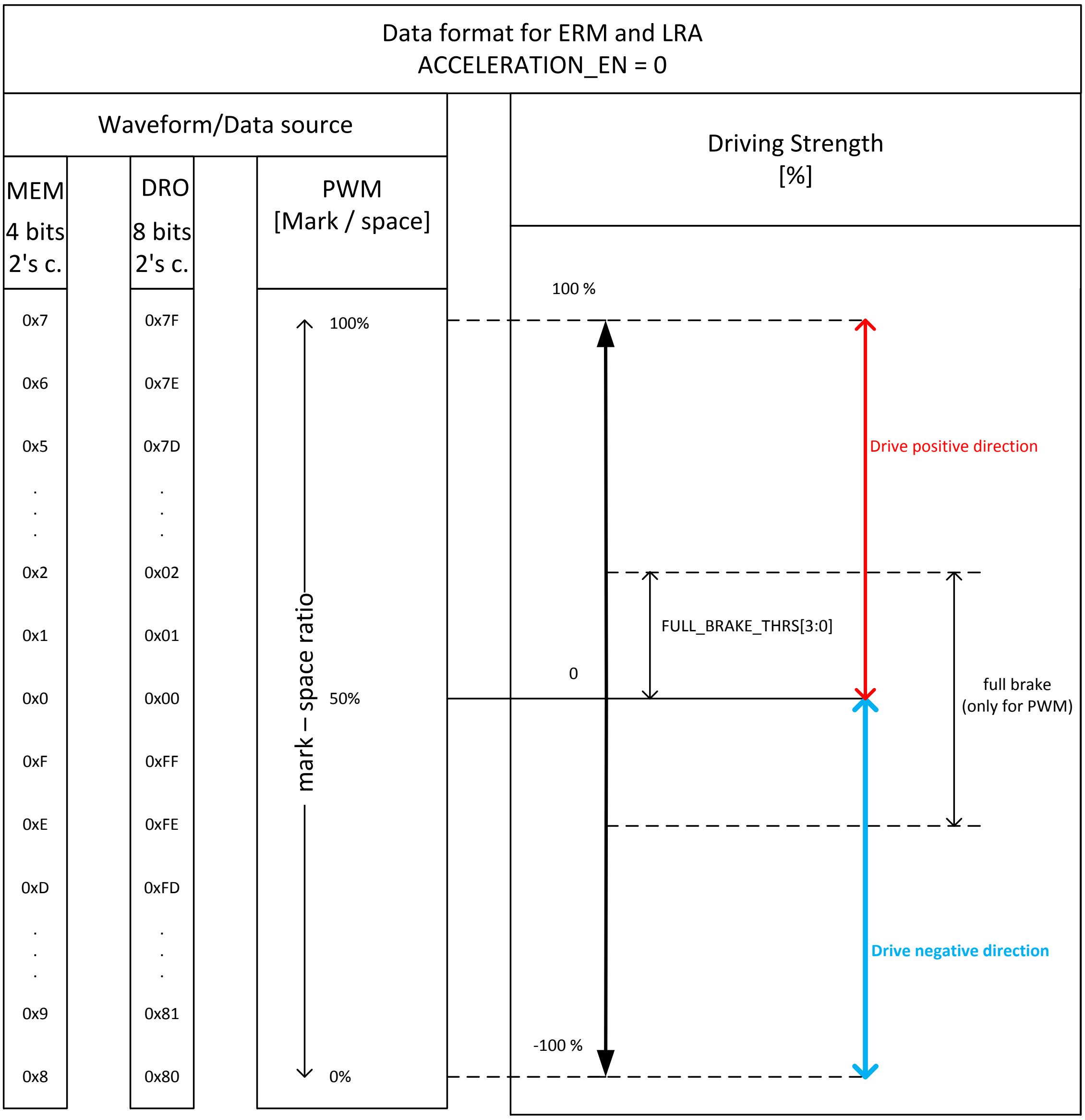


Figure 31: Overview of Data Formats with Acceleration Disabled

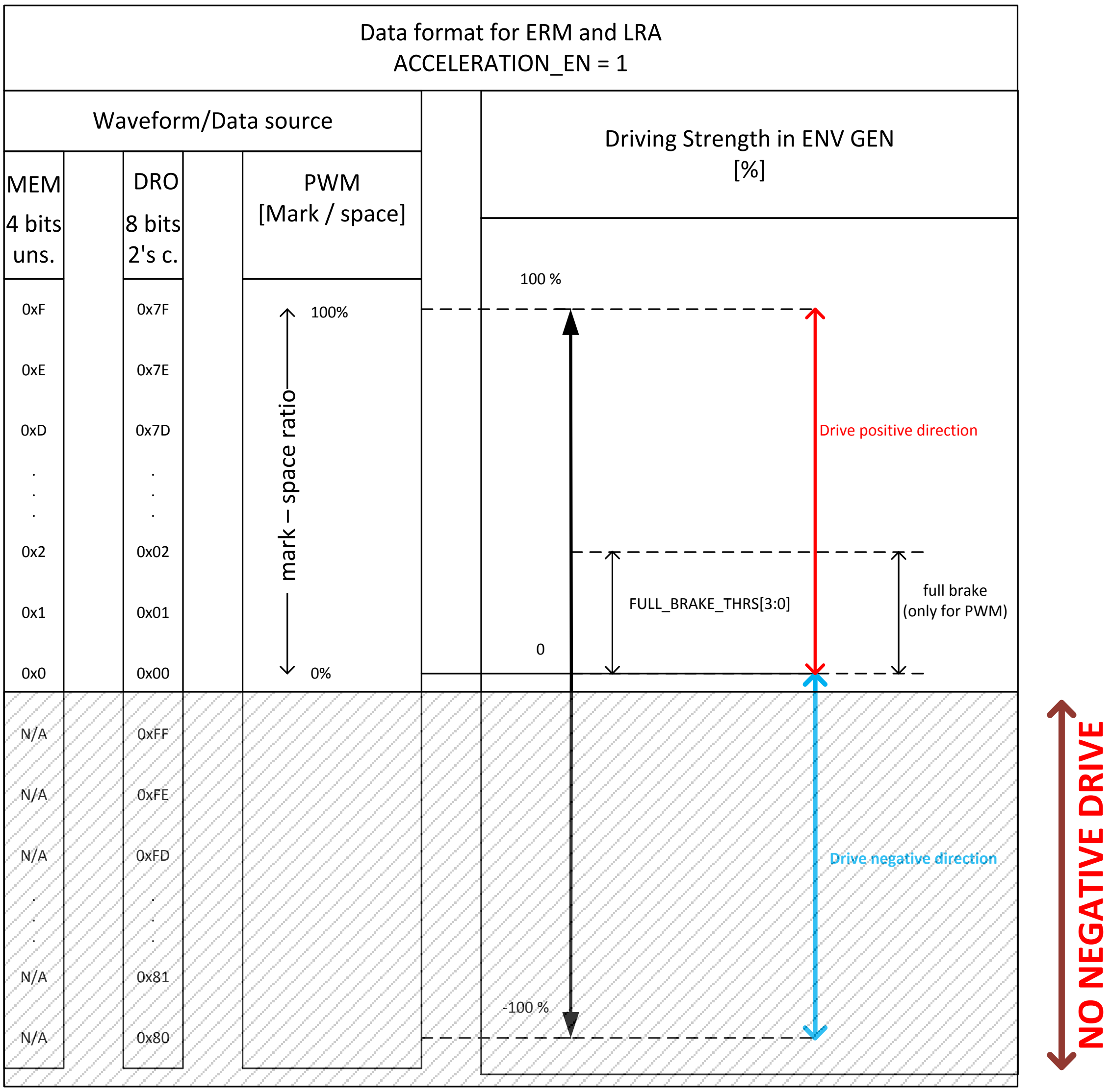


Figure 32: Overview of Data Formats with Acceleration Enabled

5.9.1 DRO Mode

DRO data is supplied from I²C and is interpreted as 8-bit two's complement signed number.

- For ACCELERATION_EN = 0:
  - The most negative value corresponds to -100 % driving strength.
  - The most positive value corresponds to +100 % driving strength.
  - A zero value corresponds to no drive.
- For ACCELERATION_EN = 1:
  - Negative values are omitted and substituted with zero.
  - The most positive value corresponds to +100 % driving strength.
  - Zero value corresponds to no drive.

5.9.2 PWM Mode

PWM provides mark / space ratio between 0 % and 100 %. The interpretation of duty cycle depends on the state of ACCELERATION_EN.

- For ACCELERATION_EN = 0:
  - A 0 % duty cycle corresponds to -100 % driving strength.
  - A 50 % duty cycle corresponds to no drive.
  - A 100 % duty cycle corresponds to +100 % driving strength.
  - FULL_BRAKE_THR defines a lower threshold for driving strength, below this threshold, drive is interpreted as zero.
- For ACCELERATION_EN = 1:
  - A 0 % duty cycle corresponds to no drive.
  - A 50 % duty cycle corresponds to +50 % driving strength.
  - A 100 % duty cycle corresponds to +100 % driving strength.
  - Negative drive is not possible.
  - FULL_BRAKE_THR defines a lower threshold for driving strength, below this threshold, drive is interpreted as zero.

The encoded value of PWM data is converted to 8-bit two's complement data using the DRO format and is written to OVERRIDE_VAL so it can be read back.

5.9.3 RTWM and ETWM Modes

- For ACCELERATION_EN = 0:
  - The 4 bits of the amplitude value are interpreted as a two's complement signed value.
  - The most negative value corresponds to -100 % driving strength.
  - The most positive value corresponds to +100 % driving strength.
  - A zero value corresponds to no drive.
- ACCELERATION_EN = 1
  - The 4 bits of the amplitude value are interpreted as an unsigned value.
  - The most positive value corresponds to +100 % driving strength.
  - Negative drive is not possible.
  - A zero value corresponds to no drive.

5.10 I²C Control Interface

DA7281 is software controlled from the host by registers accessed via an I²C compatible serial control interface. Data is shifted into or out of the DA7281 under the control of the host processor, which also provides the serial clock.

The DA7281 7-bit I²C default slave address is stored in register CIF_I2C2, bits IF_BASE_ADDR and has a value of 0x4A (1001010 binary), which is equivalent to 0x94 (8-bit) for writing and 0x95 (8-bit) for reading. However, the two LSBs of the slave address are directly controlled by the ADDR_1 and ADDR_0 pins. The control is dynamic, which means that any change of the ADDR_x pins during operation (VDD and VDDIO present) will result in the I²C base address changing to the new one presented by the ADDR_x combination. The relationship between ADDR_1 and ADDR_0 to the default base address is summarized in Table 20.

Table 20: Relationship between ADDR_x Pins and I²C Base and Effective Addresses

Default I²C Base Address (Stored in IF_BASE_ADDR) Hex / Binary	**ADDR_1**	**ADDR_0**	**Effective I²C Base Address Hex / Binary**
0x4A / 1001010	0 / GND	0 / GND	0x48 / 10010**00**
0x4A / 1001010	0 / GND	1 / VDDIO	0x49 / 10010**01**
0x4A / 1001010	1 / VDDIO	0 / GND	0x4A / 10010**10**
0x4A / 1001010	1 / VDDIO	1 / VDDIO	0x4B / 10010**11**

Up to four devices can be present in a system with a single I²C master by connecting the ADDR_x pins to VDDIO or GND, see Table 20. If more devices need to be instantiated, this could be done by modifying the base address register on some of them in the following procedure (GPI settings are for illustrative purposes, others can be used):

1. Power up VDD and VDDIO for all DA7281s present. Control ADDR_x pins on each device individually with separate GPIOs on the host side. Keep all ADDR_x pins connected to GND. Effective slave address for all devices is 0x48 (modified from the default 0x4A due to ADDR_0 and ADDR_1 being at GND).
2. On a single DA7281, change ADDR_0 and ADDR_1 to VDDIO and wait for 50 µs. This is now the only device with an effective I²C address of 0x4B.
3. Change that device IF_BASE_ADDR bits to 0x20 via an I²C write to device address 0x4B. The effective address is 0x23 (due to ADDR_0 and 1).
4. Repeat steps 2 to 3 as many times as need to activate all devices with unique I²C base addresses.

This procedure is shown in Figure 33:

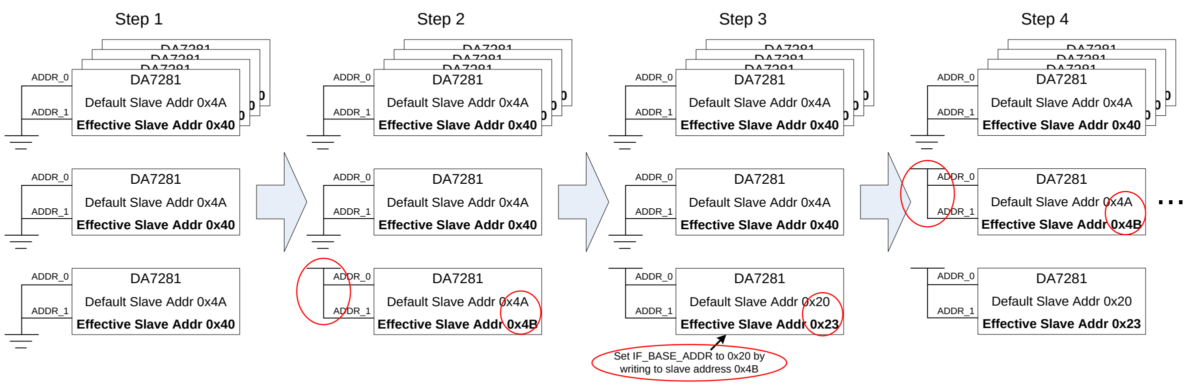


Figure 33: Instantiating More than Four DA7281s in the Same System

The I^2C clock is supplied by the SCL line and the bidirectional I^2C data is carried by the SDA line. The I^2C interface is open-drain supporting multiple devices on a single line. The bus lines have to be pulled HIGH by external pull-up resistors (1 kΩ to 20 kΩ range). The attached devices only drive the bus lines LOW by connecting them to ground. This means that two devices cannot conflict if they drive the bus simultaneously.

DA7281 supports Standard-mode, Fast-mode, and Fast-mode Plus, with the highest frequency of the bus at 1 MHz in Fast-mode Plus. The exact frequency can be determined by the application and does not have any relation to the DA7281 internal clock signals. DA7281 will follow the host clock speed within the described limitations and does not initiate any clock arbitration or slow-down.

Communication on the I^2C bus always takes place between two devices, one acting as the master and the other as the slave. The DA7281 will only operate as a slave.

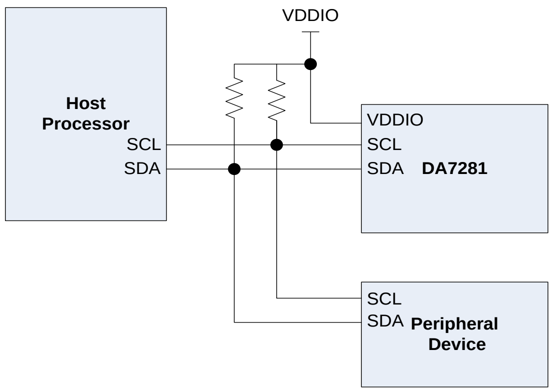


Figure 34: Schematic of the I^2C Control Interface Bus

All data is transmitted across the I^2C bus in groups of eight bits. To send a bit the SDA line is driven to the intended state while the SCL is LOW (a LOW on SCL indicates a zero bit). Once the SDA has settled, the SCL line is brought HIGH and then LOW. This pulse on SCL clocks the SDA bit into the receiver's shift register.

A two-byte serial protocol is used containing one byte for address and one byte for data. Data and address transfer is transmitted MSB first for both read and write operations. All transmission begins with the START condition from the master while the bus is in the Idle mode (the bus is free). It is initiated by a HIGH to LOW transition on the SDA line while the SCL is in the HIGH state (a STOP condition is indicated by a LOW to HIGH transition on the SDA line while the SCL line is in the HIGH state).

Figure 35: I^2C START and STOP Conditions

The I^2C bus is monitored by DA7281 for a valid slave address whenever the interface is enabled. It responds with an Acknowledge immediately when it receives its own slave address. The Acknowledge is done by pulling the SDA line LOW during the following clock cycle (white blocks marked with A in Figure 36 to Figure 40).

The protocol for a register write from master to slave consists of a START condition, a slave address with read/write bit and the 8-bit register address followed by 8 bits of data terminated by a STOP condition (DA7281 responds to all bytes with Acknowledge), see Figure 36.

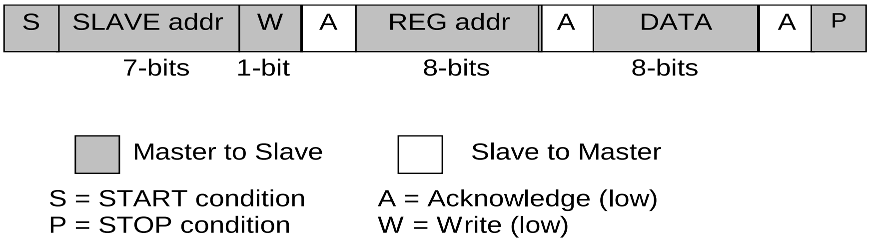


Figure 36: I²C Byte Write (SDA line)

When the host reads data from a register it first has to write access DA7281 with the target register address and then read access DA7281 with a repeated START, or alternatively a second START condition. After receiving the data the host sends a Not Acknowledge (NAK) and terminates the transmission with a STOP condition:

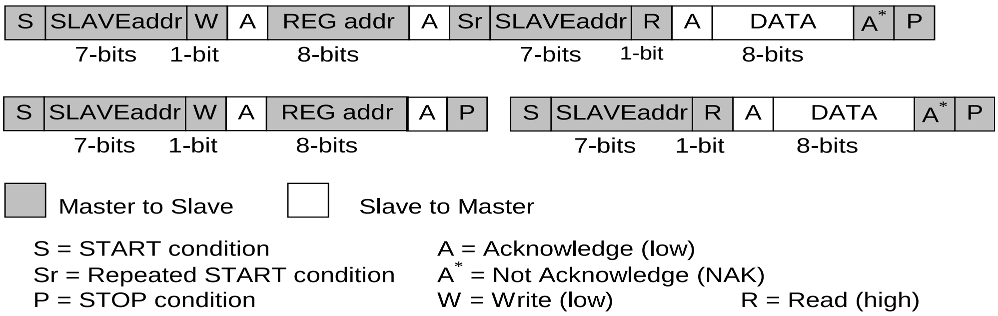


Figure 37: Examples of the I²C Byte Read (SDA line)

Consecutive (Page) Read-Out mode, I2C_WR_MODE (register CIF_I2C1) = 0, is initiated from the master by sending an Acknowledge instead of Not Acknowledge (NAK) after receipt of the data word. The I²C control block then increments the address pointer to the next I²C address and sends the data to the master. This enables an unlimited read of data bytes until the master sends an NAK directly after the receipt of data, followed by a subsequent STOP condition. If a non-existent I²C address is read out, the DA7281 will return code zero.

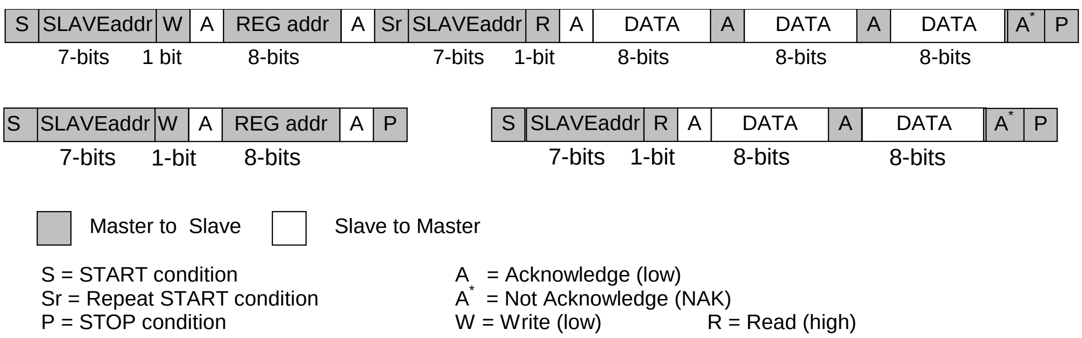


Figure 38: Examples of I2C Page Read (SDA line)

In Page mode the slave address after Sr (Repeated START condition) must be the same as the previous slave address.

Consecutive (Page) Write mode, I2C_WR_MODE = 0, is supported if the master sends several data bytes following a slave register address. The I²C control block then increments the address pointer to the next I²C address, stores the received data and sends an Acknowledge until the master sends the STOP condition.

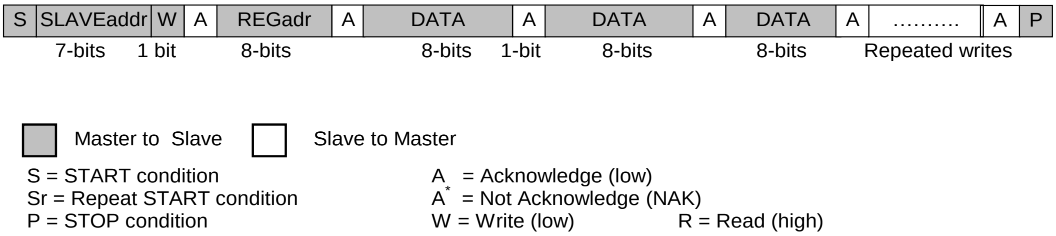


Figure 39: I²C Page Write (SDA line)

An alternative Repeated-Write mode that uses non-consecutive slave register addresses is available using the CIF_I2C1 register. In this Repeat Mode, I2C_WR_MODE = 1, the slave can be configured to support a host's repeated write operations into several non-consecutive registers. Data is stored at the previously received register address. If a new START or STOP condition occurs within a message, the bus returns to Idle mode. This is illustrated in Figure 40.

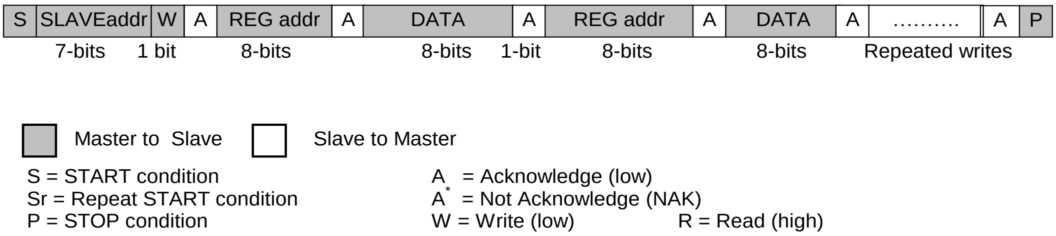


Figure 40: I²C Repeated Write (SDA line)

In Page mode, I2C_WR_MODE = 0, both Page mode reads and writes using auto-incremented addresses, and Repeat mode reads and writes using non auto-incremented addresses, are supported. In Repeat mode, I2C_WR_MODE = 1, however, only Repeat mode reads and writes are supported.

6 Register Overview

6.1 Register Map

Table 21: Register Map

Addr	Register	7	6	5	4	3	2	1	0	Reset
0x00	CHIP_REV	CHIP_REV_MINOR<3:0>			CHIP_REV_MAJOR<3:0>					0xAA
0x03	IRQ_EVENT1	E_OC_FAULT	E_ACTUATOR_FAULT	E_WARNING	E_SEQ_FAULT	E_OVERTEMP_CRIT	E_SEQ_DONE	E_UVLO	E_SEQ_CONTINUE	0x00
0x04	IRQ_EVENT_WARNING_DIAG	E_LIM_DRIVE	E_LIM_DRIVE_ACC	Reserved	E_MEM_TYPE	E_OVERTEMP_WARN	Reserved	Reserved	Reserved	0x00
0x05	IRQ_EVENT_SEQ_DIAG	E_SEQ_ID_FAULT	E_MEM_FAULT	E_PWM_FAULT	Reserved	Reserved	Reserved	Reserved	Reserved	0x00
0x06	IRQ_STATUS1	STA_OC	STA_ACTUATOR	STA_WARNING	STA_SEQ_FAULT	STA_OVERTEMP_CRIT	STA_SEQ_DONE	STA_UVLO_VBAT_OK	STA_SEQ_CONTINUE	0x00
0x07	IRQ_MASK1	OC_M	ACTUATOR_M	WARNING_M	SEQ_FAULT_M	OVERTEMP_CRIT_M	SEQ_DONE_M	E_UVLO_M	SEQ_CONTINUE_M	0x00
0x08	CIF_I2C1	I2C_WR_MODE	I2C_TO_ENABLE	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0x40
0x09	CIF_I2C2	Reserved	IF_BASE_ADDR<6:0>							0x4A
0x0A	FRQ_LRA_PER_H	LRA_PER_H<7:0>								0x25
0x0B	FRQ_LRA_PER_L	Reserved	LRA_PER_L<6:0>							0x66
0x0C	ACTUATOR1	ACTUATOR_NOMMAX<7:0>								0x56
0x0D	ACTUATOR2	ACTUATOR_ABSMAX<7:0>								0x6B
0x0E	ACTUATOR3	Reserved	Reserved	Reserved	IMAX<4:0>					0x0E
0x0F	CALIB_V2I_H	V2I_FACTOR_H<7:0>								0x00
0x10	CALIB_V2I_L	V2I_FACTOR_L<7:0>								0xF5
0x11	CALIB_IMP_H	IMPEDANCE_H<7:0>								0x58
0x12	CALIB_IMP_L	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	IMPEDANCE_L<1:0>		0x00
0x13	TOP_CFG1	EMBEDDED_MODE	Reserved	ACTUATOR_TYPE	BEMF_SENSE_EN	FREQ_TRACK_EN	ACCELERATION_EN	RAPID_STOP_EN	AMP_PID_EN	0x1E
0x14	TOP_CFG2	Reserved	Reserved	Reserved	MEM_DATA_SIGNED	FULL_BRAKE_THR<3:0>				0x01
0x15	TOP_CFG3	Reserved	Reserved	Reserved	Reserved	VDD_MARGIN<3:0>				0x03
0x16	TOP_CFG4	V2I_FACTOR_FREEZE	CALIB_IMPEDANCE_DIS	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0x40
0x17	TOP_INT_CFG1	FRQ_LOCKED_LIM<5:0>						BEMF_FAULT_LIM<1:0>		0x81
0x1C	TOP_INT_CFG6_H	FRQ_PID_Kp_H<7:0>								0x09
0x1D	TOP_INT_CFG6_L	FRQ_PID_Kp_L<7:0>								0x00
0x1E	TOP_INT_CFG7_H	FRQ_PID_Ki_H<7:0>								0x04
0x1F	TOP_INT_CFG7_L	FRQ_PID_Ki_L<7:0>								0xD0

Addr	Register	7	6	5	4	3	2	1	0	Reset
0x20	TOP_INT_CFG8	Reserved 0	RAPID_STOP_LIM<2:0>			FRQ_TRACK_BEMF_LIM<3:0>				0x53
0x22	TOP_CTL1	Reserved	Reserved	Reserved	SEQ_START	STANDBY_EN	OPERATION_MODE<2:0>			0x00
0x23	TOP_CTL2	OVERRIDE_VAL<7:0>								0x00
0x24	SEQ_CTL1	Reserved	Reserved	Reserved	Reserved	Reserved	FREQ_WAVEFORM_TIMEBASE	WAVEGEN_MODE	SEQ_CONTINUE	0x08
0x25	SWG_C1	CUSTOM_WAVE_GEN_COEFF1<7:0>								0x61
0x26	SWG_C2	CUSTOM_WAVE_GEN_COEFF2<7:0>								0xB4
0x27	SWG_C3	CUSTOM_WAVE_GEN_COEFF3<7:0>								0xEC
0x28	SEQ_CTL2	PS_SEQ_LOOP<3:0>				PS_SEQ_ID<3:0>				0x00
0x2B	GPI_CTL	Reserved	GPI_SEQUENCE_ID<3:0>				GPI_MODE	GPI_POLARITY<1:0>		0x10
0x2C	MEM_CTL1	WAV_MEM_BASE_ADDR <7:0>								0x00
0x2D	MEM_CTL2	WAV_MEM_LOCK	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0x80
0x2E	ADC_DATA_H1	ADC_VDD_H<7:0>								0xFF
0x2F	ADC_DATA_L1	Reserved	ADC_VDD_L<6:0>							0x7F
0x43	POLARITY	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	POLARITY	0x00
0x44	LRA_AVR_H	LRA_PER_AVERAGE_H<7:0>								0x00
0x45	LRA_AVR_L	Reserved	LRA_PER_AVERAGE_L<6:0>							0x00
0x46	FRQ_LRA_PER_ACT_H	LRA_PER_ACTUAL_H<7:0>								0x39
0x47	FRQ_LRA_PER_ACT_L	Reserved	LRA_PER_ACTUAL_L<6:0>							0x32
0x48	FRQ_PHASE_H	DELAY_H<7:0>								0x25
0x49	FRQ_PHASE_L	DELAY_FREEZE	Reserved	Reserved	Reserved	Reserved	DELAY_SHIFT_L<2:0>			0x05
0x4C	FRQ_CTL	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	FREQ_TRACKING_AUTO_ADJ	FREQ_TRACKING_FORCE_ON	0x02
0x5F	TRIM3	Reserved	LOOP_IDAC_DOUBLE_RANGE	LOOP_FILT_LOW_BW	REF_UVLO_THRES		Reserved	Reserved	Reserved	0x0C
0x60	TRIM4	Reserved	Reserved	Reserved	Reserved	LOOP_FILT_CAP_TRIM<1:0>		LOOP_FILT_RES_TRIM<1:0>		0x9C
0x62	TRIM6	Reserved	Reserved	Reserved	Reserved	HBRIDGE_ERC_LS_TRIM<1:0>		HBRIDGE_ERC_HS_TRIM<1:0>		0x5F
0x6E	TOP_CFG5	Reserved	Reserved	Reserved	Reserved	Reserved	DELAY_BYPASS	FRQ_PAUSE_ON_POLARITY_CHANGE	V2I_FACTOR_OFFSET_EN	0x01
0x81	IRQ_EVENT_ACTUATOR_FAULT	Reserved	E_TEST_ADC_SAT_FAULT	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0x00
0x82	IRQ_STATUS2	STA_ADC_SAT	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0x00
0x83	IRQ_MASK2	ADC_SAT_M	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0x00

Addr	Register	7	6	5	4	3	2	1	0	Reset
0x84 to 0xE7	SNP_MEM_x	SNP_MEM_x<7:0> where x = 0 to 99								0x00

6.2 Register Descriptions

Table 22: CHIP_REV (0x0000)

Bit	Mode	Symbol	Description	Reset
[7:4]	RO	CHIP_REV_MINOR	Device revision code (minor)	0xA
[3:0]	RO	CHIP_REV_MAJOR	Device revision code (major)	0xA

Table 23: IRQ_EVENT1 (0x0003)

Bit	Mode	Symbol	Description	Reset
[7]	RW	E_OC_FAULT	Over-current / short-circuit fault on the OUTP or OUTN pin (write 1 to clear)	0x0
[6]	RW	E_ACTUATOR_FAULT	Actuator fault, see Section 5.6.6 (write 1 to clear)	0x0
[5]	RW	E_WARNING	System warnings Read IRQ_EVENT_WARNING_DIAG for warning diagnostic (write 1 to clear)	0x0
[4]	RW	E_SEQ_FAULT	Sequence faults: SEQ_ID_FAULT, memory fault or PWM fault Read IRQ_EVENT_SEQ_DIAG for diagnostic information (write 1 to clear)	0x0
[3]	RW	E_OVERTEMP_CRIT	Critical chip temperature event, chip temperature has exceeded the critical limit of 125 °C (write 1 to clear)	0x0
[2]	RW	E_SEQ_DONE	IRQ indicating that sequence playback from waveform memory is complete (write 1 to clear)	0x0
[1]	RW	E_UVLO	Under-voltage fault, supply below the UVLO threshold Clear to attempt restart (write 1 to clear)	0x0
[0]	RW	E_SEQ_CONTINUE	IRQ indicating that playback of a new sequence has occurred because SEQ_CONTINUE is set to 1 (write 1 to clear)	0x0

Table 24: IRQ_EVENT_WARNING_DIAG (0x0004)

Bit	Mode	Symbol	Description	Reset
[7]	RW	E_LIM_DRIVE	IRQ indicating that playback is limited because the power supply level is lower than the sequence target (write 1 to E_WARNING to clear)	0x0
[6]	RW	E_LIM_DRIVE_ACC	IRQ indicating that acceleration is limited because the power supply level is lower than required for the acceleration target (write 1 to E_WARNING to clear)	0x0

Bit	Mode	Symbol	Description	Reset
[4]	RW	E_MEM_TYPE	Indicates that the memory data type configured in register MEM_DATA_SIGNED does not match the acceleration configuration (ACCELERATION_EN). MEM_DATA_SIGNED = 1 for ACCELERATION_EN = 0 MEM_DATA_SIGNED = 0 for ACCELERATION_EN = 1 (write 1 to E_WARNING to clear)	0x0
[3]	RW	E_OVERTEMP_WARN	Over-temperature warning, chip temperature has exceeded the warning limit of 105 °C (write 1 to E_WARNING to clear)	0x0

Table 25: IRQ_EVENT_SEQ_DIAG (0x0005)

Bit	Mode	Symbol	Description	Reset
[7]	RW	E_SEQ_ID_FAULT	IRQ indicating that requested sequence ID configured in PS_SEQ_ID is not valid (write 1 to E_SEQ_FAULTto clear)	0x0
[6]	RW	E_MEM_FAULT	Indicates that the Waveform Memory is corrupted (empty, invalid snippet ID, invalid frame structure) (write 1 to E_SEQ_FAULTto clear)	0x0
[5]	RW	E_PWM_FAULT	IRQ indicating that the PWM input signal has timed out (write 1 to E_SEQ_FAULTto clear)	0x0

Table 26: IRQ_STATUS1 (0x0006)

Bit	Mode	Symbol	Description	Reset
[7]	RO	STA_OC	Over-current / short circuit fault status	0x0
[6]	RO	STA_ACTUATOR	Actuator fault status	0x0
[5]	RO	STA_WARNING	System warnings status	0x0
[4]	RO	STA_PAT_FAULT	Sequence faults status	0x0
[3]	RO	STA_OVERTEMP_CRIT	Over-temperature status	0x0
[2]	RO	STA_PAT_DONE	Memory based sequence status	0x0
[1]	RO	STA_UVLO_VBAT_OK	UVLO output status: 0 during normal operation; 1 if there is a UVLO event	0x0
[0]	RO	STA_SEQ_CONTINUE	Continuous sequence status	0x0

Table 27: IRQ_MASK1 (0x0007)

Bit	Mode	Symbol	Description	Reset
[7]	RW	OC_M	Over-current / short circuit fault mask	0x0
[6]	RW	ACTUATOR_M	Actuator fault mask	0x0
[5]	RW	WARNING_M	System warnings mask	0x0
[4]	RW	SEQ_FAULT_M	Sequence faults mask	0x0
[3]	RW	OVERTEMP_CRIT_M	Over-temperature fault mask	0x0
[2]	RW	SEQ_DONE_M	Memory based sequence interrupt mask	0x0
[1]	RW	E_UVLO_M	Soft shutdown fault mask	0x0
[0]	RW	SEQ_CONTINUE_M	Continuous sequence interrupt mask	0x0

Table 28: CIF_I2C1 (0x0008)

Bit	Mode	Symbol	Description	Reset
[7]	RW	I2C_WR_MODE	I^2C write mode **0x0 = Auto-increment (addr, data, data, data,…)** 0x1 = Repeat (addr, data, addr, data,...)	0x0
[6]	RW	I2C_TO_ENABLE	I^2C timeout enable. If there are no negative edges on SCL for approx. 35 ms, the slave resets. 0x0 = Disabled **0x1 = Enabled**	0x1

Table 29: CIF_I2C2 (0x0009)

Bit	Mode	Symbol	Description	Reset
[6:0]	RW	I2C_BASE_ADDR	I^2C base address	0x4A

Table 30: FRQ_LRA_PER_H (0x000A)

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	LRA_PER_H	Used for specifying the LRA drive frequency. MS-bits of the initial LRA resonant frequency period. $LRA\_PER[14:0] = \frac{1}{LRA_{freq} \times 1333.32 \times 10^{-9}}$ $LRA\_PER\_H[7:0] = \frac{LRA\_PER[14:0] - LRA\_PER\_L[6:0]}{128}$ $LRA\_PER\_L[6:0] = LRA\_PER[14:0] - 128 \times LRA\_PER\_H[7:0]$ Where LRA_{freq} represents the LRA resonant frequency (in Hz) as listed in the actuator datasheet. See Section 5.6.2. **Default corresponds to 155 Hz.**	0x25

Table 31: FRQ_LRA_PER_L (0x000B)

Bit	Mode	Symbol	Description	Reset
[6:0]	RW	LRA_PER_L	Used for specifying the LRA drive frequency. LS-bits of the initial LRA resonant frequency period. $$LRA\_PER[14:0] = \frac{1}{LRA_{freq} \times 1333.32 \times 10^{-9}}$$ $$LRA\_PER\_H[7:0] = \frac{LRA\_PER[14:0] - LRA\_PER\_L[6:0]}{128}$$ $$LRA\_PER\_L[6:0] = LRA\_PER[14:0] - 128 \times LRA\_PER\_H[7:0]$$ Where LRA_{freq} represents the LRA resonant frequency in Hz as listed in the actuator datasheet. See Section 5.6.2. **Default corresponds to 155 Hz.**	0x66

Table 32: ACTUATOR1 (0x000C)

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	ACTUATOR_NOMMAX	Nominal actuator voltage rating, unsigned, see Section 5.6.2 Sets full-scale of unsigned haptic waveform when acceleration enabled (ACCELERATION_EN = 1) $$ACTUATOR\_NOMMAX = \frac{V_{actuator\_nommax}}{23.4 \times 10^{-3}}$$ **Default: 0x56 = 2.0 V**	0x56

Table 33: ACTUATOR2 (0x000D)

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	ACTUATOR_ABSMAX	Absolute actuator maximum voltage rating, see Section 5.6.2. Overdrive is limited to this value when acceleration enabled (ACCELERATION_EN = 1) Sets full-scale of unsigned haptic waveform when acceleration disabled $$ACTUATOR\_ABSMAX = \frac{V_{actuator\_absmax}}{23.4 \times 10^{-3}}$$ **Default: 0x6B = 2.5 V**	0x6B

Table 34: ACTUATOR3 (0x000E)

Bit	Mode	Symbol	Description	Reset
[4:0]	RW	IMAX	Actuator max current rating $$IMAX = \frac{I_{max\_actuator\_mA} - 28.6}{7.2}$$ where $I_{max\_actuator\_mA}$ is the actuator max rated current in mA, as listed in its datasheet, see Section 5.6.2. **Default: 0xE = 137 mA**	0xE

Table 35: CALIB_V2I_H (0x000F)

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	V2I_FACTOR_H	MS-bits for translating actuator impedance to output voltage drive level $$V2I\_FACTOR[15:0] = \frac{Z \times (IMAX[4:0] + 4)}{1.6104}$$ $$V2I\_FACTOR\_H[7:0] = \frac{V2I\_FACTOR[15:0] - V2I\_FACTOR\_L[7:0]}{256}$$ $$V2I\_FACTOR\_L[7:0] = V2I\_FACTOR[15:0] - 256 \times V2I\_FACTOR\_H[7:0]$$ Where V2I_FACTOR[15:0] is the 16-bit concatenation of V2I_FACTOR_H[7:0] and V2I_FACTOR_L[7:0], Z is the impedance of the actuator in Ω (as read from its datasheet), and IMAX[4:0] is the 5-bit value of IMAX, see Section 5.6.2.	0x0

Table 36: CALIB_V2I_L (0x0010)

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	V2I_FACTOR_L	LS-bits for translating actuator impedance to output voltage drive level $$V2I\_FACTOR[15:0] = \frac{Z \times (IMAX[4:0] + 4)}{1.6104}$$ $$V2I\_FACTOR\_H[7:0] = \frac{V2I\_FACTOR[15:0] - V2I\_FACTOR\_L[7:0]}{256}$$ $$V2I\_FACTOR\_L[7:0] = V2I\_FACTOR[15:0] - 256 \times V2I\_FACTOR\_H[7:0]$$ Where V2I_FACTOR[15:0] is the 16-bit concatenation of V2I_FACTOR_H[7:0] and V2I_FACTOR_L[7:0], Z is the impedance of the actuator in Ω (as read from its datasheet), and IMAX[4:0] is the 5-bit value of IMAX, see Section 5.6.2.	0xF5

Table 37: CALIB_IMP_H (0x0011)

Bit	Mode	Symbol	Description	Reset
[7:0]	RO	IMPEDANCE_H	MS-bits of calculated impedance (**default 22 Ω**), see Section 5.7.3. $$Impedance\ (\Omega) = 4 \times 62.5 \times 10^{-3} \times IMPEDANCE\_H + 62.5 \times 10^{-3} \times IMPEDANCE\_L$$	0x58

Table 38: CALIB_IMP_L (0x0012)

Bit	Mode	Symbol	Description	Reset
[1:0]	RO	IMPEDANCE_L	LS-bits of calculated impedance (**default 22 Ω**), see Section 5.7.3. $Impedance\ (\Omega) = 4 \times 62.5 \times 10^{-3} \times IMPEDANCE\_H + 62.5 \times 10^{-3} \times IMPEDANCE\_L$	0x0

Table 39: TOP_CFG1 (0x0013)

Bit	Mode	Symbol	Description	Reset
[7]	RW	EMBEDDED_MODE	Embedded operation enable (self-clearing IRQs), see Section 5.7.7. **0x0 = Faults cleared by host** 0x1 = DA7281 clears faults automatically	0x0
[5]	RW	ACTUATOR_TYPE	Specifies actuator type: LRA or ERM, see Section 5.6.2. **0x0 = LRA** 0x1 = ERM	0x0
[4]	RW	BEMF_SENSE_EN	Enable internal loop computations; should be disabled only in custom waveform and wideband operation, see Sections 5.7.5 and 5.7.6. 0x0 = Custom Waveform Operation **0x1 = Standard Operation**	0x1
[3]	RW	FREQ_TRACK_EN	Enable resonant frequency tracking; ignored in ERM mode, see Section 5.3. 0x0 = frequency tracking disabled **0x1 = frequency tracking enabled**	0x1
[2]	RW	ACCELERATION_EN	Enable Active Acceleration, see Section 5.4. 0x0 = Active Acceleration disabled **0x1 = Active Acceleration enabled**	0x1
[1]	RW	RAPID_STOP_EN	Enable Rapid Stop, see Section 5.4. 0x0 = Rapid Stop disabled **0x1 = Rapid Stop enabled**	0x1
[0]	RW	AMP_PID_EN	Enable Amplitude PID, see Section 5.4. **0x0 = Amplitude PID disabled** 0x1 = Amplitude PID enabled	0x0

Table 40: TOP_CFG2 (0x0014)

Bit	Mode	Symbol	Description	Reset
[4]	RW	MEM_DATA_SIGNED	Memory data format; set according to the value of ACCELERATION_EN: **0x0 = unsigned (for ACCELERATION_EN = 1)** 0x1 = signed (for ACCELERATION_EN = 0)	0x0

Bit	Mode	Symbol	Description	Reset
[3:0]	RW	FULL_BRAKE_THR	Full-brake threshold for PWM mode with step size 6.66%, see Section 5.2.5. 0x0 = brake threshold disabled **0x1 = 6.66 % of ACTUATOR_NOMMAX** 0x2 = 13.33 % of ACTUATOR_NOMMAX ... …~6.66% steps… 0x15 = 100 % of ACTUATOR_NOMMAX	0x1

Table 41: TOP_CFG3 (0x0015)

Bit	Mode	Symbol	Description	Reset
[3:0]	RW	VDD_MARGIN	V_{DD} margin setting. Target voltage needs to be below V_{DD} - VDD_MARGIN, otherwise voltage is clamped to V_{DD} - VDD_MARGIN and a LIM_DRIVE IRQ is generated. See Section 5.7.13 for further details. 0x0 = 0 mV 0x1 = 187.5 mV 0x2 = 375 mV **0x3 = 562.5 mV** ... …187.5 mV steps… 0xF = 2.8125 V	0x3

Table 42: TOP_CFG4 (0x0016)

Bit	Mode	Symbol	Description	Reset
[7]	RW	V2I_FACTOR_FREEZE	Stop automatic updates to V2I_FACTOR_x, see Section 5.7.3. **0x0 = updates enabled** 0x1 = updates disabled	0x0
[6]	RW	CALIB_IMPEDANCE_DIS	Stop automatic updates to V2I_FACTOR_x during playback, see Section 5.7.3. 0x0 = updates enabled **0x1 = updates disabled**	0x1

Table 43: TOP_INT_CFG1 (0x0017)

Bit	Mode	Symbol	Description	Reset
[7:2]	RW	FRQ_LOCKED_LIM	Limit for generating frequency locked signal that enabled scaling of the frequency tracking PID gain, see Section 5.7.1. If error is below the FRQ_LOCKED_LIM*4 frequency is locked	0x20
[1:0]	RW	BEMF_FAULT_LIM	Limit for BEMF fault generation. If voltage is below the threshold BEMF, a fault is generated, see Section 5.7.14. 0x0 = BEMF fault disabled **0x1 = 4.9 mV** 0x2 = 27.9 mV 0x3 = 49.9 mV	0x1

Table 44: TOP_INT_CFG6_H (0x001C)

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	FRQ_PID_Kp_H	MS-bits of the frequency tracking loop PID Kp proportional coefficient, see Section 5.7.1 for details	0x9

Table 45: TOP_INT_CFG6_L (0x001D)

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	FRQ_PID_Kp_L	LS-bits of the frequency tracking loop PID Kp proportional coefficient, see Section 5.7.1 for details	0x0

Table 46: TOP_INT_CFG7_H (0x001E)

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	FRQ_PID_Ki_H	MS-bits of the frequency tracking loop PID Ki integral coefficient, see Section 5.7.1 for details	0x4

Table 47: TOP_INT_CFG7_L (0x001F)

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	FRQ_PID_Ki_L	LS-bits of the frequency tracking loop PID Ki integral coefficient, see Section 5.7.1 for details	0xD0

Table 48: TOP_INT_CFG8 (0x0020)

Bit	Mode	Symbol	Description	Reset
[6:4]	RW	RAPID_STOP_LIM	Selects the Rapid Stop threshold at which DA7281 stops driving while braking, see Section 5.7.2	0x5
[3:0]	RW	FRQ_TRACK_BEMF_LIM	Selects the frequency tracking threshold at which DA7281 pauses frequency tracking, see Section 5.7.1	0x3

Table 49: TOP_CTL1 (0x0022)

Bit	Mode	Symbol	Description	Reset
[4]	RW	SEQ_START	Start/stop control of Waveform Memory sequence playback **0x0 = Stop playback and return to IDLE state** 0x1 = Start playback	0x0
[3]	RW	STANDBY_EN	Sets the state DA7281 returns to after completion of playback, see Section 5.2.1. **0x0 = Return to IDLE state after playback** 0x1 = Return to STANDBY state after playback	0x0
[2:0]	RW	OPERATION_MODE	Haptic operation mode, see Section 5.2. **0x0 = Inactive mode** 0x1 = Direct register override (DRO) mode 0x2 = Playback from PWM data source (PWM) mode 0x3 = Register triggered waveform memory (RTWM) mode 0x4 = Edge triggered waveform memory (ETWM) mode	0x0

Table 50: TOP_CTL2 (0x0023)

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	OVERRIDE_VAL	Used to set the output drive level in DRO mode. Scales the contents of ACTUATOR_ABSMAX and/or ACTUATOR_NOMMAX, depending on whether Active Acceleration is enabled. See Section 5.2.4.	0x0

OVERRIDE_VAL Value	Scaling factor when ACCELERATION_EN = 0	Scaling factor when ACCELERATION_EN = 1
0x7F	1	1
0x7E	0.992	0.992
...	…step of 0.008…	…step of 0.008…
0x01	0.0079	0.0079
0x00	0	0
0xFF	-0.0079	0
...	…step of 0.008…	…step of 0.008…
0x81	-1	0
0x80	-1	0

Table 51: SEQ_CTL1 (0x0024)

Bit	Mode	Symbol	Description	Reset
[2]	RW	FREQ_WAVEFORM_TIMEBASE	Frequency waveform timebase setting for waveform memory frames. See Section 5.8.3. **0x0 5.44, 21.76, 43.52, 87.04 ms** 0x1 1.36, 5.44, 21.76, 43.52 ms	0x0
[1]	RW	WAVEGEN_MODE	Enable bit for custom waveform operation, see Section 5.7.5. ● If WAVEGEN_MODE = 0, then set BEMF_SENSE_EN = 1 ● If WAVEGEN_MODE = 1,then set BEMF_SENSE_EN = 0 **0x0 = Normal wave mode (step/ramp sequences)** 0x1 = Custom wave mode (sinewave sequences)	0x0
[0]	RW	SEQ_CONTINUE	Control for back-to-back Waveform Memory sequence playback during RTWM and ETWM modes. If SEQ_CONTINUE = 1, new sequence playback starts at end of current sequence. Register is self-cleared when the next sequence is started, see Section 5.6.5.	0x0

Table 52: SWG_C1 (0x0025)

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	CUSTOM_WAVE_GEN_COEFF1	Coefficient1 for custom wave generation, represents a proportion of the set IMAX, see Section 5.7.5. Default corresponds to a sine wave. 0x00 = 0 % 0x01 = 0.4 % … …steps of approx. 0.4 % **0x61 = 37.9 %** ... …steps of approx. 0.4 % 0xFF = 100 %	0x61

Table 53: SWG_C2 (0x0026)

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	CUSTOM_WAVE_GEN_COEFF2	Coefficient2 for custom wave generation, represents a proportion of the set IMAX, see Section 5.7.5. Default corresponds to a sine wave. 0x00 = 0 % 0x01 = 0.4 % … …steps of approx. 0.4 % **0xB4 = 70.3 %** ... …steps of approx. 0.4 % 0xFF = 100 %	0xB4

Table 54: SWG_C3 (0x0027)

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	CUSTOM_WAVE_GEN_COEFF3	Coefficient1 for custom wave generation, represents a proportion of the set IMAX, see Section 5.7.5. Default corresponds to a sine wave. 0x00 = 0 % 0x01 = 0.4 % … …steps of approx. 0.4 % **0xEC = 92.2 %** ... …steps of approx. 0.4 % 0xFF = 100 %	0xEC

Table 55: SEQ_CTL2 (0x0028)

Bit	Mode	Symbol	Description	Reset
[7:4]	RW	PS_SEQ_LOOP	Number of times the pre-stored sequence (pointed to by PS_SEQ_ID) is repeated, see Section 5.6.5. **0x0 = No repetition (sequence played once)** 0x1 = 1 repetition (sequence played twice) … …step of 1… 0xF = 15 repetitions (sequence played 16 times)	0x0
[3:0]	RW	PS_SEQ_ID	ID of pre-stored and read-back of GPI triggered sequence, see Section 5.6.5.4.	0x0

Table 56: GPI_CTL (0x002B)

Bit	Mode	Symbol	Description	Reset
[6:3]	RW	GPI_SEQUENCE_ID	GPI mode of operation, see Section 5.2.7.	0x2
[2]	RW	GPI_MODE	GPI mode of operation, see Section 5.2.7. **0x0 = Single sequence** 0x1 = Multi-sequence	0x0
[1:0]	RW	GPI_POLARITY	Selection which GPI edge triggers an event: **0x0 = Rising edge** 0x1 = Falling edge 0x2 = Both edges	0x0

Table 57: MEM_CTL1 (0x002C)

Bit	Mode	Symbol	Description	Reset
[7:0]	RO	WAV_MEM_BASE_ADDR	Snippet memory start address, see Section 5.8.	0x0

Table 58: MEM_CTL2 (0x002D)

Bit	Mode	Symbol	Description	Reset
[7]	RW	WAV_MEM_LOCK	Lock bit for preventing access to Waveform Memory, see Section 5.6.4. 0x0 = Locked **0x1 = Unlocked**	0x1

Table 59: ADC_DATA_H1 (0x002E)

Bit	Mode	Symbol	Description	Reset
[7:0]	RO	ADC_VDD_H	Unsigned VDD measurement, see Section 5.7.13 $VDD\ Supply\ Voltage = (ADC\_VDD\_H \times 128 + ADC\_VDD\_L) \times 0.1831 mV$	0xFF

Table 60: ADC_DATA_L1 (0x002F)

Bit	Mode	Symbol	Description	Reset
[6:0]	RO	ADC_VDD_L	Unsigned VDD measurement, see Section 5.7.13 $VDD\ Supply\ Voltage = (ADC\_VDD\_H \times 128 + ADC\_VDD\_L) \times 0.1831 mV$	0x7F

Table 61: POLARITY (0x0043)

Bit	Mode	Symbol	Description	Reset
[0]	RO	POLARITY	Current polarity read-back, see Section 5.7.8	0x0

Table 62: LRA_AVR_H (0x0044)

Bit	Mode	Symbol	Description	Reset
[7:0]	RO	LRA_PER_AVERAGE_H	MS-bits of the average LRA resonant period based on the last four half-periods, see Section 5.7.1. The following formula describes the output: $LRA\ period\ (ms) = 1333.32 \times 10^{-9} \times (128 \times LRA\_PER\_AVERAGE\_H + LRA\_PER\_AVERAGE\_L)$	0x0

Table 63: LRA_AVR_L (0x0045)

Bit	Mode	Symbol	Description	Reset
[6:0]	RO	LRA_PER_AVERAGE_L	LS-bits of the average LRA resonant period based on the last four half-periods, see Section 5.7.1. The following formula describes the output: $LRA\ period\ (ms) = 1333.32 \times 10^{-9} \times (128 \times LRA\_PER\_AVERAGE\_H + LRA\_PER\_AVERAGE\_L)$	0x0

Table 64: FRQ_LRA_PER_ACT_H (0x0046)

Bit	Mode	Symbol	Description	Reset
[7:0]	RO	LRA_PER_ACTUAL_H	MS-bits of the actual LRA resonant period based on half-period, see Section 5.5.The following formula describes the output: $LRA\ period\ (ms) = 1333.32 \times 10^{-9} \times (128 \times LRA\_PER\_ACTUAL\_H + LRA\_PER\_ACTUAL\_L)$	0x39

Table 65: FRQ_LRA_PER_ACT_L (0x0047)

Bit	Mode	Symbol	Description	Reset
[6:0]	RO	LRA_PER_ACTUAL_L	LSBs of the actual LRA resonant period based on half-period, see Section 5.5.The following formula describes the output: $LRA\ period\ (ms) = 1333.32 \times 10^{-9} \times (128 \times LRA\_PER\_ACTUAL\_H + LRA\_PER\_ACTUAL\_L)$	0x32

Table 66: FRQ_PHASE_H (0x0048)

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	DELAY_H	Used during custom waveform operation, see Section 5.7.5. Only use the following settings, all other settings are reserved: 0x0 = Setting for wideband mode **0x25 = Setting for closed-loop frequency tracking mode**	0x25

Table 67: FRQ_PHASE_L (0x0049)

Bit	Mode	Symbol	Description	Reset
[7]	RW	DELAY_FREEZE	Used during custom waveform operation. Set to 1 only in wideband mode with frequency tracking disabled, see Section 5.7.5 **0x0 = Setting for closed-loop frequency tracking mode** 0x1 = Setting for wideband mode	0x0

Bit	Mode	Symbol	Description	Reset
[2:0]	RW	DELAY_SHIFT_L	Used during custom waveform operation, see Section 5.7.5. Only use the following settings, all other settings are reserved: 0x0 = Setting for wideband mode **0x5 = Setting for closed-loop frequency tracking mode**	0x5

Table 68: FRQ_CTL (0x004C)

Bit	Mode	Symbol	Description	Reset
[1]	RW	FREQ_TRACKING_AUTO_ADJ	Enables the auto-scaling of the frequency tracking proportional coefficient, see Section 5.7.1. 0x0 = No auto-scaling **0x1 = Auto-scaling**	0x1
[0]	RW	FREQ_TRACKING_FORCE_ON	Force the tracking on when the error exceeds 25 % of initial guess, see Section 5.7.1. **0x0 = Off** 0x1 = On	0x0

Table 69: TRIM3 (0x005F)

Bit	Mode	Symbol	Description	Reset
[6]	RW	LOOP_IDAC_DOUBLE_RANGE	Loop IDAC double range control, see Section 5.7.12	0x0
[5]	RW	LOOP_FILT_LOW_BW	Loop filter low bandwidth, see Section 5.7.9	0x0
[4:3]	RW	REF_UVLO_THRES	UVLO threshold, see Section 5.7.10 00 = 2.7 V **01 = 2.8 V** 10 = 2.9 V 11 = 3.0 V	0x1

Table 70: TRIM4 (0x0060)

Bit	Mode	Symbol	Description	Reset
[3:2]	RW	LOOP_FILT_CAP_TRIM	Loop capacitor trim, see Section 5.7.9	0x3
[1:0]	RW	LOOP_FILT_RES_TRIM	Loop resistance trim, see Section 5.7.9	0x0

Table 71: TRIM6 0x(0062)

Bit	Mode	Symbol	Description	Reset
[3:2]	RW	HBRIDGE_ERC_LS_TRIM	Low side edge rate control setting, see Section 5.7.11. 00 = 25 mV/ns 01 = 50 mV/ns 10 = 75 mV/ns **11 = 100 mV/ns**	0x3

Bit	Mode	Symbol	Description	Reset
[1:0]	RW	HBRIDGE_ERC_HS_TRIM	High side edge rate control setting, see Section 5.7.11 00 = 25 mV/ns 01 = 50 mV/ns 10 = 75 mV/ns **11 = 100 mV/ns**	0x3

Table 72: D2602_TOP_CFG5 (0x006E)

Bit	Mode	Symbol	Description	Reset
[2]	RW	DELAY_BYPASS	Delay comparator bypass enable	0x0
[1]	RW	FRQ_PAUSE_ON_POLARITY_CHANGE	Pause the frequency update when the drive polarity changes (during rapid stop, negative accelaration, negative DRO value) **0x0 = Pause disabled** 0x1 = Pause enabled	0x0
[0]	RW	V2I_FACTOR_OFFSET_EN	Apply a 50 mV offset to the V2I factor calculation 0x0 = No offset applied **0x1 = 50 mV offset applied**	0x1

Table 73: IRQ_EVENT_ACTUATOR_FAULT (0x0081)

Bit	Mode	Symbol	Description	Reset
[2]	RO	ADC_SAT_FAULT	ADC produced saturated result, which is not expected to happen (write 1 to E_ACTUATOR to clear)	0x0

Table 74: IRQ_STATUS2 (0x0082)

Bit	Mode	Symbol	Description	Reset
[7]	RO	STA_ADC_SAT	Status of ADC saturation fault: ADC_SAT_FAULT	0x0

Table 75: IRQ_MASK2 (0x0083)

Bit	Mode	Symbol	Description	Reset
[7]	RW	ADC_SAT_M	Masking for ADC saturation fault: ADC_SAT_FAULT	0x0

Register SNP_MEM_xx

Table 76 shows the first, intermediary, and last snippet memory registers.

- The snippet register addresses increment by 1 for each snippet.
- The Bit ([7:0]), Mode (RW), and Reset (0x0) are identical for each snippet register.
- For further details on the Waveform Memory, see Section 5.8.

Table 76: SNP_MEM_xx (0x0084 to 0x00E7)

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	SNP_MEM_00	Snippet memory byte 0	0x0
[7:0]	RW	SNP_MEM_xx	Snippet memory byte x	0x0
[7:0]	RW	SNP_MEM_99	Snippet memory byte 99	0x0

7 Package Information

7.1 WLCSP Package Outline

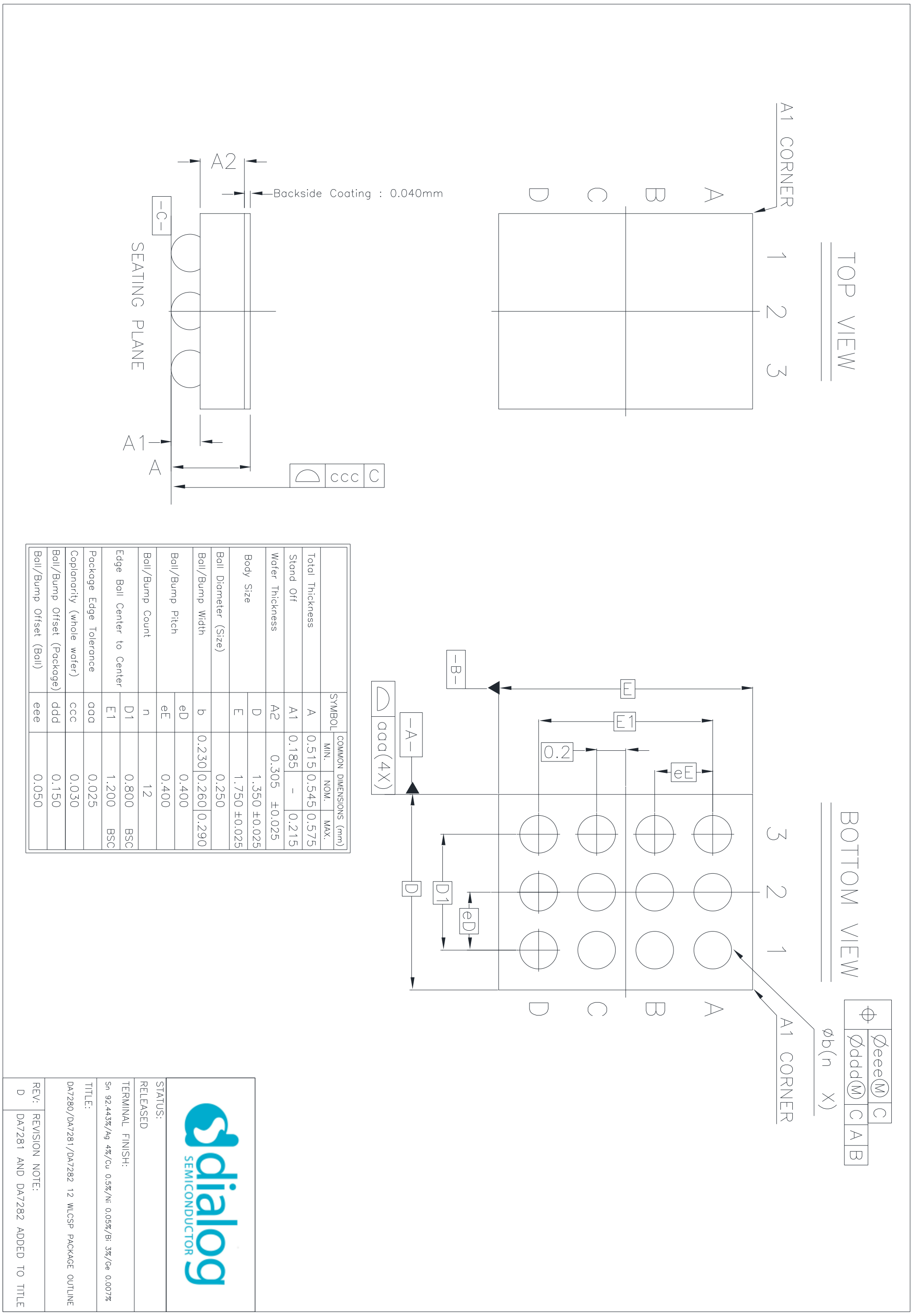
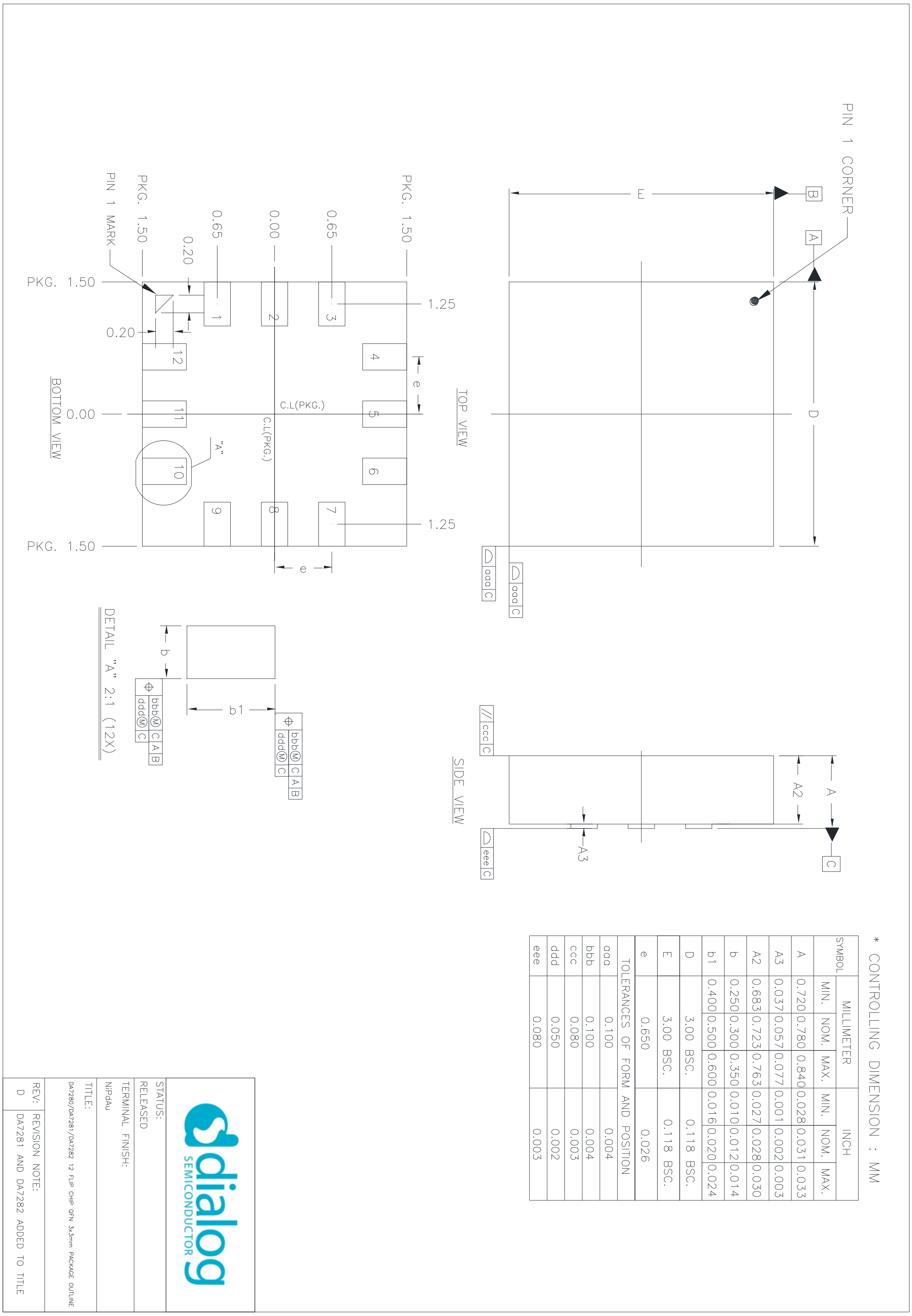


Figure 41: WLCSP Package Outline Drawing

7.2 QFN Package Outline



SYMBOL	MILLIMETER MIN.	MILLIMETER NOM.	MILLIMETER MAX.	INCH MIN.	INCH NOM.	INCH MAX.
A	0.720	0.780	0.840	0.028	0.031	0.033
A3	0.037	0.057	0.077	0.001	0.002	0.003
A2	0.683	0.723	0.763	0.027	0.028	0.030
b	0.250	0.300	0.350	0.010	0.012	0.014
b1	0.400	0.500	0.600	0.016	0.020	0.024
D		3.00 BSC.			0.118 BSC.	
E		3.00 BSC.			0.118 BSC.	
e		0.650			0.026	
TOLERANCES OF FORM AND POSITION						
aaa		0.100			0.004	
bbb		0.100			0.004	
ccc		0.080			0.003	
ddd		0.050			0.002	
eee		0.080			0.003	

* CONTROLLING DIMENSION : MM

Figure 42: QFN Package Outline Drawing

7.3 Moisture Sensitivity Level

The Moisture Sensitivity Level (MSL) is an indicator for the maximum allowable time period (floor lifetime) in which a moisture sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a specified maximum temperature and a maximum relative humidity before the solder reflow process. The MSL classification is defined in Table 77.

For detailed information on MSL levels refer to the IPC/JEDEC standard J-STD-020, which can be downloaded from http://www.jedec.org.

The WLCSP package is qualified for MSL 1.

Table 77: MSL Classification

MSL Level	Floor Lifetime	Conditions
MSL 4	72 hours	30 °C / 60 % RH
MSL 3	168 hours	30 °C / 60 % RH
MSL 2A	4 weeks	30 °C / 60 % RH
MSL 2	1 year	30 °C / 60 % RH
MSL 1	Unlimited	30 °C / 85 % RH

7.4 WLCSP Handling

Manual handling of WLCSP packages should be reduced to the absolute minimum. In cases where it is still necessary, a vacuum pick-up tool should be used. In extreme cases plastic tweezers could be used, but metal tweezers are not acceptable, since contact may easily damage the silicon chip.

Removal of a WLCSP package will cause damage to the solder balls. Therefore a removed sample cannot be reused.

WLCSP packages are sensitive to visible and infrared light. Precautions should be taken to properly shield the chip in the final product.

7.5 Soldering Information

Refer to the IPC/JEDEC standard J-STD-020 for relevant soldering information. This document can be downloaded from http://www.jedec.org.

8 Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, please consult Dialog Semiconductor's customer support portal or your local sales representative.

Table 78: Ordering Information

Part Number	Package	Size (mm)	Shipment Form	Pack Quantity
DA7281-00V42	WLCSP	1.35 x 1.75	Tape and reel	4500
DA7281-00V4C	WLCSP	1.35 x 1.75	Tape and reel	250
DA7281-00FV2	QFN	3.0 x 3.0	Tape and reel	6000
DA7281-00FVC	QFN	3.0 x 3.0	Tape and reel	250

9 Application Information

The Dialog GUI enables easy access to the device and can be used to accelerate product development time. For further information, contact your Dialog Semiconductor representative.

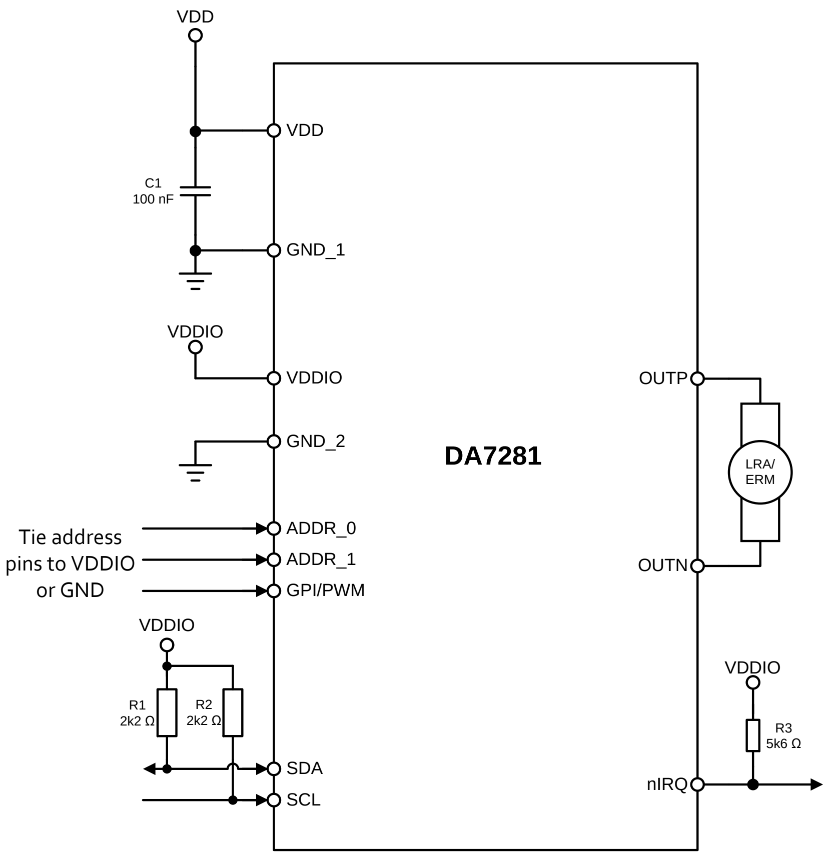


Figure 43: External Components Diagram

10 Layout Guidelines

For optimal layout, place the 100 nF capacitor as close to VDD and GND_1 pins as possible. It is also advisable to use solid a ground plane under the device.

The QFN can be routed out on a single layer. It is recommended to connect GND_1 and GND_2 to a local ground plane on the top layer with a low-impedance via connection to the main ground plane, see Figure 45.

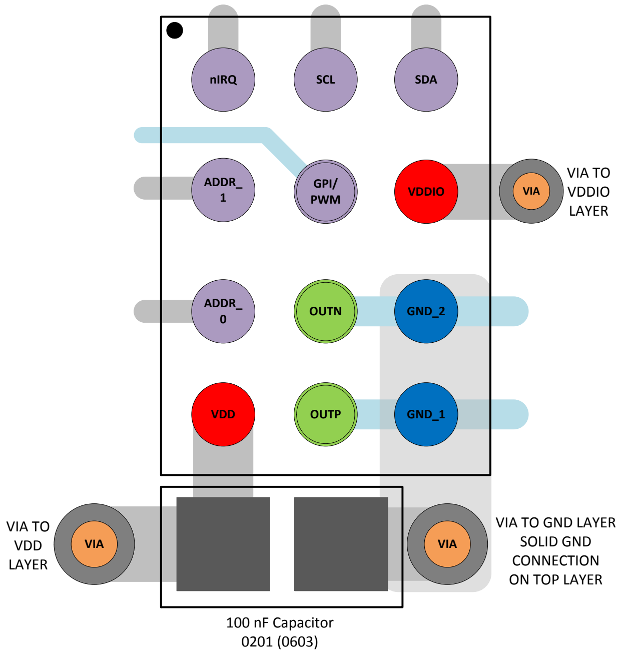


Figure 44: WLCSP Example PCB Layout

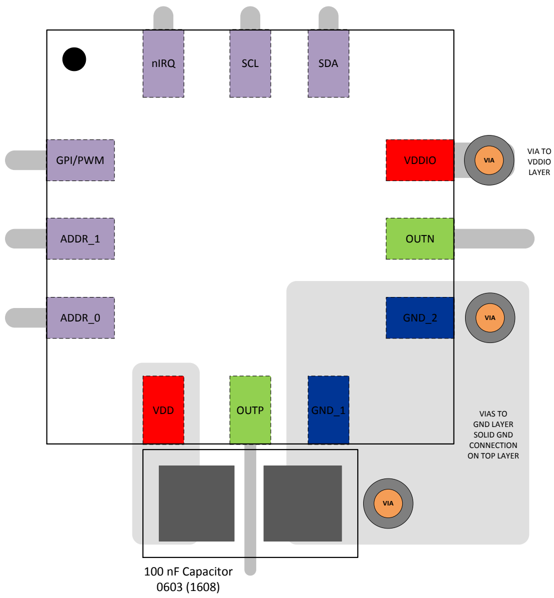


Figure 45: QFN Example PCB Layout

Status Definitions

Revision	Datasheet Status	Product Status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may be changed in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
3.<n>	Final	Production	This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Major specification changes are communicated via Customer Product Notifications. Datasheet changes are communicated via www.dialog-semiconductor.com.
4.<n>	Obsolete	Archived	This datasheet contains the specifications for discontinued products. The information is provided for reference only.

Disclaimer

RoHS Compliance

Dialog Semiconductor's suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request.

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