

## SNx4HCT14 Hex Schmitt-Trigger Inverters

### 1 Features

- Operating Voltage Range of 4.5 V to 5.5 V
- Outputs Can Drive Up to 10 LSTTL Loads
- Low Power Consumption: 20- $\mu$ A Maximum  $I_{CC}$
- Typical  $t_{pd} = 18$  ns
- $\pm 4$ -mA Output Drive at 5 V
- Maximum Low Input Current of 1  $\mu$ A Maximum
- Inputs Are TTL-Voltage Compatible

### 2 Applications

- UPS
- White Goods
- Computer Peripherals
- Printers
- AC Servo Drives
- Desktop Computers

### 3 Description

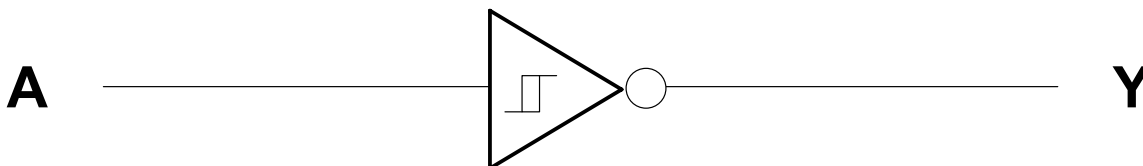
The SNx4HCT14 devices contain six independent inverters. The devices perform the Boolean function  $Y = \bar{A}$  in positive logic.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN54HCT14	CFP (14)	9.21 mm x 5.97 mm
	CDIP (14)	19.56 mm x 6.67 mm
	LCCC (20)	8.89 mm x 8.89 mm
SN74HCT14	SOIC (14)	8.65 mm x 3.91 mm
	TVSOP (14)	3.60 mm x 4.40 mm
	PDIP (14)	19.30 mm x 6.35 mm
	TSSOP (14)	5.00 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Logic Diagram (Positive Logic)



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

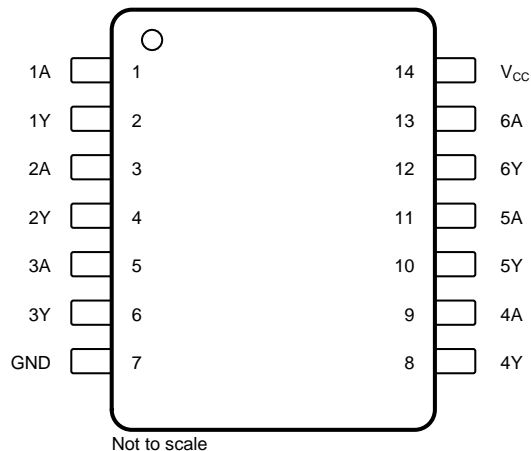
### Changes from Revision F (October 2010) to Revision G

Page

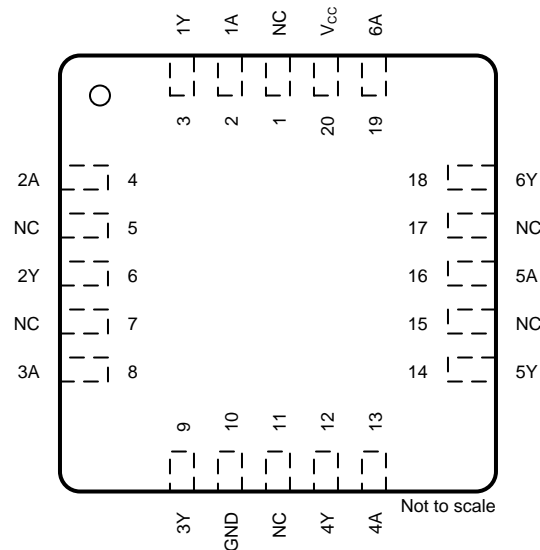
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section .....
- Deleted *Ordering Information* table; see *Package Option Addendum* at the end of the data sheet.....
- Changed Package thermal impedance,  $R_{\theta JA}$ , values in *Thermal Information* table From: 86 To: 90.9 (D), From: 96 To: 105 (DB), From: 127 To: 132.2 (DGV), From: 80 To: 55.3 (N), and From: 113 To: 120.2 (PW).....

## 5 Pin Configuration and Functions

**D, DB, DGV, J, N, PW, or W Package**  
X-Pin SOIC, SSOP, TVSOP, CDIP, PDIP, TSSOP, or CFP  
Top View



**FK Package**  
X-Pin LCCC  
Top View



### Pin Functions

NAME	PIN		I/O	DESCRIPTION
	SOIC, SSOP, TVSOP, CDIP, PDIP, TSSOP, CFP	LCCC		
1A	1	2	I	Channel 1 input
1Y	2	3	O	Channel 1 output
2A	3	4	I	Channel 2 input
2Y	4	6	O	Channel 2 output
3A	5	8	I	Channel 3 input
3Y	6	9	O	Channel 3 output
4A	9	13	I	Channel 4 input
4Y	8	12	O	Channel 4 output
5A	11	16	I	Channel 5 input
5Y	10	14	O	Channel 5 output
6A	13	19	I	Channel 6 input
6Y	12	18	O	Channel 6 output
GND	7	10	—	Ground
NC	—	1, 5, 7, 11, 15, 17	—	No internal connection
V <sub>CC</sub>	14	20	—	Power supply

## 6 Specifications

### 6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Supply voltage, $V_{CC}$		-0.5	7	V
Input voltage, $V_I$ <sup>(2)</sup>		-0.5	$V_{CC} + 0.5$	V
Output voltage, $V_O$ <sup>(2)</sup>		-0.5	$V_{CC} + 0.5$	V
Input clamp current, $I_{IK}$	$V_I < 0$ or $V_I > V_{CC}$		$\pm 20$	mA
Output clamp current, $I_{OK}$	$V_O < 0$ or $V_O > V_{CC}$		$\pm 20$	mA
Continuous output current, $I_O$	$V_O = 0$ to $V_{CC}$		$\pm 25$	mA
Continuous current through $V_{CC}$ or GND			$\pm 50$	mA
Operating junction temperature, $T_J$			150	°C
Storage temperature, $T_{stg}$		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	$\pm 2000$	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	$\pm 1000$	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

 see<sup>(1)</sup>

		MIN	MAX	UNIT	
$V_{CC}$	Supply voltage	4.5	5.5	V	
$V_I$	Input voltage	0	$V_{CC}$	V	
$V_O$	Output voltage	0	$V_{CC}$	V	
$T_A$	Operating free-air temperature	SN54HCT14	-55	125	°C
		SN74HCT14	-40	85	

- (1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN74HCT14					UNIT
		D (SOIC)	DB (SSOP)	DGV (TVSOP)	N (PDIP)	PW (TSSOP)	
		14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	90.9	105	132.2	55.3	120.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51	57	51.7	42.5	48.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45.2	52.4	61.4	35.1	61.9	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	18.4	22.2	5.5	27.2	5.7	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	44.9	51.8	60.7	35	61.3	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{T+}$	Positive-going threshold	$V_{CC} = 4.5\text{ V}$	$T_A = 25^\circ\text{C}$	1.2	1.5	1.9	V
			SN54HCT14	1.2		1.9	
			SN74HCT14	1.2		1.9	
		$V_{CC} = 5.5\text{ V}$	$T_A = 25^\circ\text{C}$	1.4	1.7	2.1	
			SN54HCT14	1.4		2.1	
			SN74HCT14	1.4		2.1	
$V_{T-}$	Negative-going threshold	$V_{CC} = 4.5\text{ V}$	$T_A = 25^\circ\text{C}$	0.5	0.9	1.2	V
			SN54HCT14	0.5		1.2	
			SN74HCT14	0.5		1.2	
		$V_{CC} = 5.5\text{ V}$	$T_A = 25^\circ\text{C}$	0.6	1	1.4	
			SN54HCT14	0.6		1.4	
			SN74HCT14	0.6		1.4	
$\Delta V_T$	Hysteresis ( $V_{T+} - V_{T-}$ )	$V_{CC} = 4.5\text{ V}$	$T_A = 25^\circ\text{C}$	0.4	0.6	1.4	V
			SN54HCT14	0.4		1.4	
			SN74HCT14	0.4		1.4	
		$V_{CC} = 5.5\text{ V}$	$T_A = 25^\circ\text{C}$	0.4	0.65	1.5	
			SN54HCT14	0.4		1.5	
			SN74HCT14	0.4		1.5	
$V_{OH}$	High-level output voltage	$I_{OH} = -20\ \mu\text{A}$ and $V_{CC} = 4.5\text{ V}$	$T_A = 25^\circ\text{C}$	4.4	4.49		V
			SN54HCT14	4.4			
			SN74HCT14	4.4			
		$I_{OH} = -4\text{ mA}$ and $V_{CC} = 4.5\text{ V}$	$T_A = 25^\circ\text{C}$	3.98	4.3		
			SN54HCT14	3.7			
			SN74HCT14	3.84			
$V_{OL}$	Low-level output voltage	$I_{OL} = 20\ \mu\text{A}$ and $V_{CC} = 4.5\text{ V}$	$T_A = 25^\circ\text{C}$		0.001	0.1	V
			SN54HCT14			0.1	
			SN74HCT14			0.1	
		$I_{OL} = 4\text{ mA}$ and $V_{CC} = 4.5\text{ V}$	$T_A = 25^\circ\text{C}$		0.17	0.26	
			SN54HCT14			0.4	
			SN74HCT14			0.33	
$I_I$	Input current	$V_I = V_{CC}$ or GND and $V_{CC} = 5.5\text{ V}$	$T_A = 25^\circ\text{C}$			$\pm 0.1$	$\mu\text{A}$
			SN54HCT14			$\pm 1$	
			SN74HCT14			$\pm 1$	
$I_{CC}$	Supply current	$V_I = V_{CC}$ or GND, $I_O = 0$ , and $V_{CC} = 5.5\text{ V}$	$T_A = 25^\circ\text{C}$			2	$\mu\text{A}$
			SN54HCT14			40	
			SN74HCT14			20	
$\Delta I_{CC}^{(1)}$	Change in supply current	One input at 0.5 V or 2.4 V, other inputs at GND or $V_{CC}$ , and $V_{CC} = 5.5\text{ V}$	$T_A = 25^\circ\text{C}$		0.2	2.4	mA
			SN54HCT14			3	
			SN74HCT14			2.9	
$C_i$	Input capacitance	$V_I = V_{CC}$ or GND and $V_{CC} = 5\text{ V}$	$T_A = 25^\circ\text{C}$		3	10	pF
			SN54HCT14			10	
			SN74HCT14			10	

(1) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or  $V_{CC}$ .

### 6.6 Switching Characteristics

over recommended operating free-air temperature range and  $C_L = 50$  pF (unless otherwise noted; see Figure 5)

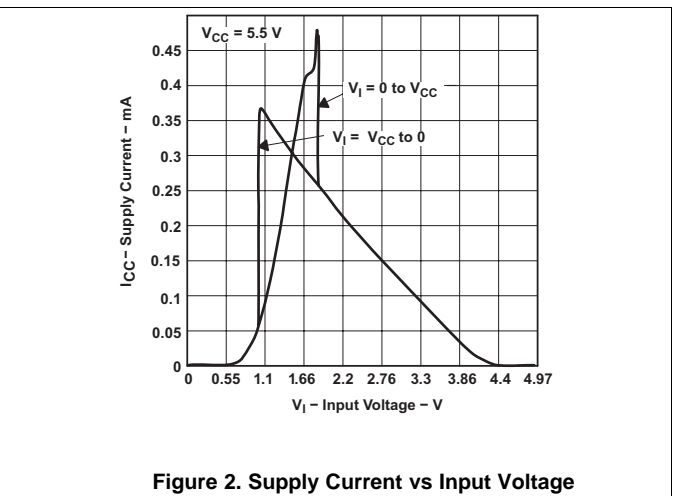
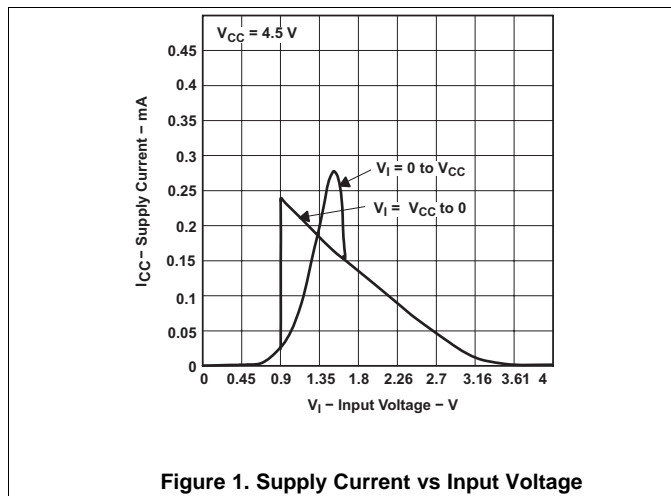
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{pd}$ Propagation (delay) time	A	Y	$V_{CC} = 4.5$ V	$T_A = 25^\circ\text{C}$		20	32	ns
				SN54HCT14			48	
				SN74HCT14			40	
			$V_{CC} = 5.5$ V	$T_A = 25^\circ\text{C}$		18	30	
				SN54HCT14			45	
				SN74HCT14			38	
$t_t$	—	Y	$V_{CC} = 4.5$ V	$T_A = 25^\circ\text{C}$		7	15	ns
				SN54HCT14			22	
				SN74HCT14			19	
			$V_{CC} = 5.5$ V	$T_A = 25^\circ\text{C}$		6	14	
				SN54HCT14			20	
				SN74HCT14			17	

### 6.7 Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	No load	10	pF

### 6.8 Typical Characteristics



Typical Characteristics (continued)

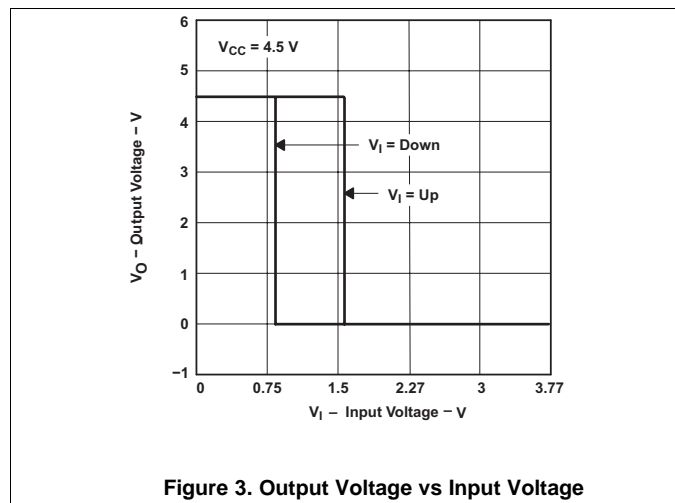


Figure 3. Output Voltage vs Input Voltage

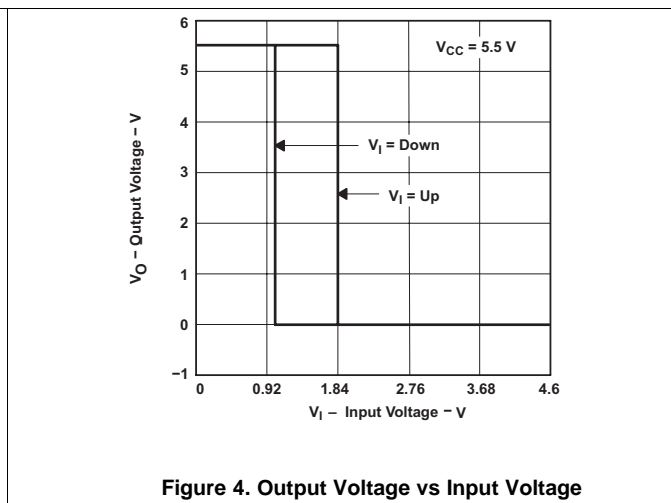
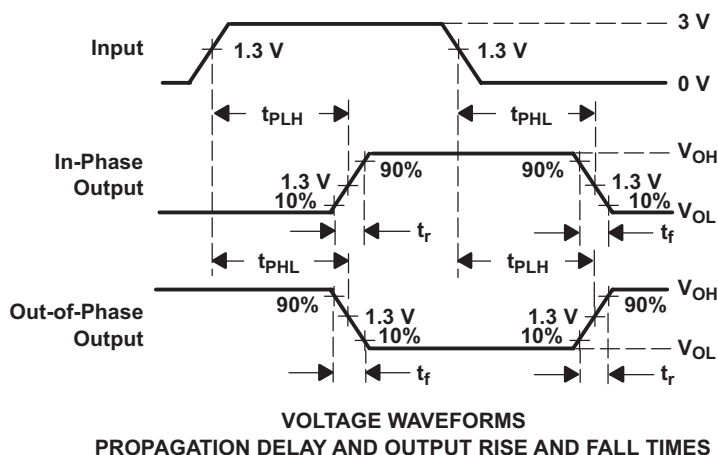
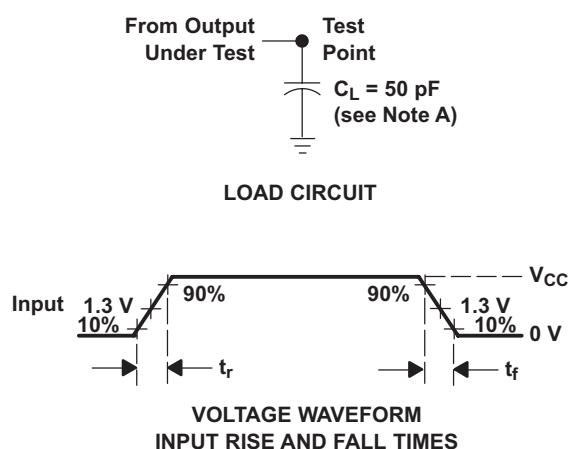


Figure 4. Output Voltage vs Input Voltage

7 Parameter Measurement Information



- A.  $C_L$  includes probe and test-fixture capacitance.
- B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 6 \text{ ns}$ ,  $t_f = 6 \text{ ns}$ .
- C. The outputs are measured one at a time with one input transition per measurement.
- D.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 5. Load Circuit and Voltage Waveforms

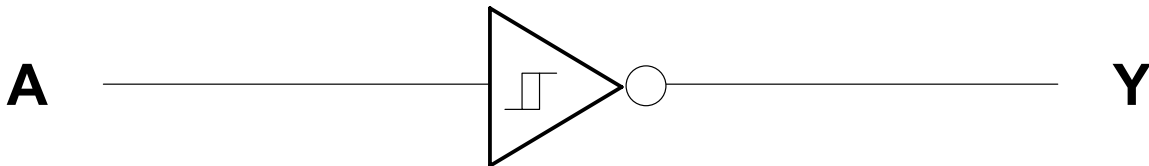
## 8 Detailed Description

### 8.1 Overview

The  $\text{SNx4HCT14}$  Schmitt-Trigger devices contain six independent inverters. They perform the Boolean function  $Y = \bar{A}$  in positive logic.

Schmitt-Trigger inputs are designed to provide a minimum separation between positive and negative switching thresholds. This allows for noisy or slow inputs that would cause problems such as oscillation or excessive current draw with normal CMOS inputs.

### 8.2 Functional Block Diagram



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### 8.3 Feature Description

The wide operating range of these devices allow them to be used in a variety of systems that use different logic levels. The outputs can drive up to 10 LSTTL loads each. The balanced drive outputs can source or sink 8 mA at 5-V  $V_{CC}$ . This device is also input TTL compatible.

### 8.4 Device Functional Modes

[Table 1](#) lists the functional modes of the  $\text{SNx4HCT14}$ .

**Table 1. Function Table**

INPUT A	OUTPUT Y
H	L
L	H



## 9 Application and Implementation

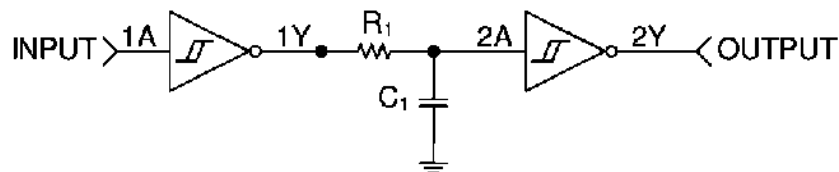
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The SN74HCT14 device is a Schmitt-Trigger input CMOS device that can be used for a multitude of inverting buffer type functions. The application shown here takes advantage of the Schmitt-Trigger inputs to produce a delay for a logic input.

### 9.2 Typical Application



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Figure 6. Simplified Application Schematic

#### 9.2.1 Design Requirements

This device uses CMOS technology. Take care to avoid bus contention, because it can drive currents that would exceed maximum limits. Parallel output drive can create fast edges into light loads, so consider routing and load conditions to prevent ringing.

#### 9.2.2 Detailed Design Procedure

This circuit is designed around an RC network that produces a slow input to the second inverter. The RC time constant,  $\tau$ , is calculated from:  $\tau = RC$ .

The delay time for this circuit is from  $t_{\text{delay}(\text{min})} = -\ln |1 - V_{T+}(\text{min}) / V_{CC}| \tau$  to  $t_{\text{delay}(\text{max})} = -\ln |1 - V_{T+}(\text{max}) / V_{CC}| \tau$ . It must be noted that the delay is consistent for each device, but because the switching threshold is only ensured between the minimum and maximum value, the output pulse length varies between devices. These values must be calculated by using the minimum and maximum ensured  $V_{T+}$  values in the [Electrical Characteristics](#).

The resistor value must be chosen such that the maximum current to and from the SN74HCT14 is 8 mA at  $5-V V_{CC}$ .

## Typical Application (continued)

### 9.2.3 Application Curve

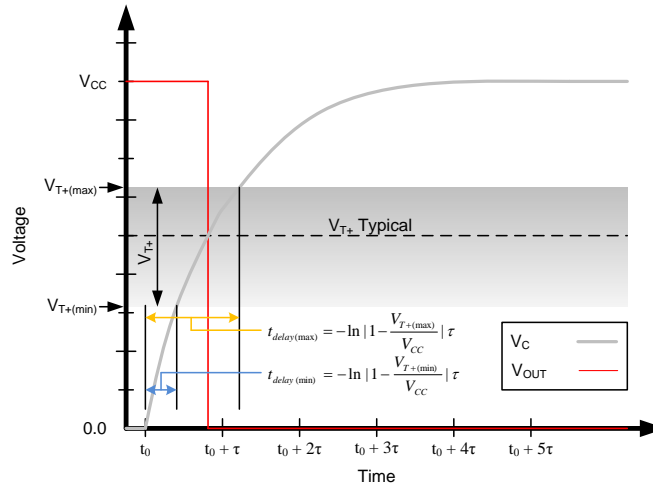


Figure 7. Ideal Capacitor Voltage and Output Voltage With Positive Switching Threshold

## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Recommended Operating Conditions](#). The  $V_{CC}$  terminal must have a good bypass capacitor to prevent power disturbance. TI recommends using a 0.1- $\mu\text{F}$  capacitor on the  $V_{CC}$  terminal, and must be placed as close as possible to the pin for best results.

## 11 Layout

### 11.1 Layout Guidelines

When using multiple bit logic devices, inputs must never float. In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only three of the four buffer gates are used. Such inputs must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient. Floating outputs are generally acceptable, unless the part is a transceiver.

### 11.2 Layout Example

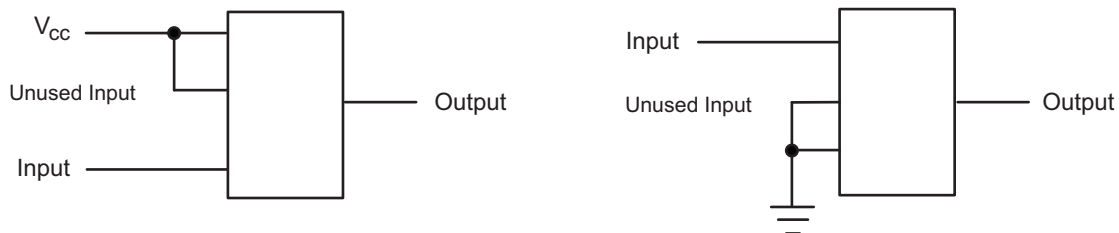


Figure 8. Layout Diagram

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation see the following:

[Implications of Slow or Floating CMOS Inputs](#) (SCBA004)

### 12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 2. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54HCT14	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
SN74HCT14	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.4 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.5 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

### 12.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-86890012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-86890012A SNJ54HCT 14FK	<a href="#">Samples</a>
5962-8689001CA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8689001CA SNJ54HCT14J	<a href="#">Samples</a>
5962-8689001DA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8689001DA SNJ54HCT14W	<a href="#">Samples</a>
SN74HCT14D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT14	<a href="#">Samples</a>
SN74HCT14DBLE	OBSOLETE	SSOP	DB	14		TBD	Call TI	Call TI	-40 to 85		
SN74HCT14DBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT14	<a href="#">Samples</a>
SN74HCT14DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT14	<a href="#">Samples</a>
SN74HCT14DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT14	<a href="#">Samples</a>
SN74HCT14DGVR	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT14	<a href="#">Samples</a>
SN74HCT14DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-40 to 85	HCT14	<a href="#">Samples</a>
SN74HCT14DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT14	<a href="#">Samples</a>
SN74HCT14DRG3	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	HCT14	<a href="#">Samples</a>
SN74HCT14DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT14	<a href="#">Samples</a>
SN74HCT14DT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT14	<a href="#">Samples</a>
SN74HCT14DTG4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT14	<a href="#">Samples</a>
SN74HCT14N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74HCT14N	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HCT14NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74HCT14N	<a href="#">Samples</a>
SN74HCT14PWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 85		
SN74HCT14PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-40 to 85	HT14	<a href="#">Samples</a>
SN74HCT14PWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT14	<a href="#">Samples</a>
SN74HCT14PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT14	<a href="#">Samples</a>
SN74HCT14PWT	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT14	<a href="#">Samples</a>
SN74HCT14PWTG4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT14	<a href="#">Samples</a>
SNJ54HCT14FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-86890012A SNJ54HCT 14FK	<a href="#">Samples</a>
SNJ54HCT14J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8689001CA SNJ54HCT14J	<a href="#">Samples</a>
SNJ54HCT14W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8689001DA SNJ54HCT14W	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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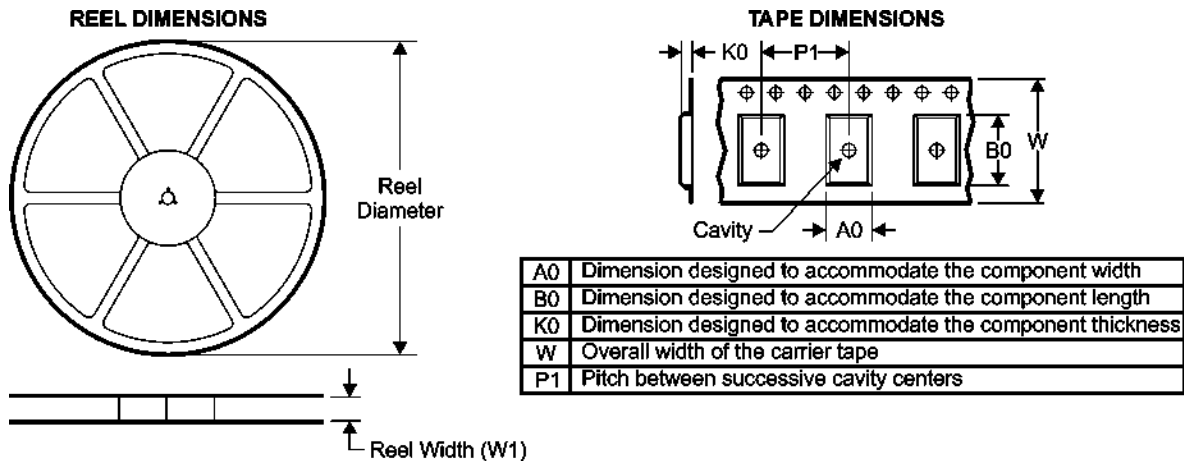
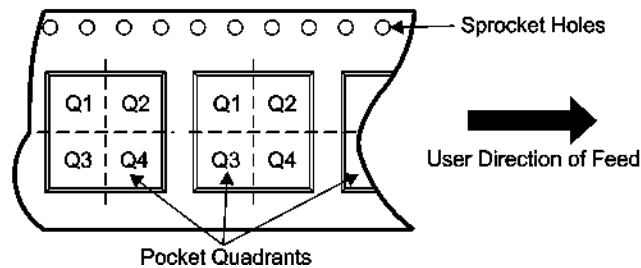
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**OTHER QUALIFIED VERSIONS OF SN54HCT14, SN74HCT14 :**

- Catalog: [SN74HCT14](#)
- Automotive: [SN74HCT14-Q1](#), [SN74HCT14-Q1](#)
- Military: [SN54HCT14](#)

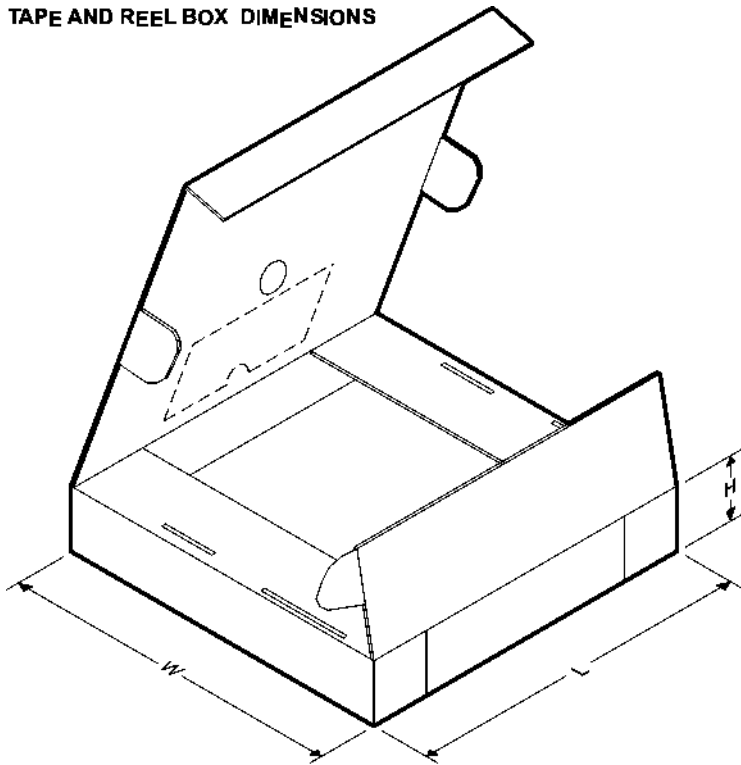
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCT14DBR	SSOP	DB	14	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74HCT14DGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74HCT14DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HCT14DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HCT14DR	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.3	8.0	16.0	Q1
SN74HCT14DRG3	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.3	8.0	16.0	Q1
SN74HCT14DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HCT14DT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HCT14PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HCT14PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HCT14PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HCT14PWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCT14DBR	SSOP	DB	14	2000	367.0	367.0	38.0
SN74HCT14DGVR	TVSOP	DGV	14	2000	367.0	367.0	35.0
SN74HCT14DR	SOIC	D	14	2500	333.2	345.9	28.6
SN74HCT14DR	SOIC	D	14	2500	367.0	367.0	38.0
SN74HCT14DR	SOIC	D	14	2500	364.0	364.0	27.0
SN74HCT14DRG3	SOIC	D	14	2500	364.0	364.0	27.0
SN74HCT14DRG4	SOIC	D	14	2500	333.2	345.9	28.6
SN74HCT14DT	SOIC	D	14	250	367.0	367.0	38.0
SN74HCT14PWR	TSSOP	PW	14	2000	364.0	364.0	27.0
SN74HCT14PWR	TSSOP	PW	14	2000	367.0	367.0	35.0
SN74HCT14PWRG4	TSSOP	PW	14	2000	367.0	367.0	35.0
SN74HCT14PWT	TSSOP	PW	14	250	367.0	367.0	35.0



J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F14

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/G 08/15

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.



DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

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