



The Future of Analog IC Technology®

MP5075L

5.5V, 1A,

Low $R_{DS(ON)}$ Load Switch

DESCRIPTION

The MP5075L provides up to 1A of load protection over a 3V to 5.5V voltage range with a small $R_{DS(ON)}$ in a space-saving package. The MP5075L is a very high-efficiency and space-saving solution for notebooks, tablets, and other portable and battery-operated applications.

With a fixed soft-start function, the MP5075L can prevent inrush current during circuit start-up. The MP5075L also provides output discharge functions, over-current protection (OCP), and thermal shutdown features.

The max load at the output (source) is current-limited. This is accomplished by utilizing sense FET topology.

An internal charge pump drives the gate of the power device, allowing for a very low on-resistance DMOS power FET of just 80mΩ.

The MP5075L is available in a space-saving SOT563 (1.6mmx1.6mm) package.

FEATURES

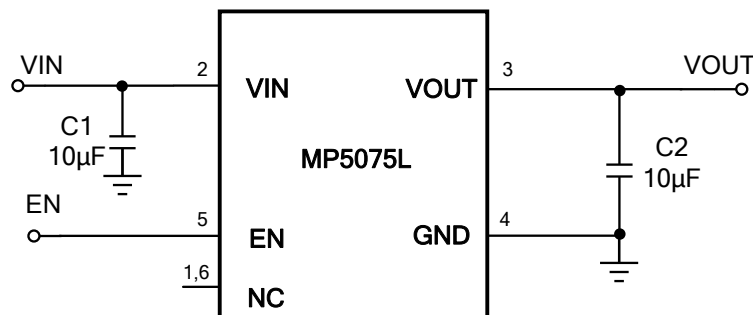
- Integrated 80mΩ Low $R_{DS(ON)}$ MOSFETs
- Wide VIN Range from 3V to 5.5V
- <5μA Shutdown Current
- Typical 1.4A Current Limit
- Output Discharge Function
- Internal Fixed 450μs Soft-Start Time
- <200ns Short-Circuit Protection Response Time
- Thermal Protection
- Available in a SOT563 (1.6mmx1.6mm) Package

APPLICATIONS

- Notebook and Tablet Computers
- Portable Devices
- Solid-State Drives
- Handheld Devices
- USB Power Distribution
- USB Dongles

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TYPICAL APPLICATION



ORDERING INFORMATION

| Part Number* | Package | Top Marking |
|--------------|---------|-------------|
| MP5075LGTF | SOT563 | See Below |

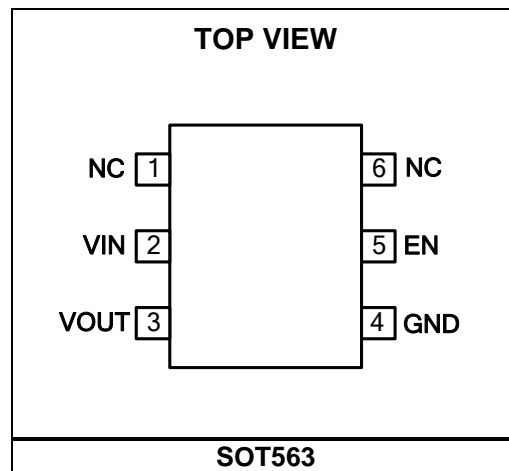
* For Tape & Reel, add suffix -Z (e.g. MP5075LGTF-Z)

TOP MARKING**AWPY****LLL**

AWP: Product code of MP5075LGTF

Y: Year code

LLL: Lot number

PACKAGE REFERENCE

ABSOLUTE MAXIMUM RATINGS (1)

| | |
|---|----------------|
| VIN | -0.3V to +6.5V |
| VOUT | -0.3V to +6.5V |
| EN | -0.3V to +6.5V |
| Junction temperature | 150°C |
| Lead temperature | 260°C |
| Continuous power dissipation (T _A = +25°C) (2) | 1W |

Recommended Operating Conditions (3)

| | |
|--|-----------------|
| Supply voltage (VIN) | 3V to 5.5V |
| Output voltage (VOUT) | 3V to 5.5V |
| Output current (I _{OUT}) | 1A |
| Operating junction temp. (T _J) ... | -40°C to +125°C |

| Thermal Resistance (4) | θ_{JA} | θ_{JC} | |
|-------------------------------|-----------------------|-----------------------|------|
| SOT563 | 130..... | 60... | °C/W |

NOTES:

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 3) The device is not guaranteed to function outside of its operating conditions.
- 4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

$V_{IN} = 5V$, $T_J = -40^{\circ}C$ to $125^{\circ}C$ ⁽⁵⁾, typical value is tested at $T_J = 25^{\circ}C$, unless otherwise noted.

| Parameters | Symbol | Condition | Min | Typ | Max | Units |
|--|----------------|---------------------------------------|-----|-----|-----|-------------|
| Input and Supply Voltage Range | | | | | | |
| Input voltage | V_{IN} | | 3 | | 5.5 | V |
| Supply Current | | | | | | |
| Off-state leakage current | I_{OFF} | $V_{IN} = 5V, EN = 0$ | | | 5 | μA |
| VIN standby current | I_{STBY} | $V_{IN} = 5V, EN = 0$ | | 0.1 | 5 | μA |
| | | $V_{IN} = 5V, \text{enable, no load}$ | | 230 | 300 | |
| Power FET | | | | | | |
| On resistance | $R_{DS(ON)}$ | $V_{IN} = 5V$ | | 80 | | m Ω |
| | | $V_{IN} = 3.3V$ | | 110 | | |
| Thermal Shutdown and Recovery | | | | | | |
| Shutdown temperature ⁽⁶⁾ | T_{STD} | | | 150 | | $^{\circ}C$ |
| Hysteresis ⁽⁶⁾ | T_{HYS} | | | 30 | | $^{\circ}C$ |
| Under-Voltage Protection (UVLO) | | | | | | |
| VIN under-voltage lockout threshold | V_{IN_UVLO} | UVLO rising threshold | 2.3 | 2.6 | 2.9 | V |
| UVLO hysteresis | $V_{UVLO-HYS}$ | | | 200 | | mV |
| Soft Start (SS) | | | | | | |
| SS time | T_{SS} | 0% to 100% | | 450 | | μs |
| Enable (EN) | | | | | | |
| EN rising threshold | V_{ENH} | | 1.3 | 1.5 | 1.7 | V |
| EN hysteresis | V_{EN-HYS} | | | 200 | | mV |
| EN pull-down resistor | R_{PUD} | | | 1 | | M Ω |
| ILIM | | | | | | |
| Current limit | I_{OUT} | | 1.2 | 1.4 | 1.6 | A |
| Discharge Resistance | | | | | | |
| Discharge resistance | R_{DIS} | | | 150 | | Ω |

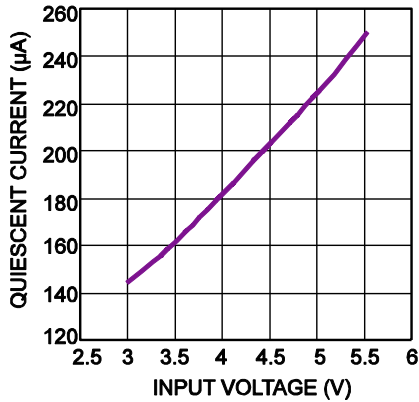
NOTES:

- 5) Guaranteed by over-temperature correlation, not tested in production.
- 6) Guaranteed by characterization, not tested in production.

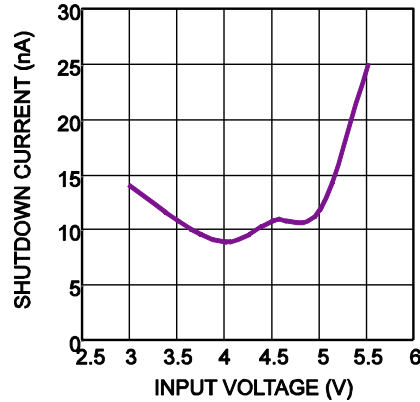
TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = EN = 5V$, $T_A = 25^\circ C$, unless otherwise noted.

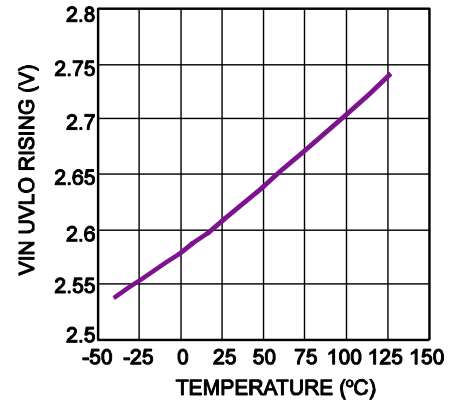
Quiescent Current vs. Input Voltage



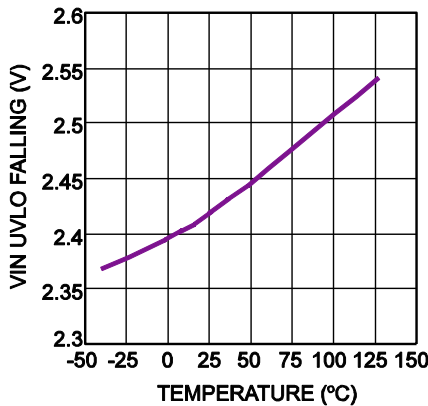
Shutdown Current vs. Input Voltage



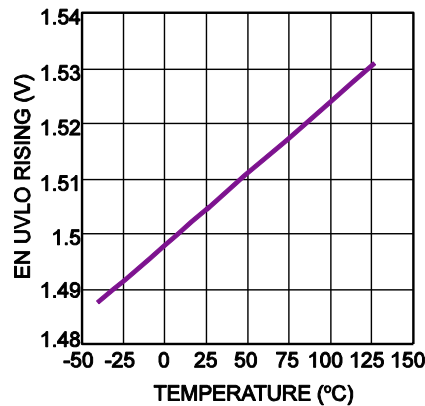
V_{IN} UVLO Rising Threshold vs. Temperature



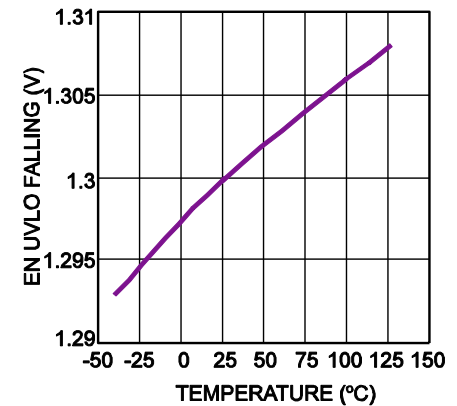
V_{IN} UVLO Falling Threshold vs. Temperature



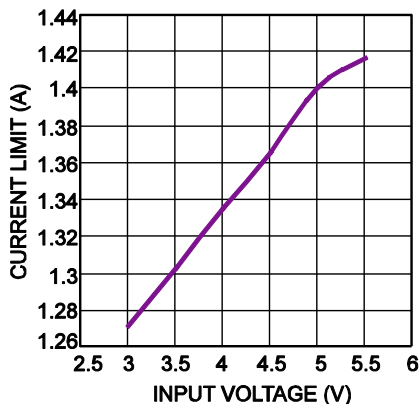
EN Rising Threshold vs. Temperature



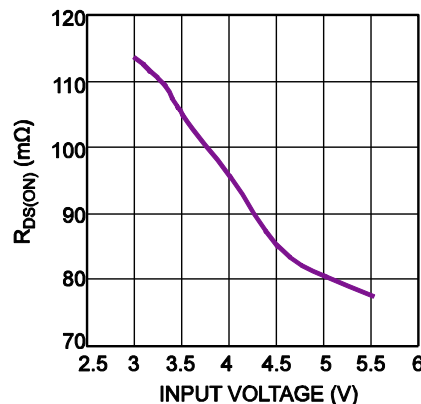
EN Falling Threshold vs. Temperature



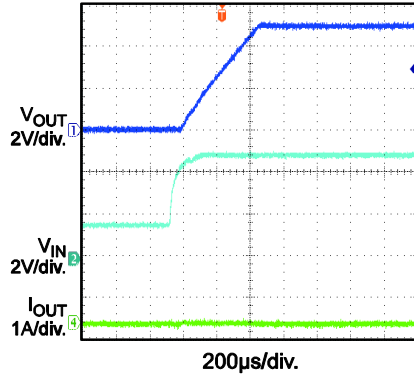
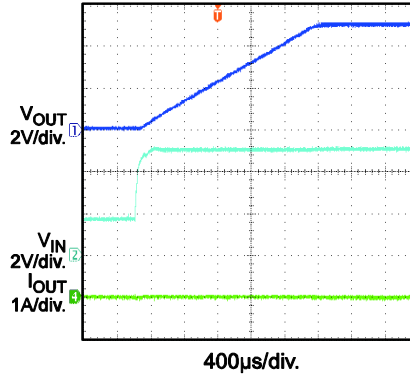
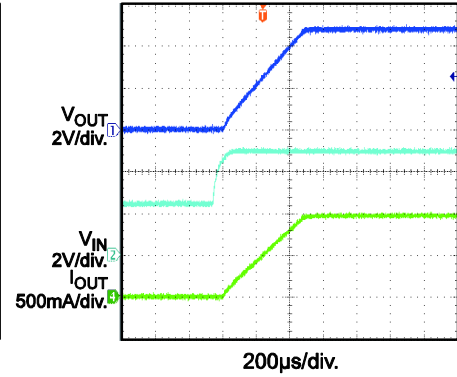
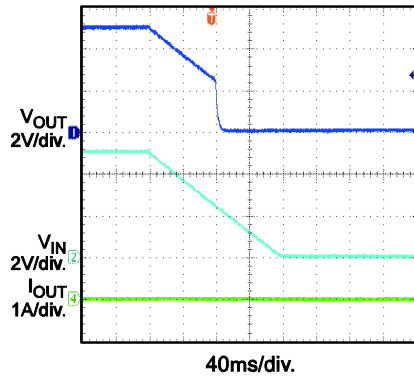
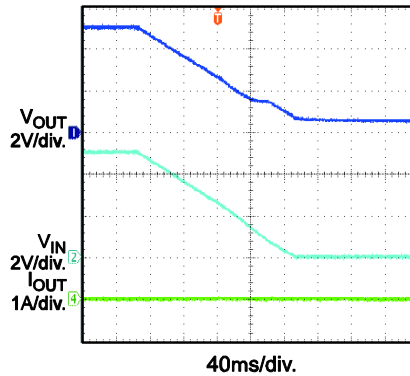
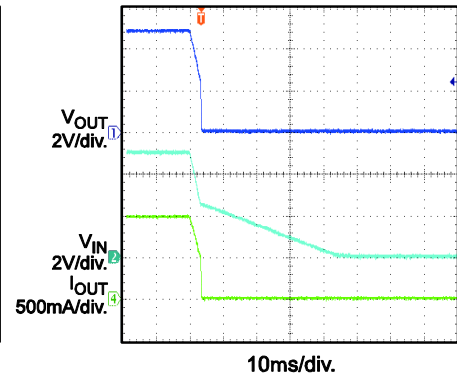
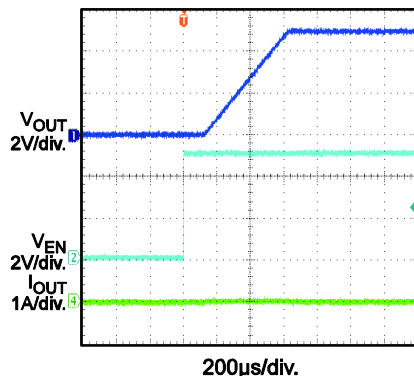
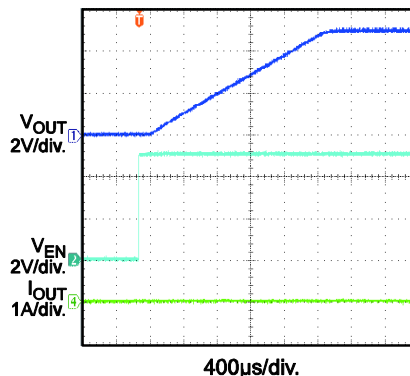
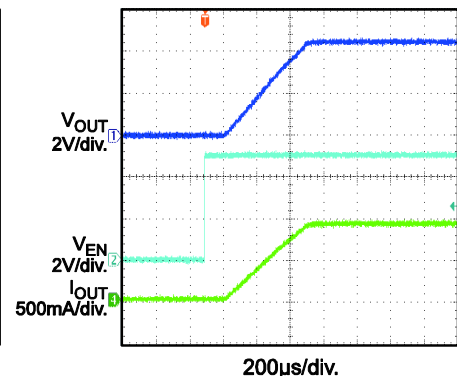
Current Limit vs. Input Voltage



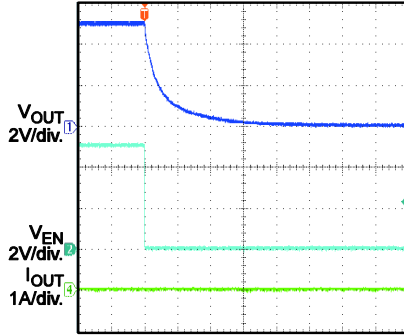
$R_{DS(ON)}$ vs. Input Voltage



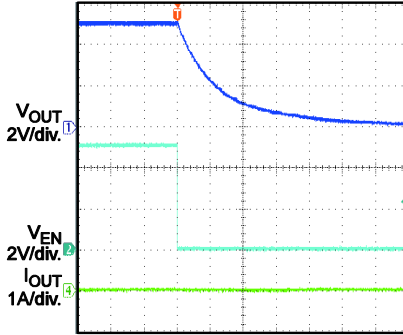
TYPICAL PERFORMANCE CHARACTERISTICS (continued)
 $V_{IN} = V_{EN} = 5V$, $T_A = 25^\circ C$, unless otherwise noted.

Start-Up through Input Voltage
 $V_{IN} = 5V$, $I_{OUT} = 0A$

Start-Up through Input Voltage
 $V_{IN} = 5V$, $I_{OUT} = 0A$, $C_{OUT} = 470\mu H$

Start-Up through Input Voltage
 $V_{IN} = 5V$, $I_{OUT} = 1A$

Shutdown through Input Voltage
 $V_{IN} = 5V$, $I_{OUT} = 0A$

Shutdown through Input Voltage
 $V_{IN} = 5V$, $I_{OUT} = 0A$, $C_{OUT} = 470\mu H$

Shutdown through Input Voltage
 $V_{IN} = 5V$, $I_{OUT} = 1A$

Start-Up through EN
 $V_{IN} = 5V$, $I_{OUT} = 0A$

Start-Up through EN
 $V_{IN} = 5V$, $I_{OUT} = 0A$, $C_{OUT} = 470\mu H$

Start-Up through EN
 $V_{IN} = 5V$, $I_{OUT} = 1A$


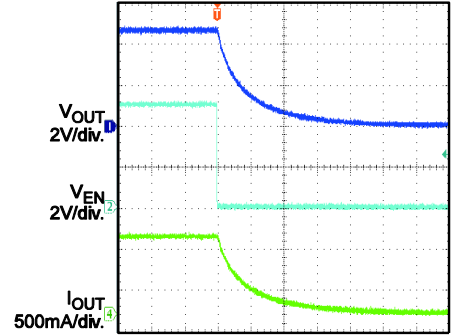
TYPICAL PERFORMANCE CHARACTERISTICS (continued)
 $V_{IN} = V_{EN} = 5V$, $T_A = 25^\circ C$, unless otherwise noted.

Shutdown through EN
 $V_{IN} = 5V$, $I_{OUT} = 0A$


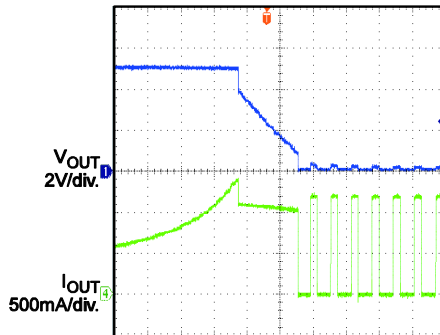
2ms/div.

Shutdown through EN
 $V_{IN} = 5V$, $I_{OUT} = 0A$, $C_{OUT} = 470\mu H$


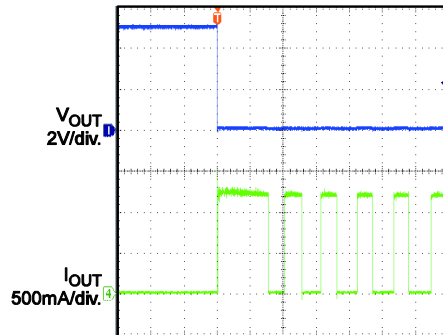
40ms/div.

Shutdown through EN
 $V_{IN} = 5V$, $I_{OUT} = 1A$


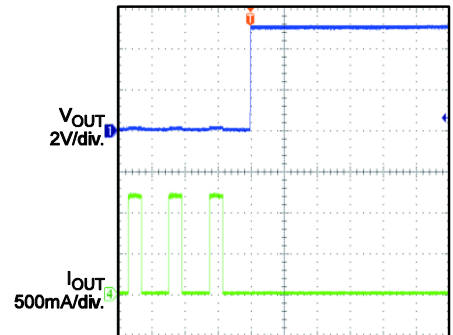
40µs/div.

OCP Current Limit with Resistive Load


40ms/div.

SCP Entry


20ms/div.

SCP Recovery


20ms/div.

PIN FUNCTIONS

| SOT563 Pin # | Name | Description |
|-------------------------|-------------|---|
| 1, 6 | NC | No connection. |
| 2 | VIN | Input power supply. |
| 3 | VOUT | Output to the load. |
| 4 | GND | Ground. |
| 5 | EN | Enable input. EN has an internal 1M Ω pull-down resistor. Float EN to shut down the IC. |

BLOCK DIAGRAM

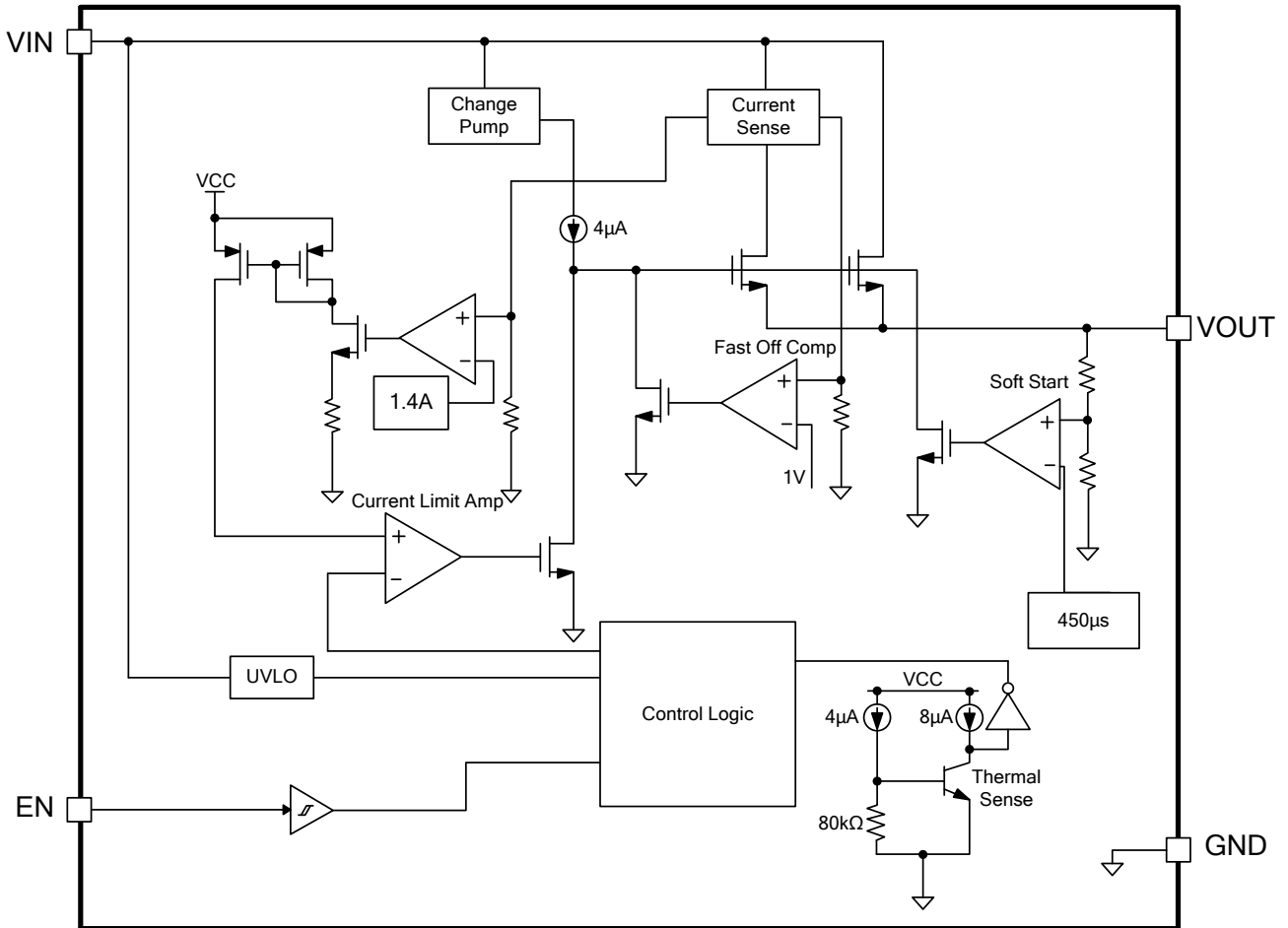


Figure 1: Functional Block Diagram

OPERATION

The MP5075L is designed to limit the inrush current to the load when a circuit card is inserted into a live backplane power source, thereby limiting the backplane's voltage drop and the slew rate of the voltage to the load. The MP5075L provides an integrated solution to monitor the input voltage, output voltage, and output current to eliminate the need for an external current power MOSFET and current switch device.

Enable (EN)

When the input voltage is greater than the under-voltage lockout (UVLO) threshold (typically 2.6V), the MP5075L can be enabled by pulling EN above 1.5V. Pull EN down to ground to disable the MP5075L.

Current Limit

The MP5075L provides an internal, fixed, 1.4A, constant current limit. Once the device reaches its current limit threshold, the internal circuit regulates the gate voltage to hold the current in the power MOSFET constant. The typical response time is about 20 μ s. The output current may have a small overshoot during this time period.

If the current limit block starts to regulate the output current, the power loss on the power MOSFET causes the IC temperature to rise. If the junction temperature rises high enough, thermal shutdown is triggered. After thermal shutdown occurs, the output is disabled until the over-temperature fault is removed. The over-temperature threshold is 150°C, and hysteresis is 30°C.

Short-Circuit Protection (SCP)

If the load current increases rapidly due to a short circuit, the current may exceed the current limit threshold greatly before the control loop can respond. If the current reaches an internal secondary current limit level (typically 7A), a fast turn-off circuit activates to turn off the power MOSFET. This limits the peak current through the switch to limit the input voltage drop. The total short-circuit response time is about 200ns. If fast turn-off is effective, the power MOSFET remains off for 80 μ s. Afterward, the power MOSFET is turned on again. If the part is

still in the short-circuit condition, the MP5075L enters current limit until the part is hot enough to trigger thermal shutdown. After the short-circuit condition is removed, the MP5075L auto-retries after the silicon temperature drops.

Output Discharge

The MP5075L has an output discharge function. This function can discharge VOUT by the internal pull-down resistance when the IC is disabled and the load is very light.

Soft Start (SS)

Soft start prevents large inrush current. The soft-start time is set to 450 μ s internally.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For best results, refer to Figure 2 and follow the guidelines below.

1. Place an input capacitor close to VIN.
2. Connect NC to GND for an easier layout.
3. Place enough vias around the IC and enough copper area near VIN and VOUT to achieve better thermal performance.

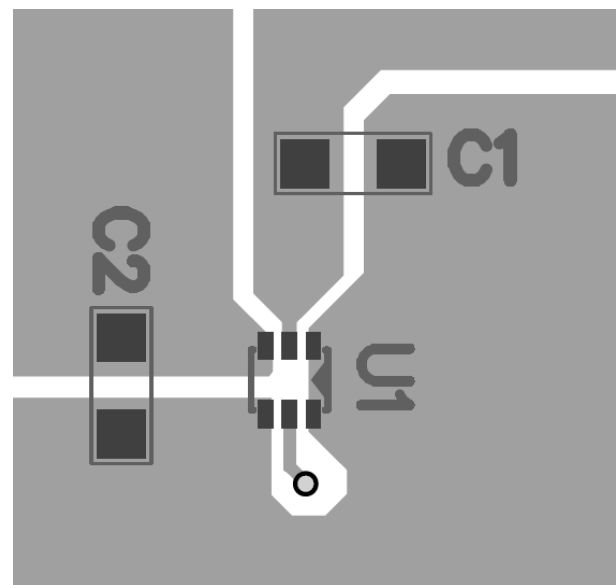
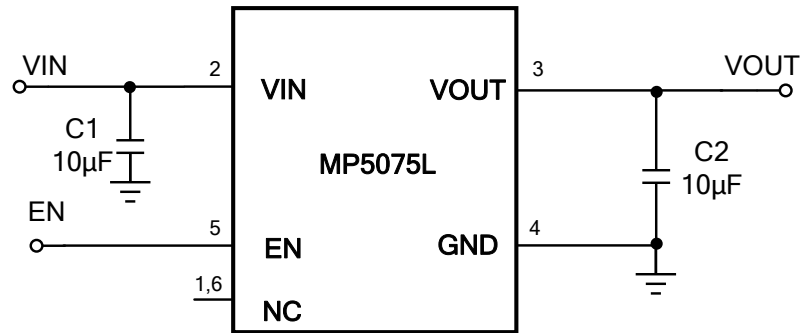
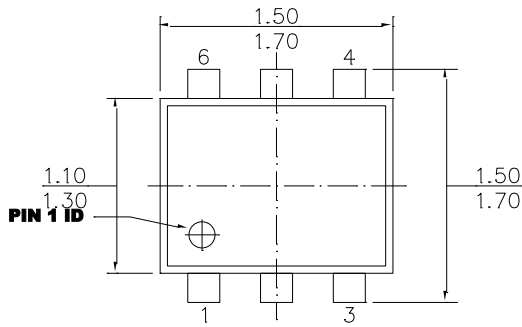
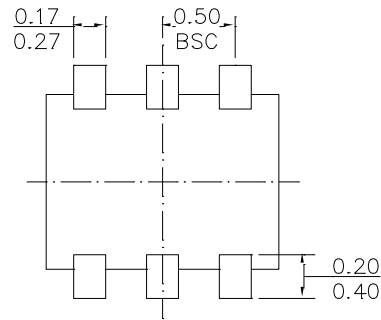
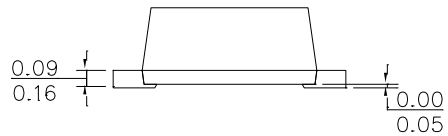
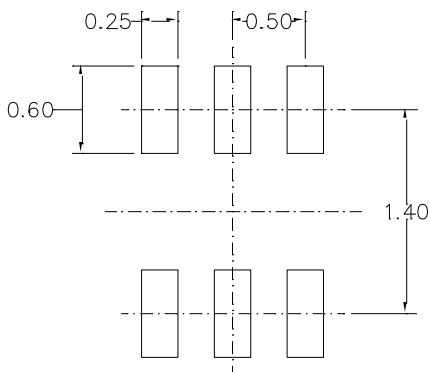


Figure 2: Recommended Layout

TYPICAL APPLICATION CIRCUIT

PACKAGE INFORMATION
SOT563

TOP VIEW

BOTTOM VIEW

FRONT VIEW

SIDE VIEW

RECOMMENDED LAND PATTERN
NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
- 5) DRAWING CONFORMS TO JEDEC MO-293, VARIATION UAAD.
- 6) DRAWING IS NOT TO SCALE.

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