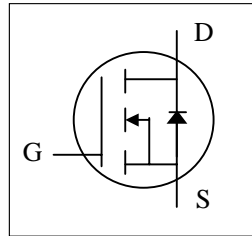


- ▼ 100% R_g & UIS Test
- ▼ Simple Drive Requirement
- ▼ Ultra Low On-resistance
- ▼ RoHS Compliant & Halogen-Free

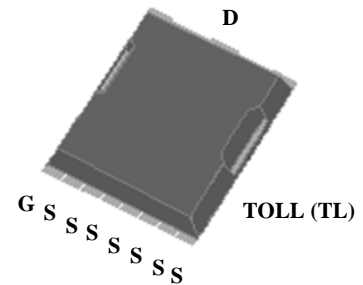


BV_{DSS}	80V
$R_{DS(ON)}$	1.2m Ω

Description

XP8NA1R2 series are innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The TOLL package is a perfect solution for high power density and high power efficiency application.



Absolute Maximum Ratings @T_j=25°C (unless otherwise specified)

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	80	V
V _{GS}	Gate-Source Voltage	+20	V
I _D @T _C =25°C	Drain Current, V _{GS} @ 10V ⁴ (Silicon Limited)	400	A
I _D @T _C =25°C	Drain Current, V _{GS} @ 10V ⁴	300	A
I _D @T _C =100°C	Drain Current, V _{GS} @ 10V	280	A
I _{DM}	Pulsed Drain Current ¹	1200	A
P _D @T _C =25°C	Total Power Dissipation	333	W
P _D @T _A =25°C	Total Power Dissipation ³	3.75	W
E _{AS}	Single Pulse Avalanche Energy ⁵	500	mJ
T _{STG}	Storage Temperature Range	-55 to 175	°C
T _J	Operating Junction Temperature Range	-55 to 175	°C

Thermal Data

Symbol	Parameter	Value	Units
R _{thj-c}	Maximum Thermal Resistance, Junction-case	0.45	°C/W
R _{thj-a}	Maximum Thermal Resistance, Junction-ambient (PCB mount) ³	40	°C/W

Electrical Characteristics @ $T_j=25^{\circ}\text{C}$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	80	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=100A$	-	-	1.2	m Ω
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	3	-	5	V
g_{fs}	Forward Transconductance	$V_{DS}=5V, I_D=100A$	-	200	-	S
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=64V, V_{GS}=0V$	-	-	25	μA
I_{GSS}	Gate-Source Leakage	$V_{GS}=+20V, V_{DS}=0V$	-	-	+0.1	μA
Q_g	Total Gate Charge	$I_D=100A$	-	265	424	nC
Q_{gs}	Gate-Source Charge	$V_{DS}=40V$	-	100	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	$V_{GS}=10V$	-	75	-	nC
$t_{d(on)}$	Turn-on Delay Time	$V_{DS}=40V$	-	56	-	ns
t_r	Rise Time	$I_D=100A$	-	110	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=3.3\Omega$	-	90	-	ns
t_f	Fall Time	$V_{GS}=10V$	-	180	-	ns
C_{iss}	Input Capacitance	$V_{GS}=0V$	-	15700	25120	pF
C_{oss}	Output Capacitance	$V_{DS}=60V$	-	2200	-	pF
C_{rss}	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	170	-	pF
R_g	Gate Resistance	$f=1.0\text{MHz}$	-	1	2	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage ²	$I_S=100A, V_{GS}=0V$	-	-	1.3	V
t_{rr}	Reverse Recovery Time	$I_S=100A, V_{GS}=0V$	-	120	-	ns
Q_{rr}	Reverse Recovery Charge	$di/dt=100A/\mu s$	-	310	-	nC

Notes:

- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse test
- 3.Surface mounted on 1 in² copper pad of FR4 board
- 4.Package limitation current is 300A .
- 5.Starting $T_j=25^{\circ}\text{C}$, $V_{DD}=40V$, $L=0.1\text{mH}$, $R_G=25\Omega$

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT, AUTOMOTIVE OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

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XSEMI RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN.

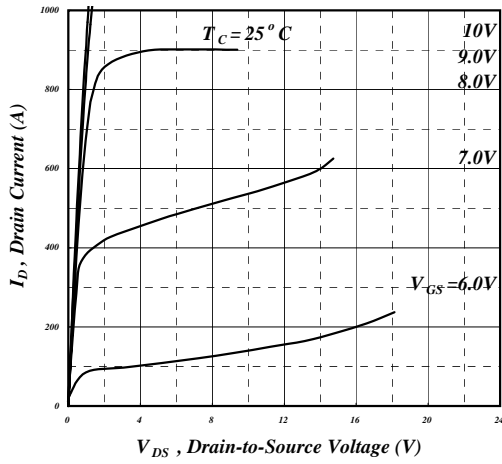


Fig 1. Typical Output Characteristics

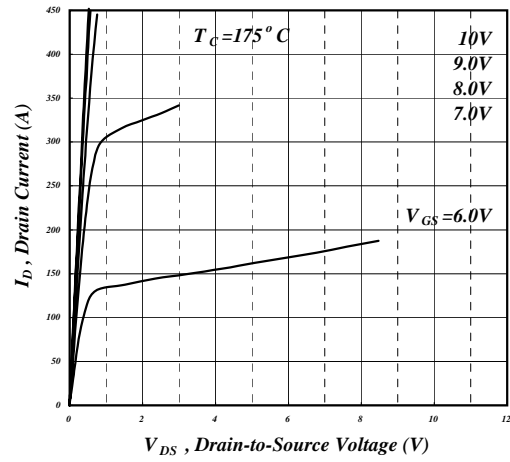


Fig 2. Typical Output Characteristics

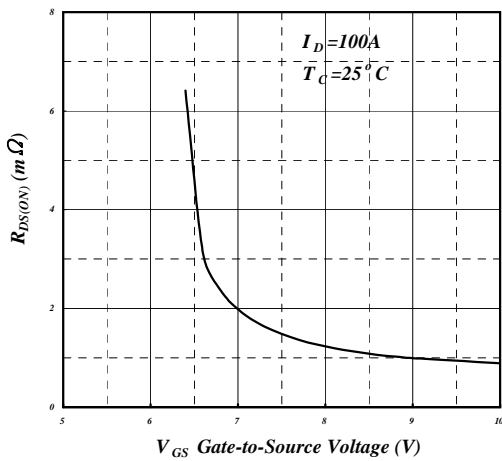


Fig 3. On-Resistance v.s. Gate Voltage

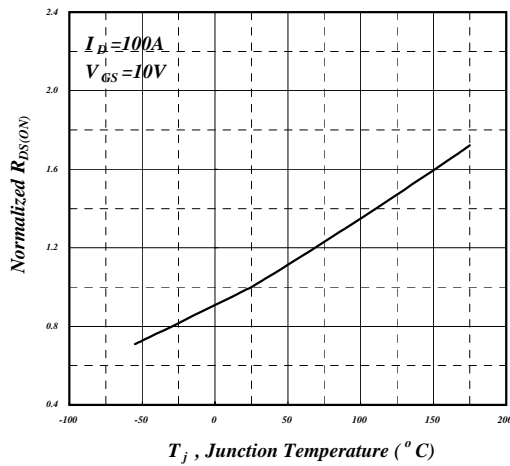


Fig 4. Normalized On-Resistance v.s. Junction Temperature

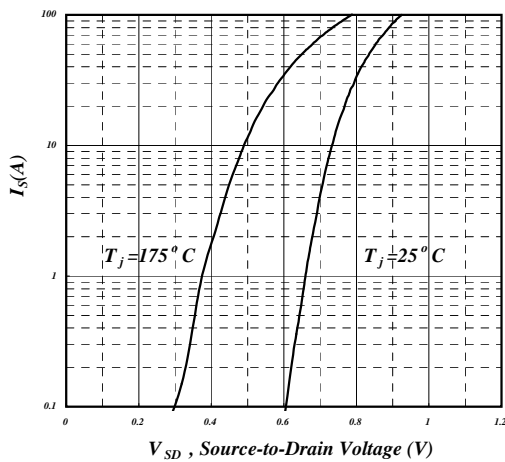


Fig 5. Forward Characteristic of Reverse Diode

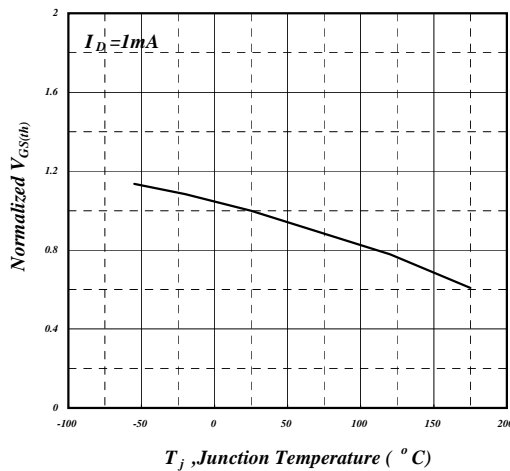


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

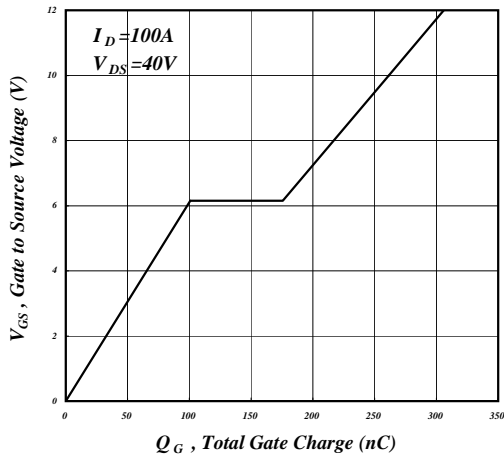


Fig 7. Gate Charge Characteristics

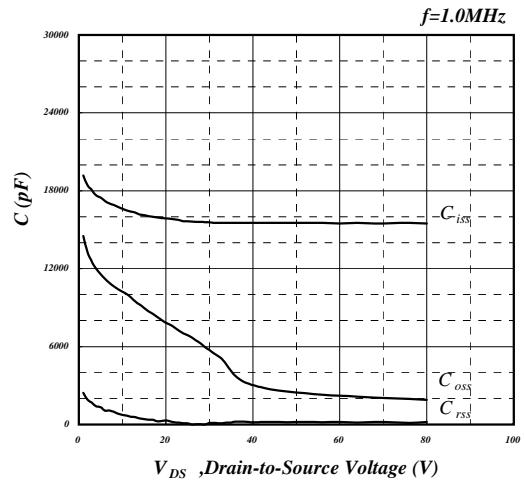


Fig 8. Typical Capacitance Characteristics

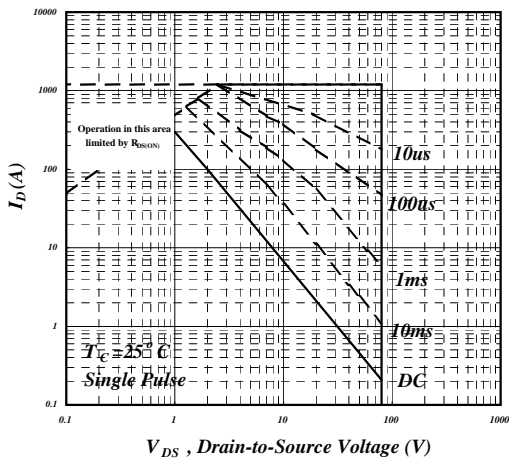


Fig 9. Maximum Safe Operating Area

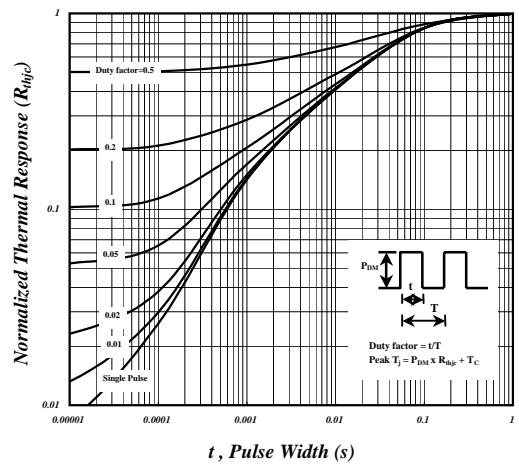


Fig 10. Effective Transient Thermal Impedance

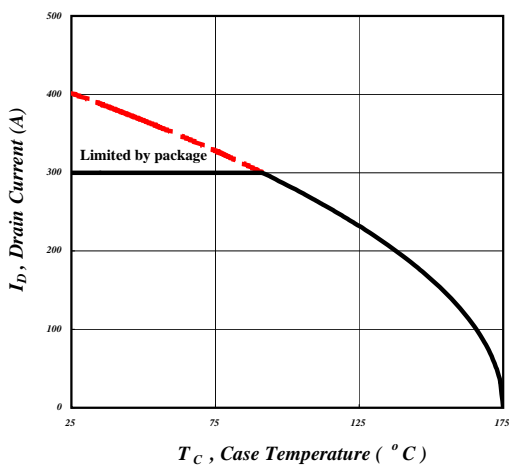


Fig 11. Drain Current v.s. Case Temperature

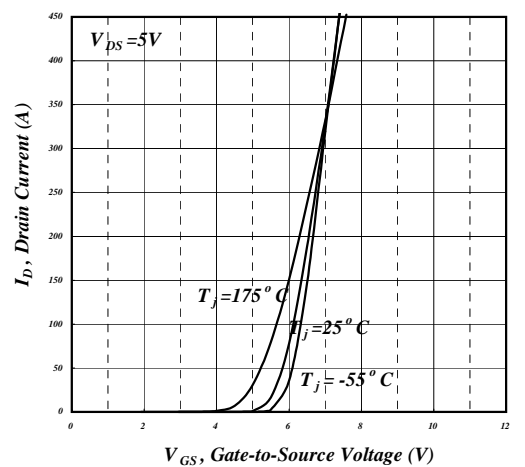


Fig 12. Transfer Characteristics

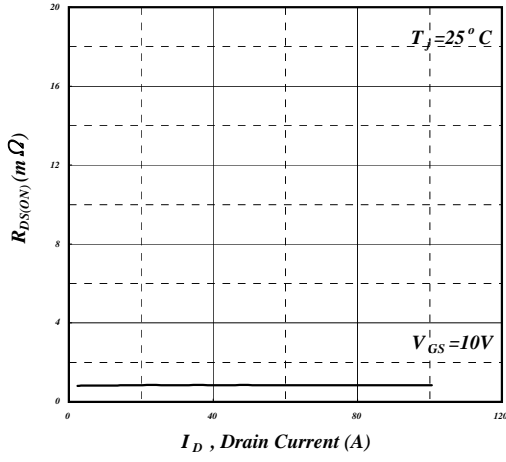


Fig 13. Typ. Drain-Source on State Resistance

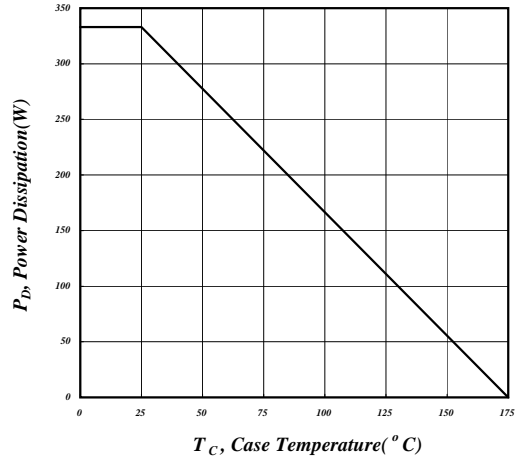
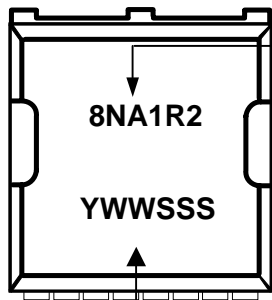


Fig 14. Total Power Dissipation

MARKING INFORMATION



Part Number

Date Code (YWWSSS)

Y : Last Digit Of The Year

WW : Week

SSS : Sequence