

Universal Programming Module 2

OVERVIEW

The Universal Programming Module (UPM) 2 is a handy, low-cost board that supports the programming of Microchip devices using MPLAB® in-circuit emulators and debuggers. The UPM can also be used with the MPLAB PM3 to ICD Adapter (AC164111) for in-circuit programming with the MPLAB PM3. The Zero Insertion Force (ZIF) socket in the UPM supports the programming of devices in DIP packages up to 40 pins with the aforementioned development tools.

PICkit Tag MICROCHIP GND (**BOARD** VDD 02-01997 © 2010 **BOARD** VDD ICD VDD VDD CORE VDD GND GND **MCLR MCLR** RESET PULL-UP LED0 LED1 LED2 AC162409-2 Universal Programming Module 2, DIP

FIGURE 1: **BOARD CONFIGURATION**

Universal Programming Module 2

CONFIGURATION

- 1. **Debugger/Programmer Connectors:** The debugger/programmer input connectors are located at J1, J6, J22 and J23 (all signals are mapped to J2).
 - J1 (ICD): RJ-11 connector used with the MPLAB ICD 3 in-circuit debugger, the MPLAB REAL ICE™ in-circuit emulator (using the standard driver board) and the MPLAB PM3 programmer
 - J6 (LVDS): Used with MPLAB REAL ICE Performance Pak (AC244002)
 - J22 (PICkit): Used with PICkit™ series programmers/debuggers
 - J23 (Tag Connect): Used with tag-connect in-circuit programming cables (TC2030-MCP)
- 2. **J2 Connector:** The J2 connector contains all of the signals for programming and/or debugging. These lines must be connected to pins marked 1 through 40 on the two 20-pin headers (J3 and J4) using the supplied jumper wires. The following are the required connections needed for programming and/or debugging (see the device data sheet or programming specification for specific pinouts).
 - PGC: Programming clock from debugger
 - · PGD: Programming data from debugger
 - VDD: Device VDD from debugger or on-board voltage regulator
 - VPP: Programming voltage/master clear input (from debugger/board)
 - GND: Device Vss pin

Optional signals needed for programming and/or debugging (see device data sheet or programming specification for specific requirements):

- PGM: Low voltage programming pin (from debugger)
- VDDC: Voltage for VCAP/VDDCORE pin (from on-board CORE VDD regulator)
- VCAP: Capacitor for VCAP/VDDCORE pin
- CLK: Clock oscillator input (from Y1)
- LED0-LED3 (connected to on-board LEDs)
- 3. J3 and J4 Connectors: These header pins map directly to the 40 pins of the device ZIF socket. For devices with less than 40 pins, J5 numbering will not match the device numbering, e.g., for a 20-pin device, J4 pin 40 will be device pin 20, J4 pin 39 will be device pin 19, etc. Consult the device data sheet for the proper jumper configuration. Further, the release notes for the tool in use may also offer other detailed information about programming the device. Release notes for MPLAB IDE v8 and earlier may be found under the Help menu. Release notes for MPLAB X IDE may be found on the Start Page under "Release Notes and Support Documentation".
- 4. Power Supply: Power is supplied to the UPM 2 by either the development tool in use, or the on-board adjustable VDD regulator, but not both. The selection is made by setting Jumper J7 to select either ICSP™ VDD (supplied by debugger) or Board VDD (supplied by on-board regulator). The UPM 2 contains rudimentary on-board debugging resources. The UPM2 has two on board adjustable regulators that each require an optional separate 9V power supply (AC162039).
 - BOARD VDD: Adjusts from 1.2V-5.5V (J7 needs to be in the BOARD VDD position)
 - CORE VDD: Adjusts from 1.2V-2.7V. Used to supply the VDDCORE/VCAP pin voltage

Universal Programming Module 2

- 5. **Debugging Resources:** The UPM 2 contains rudimentary on-board debugging resources:
 - Clock oscillator Y1 (connected directly to the CLK pin at J2)
 - HS/XT/LP crystal/capacitor sockets (Y2, C6 and C7), to be connected to the appropriate pins at J3-J4
 - Master Clear pull-up at J10 (47 kΩ resistor connected to VDD)
 - Master Clear reset button (S15)
 - LED0-LED3 (connected to the LEDx pins at J2 (LED0 and LED1 are active high, LED2 and LED3 are active low)

LOADING/PROGRAMMING A DEVICE

The ZIF socket (SKT1) will support up to 40-pin DIP packaged devices. Verify that power is removed prior to inserting the device into the ZIF socket. Also, the handle for the ZIF socket should be in the unlocked position. The device should drop in with zero force. Insert the device so that the top is aligned with the top of the ZIF socket (i.e., pin 1 to pin 1). Once the device is inserted, set the handle on the socket to the fully locked position.

REMOVING A DEVICE

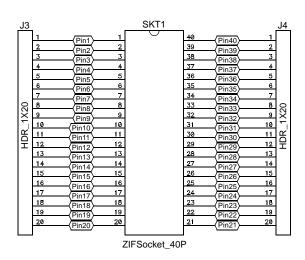
When programming a device, wait until MPLAB IDE or MPLAB PM3 in Stand-Alone mode acknowledge that programming is complete. When debugging a device, ensure the device is halted. Then remove power from the module by either unplugging the power cord (if powered by power supply) or the tool connection (if powered by tool). Unlock the ZIF socket to lift out the device, which should be able to be removed without any resistance.

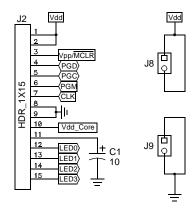
DO NOT remove the device while any debugging or programming operation is occurring or while power is applied.

RESOLVING PROGRAMMING/CONNECTION ISSUES

A capacitor (0.1 uF to 10 uF) may need to be placed between VDD and Vss.

FIGURE 2: BOARD SCHEMATICS, PART 1



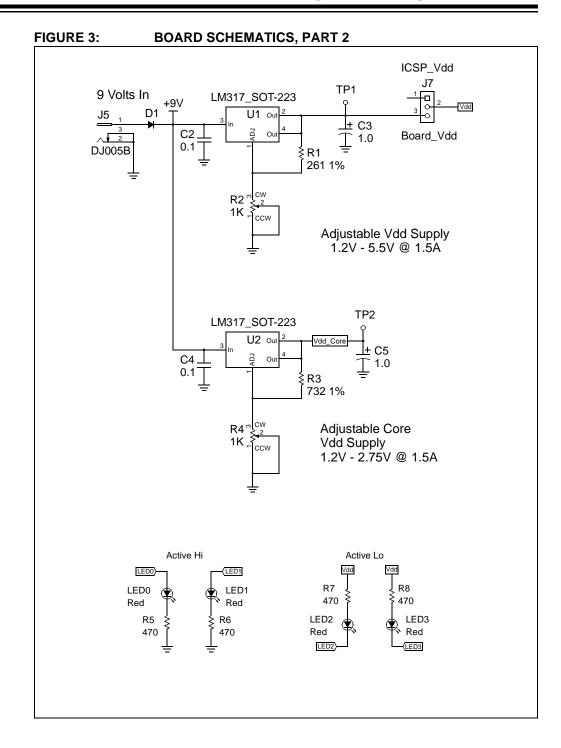


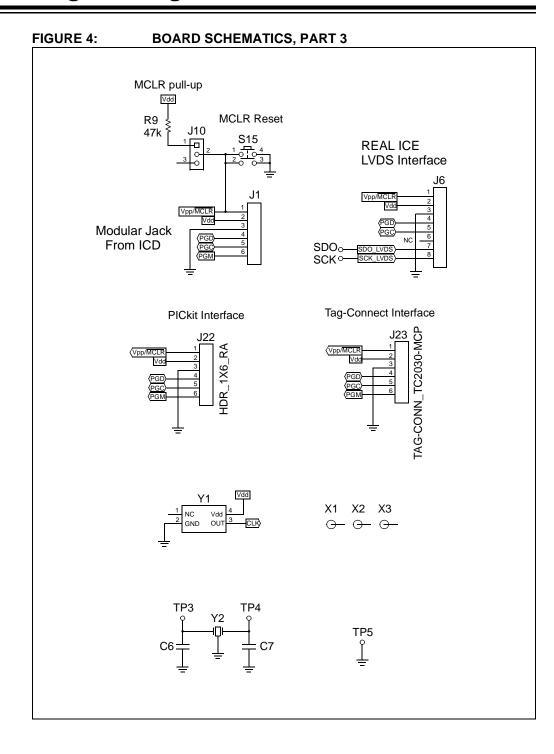
Notes:

Unless otherwise specified, resistance values are in Ohms, 5%, 1/10 W, and capacitance values are in microfarads.

Device names/numbers shown here are for reference only and may differ from actual names/numbers. Actual names/numbers are found in the BOM from this assembly.

All components are RoHS compliant.





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