

# 3N163/3N164

## P-Channel Enhancement-Mode MOSFET Transistors

### Product Summary

Part Number	$V_{(BR)DSS}$ Min (V)	$V_{GS(th)}$ (V)	$r_{DS(on)}$ Max ( $\Omega$ )	$I_{D(on)}$ Min (mA)	$C_{rss}$ Max (pF)	$t_{ON}$ Typ (ns)
3N163	-40	-2 to -5	250	-5	0.7	18
3N164	-30	-2 to -5	300	-3	0.7	18

### Features

- Ultra-Low Input Leakage: 0.02 pA Typ.
- High Gate Breakdown Voltage:  $\pm 125$  V
- Normally Off

### Benefits

- High Input Impedance Isolation
- Minimize Handling ESD Problems
- High Off Isolation without Power

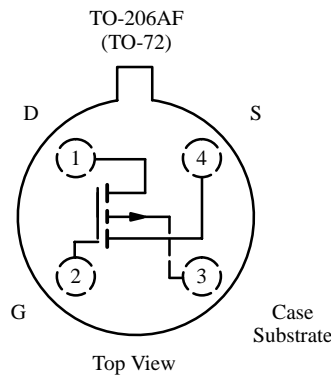
### Applications

- Ultra-High Input Impedance Amplifier
- Smoke Detectors
- Electrometers
- Analog Switching
- Digital Switching

### Description

The 3N163/164 are lateral p-channel MOSFETs designed for analog switch and preamplifier applications where high speed and low parasitic capacitances are required.

The hermetic TO-206AF package is compatible with military processing per military standards (see Military information).



### Absolute Maximum Ratings ( $T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Drain-Source Voltage	(3N163) ..... -40 V	Storage Temperature	..... -65 to 200°C
	(3N164) ..... -30 V	Operating Junction Temperature	..... -55 to 150°C
Gate-Source Voltage	..... $\pm 30$ V	Power Dissipation <sup>a</sup>	..... 375 mW
Continuous Drain Current	..... -50 mA	Notes:	
Lead Temperature ( $1/16$ " from case for 10 seconds)	..... 300°C	a. Derate 3 mW/°C above 25°C	

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70228.

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## Specifications<sup>a</sup>

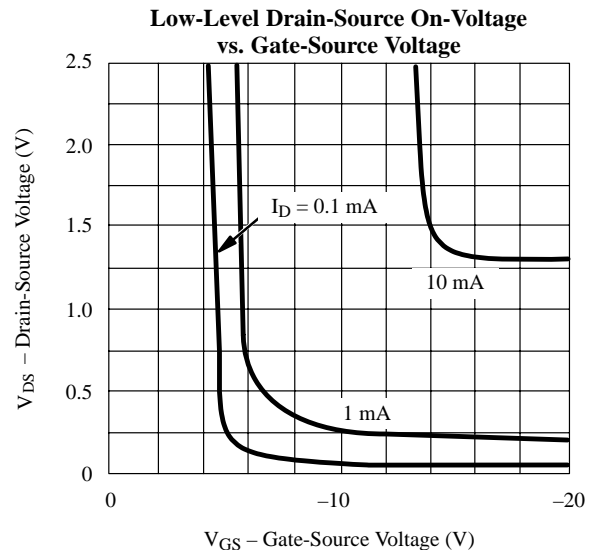
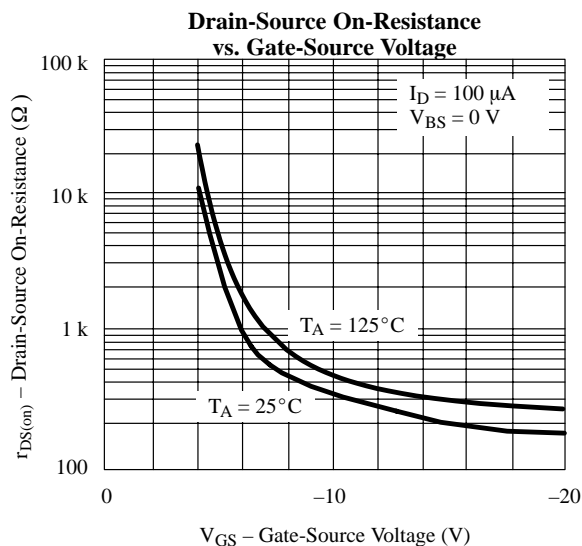
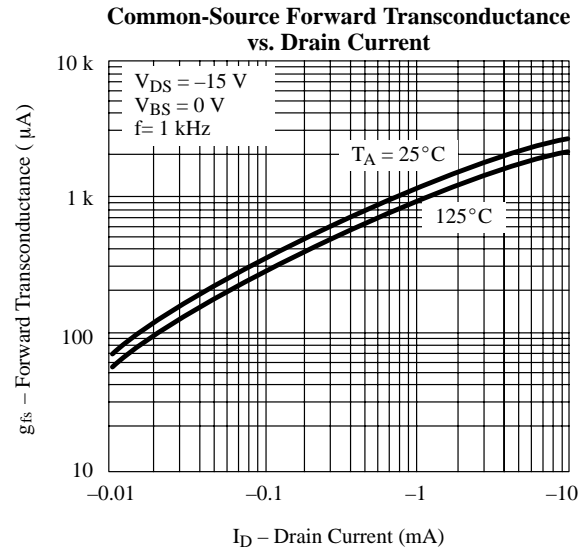
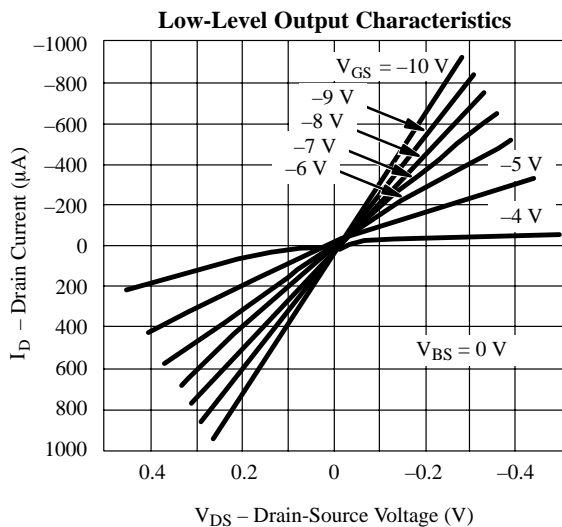
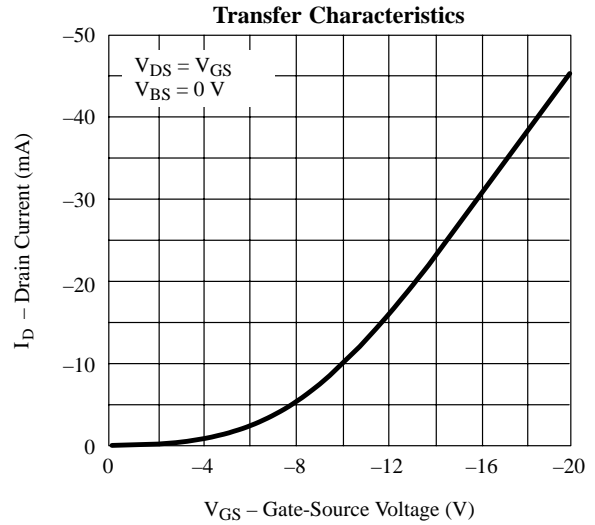
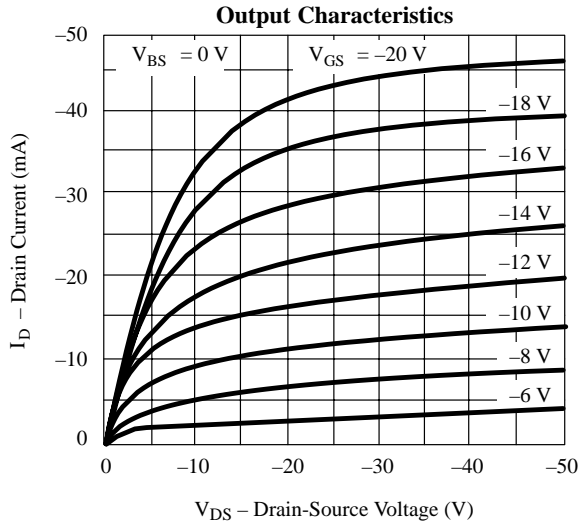
Parameter	Symbol	Test Conditions	Typ <sup>b</sup>	Limits				Unit
				3N163		3N164		
				Min	Max	Min	Max	
<b>Static</b>								
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$I_D = -10 \mu A, V_{DS} = 0 V$	-70	-40		-30		V
Source-Drain Breakdown Voltage	$V_{(BR)SDS}$	$I_S = -10 \mu A, V_{GD} = V_{BD} = 0 V$	-70	-40		-30		
Gate-Threshold Voltage	$V_{GS(th)}$	$I_D = -10 \mu A, V_{GS} = V_{DS}$	-2.5	-2	-5	-2	-5	
Gate-Source Voltage	$V_{GS}$	$I_D = -0.5 mA, V_{DS} = -15 V$	-3.5	-3	-6.5	-2.5	-6.5	
Gate-Body Leakage	$I_{GSS}$	$V_{GS} = -40 V, V_{DS} = 0 V$	<-1		-10			pA
		$T_A = 125^\circ C^d$	-1					
		$V_{GS} = -30 V, V_{DS} = 0 V$	<-1				-10	
Zero-Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -15 V, V_{GS} = 0 V$	-8		-200		-400	nA
		$T_A = 125^\circ C^d$	-20					
Zero-Gate Voltage Source Current	$I_{SDS}$	$V_{GD} = V_{BD} = 0 V, V_{SD} = -20 V$	-10		-400		-800	pA
		$T_A = 125^\circ C^d$	-25					nA
On-State Drain Current <sup>c</sup>	$I_{D(on)}$	$V_{DS} = -15 V, V_{GS} = -10 V$	-10	-5	-30	-3	-30	mA
Drain-Source On-Resistance	$r_{DS(on)}$	$V_{GS} = -20 V, I_D = -100 \mu A$	180		250		300	$\Omega$
		$T_A = 125^\circ C^d$	270					
<b>Dynamic</b>								
Forward Transconductance <sup>c</sup>	$g_{fs}$	$V_{DS} = -15 V, I_D = -10 mA$ $f = 1 kHz$	2.7	2	4	1	4	mS
Common-Source Output Conductance <sup>c</sup>	$g_{os}$		150		250		250	$\mu S$
Input Capacitance	$C_{iss}$	$V_{DS} = -15 V, I_D = -10 mA$ $f = 1 MHz$	2.4		3.5		3.5	pF
Output Capacitance	$C_{oss}$		2.5		3		3	
Reverse Transfer Capacitance	$C_{rss}$		0.5		0.7		0.7	
<b>Switching<sup>e</sup></b>								
Turn-On Time	$t_{d(on)}$	$V_{DD} = -15 V, R_L = 1500 \Omega$ $I_D \cong -10 mA, V_{GEN} = -12 V$ $R_G = 50 \Omega$	5		12		12	ns
	$t_r$		13		24		24	
Turn-Off Time	$t_{d(off)}$		25		50		50	

Notes:

- $T_A = 25^\circ C$  unless otherwise noted.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- Pulse test:  $PW \leq 300 \mu s$  duty cycle  $\leq 3\%$ .
- This parameter not registered with JEDEC.
- Switching time is essentially independent of operating temperature.

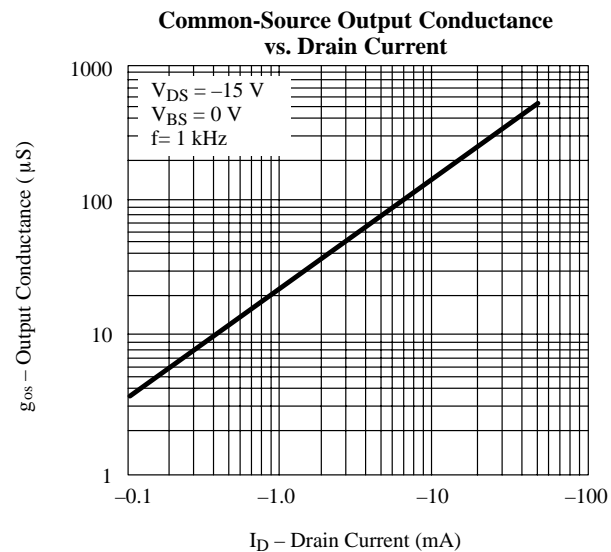
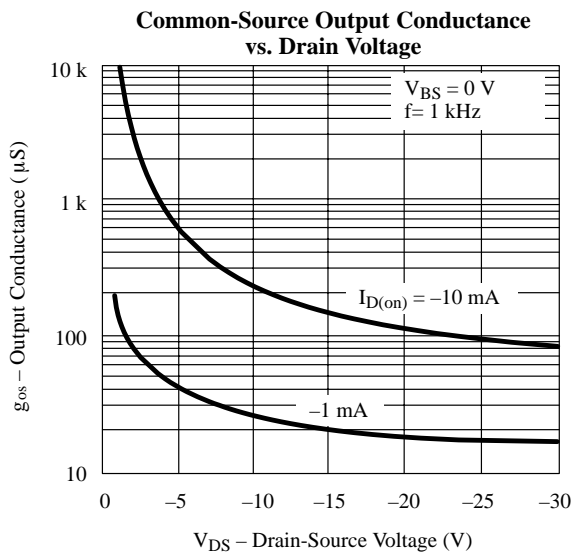
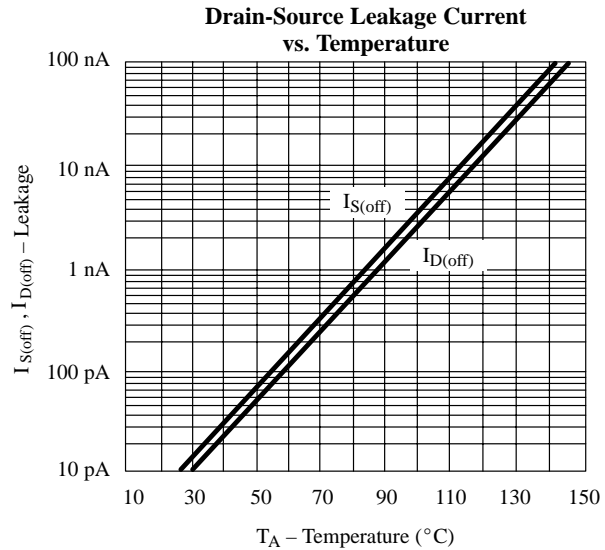
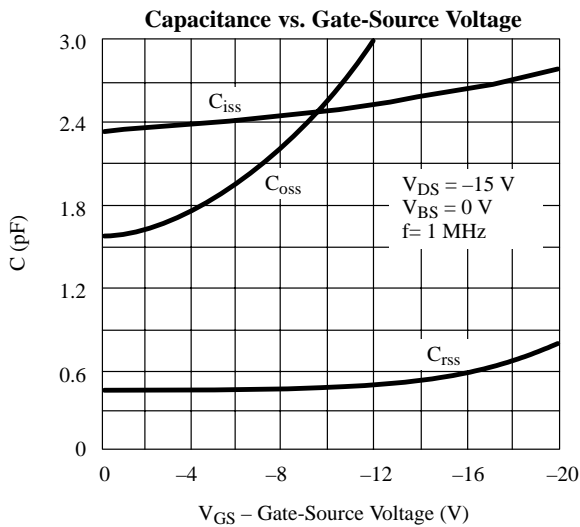
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## Typical Characteristics



# 3N163/3N164

## Typical Characteristics (Cont'd)



## Switching Time Test Circuit

