Product Bulletin

Document #:PB25125Z
Issue Date:30 Nov 2022

Title of Change:	Update of NCV7462DQ1R2G datasheet
Effective date:	30 Nov 2022
Contact information:	Contact your local onsemi Sales Office or Jelle.Genne@onsemi.com
Type of notification:	This Product Bulletin is for notification purposes only. onsemi will proceed with implementation of this change upon publication of this Product Bulletin.
Change Category:	Information Only
Change Sub-Category(s):	Datasheet/Product Doc change

Sites Affected:

onsemi Sites	**External Foundry/Subcon Sites**
None	None

Description and Purpose:

Update of NCV7462DQ1R2G datasheet:

- All references to NCV7462DQ0R2G / NCV7462-0 removed from datasheet
- Application diagram updated
- Recommended external components list added
- Watchdog failure behavior description updated

	From	To
Datasheet	NCV7462/D, Rev. 6	NCV7462-1/D, Rev. 0

Details:

Application Diagram updated

Recommended External Components list added

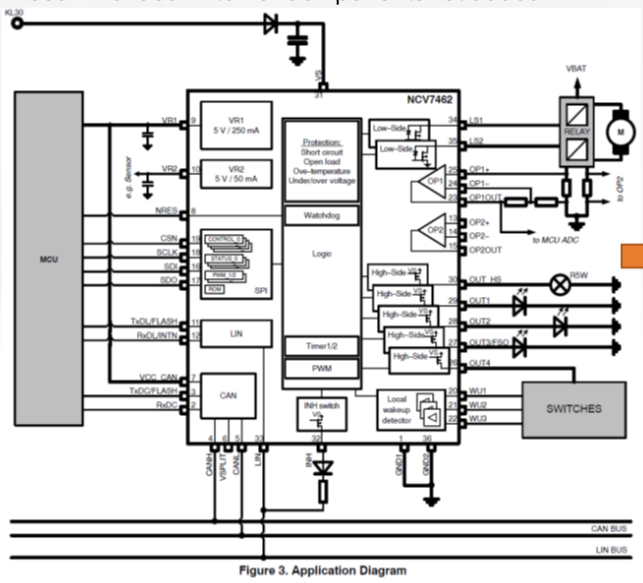

Figure 3. Application Diagram

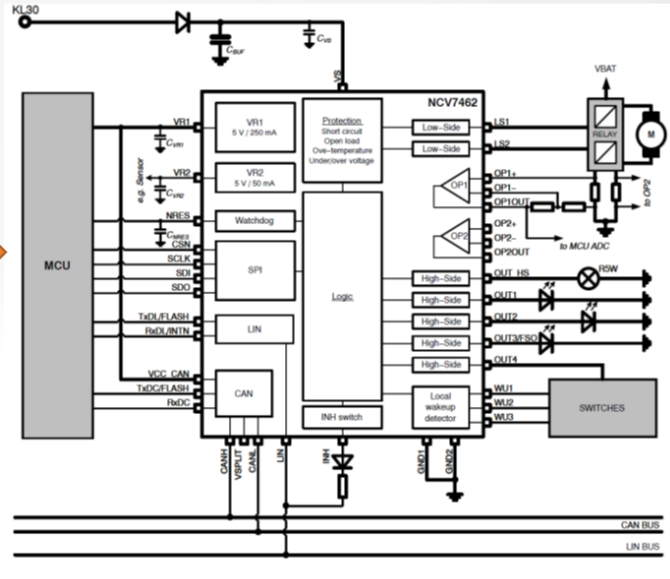

Figure 3. Application Diagram

Watchdog failure behavior description updated

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Failure: If the watchdog is not triggered correctly (trigger not sent during timeout or open window; or sent during the closed window), reset is generated on pin NRES and the “WD_TRIG” bit is reset to low. After the NRES release, the watchdog always starts in the timeout mode. Watchdog failures are counted and their number can be read from the SPI status registers. After eight watchdog failures in sequence, the VR1 regulator is switched off for 200 ms. In case of seven more watchdog failures, VR1 is completely turned off and the device goes into forced sleep mode until a wake−up occurs (e.g. via the LIN or CAN bus). First successful watchdog trigger resets the failure counter.

Failure: If the watchdog is not triggered correctly (trigger not sent during timeout or open window; or sent during the closed window), two reset pulses are generated on pin NRES and the “WD_TRIG” bit is reset to low. After the second NRES release, the watchdog always starts in the timeout mode. NRES pulses due to watchdog failures are counted and their number can be read from the SPI status registers. After four watchdog failures in sequence, the VR1 regulator is switched off for 200 ms. In case of three more watchdog failures, VR1 is completely turned off and the device goes into forced sleep mode until a wake−up occurs (e.g. via the LIN or CAN bus). First successful watchdog trigger resets the failure counter.

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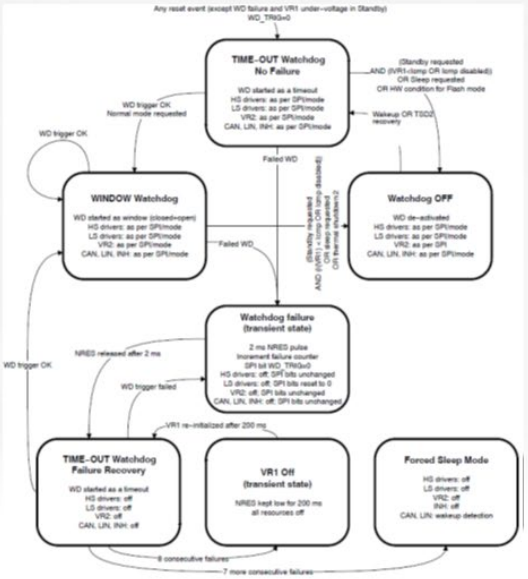

Figure 14. Watchdog Operation

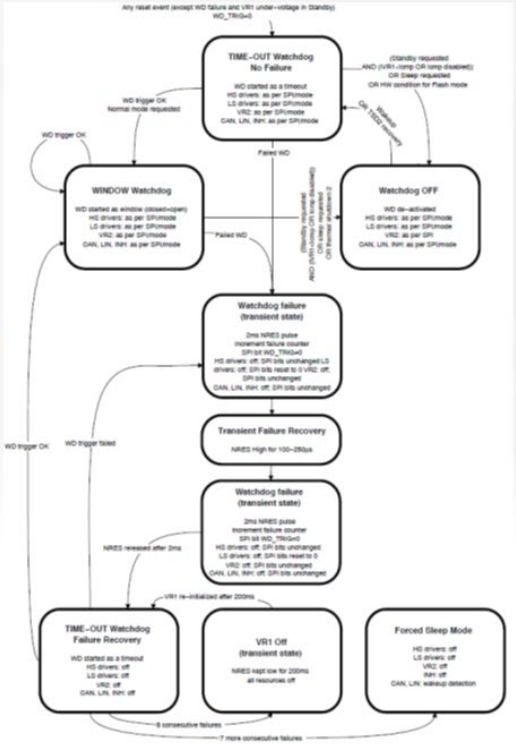

Figure 14. Watchdog Operation

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Watchdog Failure Counter	WD_CNT.[3:0]		Number of Watchdog Failures
	0	default	No watchdog failure encountered
	$1 .. $F		Non−zero number of watchdog failures encountered

Watchdog Failure Counter	WD_CNT.[3:0]		Number of NRES Pulses due to Watchdog Failure
	0	default	No watchdog failure encountered
	$1 .. $F		Non−zero number of watchdog failures encountered

List of Affected Standard Parts:

***Note**: Only the standard (off the shelf) part numbers are listed in the parts list. Any custom parts affected by this PCN are shown in the customer specific PCN addendum in the PCN email notification, or on the **PCN Customized Portal**.*

NCV7462DQ1R2G		