AVR® DB

Product Brief

Introduction

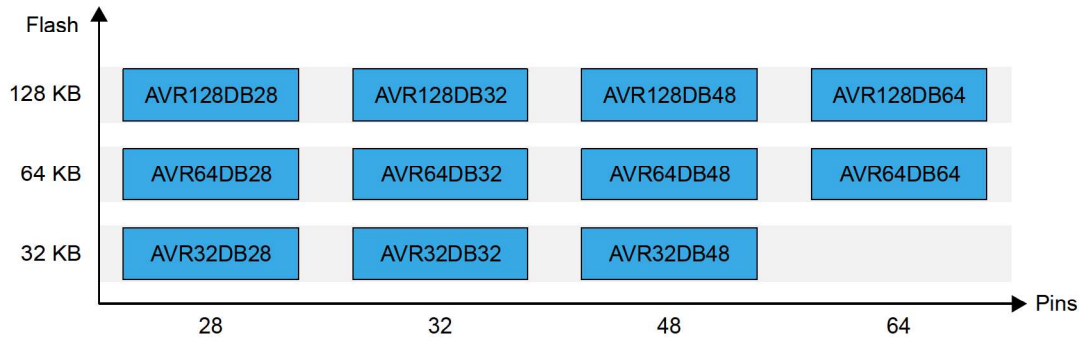
The AVR® DB Family of microcontrollers is using the AVR® CPU with hardware multiplier running at clock speeds up to 24 MHz, with up to 128 KB of Flash, 16 KB of SRAM, and 512 bytes of EEPROM in 28-, 32-, 48- or 64-pin packages. The AVR® DB Family uses the latest technologies from Microchip with a flexible and low-power architecture, including Event System, accurate analog subsystems, and advanced digital peripherals.

AVR® DB Family Overview

The figure below shows the AVR® DB Family of devices, laying out pin count variants and memory sizes:

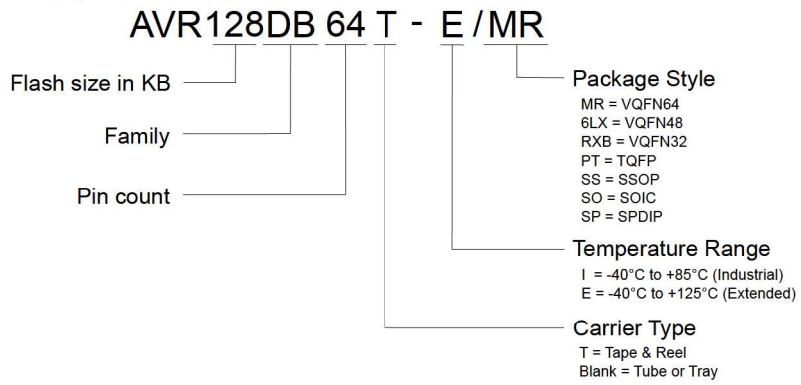
- Vertical migration is possible without code modification, as these devices are fully pin and feature compatible
- Horizontal migration to the left reduces the pin count and therefore the available features

Figure 1. AVR® DB Family Overview



The name of a device in the AVR® DB Family is decoded as follows:

Figure 2. AVR® DB Family Device Designation



Memory Overview

Table 1. Memory Overview

Devices	AVR32DB28 AVR32DB32 AVR32DB48	AVR64DB28 AVR64DB32 AVR64DB48 AVR64DB64	AVR128DB28 AVR128DB32 AVR128DB48 AVR128DB64
Flash memory	32 KB	64 KB	128 KB
SRAM	4 KB	8 KB	16 KB
EEPROM	512B	512B	512B
User row	32B	32B	32B

Peripheral Overview

Table 2. Peripheral Overview

Feature	AVR32DB28 AVR64DB28 AVR128DB28	AVR32DB32 AVR64DB32 AVR128DB32	AVR32DB48 AVR64DB48 AVR128DB48	AVR64DB64 AVR128DB64
Pins	**28**	**32**	**48**	**64**
Max. frequency (MHz)	24	24	24	24
16-bit Timer/Counter type A (TCA)	1	1	2	2
16-bit Timer/Counter type B (TCB)	3	3	4	5
12-bit Timer/Counter type D (TCD)	1	1	1	1
Real-Time Counter (RTC)	1	1	1	1
USART	3	3	5	6
SPI	2	2	2	2
TWI/I^2C	1(1)	2(1)	2(1)	2(1)
12-bit differential ADC (channels)	1 (9)	1 (13)	1 (18)	1 (22)
10-bit DAC (outputs)	1 (1)	1 (1)	1 (1)	1 (1)
Analog Comparator (AC)	3	3	3	3
Zero-Cross Detector (ZCD)	1	1	2	3
Peripheral Touch Controller (PTC)	-	-	-	-
Op amp (OP)	2	2	3	3
Configurable Custom Logic Look-up Table (CCL LUT)	4	4	6	6
Watchdog Timer (WDT)	1	1	1	1
Event System channels (EVSYS)	8	8	10	10
General Purpose I/O(2)	22/21(2)	26/25(2)	41/40(2)	55/54(2)

.....continued				
Feature	**AVR32DB28 AVR64DB28 AVR128DB28**	**AVR32DB32 AVR64DB32 AVR128DB32**	**AVR32DB48 AVR64DB48 AVR128DB48**	**AVR64DB64 AVR128DB64**
Pins	**28**	**32**	**48**	**64**
PORT	PA[7:0] PC[3:0] PD[7:1] PF[6,1,0]	PA[7:0] PC[3:0] PD[7:1] PF[6:0]	PA[7:0] PB[5:0] PC[7:0] PD[7:0] PE[3:0] PF[6:0]	PA[7:0] PB[7:0] PC[7:0] PD[7:0] PE[7:0] PF[6:0] PG[7:0]
External Interrupts	22	26	41	55
CRCSCAN	1	1	1	1
Unified Program and Debug Interface (UPDI)	1	1	1	1

Notes:

1. The TWI/I^2C can operate simultaneously as host and client on different pins.
2. PF6/$\overline{\text{RESET}}$ pin is input only.

Features

- AVR® CPU
  - Running at up to 24 MHz
  - Single-cycle I/O register access
  - Two-level interrupt controller
  - Two-cycle hardware multiplier
  - Supply voltage range: 1.8V-5.5V
- Memories
  - 32/64/128 KB In-System self-programmable Flash memory
  - 512B EEPROM
  - 4/8/16 KB SRAM
  - 32B of user row in nonvolatile memory that can keep data during chip-erase and be programmed while the device is locked
  - Write/erase endurance
    - Flash: 10,000 cycles
    - EEPROM: 100,000 cycles
  - Data retention: 40 Years at 55°C
- System
  - Power-on Reset (POR) circuit
  - Brown-out Detector (BOD) with user-programmable levels
  - Voltage Level Monitor (VLM) with interrupt at a programmable level above the BOD level
  - Clock failure detection
  - Clock options
    - High-precision internal oscillator with selectable frequency up to 24 MHz (OSCHF)
      - Auto-tuning for improved internal oscillator accuracy
    - Internal PLL up to 48 MHz for high-frequency operation of Timer/Counter type D (PLL)
    - Internal ultra-low power 32.768 kHz oscillator (OSC32K)
    - External 32.768 kHz crystal oscillator (XOSC32K)
    - External clock input
    - External high-frequency crystal oscillator (XOSCHF) with clock failure detection
  - Single pin Unified Program and Debug Interface (UPDI)
  - Three sleep modes
    - Idle with all peripherals running for immediate wake-up
    - Standby
      - Configurable operation of selected peripherals
      - SleepWalking peripherals
    - Power-Down with full data retention
- Peripherals
  - Up to two 16-bit Timer/Counters type A (TCA) with three compare channels for PWM and waveform generation
  - Up to five 16-bit Timer/Counters type B (TCB) with input capture for capture and signal measurements
  - One 12-bit PWM Timer/Counter type D (TCD) optimized for power control
  - One 16-bit Real-Time Counter (RTC) that can run from external crystal or internal oscillator
  - Up to six USARTs
    - Operation modes: RS-485, LIN client, host SPI, and IrDA
    - Fractional baud rate generator, auto-baud, and start-of-frame detection
  - Two SPIs with host/client operation modes
  - Up to two Two-Wire Interface (TWI) with dual address match
    - Independent host and client operation (Dual mode)

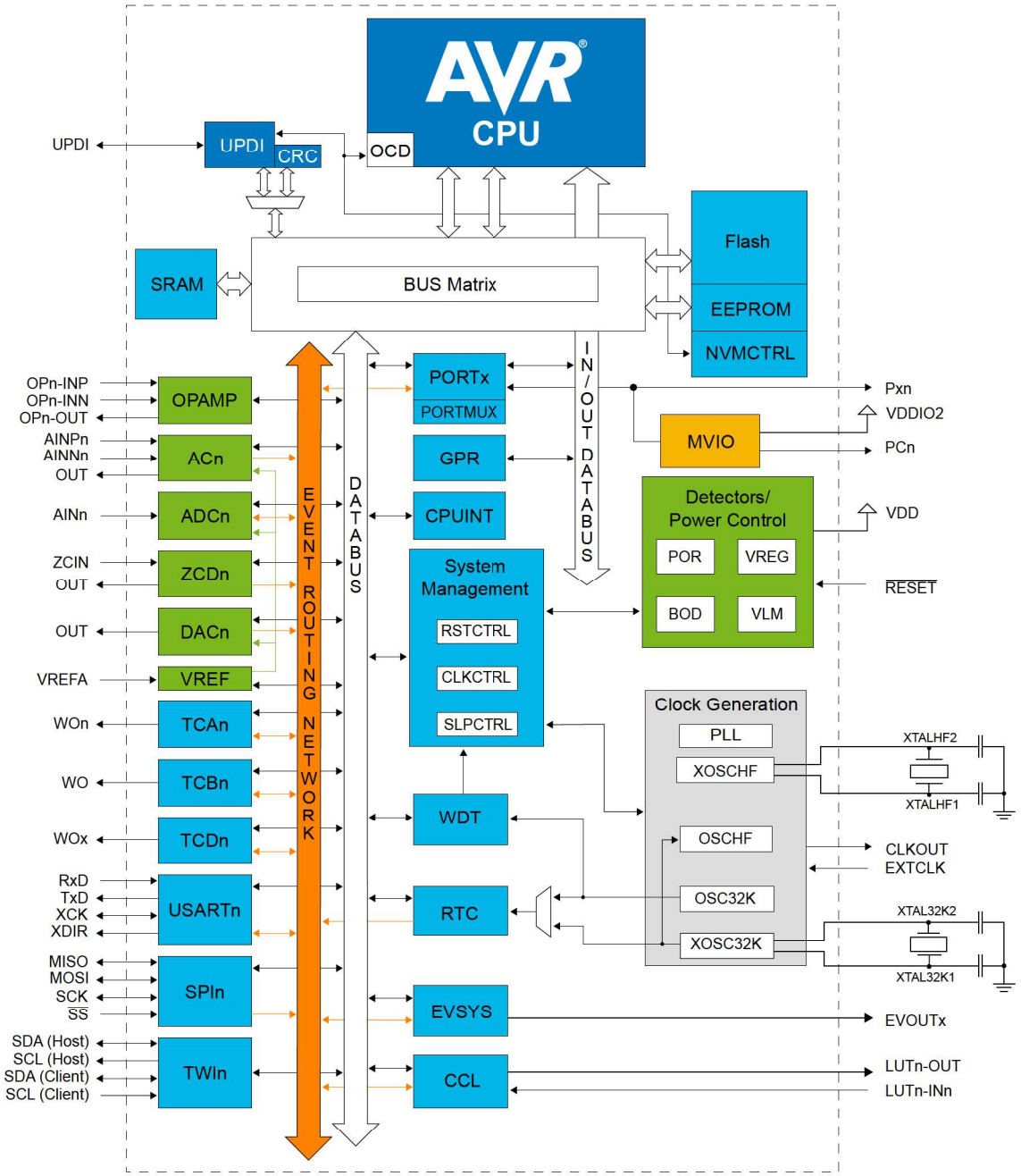
    - Phillips I²C compatible
    - Standard mode (Sm, 100 kHz)
    - Fast mode (Fm, 400 kHz)
    - Fast mode plus (Fm+, 1 MHz)(1)
  - Event System for CPU independent and predictable inter-peripheral signaling
  - Configurable Custom Logic (CCL) with up to six programmable Look-up Tables (LUTs)
  - One 12-bit 130 ksps differential Analog-to-Digital Converter (ADC)
  - Three Analog Comparators (ACs) with window compare functions
  - One 10-bit Digital-to-Analog Converter (DAC)
  - Up to three Zero-Cross Detectors (ZCDs)
  - Analog Signal Conditioning (OPAMP) peripheral with up to three op amps, each with an internal resistor ladder that allows for many useful configurations with no external components
  - Multiple voltage references (VREF)
    - 1.024V
    - 2.048V
    - 2.500V
    - 4.096V
    - External Voltage Reference (VREFA)
    - Supply Voltage (V_{DD})
  - Automated Cyclic Redundancy Check (CRC) Flash program memory scan
  - Watchdog Timer (WDT) with Window mode, and separate on-chip oscillator
  - External interrupt on all general purpose pins
- I/O and Packages:
  - Multi-Voltage I/O (MVIO) on I/O port C
  - Selectable input voltage threshold
  - Up to 55/54 programmable I/O pins
  - 28-pin SSOP, SOIC and SPDIP
  - 32-pin VQFN 5x5 mm and TQFP 7x7 mm
  - 48-pin VQFN 5x5 mm and TQFP 7x7 mm
  - 64-pin VQFN 9x9 mm and TQFP 10x10 mm
- Temperature Ranges
  - Industrial: -40°C to 85°C
  - Extended: -40°C to 125°C

Note:

1. I²C Fm+ is only supported for supply voltage V_{DD} above 2.7 VDC.

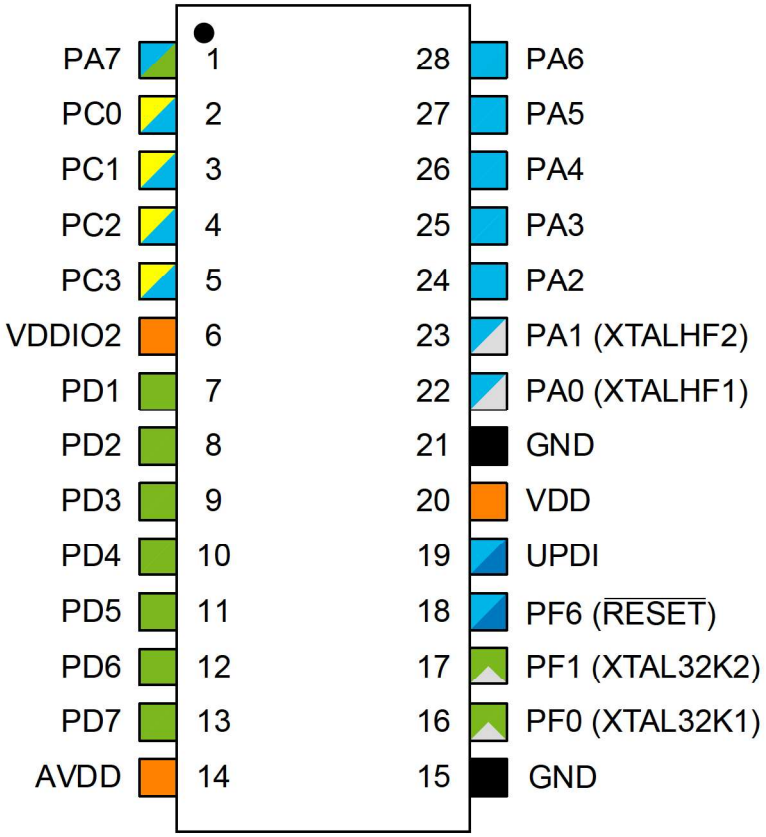
Table of Contents

1. Block Diagram



2. Pinout

2.1 28-pin SSOP, SOIC and SPDIP



Note: For the AVR® DB Family of devices, AVDD is internally connected to VDD (not separate power domains).

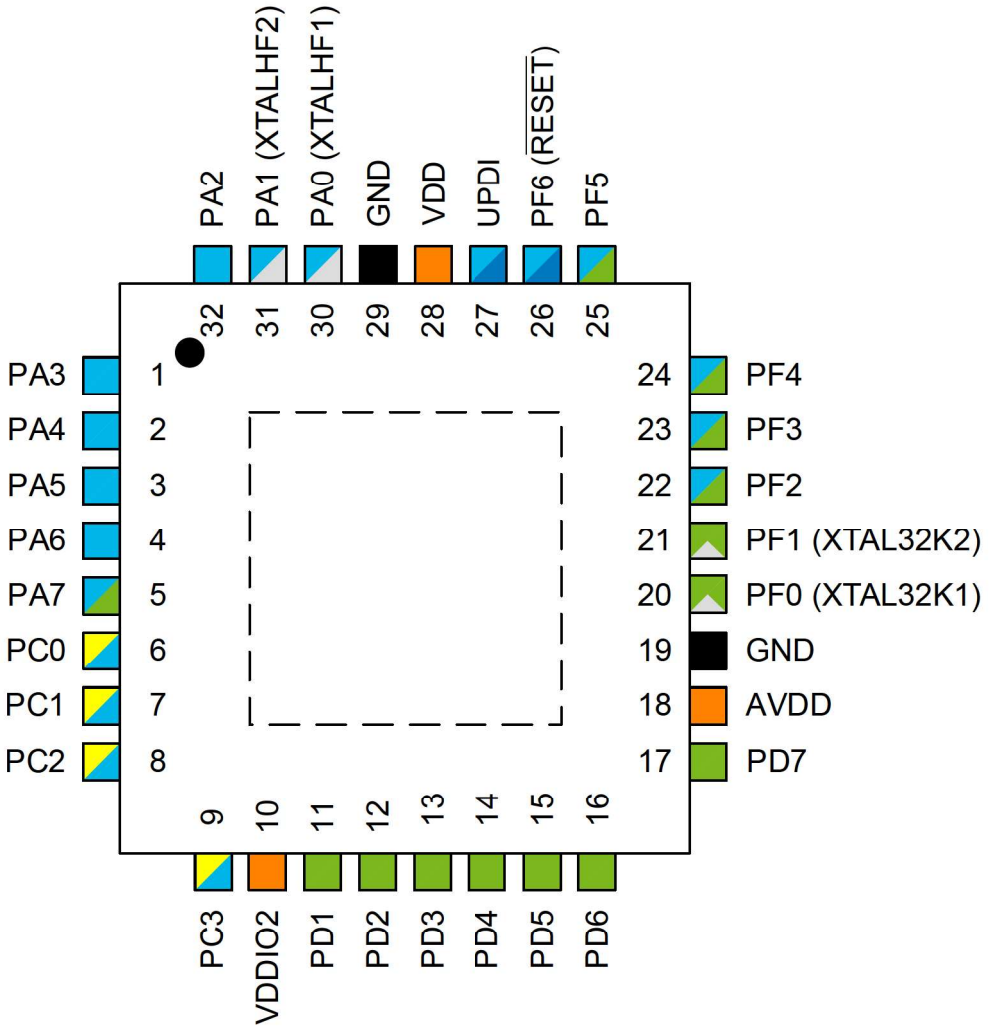
Power

- Power Supply
- Ground
- Pin on VDD Power Domain
- Pin on AVDD Power Domain
- Pin on VDDIO2 Power Domain

Functionality

- Programming/Debug
- Clock/Crystal
- Digital Function Only
- Analog Function

2.2 32-pin VQFN and TQFP



Note: For the AVR® DB Family of devices, AVDD is internally connected to VDD (not separate power domains).

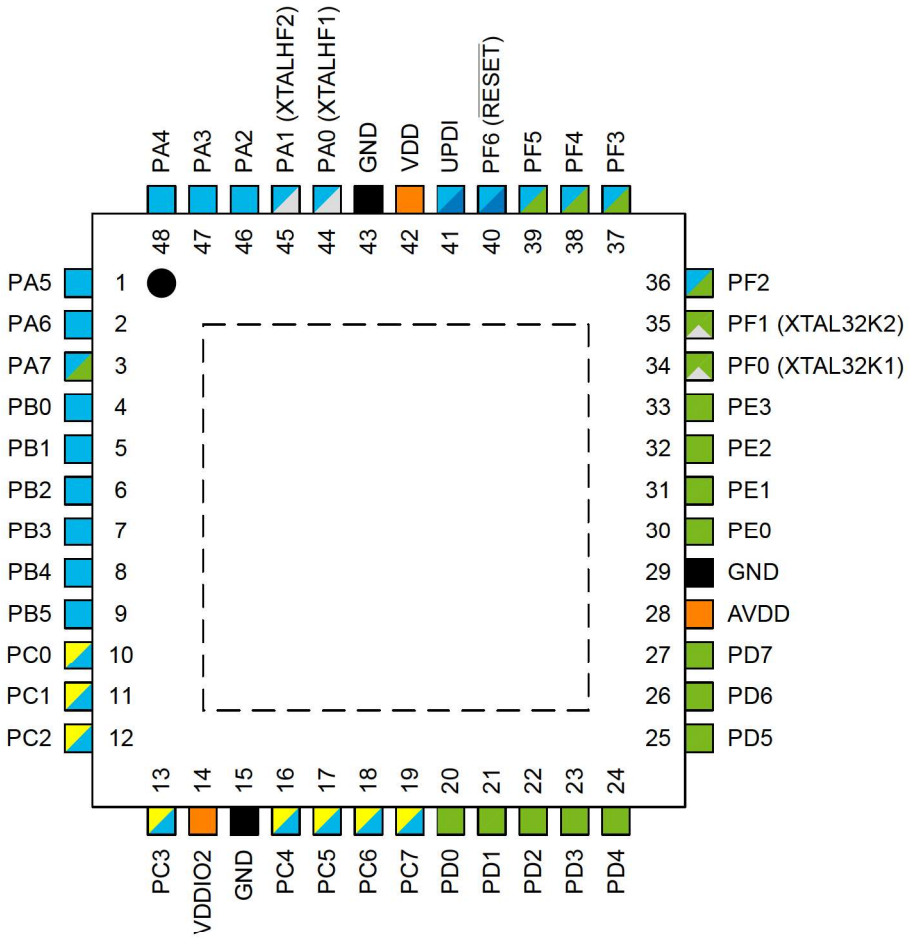
Power

- Power Supply
- Ground
- Pin on VDD Power Domain
- Pin on AVDD Power Domain
- Pin on VDDIO2 Power Domain

Functionality

- Programming/Debug
- Clock/Crystal
- Digital Function Only
- Analog Function

2.3 48-pin VQFN and TQFP



Note: For the AVR® DB Family of devices, AVDD is internally connected to VDD (not separate power domains).

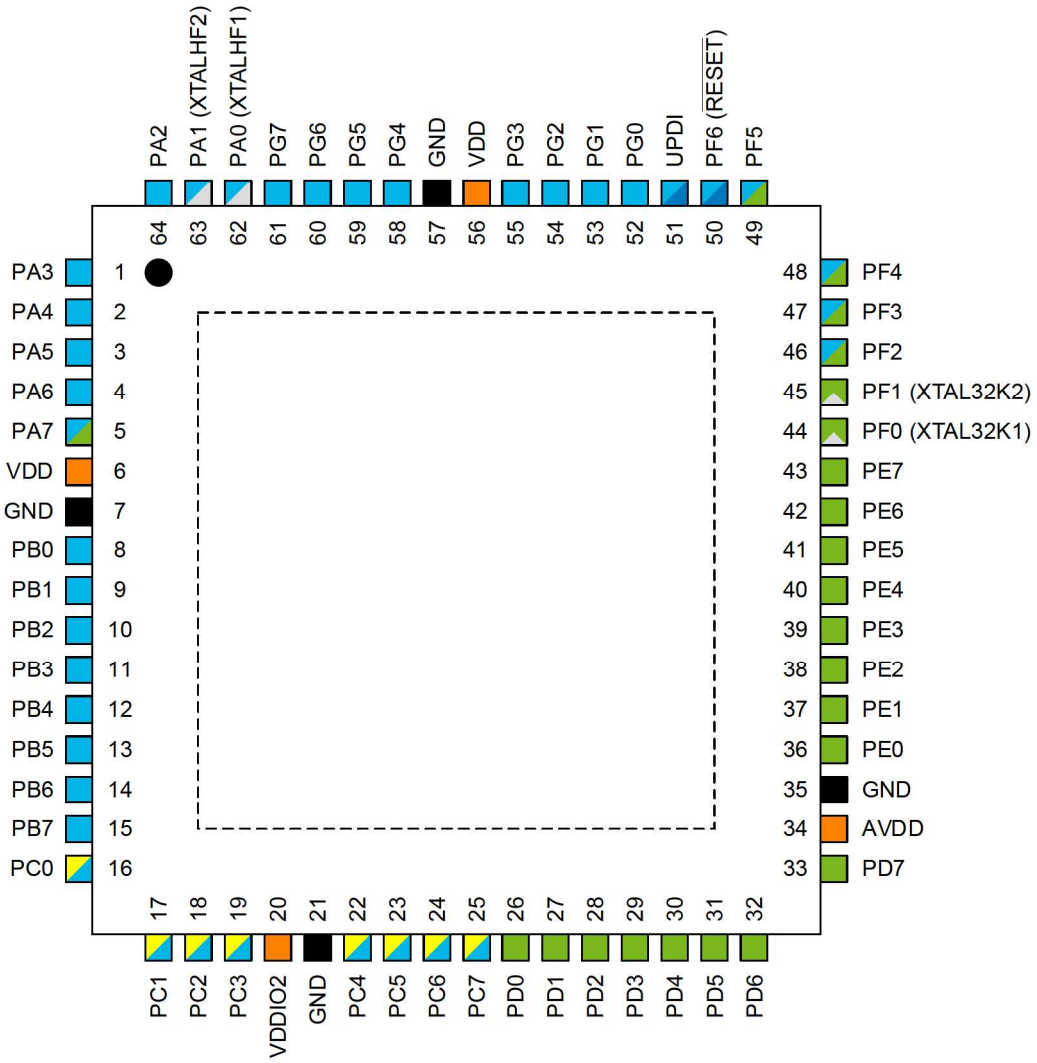
Power

- Power Supply
- Ground
- Pin on VDD Power Domain
- Pin on AVDD Power Domain
- Pin on VDDIO2 Power Domain

Functionality

- Programming/Debug
- Clock/Crystal
- Digital Function Only
- Analog Function

2.4 64-pin VQFN and TQFP



Note: For the AVR® DB Family of devices, AVDD is internally connected to VDD (not separate power domains).

Power

- Power Supply
- Ground
- Pin on VDD Power Domain
- Pin on AVDD Power Domain
- Pin on VDDIO2 Power Domain

Functionality

- Programming/Debug
- Clock/Crystal
- Digital Function Only
- Analog Function

3. I/O Multiplexing and Considerations

3.1 I/O Multiplexing

VQFN64/ TQFP64	VQFN48/ TQFP48	VQFN32/ TQFP32	SOIC28/ SSOP28/SPDIP28	Pin name(1,2)	Special	ADC0	ACn	DAC0	OPAMP	ZCDn	USARTn	SPIn	TWIn(4)	TCAn	TCBn	TCD0	EVSYS	CCL
62	44	30	22	PA0	XTALHF1 EXTCLK						0, TxD			0, WO0				LUT0, IN0
63	45	31	23	PA1	XTALHF2						0, RxD			0, WO1				LUT0, IN1
64	46	32	24	PA2	TWI Fm+						0, XCK		0, SDA(HC)	0, WO2	0, WO		EVOUTA	LUT0, IN2
1	47	1	25	PA3	TWI Fm+						0, XDIR		0, SCL(HC)	0, WO3	1, WO			LUT0, OUT
2	48	2	26	PA4							0, TxD(3)	0, MOSI		0, WO4		WOA		
3	1	3	27	PA5							0, RxD(3)	0, MISO		0, WO5		WOB		
4	2	4	28	PA6							0, XCK(3)	0, SCK				WOC		LUT0, OUT(3)
5	3	5	1	PA7	CLKOUT		0, OUT 1, OUT 2, OUT			0, OUT 1, OUT 2, OUT	0, XDIR(3)	0, $\overline{SS}$				WOD	EVOUTA(3)	
6				VDD														
7				GND														
8	4			PB0							3, TxD			0, WO0(3) 1, WO0				LUT4, IN0
9	5			PB1							3, RxD			0, WO1(3) 1, WO1				LUT4, IN1
10	6			PB2	TWI						3, XCK		1, SDA(HC) (3)	0, WO2(3) 1, WO2			EVOUTB	LUT4, IN2
11	7			PB3	TWI						3, XDIR		1, SCL(HC) (3)	0, WO3(3) 1, WO3				LUT4, OUT
12	8			PB4							3, TxD(3)	1, MOSI(3)		0, WO4(3) 1, WO4	2, WO(3)	WOA(3)		
13	9			PB5							3, RxD(3)	1, MISO(3)		0, WO5(3) 1, WO5	3, WO	WOB(3)		
14				PB6							3, XCK(3)	1, SCK(3)	1, SDA(C) (3)			WOC(3)		LUT4, OUT(3)
15				PB7							3, XDIR(3)	1, $\overline{SS}$(3)	1, SCL(C)(3)			WOD(3)	EVOUTB(3)	
16	10	6	2	PC0							1, TxD	1, MOSI		0, WO0(3)	2, WO			LUT1, IN0
17	11	7	3	PC1							1, RxD	1, MISO		0, WO1(3)	3, WO(3)			LUT1, IN1
18	12	8	4	PC2	TWI Fm+						1, XCK	1, SCK	0, SDA(HC) (3)	0, WO2(3)			EVOUTC	LUT1, IN2
19	13	9	5	PC3	TWI Fm+						1, XDIR	1, $\overline{SS}$	0, SCL(HC) (3)	0, WO3(3)				LUT1, OUT
20	14	10	6	VDDIO2														
21	15			GND														
22	16			PC4							1, TxD(3)	1, MOSI(3)		0, WO4(3) 1, WO0(3)				
23	17			PC5							1, RxD(3)	1, MISO(3)		0, WO5(3) 1, WO1(3)				
24	18			PC6			0, OUT(3) 1, OUT(3) 2, OUT(3)				1, XCK(3)	1, SCK(3)	0, SDA(C) (3)	1, WO2(3)				LUT1, OUT(3)

.....continued

VQFN64/ TQFP64	VQFN48/ TQFP48	VQFN32/ TQFP32	SOIC28/ SSOP28/SPDIP28	Pin name(1,2)	Special	ADC0	ACn	DAC0	OPAMP	ZCDn	USARTn	SPIn	TWIn(4)	TCAn	TCBn	TCD0	EVSYS	CCL
25	19			PC7						0, OUT(3) 1, OUT(3) 2, OUT(3)	1, XDIR(3)	1, SS(3)	0, SCL(C)(3)				EVOUTC(3)	
26	20			PD0		AIN0	0, AINN1 1, AINN1 2, AINN1							0, WO0(3)				LUT2, IN0
27	21	11	7	PD1		AIN1			OP0, INP	0, ZCIN				0, WO1(3)				LUT2, IN1
28	22	12	8	PD2		AIN2	0, AINP0 1, AINP0 2, AINP0		OP0, OUT					0, WO2(3)			EVOUTD	LUT2, IN2
29	23	13	9	PD3		AIN3	0, AINN0 1, AINP1		OP0, INN					0, WO3(3)				LUT2, OUT
30	24	14	10	PD4		AIN4	1, AINP2 2, AINP1		OP1, INP					0, WO4(3)				
31	25	15	11	PD5		AIN5	1, AINN0		OP1, OUT					0, WO5(3)				
32	26	16	12	PD6		AIN6	0, AINP3 1, AINP3 2, AINP3	OUT										LUT2, OUT(3)
33	27	17	13	PD7	VREFA	AIN7	0, AINN2 1, AINN2 2, AINN0/ AINN2		OP1, INN								EVOUTD(3)	
34	28	18	14	AVDD														
35	29	19	15	AGND														
36	30			PE0		AIN8	0, AINP1				4, TxD	0, MOSI(3)		0, WO0(3)				
37	31			PE1		AIN9	2, AINP2		OP2, INP		4, RxD	0, MISO(3)		0, WO1(3)				
38	32			PE2		AIN10	0, AINP2		OP2, OUT		4, XCK	0, SCK(3)		0, WO2(3)			EVOUTE	
39	33			PE3		AIN11			OP2, INN	1, ZCIN	4, XDIR	0, SS(3)		0, WO3(3)				
40				PE4		AIN12					4, TxD(3)			0, WO4(3) 1, WO0(3)				
41				PE5		AIN13					4, RxD(3)			0, WO5(3) 1, WO1(3)				
42				PE6		AIN14					4, XCK(3)			1, WO2(3)				
43				PE7		AIN15				2, ZCIN	4, XDIR(3)						EVOUTE(3)	
44	34	20	16	PF0	XTAL32K1	AIN16(5)					2, TxD			0, WO0(3)		WOA(3)		LUT3, IN0
45	35	21	17	PF1	XTAL32K2	AIN17(5)					2, RxD			0, WO1(3)		WOB(3)		LUT3, IN1
46	36	22		PF2	TWI Fm+	AIN18(5)					2, XCK		1, SDA(HC)	0, WO2(3)		WOC(3)	EVOUTF	LUT3, IN2
47	37	23		PF3	TWI Fm+	AIN19(5)					2, XDIR		1, SCL(HC)	0, WO3(3)		WOD(3)		LUT3, OUT
48	38	24		PF4		AIN20(5)					2, TxD(3)			0, WO4(3)	0, WO(3)			
49	39	25		PF5		AIN21(5)					2, RxD(3)			0, WO5(3)	1, WO(3)			
50	40	26	18	PF6(6)	RESET													
51	41	27	19	UPDI	UPDI													

.....continued

VQFN64/ TQFP64	VQFN48/ TQFP48	VQFN32/ TQFP32	SOIC28/ SSOP28/SPDIP28	Pin name[1,2]	Special	ADC0	ACn	DAC0	OPAMP	ZCDn	USARTn	SPIn	TWIn[4]	TCAn	TCBn	TCD0	EVSYS	CCL
52				PG0							5, TxD			0, WO0[3] 1, WO0[3]				LUT5, IN0
53				PG1							5, RxD			0, WO1[3] 1, WO1[3]				LUT5, IN1
54				PG2							5, XCK			0, WO2[3] 1, WO2[3]			EVOUTG	LUT5, IN2
55				PG3							5, XDIR			0, WO3[3] 1, WO3[3]	4, WO			LUT5, OUT
56	42	28	20	VDD														
57	43	29	21	GND														
58				PG4							5, TxD[3]	0, MOSI[3]		0, WO4[3] 1, WO4[3]		WOA[3]		
59				PG5							5, RxD[3]	0, MISO[3]		0, WO5[3] 1, WO5[3]		WOB[3]		
60				PG6							5, XCK[3]	0, SCK[3]				WOC[3]		LUT5, OUT[3]
61				PG7							5, XDIR[3]	0, $\overline{SS}$[3]				WOD[3]	EVOUTG[3]	

Notes:

1. Pin names are of type P*xn*, with *x* being the PORT instance (A, B, C, ...) and *n* the pin number. Notation for signals is PORT*x*_PIN*n*. All pins can be used as event inputs.
2. All pins can be used for external interrupt, where pins P*x*2 and P*x*6 of each port have full asynchronous detection.
3. Alternative pin positions.
4. TWI pins are marked *HC* if they can be used as TWI Host or Client pins, and *C* if they can only be used as TWI Client pins.
5. AIN16 - AIN21 cannot be used as a negative ADC input for differential measurements.
6. Input only.

4. Product Brief Revision History

Note: The product brief revision is independent of the die revision and the device variant (last letter of the ordering number).

4.1 Revision History

Doc. Rev.	Date	Comments
B	10/2020	Updated the document to include the latest data sheet updates
A	11/2019	Initial release

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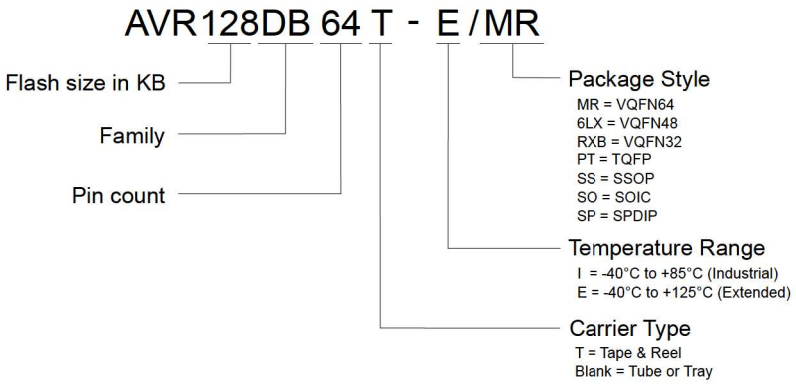

Note: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
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