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NTE74180
Integrated Circuit
TTL – 9–Bit Odd/Even Parity Generator/Checker

Description:

The NTE74180 is a universal, monolithic, 9–bit (8 data bits plus 1 parity bit) parity generator/checker in a 14–Lead plastic DIP type package that utilizes familiar Series 74 TTL circuitry and features odd/even outputs and control inputs to facilitate operations in either odd or even–parity applications. Depending on whether even or odd parity is being generated or checked, the even or odd inputs can be utilized as the parity or 9th–bit input. The word length capability is easily expanded by cascading.

The NTE74180 is fully compatible with other TTL or DTL circuits. Input buffers are provided so that each data input represents only one normalized Series 74 load. A full fan–out to 10 normalized Series 74 load is available from each of the outputs ta a low logic level. A fan–out to 20 normalized loads is provided at a high logic level to facilitate the connection of unused inputs to used inputs. Typical power dissipation is 170mW.

Absolute Maximum Ratings: (Note 1)

Supply Voltage, V_{CC} 7V
DC Input Voltage, V_{IN} 5.5V
Operating Temperature Range, T_A . . . . . 0°C to +70°C
Storage Temperature Range, T_{stg} . . . . . –65°C to +150°C

Note 1. Voltage values are with respect to network ground terminal.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
High–Level Output Current	I_{OH}	–	–	–800	μA
Low–Level Output Current	I_{OL}	–	–	16	mA
Operating Temperature Range	T_A	0	–	+70	°C

Electrical Characteristics: (Note 2, Note 3)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
High−Level Input Voltage	V_{IH}			2	–	–	V
Low−Level Input Voltage	V_{IL}			–	–	0.8	V
Input Clamp Voltage	V_{IK}	V_{CC} = MIN, I_I = −12mA		–	–	−1.5	V
High−Level Output Voltage	V_{OH}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −800μA		2.4	3.3	–	V
Low−Level Output Voltage	V_{OL}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16mA		–	0.2	0.4	V
Input Current	I_I	V_{CC} = MAX, V_I = 5.5V		–	–	1	mA
High−Level Input Current	I_{IH}	V_{CC} = MAX, V_I = 2.4V	Any Data Input	–	–	40	μA
			Even or Odd Input	–	–	80	μA
Low−Level Input Current	I_{IL}	V_{CC} = MAX, V_I = 0.4V	Any Data Input	–	–	−1.6	mA
			Even or Odd Input	–	–	−3.2	mA
Short−Circuit Output Current	I_{OS}	V_{CC} = MAX, Note 5		−18	–	−55	mA
Supply Current	I_{CC}	V_{CC} = MAX, Note 6		–	34	56	mA

Note 2. .For conditions shown as MIN or MAX, use the appropriate value specified under “Recommended Operation Conditions”.

Note 3. All typical values are at V_{CC} = 5V, T_A = +25°C.

Note 4. Not more than one output should be shorted at a time.

Note 5. I_{CC} is measured with even and odd inputs at 4.5V, all other inputs and outputs open.

Switching Characteristics: (V_{CC} = 5V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Propagation Delay Time (From Data Input to Σ Even Output)	t_{PLH}	R_L = 400Ω, C_L = 15pF, Odd Input Grounded	–	40	60	ns
	t_{PHL}		–	45	68	ns
Propagation Delay Time (From Data Input to Σ Odd Output)	t_{PLH}		–	32	48	ns
	t_{PHL}		–	25	38	ns
Propagation Delay Time (From Data Input to Σ Even Output)	t_{PLH}	R_L = 400Ω, C_L = 15pF, Even Input Grounded	–	32	48	ns
	t_{PHL}		–	25	38	ns
Propagation Delay Time (From Data Input to Σ Odd Output)	t_{PLH}		–	40	60	ns
	t_{PHL}		–	45	68	ns
Propagation Delay Time (From Seven or Odd Input to Σ Even or Σ Odd Output)	t_{PLH}	R_L = 400Ω, C_L = 15pF	–	13	20	ns
	t_{PHL}		–	7	10	ns

Function Table:

Inputs			Outputs	
Σ of H's at A thru H	**Even**	**Odd**	**Σ Even**	**Σ Odd**
Even	H	L	H	L
Odd	H	L	L	H
Even	L	H	L	H
Odd	L	H	H	L
X	H	H	L	L
X	L	L	H	H

H = High Level
L = Low Level
X = Irrelevant

Pin Connection Diagram