swissbit®

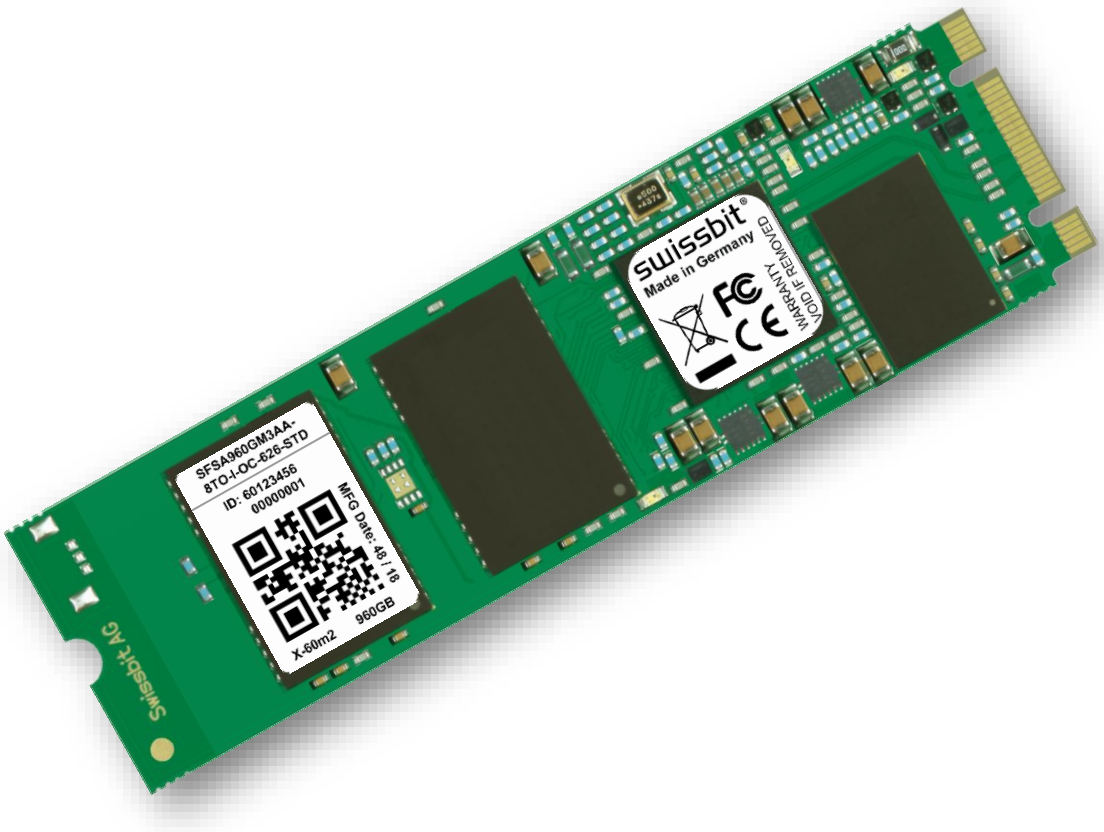
Product Data Sheet

# Industrial M.2 SATA SSD

## X-60m2 Series

**SATA III - 6.0 Gbit/s**

Standard and Industrial Temperature Grade




made in germany

# Contents

# X-60m2 Series – Industrial M.2 Solid State Drive 30 GBytes up to 960 GBytes (PCI Express™ M.2)

## 1. Product Summary

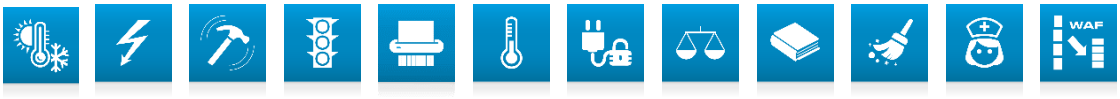
- **Capacities:**
  - 2280: 30 GBytes, 60 GBytes, 120 GBytes, 240 GBytes, 480 GBytes, 960 GBytes
  - 2260: 30 GBytes, 60 GBytes, 120 GBytes, 240 GBytes, 480 GBytes
  - 2242: 30 GBytes, 60 GBytes, 120 GBytes, 240 GBytes
- **Form Factors:**
  - 2280: PCI Express M.2 (2280) (80 mm x 22 mm x 3.3mm)
  - 2260: PCI Express M.2 (2260) (60 mm x 22 mm x 3.3 mm)
  - 2242: PCI Express M.2 (2242) (42 mm x 22 mm x 3.3 mm)
- **Compliance:** SATA Rev 3.1 – 6 Gbit/s (3 Gbit/s and 1.5 Gbit/s backward compatible)
- **Command Sets:** Supports ATA/ATAPI-8 and ACS-2 (2011/06/22)
- **Performance:**
  - Burst Transfer Rate: Up to 600 MBytes/s in SATA III – 6.0 Gbit/s
  - Read Performance: Sequential Read up to 520 MBytes/s, Random Read IOPs up to 75,000
  - Write Performance: Sequential Write up to 460 MB/s, Random Write IOPs up to 75,000
- **Operating Temperature Range[1]:**
  - Commercial: 0 °C to 70 °C
  - Industrial: -40 °C to 85 °C
- **Storage Temperature Range:** -40 °C to 85 °C
- **Operating Voltage:** 3.3 V ± 5%
- **Power (Max Capacity):**
  - Read (Active): 1.6 W
  - Write (Active): 3.4 W
  - Idle: 415 mW
  - Slumber: 115 mW
- **Data Retention:** 10 Years @ Life Begin; 1 Year @ Life End
- **Endurance:** TeraBytes Written (TBW) @ Max Capacity[2]
  - Client > 2165
  - Embedded > 595
  - Enterprise > 555
- **Shock/Vibration:** 1,500 *g* / 50 *g*
- **High-Performance 32-Bit Processor with Integrated, Parallel Flash Interface Engines:**
  - Multi-Level (MLC) NAND Flash
  - Hardware BCH Code ECC (up to 66 bit correction per 1 KByte page)
- **High Reliability:**
  - Mean Time Between Failure (MTBF): > 2,000,000 hours
  - Data Reliability: < 1 non-recoverable error per $10^{16}$ bits read

[1] Adequate airflow is required to ensure the drive temperature, as reported in the S.M.A.R.T. data, does not exceed the specified maximum operating temperature.

[2] According to JEDEC (JESD47I), the time to write the full TBW is 18 months. Higher average daily data volume reduces the specified TBW.

# 2. Product Features

- Best-in-Class Performance and Endurance with durabit™ Technology
- Dynamic and Static Wear Leveling
- Subpage Mode Flash Translation Layer (FTL)
- Data Care Management
  - Active: Adaptive Read Refresh
  - Passive: Background Media Scan
- Lifetime Enhancements
  - Dynamic Bad Block Remapping
  - Write Amplification Reduction
- On-Board Power Fail Protection
- AHCI, TRIM, and NCQ Support
- ATA Security Feature Set Support
- DEVSLP Compatible
- In-Field Firmware Update
- Enterprise-Grade Self-Monitoring, Analysis, and Reporting Technology (S.M.A.R.T.)
- 30 µinch Gold-Plated Connector (IPC-6012B Class 2 Compliant)
- Life Cycle Management
- Controlled "Locked" BOM
- RoHS-6 Compliant
- AES256 Encryption (on request)
- Swissbit Life Time Monitoring (SBLTM) Tool and SDK for SBLTM (on request)



# 3. Ordering Information

**Table 1: Standard Product List**

| Capacity | 2280 | 2260 | 2242 |
|---|---|---|---|
| 30 GBytes | SFSA030GMxAA1T0-t-LB-5y6-STD | SFSA030GMxAA1T0-t-LB-4y6-STD | SFSA030GMxAA1T0-t-LB-2y6-STD |
| 60 GBytes | SFSA060GMxAA2T0-t-LB-5y6-STD | SFSA060GMxAA2T0-t-LB-4y6-STD | SFSA060GMxAA2T0-t-LB-2y6-STD |
| 120 GBytes | SFSA120GMxAA4T0-t-LB-6y6-STD | SFSA120GMxAA4T0-t-LB-4y6-STD | SFSA120GMxAA2T0-t-HC-2y6-STD |
| 240 GBytes | SFSA240GMxAA4T0-t-HC-6y6-STD | SFSA240GMxAA4T0-t-HC-4y6-STD | SFSA240GMxAA2T0-t-0C-2y6-STD |
| 480 GBytes | SFSA480GMxAA4T0-t-0C-6y6-STD | SFSA480GMxAA4T0-t-0C-4y6-STD | Not Available |
| 960 GBytes | SFSA960GMxAA8T0-t-0C-6y6-STD | Not Available | Not Available |

x = product generation; t = temperature; y = firmware revision

**Table 2: Part Numbers Available for Ordering**

| FW SBR11015 | | | |
|---|---|---|---|
| **Commercial Temperature** | | | |
| **Capacity** | **2280** | **2260** | **2242** |
| 30 GBytes | SFSA030GM1AA1T0-C-LB-516-STD | SFSA030GM1AA1T0-C-LB-416-STD | SFSA030GM1AA1T0-C-LB-216-STD |
| 60 GBytes | SFSA060GM1AA2T0-C-LB-516-STD | SFSA060GM1AA2T0-C-LB-416-STD | SFSA060GM1AA2T0-C-LB-216-STD |
| 120 GBytes | SFSA120GM1AA4T0-C-LB-616-STD | SFSA120GM1AA4T0-C-LB-416-STD | SFSA120GM1AA2T0-C-HC-216-STD |
| 240 GBytes | SFSA240GM1AA4T0-C-HC-616-STD | SFSA240GM1AA4T0-C-HC-416-STD | SFSA240GM1AA2T0-C-0C-216-STD |
| 480 GBytes | SFSA480GM1AA4T0-C-0C-616-STD | SFSA480GM1AA4T0-C-0C-416-STD | Not Available |
| 960 GBytes | SFSA960GM3AA8T0-C-0C-626-STD | Not Available | Not Available |
| **Industrial Temperature** | | | |
| **Capacity** | **2280** | **2260** | **2242** |
| 30 GBytes | SFSA030GM1AA1T0-I-LB-516-STD | SFSA030GM1AA1T0-I-LB-416-STD | SFSA030GM1AA1T0-I-LB-216-STD |
| 60 GBytes | SFSA060GM1AA2T0-I-LB-516-STD | SFSA060GM1AA2T0-I-LB-416-STD | SFSA060GM1AA2T0-I-LB-216-STD |
| 120 GBytes | SFSA120GM1AA4T0-I-LB-616-STD | SFSA120GM1AA4T0-I-LB-416-STD | SFSA120GM1AA2T0-I-HC-216-STD |
| 240 GBytes | SFSA240GM1AA4T0-I-HC-616-STD | SFSA240GM1AA4T0-I-HC-416-STD | SFSA240GM1AA2T0-I-0C-216-STD |
| 480 GBytes | SFSA480GM1AA4T0-I-0C-616-STD | SFSA480GM1AA4T0-I-0C-416-STD | Not Available |
| 960 GBytes | SFSA960GM3AA8T0-I-0C-626-STD | Not Available | Not Available |

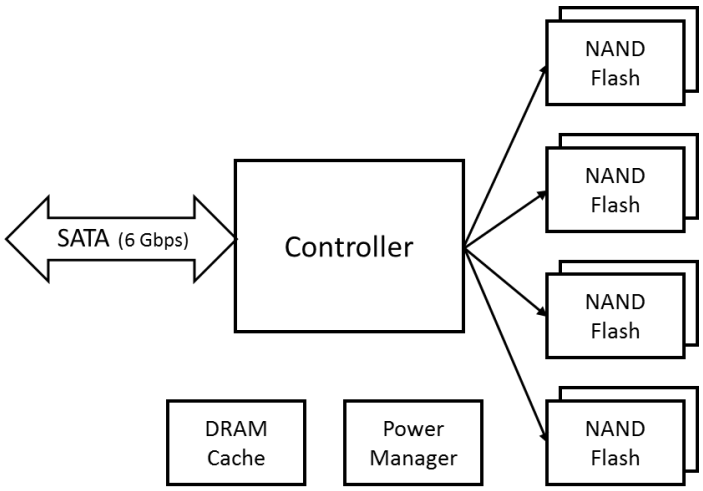
| FW SBR13056 | | | |
|---|---|---|---|
| **Commercial Temperature** | | | |
| **Capacity** | **2280** | **2260** | **2242** |
| 960 GBytes | SFSA960GM3AA8T0-C-0C-626-STD | Not Available | Not Available |
| **Industrial Temperature** | | | |
| **Capacity** | **2280** | **2260** | **2242** |
| 960 GBytes | SFSA960GM3AA8T0-I-0C-626-STD | Not Available | Not Available |

| FW SBR12055 | | | |
|---|---|---|---|
| **Commercial Temperature** | | | |
| **Capacity** | **2280** | **2260** | **2242** |
| 30 GBytes | SFSA030GM3AA1T0-C-LB-526-STD | SFSA030GM3AA1T0-C-LB-326-STD | SFSA030GM3AA1T0-C-LB-126-STD |
| 60 GBytes | SFSA060GM3AA2T0-C-LB-526-STD | SFSA060GM3AA2T0-C-LB-326-STD | SFSA060GM3AA2T0-C-LB-226-STD |
| 120 GBytes | SFSA120GM3AA4T0-C-LB-626-STD | SFSA120GM3AA4T0-C-LB-426-STD | SFSA120GM3AA2T0-C-HC-226-STD |
| 240 GBytes | SFSA240GM3AA4T0-C-HC-626-STD | SFSA240GM3AA4T0-C-HC-426-STD | SFSA240GM3AA2T0-C-OC-226-STD |
| 480 GBytes | SFSA480GM3AA4T0-C-OC-626-STD | SFSA480GM3AA4T0-C-OC-426-STD | Not Available |
| 960 GBytes | Not Available | Not Available | Not Available |
| **Industrial Temperature** | | | |
| **Capacity** | **2280** | **2260** | **2242** |
| 30 GBytes | SFSA030GM3AA1T0-I-LB-526-STD | SFSA030GM3AA1T0-I-LB-326-STD | SFSA030GM3AA1T0-I-LB-126-STD |
| 60 GBytes | SFSA060GM3AA2T0-I-LB-526-STD | SFSA060GM3AA2T0-I-LB-326-STD | SFSA060GM3AA2T0-I-LB-226-STD |
| 120 GBytes | SFSA120GM3AA4T0-I-LB-626-STD | SFSA120GM3AA4T0-I-LB-426-STD | SFSA120GM3AA2T0-I-HC-226-STD |
| 240 GBytes | SFSA240GM3AA4T0-I-HC-626-STD | SFSA240GM3AA4T0-I-HC-426-STD | SFSA240GM3AA2T0-I-OC-226-STD |
| 480 GBytes | SFSA480GM3AA4T0-I-OC-626-STD | SFSA480GM3AA4T0-I-OC-426-STD | Not Available |
| 960 GBytes | Not Available | Not Available | Not Available |

# 4. Product Description

The Swissbit® X-60m2 Solid State Drive (SSD) leverages the M.2 standard (formerly known as NGFF), which defines a variety of optional board sizes, and the connector supports both SATA and PCIe electrical interfaces. The SATA Gen III controller and Multi-Level Cell (MLC) NAND flash technology provides a robust, non-volatile storage solution for today's embedded computing applications. A functional block diagram of the X-60m2 SSD is provided below in Figure 1.

**Figure 1: X-60m2 Functional Block Diagram**




The X-60m2 SSD incorporates a 75-position edge connector with B and M keys to support host read/write, control, and power activity per the applicable JEDEC and SATA IO specifications[3].

The on-board SATA III controller manages the interface between the host and the non-volatile NAND flash memory array. The controller is designed to support SATA Gen III (6 Gbit/s) interface speeds and is fully backward compatible with SATA Gen II (3 Gbit/s) and SATA Gen I (1.5 Gbit/s) to enable the broadest possible range of platform compatibility. The controller utilizes an ARC 700 processing core, providing an optimum balance between read/write performance, Data Care Management, and power fail protection.

Swissbit's durabit™ X-60m2 SSDs deliver an impressive IOPS rate and highest endurance by combining MLC flash technology with a high-end controller architecture, firmware, and an optimized configuration. The durabit™ SSDs are designed for applications requiring high data transfer rates (see Table 3: Read/Write Performance (SBR11105, SBR120155, SBR13056)). This performance is achieved through an on-board DRAM cache and the controller 4-channel NAND flash interface that supports ONFI and Toggle 2 (400 MT/s) interface speeds. In addition, the X-60m2 series feature Swissbit's proven power fail safety and support for the ATA security feature set, NCQ, TRIM, advanced wear leveling and bad block management, and in-field firmware updates.

An on-controller BCH Error Correction Code (ECC) engine provides the X-60m2 hardware ECC, which is capable of correcting up to 66 bits per 1 KByte page. This engine, combined with Swissbit's Data Care Management firmware, provides both passive and active data management strategies to ensure data integrity and extract the maximum possible endurance and reliability from the NAND flash array. These strategies include, but are not limited to, Global Wear Leveling, Adaptive Read Refresh, Background Media Scan, and Dynamic Block Remapping.

The risk of data loss as a result of an unexpected power fail event is mitigated using a robust sequence of voltage regulators and detectors designed to ensure a graceful shutdown of the controller and NAND flash array. A combination of both hardware and firmware power fail features prevent the possibility of resident data being corrupted during an unexpected power failure.

3 SerialATA IO rev 3.2 Section 6.6, Aug 7, 2013
https://www.jedec.org/standards-documents/focus/flash/solid-state-drives
https://www.sata-io.org/sata-m2-card
http://pcisig.com/specifications Nov 2013

## Related Documentation

- Serial Transport Protocols and Physical Interconnect (ATA/ATAPI-8)
- AT Attachment Interface Document, American National Standards Institute, X3.298-1997
- PCI Express M.2 standard – PCI Express M.2 Specification, Revision 0.9, June 18, 2013

## *4.1 Performance Specifications*

The X-60m2 read/write sequential and random I/O performance benchmarks are detailed below in Table 3.

**Table 3: Read/Write Performance (SBR11105, SBR120155, SBR13056)[4]**

| Drive Capacity | Sequential Read (MBPS) | | Sequential Write (MBPS) | | Random Read (IOPs) | | Random Write (IOPs) | |
|---|---|---|---|---|---|---|---|---|
| | 2242 | 2260/ 2280 | 2242 | 2260/ 2280 | 2242 | 2260/ 2280 | 2242 | 2260/ 2280 |
| 30 GBytes | 280 | 280 | 50 | 50 | 26,500 | 26,500 | 11,500 | 11,500 |
| 60 GBytes | 520 | 520 | 90 | 90 | 51,000 | 51,000 | 23,000 | 23,000 |
| 120 GBytes | 520 | 520 | 180 | 185 | 71,000 | 73,500 | 43,000 | 45,500 |
| 240 GBytes | 520 | 520 | 340 | 355 | 72,000 | 75,000 | 78,000 | 75,000 |
| 480 GBytes | NA | 520 | NA | 450 | NA | 75,000 | NA | 75,000 |
| 960 GBytes | NA | 520 | NA | 460 | NA | 75,000 | NA | 75,000 |

## *4.2 Current Consumption*

The drive-level current consumption as a function of operating mode is shown below in Table 4.

**Table 4: Current Consumption (SBR11105, SBRSBR13056, SBR120155)[5]**

| Drive Capacity | 2260 and 2280 | | | | | | |
|---|---|---|---|---|---|---|---|
| | Sequential Read | Sequential Write | Random Read | Random Write | Idle | Slumber | Unit |
| 30 GBytes | 265 | 265 | 255 | 265 | 105 | 35 | mA |
| 60 GBytes | 365 | 370 | 330 | 365 | 110 | 35 | |
| 120 GBytes | 405 | 500 | 375 | 500 | 110 | 35 | |
| 240 GBytes | 440 | 805 | 415 | 800 | 110 | 35 | |
| 480 GBytes | 440 | 960 | 420 | 950 | 115 | 35 | |
| 960 GBytes | 470 | 1020 | 430 | 1020 | 125 | 35 | |
| **Drive Capacity** | **2242** | | | | | | |
| | **Sequential Read** | **Sequential Write** | **Random Read** | **Random Write** | **Idle** | **Slumber** | **Unit** |
| 30 GBytes | 265 | 265 | 255 | 265 | 105 | 35 | mA |
| 60 GBytes | 365 | 370 | 330 | 365 | 110 | 35 | |
| 120 GBytes | 380 | 485 | 355 | 485 | 105 | 35 | |
| 240 GBytes | 390 | 495 | 360 | 495 | 110 | 35 | |

[4] The values are measured using CDM across the full drive density. Performance depends on flash type and number, file/cluster size, and burst speed.

[5] All values are the maximum recorded at 25 ° C, with nominal supply voltage, and SATA III performance test with IOMeter (512 byte-1 MByte transfer sizes).

## 4.3 Environmental Specifications

### 4.3.1 Recommended Operating Conditions

The recommended operating conditions for the X-60m2 SSD are provided in Table 5 below.

**Table 5: Recommended Operating Conditions[6]**

| Parameter | Value |
|---|---|
| Commercial Operating Temperature | 0 °C to 70 °C |
| Industrial Operating Temperature | -40 °C to 85 °C |
| Power Supply $V_{CC}$ Voltage | 3.3 V ± 5% |

### 4.3.2 Recommended Storage Conditions

The recommended storage conditions are listed below in Table 6.

**Table 6: Recommended Storage Conditions**

| Parameter | Value |
|---|---|
| Commercial Storage Temperature | -40 °C to 85 °C |
| Industrial Storage Temperature | -40 °C to 85 °C |

### 4.3.3 Shock, Vibration and Humidity

The maximum shock, vibration and humidity conditions are listed below in Table 7.

**Table 7: Shock, Vibration, and Humidity**

| Parameter | Value |
|---|---|
| Non-Operating Shock | 1,500 *g*, 0.5 ms pulse duration, half-sine wave (IEC 60068-2-27 and JESD22-B110 cond. B) |
| Non-Operating Vibration | 50 *g*, 131-2,000 Hz, 3 axes, 12 cycles (IEC 60068-2-6, MIL-STD-893 H Method 2007.3) |
| Humidity (Non-Condensing) | 85% RH 85 °C, 1000 hrs, max. supply voltage (JESD22-A101B) |

[6] Adequate airflow is required to ensure the drive temperature, as reported in the S.M.A.R.T. data, does not exceed the specified maximum operating temperature.

## 4.4 Regulatory Compliance

The X-60m2 devices comply with the standards listed in the following table.

**Table 8: Regulatory Compliance**

| Compliance | Country | Type | Standard(s)/Directive |
|---|---|---|---|
| CE | European Union | Certificate | 2011/65/EU, 2012/19/EU, 2014/30/EU |
| CE/EMC | European Union | Compliance | 2004/108/EC (AS/NZS CISPR22 :2009 +A1:2010, EN 61000-6-2:2005/AC:2005,EN 61000-6-4:2007/A1:2011 [EN55022:2010 Class B]) |
| CE/RoHS | European Union | Compliance | 2011/65/EU |
| CE/WEEE | European Union | Compliance | 2012/19/EU |
| REACH | European Union | Certificate | 1907/2006 |
| FCC | United States | Certificate | 47CFR Part 15, Class B |
| UL | United States | Compliance | UL/CSA 60950-1, Second Edition |
| VCCI | Japan | Compliance | ITE (Class A) |
| CCC | China | Compliance | Laws and Regulations of the People's Republic of China Governing Foreign-Related Matters (1991.7) |
| C-Tick | Australia | Compliance | AS/NZS CISPR22 |
| TüV | Germany | Compliance | TüV IEC 60950-1; UL/CSA 60950-1, Second Edition |
| SATA-IO | International | Compliance | SATA Revision 1.4 Interoperability |

## 4.5 Mechanical Specifications

The X-60m2 SSD consists of a flash controller and NAND flash memory devices. The controller interfaces with a host system, allowing data to be written to and read from the flash memory array. The SSD has a PCIe mini connector with a SATA interface. Physical dimensions are detailed in Table 9 below. Figure 3 on page 13 illustrates the X-60m2 dimensions and connector location.

**Table 9: Measured Physical Dimensions**

| Physical Dimensions | 2280 | 2260 | 2242 | Unit |
|---|---|---|---|---|
| Length | 80.00±0.15 | 60.00±0.15 | 42.00±0.15 | mm |
| Width | 22.00±0.15 | 22.00±0.15 | 22.00±0.15 | |
| Thickness (Max Capacity) | 3.30±0.08 | 3.30±0.08 | 3.30±0.08 | |
| Weight (2280 Max Capacity) | 10.2 | | | g |

## 4.6 Reliability and Endurance

The Mean Time Between Failure (MTBF) is specified to exceed the value listed below. Data reliability with effective error tolerance and data retention at the beginning and end of life is also provided.

**Table 10: Reliability**

| Parameter | Value |
|---|---|
| MTBF (at 25 °C) | > 2,000,000 hours |
| Data Reliability | < 1 Non-Recoverable Error per $10^{16}$ bits Read |
| Data Retention | 10 Years at Start (JESD47), 1 Year at EOL |

Endurance represented as both TeraBytes Written (TBW) and Drive Writes Per Day (DWPD) for three different application scenarios is provided in the following table.

**Table 11: Endurance**

| Drive Capacity | Client | | Enterprise | | Embedded | |
|---|---|---|---|---|---|---|
| | TBW | DWPD | TBW | DWPD | TBW | DWPD |
| 30 GBytes | 67.74 | 1.98 | 17.44 | 0.51 | 18.75 | 0.55 |
| 60 GBytes | 135.48 | | 34.88 | | 37.50 | |
| 120 GBytes | 270.95 | | 69.74 | | 75.00 | |
| 240 GBytes | 541.91 | | 139.52 | | 150.00 | |
| 480 GBytes | 1083.82 | | 279.04 | | 300.00 | |
| 960 GBytes | 2167.63 | | 558.07 | | 600.00 | |

## 4.7 Drive Geometry Specification

The X-60m2 drive geometry is set to report industry-standard LBA settings per the IDEMA standard (LBA1-03). The values for each capacity are shown below in Table 12.

**Table 12: Drive Geometry**

| Drive Capacity | User Capacity[7] | Total LBA | User Addressable Bytes |
|---|---|---|---|
| | | Decimal | (Unformatted) |
| 32 GBytes | 30 GBytes | 58,626,288 | 30,016,659,456 |
| 64 GBytes | 60 GBytes | 117,231,408 | 60,022,480,896 |
| 128 GBytes | 120 GBytes | 234,441,648 | 120,034,123,776 |
| 256 GBytes | 240 GBytes | 468,862,128 | 240,057,409,536 |
| 512 GBytes | 480 GBytes | 937,703,088 | 480,103,981,056 |
| 1024 GBytes | 960 GBytes | 1,875,385,008 | 960,197,124,096 |

[7] 1 GByte = $10^9$ bytes

# 5. Electrical Interface

This 75-position M.2 connector incorporates both the B and M keys for Socket 2 SATA-based SSDs and follows the applicable JEDEC specifications. M.2 SSDs follow the SATA I/O specification, offering a maximum performance of 6 Gbit/s.

**Figure 2: X-60m2 Electrical Interface**

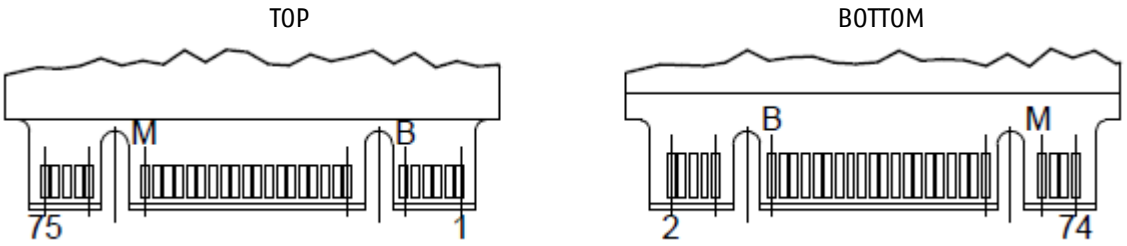



**Table 13: Pin Assignment, Name, and Description**

| Description | Assignment | Pin | Pin | Assignment | Description |
|---|---|---|---|---|---|
| Config_3 | GND | 1 | 2 | +3.3V | 3.3V Source |
| Ground | GND | 3 | 4 | +3.3V | 3.3V Source |
| No Connect | NC | 5 | 6 | NC | No Connect |
| No Connect | NC | 7 | 8 | NC | No Connect |
| No Connect | NC | 9 | 10 | DAS/DSS | DEVACT Device Activity Signal |
| No Connect | NC | 11 | 12-19 | Removed | Mechanical Notch B |
| Reserved | NC | 20 | 21 | GND | CONFIG_0 |
| Reserved | NC | 22 | 23 | NC | No Connect |
| Reserved | NC | 24 | 25 | NC | No Connect |
| Reserved | NC | 26 | 27 | GND | Ground |
| No Connect | NC | 28 | 29 | NC | No Connect |
| No Connect | NC | 30 | 31 | NC | No Connect |
| No Connect | NC | 32 | 33 | GND | Ground |
| Reserved | NC | 34 | 35 | NC | No Connect |
| Reserved | NC | 36 | 37 | NC | No Connect |
| Device Sleep, Input | DEVSLP | 38 | 39 | GND | Ground |
| Reserved | NC | 40 | 41 | B+ | +SATA Differential Receive Signal |
| Reserved | NC | 42 | 43 | B- | -SATA Differential Receive Signal |
| No Connect | NC | 44 | 45 | GND | Ground |
| Reserved | NC | 46 | 47 | A- | -SATA Differential Transmit Signal |
| Reserved | NC | 48 | 49 | A+ | +SATA Differential Transmit Signal |
| No Connect | NC | 50 | 51 | GND | Ground |
| No Connect | NC | 52 | 53 | NC | No Connect |
| No Connect | NC | 54 | 55 | NC | No Connect |
| Reserved | NC | 56 | 57 | GND | Ground |
| Reserved | NC | 58 | 59-66 | Removed | Mechanical Notch M |
| No Connect | NC | 67 | 68 | NC | No Connect |
| Config_1 | GND | 69 | 70 | 3.3V | Supply pin, 3.3V |
| Ground | GND | 71 | 72 | 3.3V | Supply pin, 3.3V |
| Ground | GND | 73 | 74 | 3.3V | Supply pin, 3.3V |
| Config_2 | GND | 75 | | | |

# 6. Package Mechanical

**NOTE:** The dimensions in the following figure are the maximum values based on the JEDEC standard. For the product dimensions, see the *Mechanical Specifications* section on page 10.

**Figure 3: M.2 SSD Drive Dimensions in mm [in]**

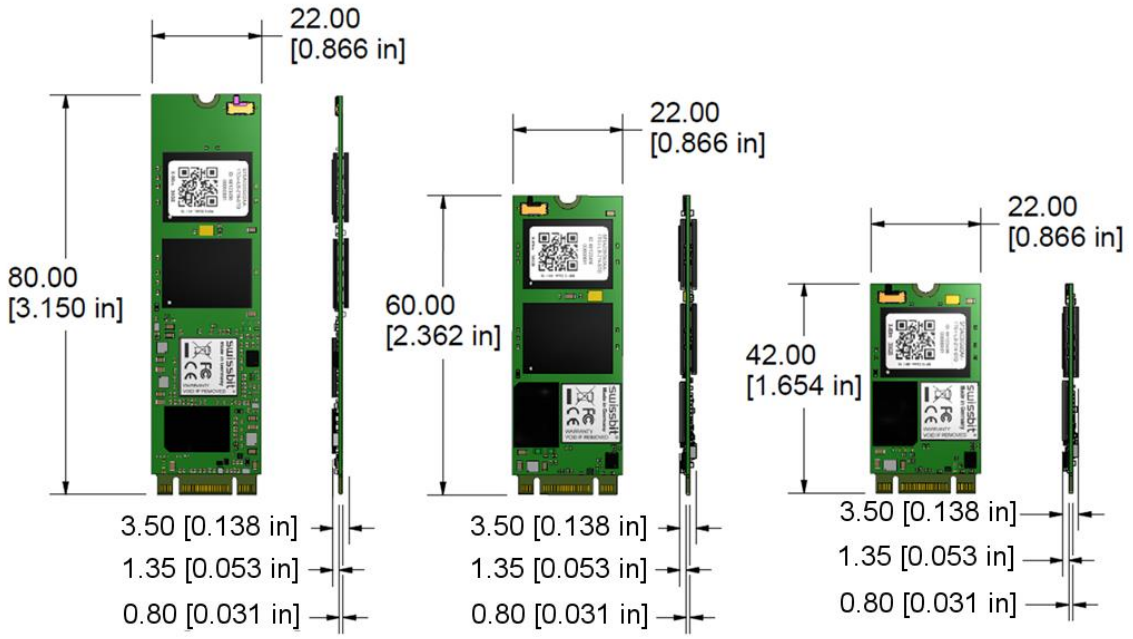
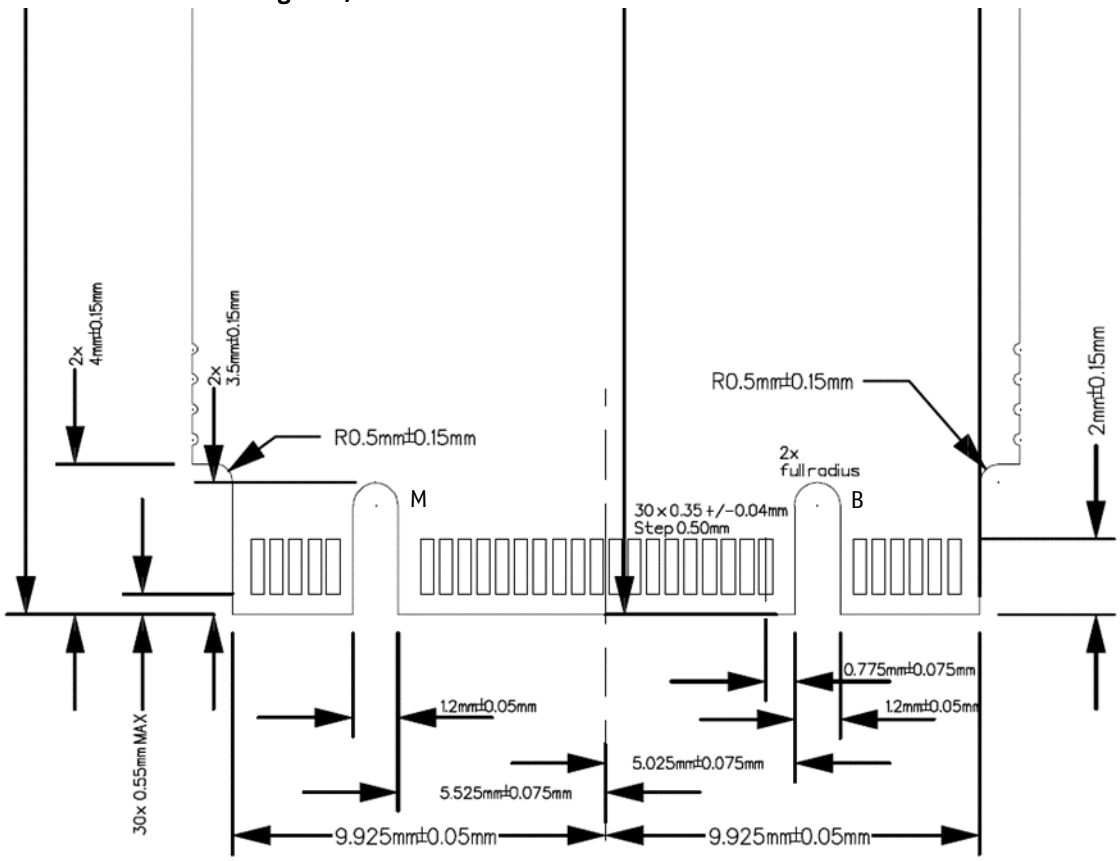



**Figure 4: M.2 Connector Dimensions in mm**



# 7. ATA Commands

This section provides information on the ATA commands supported by the SSD. The commands are issued to the ATA by loading the required registers in the command block with the supplied parameter, and then writing the command code to the register. For backward compatibility, some commands are implemented as a "no operation". See Table 14 for a list of ATA commands the device supports. For details about setting up the command registers, see the latest ATA Specification.

**Table 14: ATA Command Set**

| Command | Code | Protocol |
|---|---|---|
| **General Feature Set** | | |
| Execute Device Diagnostic | 90h | Execute Device Diagnostic |
| Flush Cache | E7h | Non-data |
| Identify Device | ECh | PIO data-in |
| Initialize Drive Parameters | 91h | Non-data |
| Read DMA | C8h | DMA |
| Read Log Ext | 2Fh | PIO data-in |
| Read Multiple | C4h | PIO data-in |
| Read Sector(s) | 20h | PIO data-in |
| Read Verify Sector(s) | 40h or 41h | Non-data |
| Set Feature | EFh | Non-data |
| Set Multiple Mode | C6h | Non-data |
| Write DMA | CAh | DMA |
| Write Multiple | C5h | PIO data-out |
| Write Sector(s) | 30h | PIO data-out |
| NOP | 00h | Non-data |
| Read Buffer | E4h | PIO data-in |
| Write Buffer | E8h | PIO data-out |
| **Power Management Feature Set** | | |
| Check Power Mode | E5h or 98h | Non-data |
| Idle | E3h or 97h | Non-data |
| Idle Immediate | E1h or 95h | Non-data |
| Sleep | E6h or 99h | Non-data |
| Standby | E2h or 96h | Non-data |
| Standby Immediate | E0h or 94h | Non-data |
| **Security Mode Feature Set** | | |
| Security Set Password | F1h | PIO data-out |
| Security Unlock | F2h | PIO data-out |
| Security Erase Prepare | F3h | Non-data |
| Security Erase Unit | F4h | PIO data-out |
| Security Freeze Lock | F5h | Non-data |
| Security Disable Password | F6h | PIO data-out |
| **S.M.A.R.T. Feature Set** | | |
| S.M.A.R.T. Disable Operations | B0h | Non-data |
| S.M.A.R.T. Enable/Disable Autosave | B0h | Non-data |
| S.M.A.R.T. Enable Operations | B0h | Non-data |
| S.M.A.R.T. Execute Off-Line Immediate | B0h | Non-data |
| S.M.A.R.T. Read Data | B0h | PIO data-in |
| S.M.A.R.T. Read Log | B0h | PIO data-in |
| S.M.A.R.T. Read Threshold | B0h | PIO data-in |
| S.M.A.R.T. Return Status | B0h | Non-data |
| S.M.A.R.T. Save Attribute Values | B0h | Non-data |
| S.M.A.R.T. Write Attribute Values | B0h | Non-data |
| S.M.A.R.T. Write Log | B0h | PIO data-out |

| Command | Code | Protocol |
|---|---|---|
| **Host Protected Area Feature Set** | | |
| Read Native Max Address | F8h | Non-data |
| Set Max Address | F9h | Non-data |
| Set Max Set Password | F9h | PIO data-out |
| Set Max Lock | F9h | Non-data |
| Set Max Freeze Lock | F9h | Non-data |
| Set Max Unlock | F9h | PIO data-out |
| **48-Bit Address Feature Set** | | |
| Flush Cache Ext | EAh | Non-data |
| Read Sector(s) Ext | 24h | PIO data-in |
| Read DMA Ext | 25h | DMA |
| Read Multiple Ext | 29h | PIO data-in |
| Read Native Max Address Ext | 27h | Non-data |
| Read Verify Sector(s) Ext | 42h | Non-data |
| Set Max Address Ext | 37h | Non-data |
| Write DMA Ext | 35h | DMA |
| Write DMA FUA Ext | 3Dh | DMA |
| Write Multiple Ext | 39h | PIO data-out |
| Write Multiple FUA Ext | CEh | PIO data-out |
| Write Sector(s) Ext | 34h | PIO data-out |
| **NCQ Feature Set** | | |
| Read FPDMA Queued | 60h | DMA Queued |
| Write FPDMA Queued | 61h | DMA Queued |
| **Others** | | |
| Data Set Management | 06h | DMA |
| Seek | 70h | Non-data |

# 8. Identify Device Information

The following table describes the 512 bytes of data the drive returns for the Identify Device command (ECh).

**Table 15: Identify Device Information**

| Word(s) | Default Value | Total Bytes | Data Field Type Information |
|---|---|---|---|
| 0 | 0040h* | 2 | Standard Configuration Fixed (optional 848Ah for removable) |
| 1 | XXXXh | 2 | Default number of cylinders |
| 2 | 0000h | 2 | Reserved |
| 3 | 00XXh | 2 | Default number of heads |
| 4-5 | 0000h | 4 | Obsolete |
| 6 | XXXXh | 2 | Default number of sectors per track |
| 7-8 | XXXXh | 4 | Number of sectors per Drive (Word 7 = MSW, Word 8 = LSW) |
| 9 | 0000h | 2 | Obsolete |
| 10-19 | aaaa | 20 | Serial number in ASCII (right-justified) |
| 20-22 | 0000h | 6 | Obsolete |
| 23-26 | XXXX* | 8 | Firmware revision in ASCII (big-endian byte order in Word) |
| 27-46 | XXXX* | 40 | Model number in ASCII (right-justified) |
| 47 | 8002h | 2 | Maximum number of sectors on Read/Write Multiple command |
| 48 | 4000h | 2 | Trusted Computing feature set not supported |
| 49 | 2F00h* | 2 | Standby Timer, DMA, LBA, IORDY supported |
| 50 | 4000h | 2 | Capabilities |
| 51 | 0000h | 2 | PIO data transfer cycle timing mode 0 |
| 52 | 0000h | 2 | Obsolete |
| 53 | 0007h* | 2 | Words 88 and 64-70 valid |
| 54 | XXXXh | 2 | Current numbers of cylinders |
| 55 | XXXXh | 2 | Current numbers of heads |
| 56 | XXXXh | 2 | Current sectors per track |
| 57-58 | XXXXh | 4 | Current capacity in LBAs (Word 57 = LSW, Word 58 = MSW) |
| 59 | 910Xh* | 2 | Multiple sector setting (host changeable) |
| 60-61 | XXXXh | 4 | Total number of sectors addressable in LBA Mode |
| 62 | 0000h | 2 | Obsolete |
| 63 | 0007h* | 2 | Multiword DMA transfer support modes 2, 1, and 0 (host changeable) |
| 64 | 0003h | 2 | Advanced PIO modes supported |
| 65 | 0078h* | 2 | Minimum Multiword DMA transfer cycle time per Word |
| 66 | 0078h* | 2 | Recommended Multiword DMA transfer cycle time |
| 67 | 0078h* | 2 | Minimum PIO transfer cycle time without flow control |
| 68 | 0078h* | 2 | Minimum PIO transfer cycle time with IORDY flow control |
| 69 | 4D20h | 2 | Trimmed range returning zeros, 28-bit commands supported, download |
| 70-74 | 0000h | 10 | Reserved |
| 75 | 001Fh | 1 | Queue Depth |
| 76 | 830Eh | 2 | SATA Capabilities |
| 77 | 0086h | 1 | Additional SATA Capabilities |
| 78 | 014Ch | 2 | SATA feature support |
| 79 | 0040h* | 2 | SATA features enabled (host changeable) |
| 80 | 03F0h | 2 | Major revision |
| 81 | 0000h | 2 | Minor revision |
| 82 -84 | 746Bh* | 6 | Features/command sets supported |
| 85-87 | 7469h* | 6 | Features/command sets enabled (may change in operation) |
| 88 | 407Fh* | 2 | UDMA mode supported |
| 89 | 0002h* | 2 | Time for security erase unit completion |
| 90 | 0002h* | 4 | Time for enhanced security erase time |
| 91 | 0000h | 2 | Power Management |
| 92 | FFFEh* | 2 | Master password revision code |

| Word(s) | Default Value | Total Bytes | Data Field Type Information |
|---|---|---|---|
| 93–99 | 0000h* | 70 | Reserved |
| 100–103 | XXXXh | 8 | Max user LBA48 address feature set |
| 104–105 | 0000h | 4 | Reserved |
| 106 | 4000h | 2 | Sector size |
| 107–118 | 0000h | 24 | Reserved |
| 119–120 | 4018h | 4 | Command set supported settings |
| 121–127 | 0000h | 14 | Reserved |
| 128 | 0021h* | 2 | Security status (may change in operation) |
| 129–159 | XXXXh | 62 | "Swissbit SSD" |
| 160 | 0000h* | 2 | Power requirement |
| 161 | 0000h | 2 | Reserved |
| 162 | 0000h | 2 | Management schemes |
| 163 | 0000h | 2 | IDE Timing |
| 164 | 0000h | 2 | IO Timing |
| 165–168 | 0000h | 8 | Reserved |
| 169 | 0001h | 2 | Data Set Management supported |
| 170–208 | XXXXh | 78 | Reserved |
| 209 | 4000h | 2 | Logical block alignment |
| 210–216 | 0000h | 14 | Reserved |
| 217 | 0001h* | 2 | Nominal media rotation rate: Solid State Device |
| 218–221 | 0000h | 8 | Reserved |
| 222 | 107Fh | 2 | Transport major revision |
| 223–233 | 0000h | 22 | Reserved |
| 234 | 0001h | 2 | Minimum number of 512-byte units per segmented download |
| 235 | 0200h | 2 | Maximum number of 512-byte units per segmented download |
| 236–254 | 0000h | 38 | Reserved |
| 255 | XXXXh | 2 | Integrity Word |

* Standard values for full functionality are listed. Values depend on device configuration.

# 9. S.M.A.R.T. Functionality

The X-60m2 SSDs fully support the ATA Specification for Self-Monitoring, Analysis, and Reporting Technology (S.M.A.R.T.). For details about the S.M.A.R.T. subcommands and attributes, see the *S.M.A.R.T. Attribute Technical Reference Guide*.

## *9.1 S.M.A.R.T. Subcommands*

The following table lists the supported S.M.A.R.T. subcommands and the Features register values.

**Table 16: S.M.A.R.T. Features Supported**

| Features | Operation |
|---|---|
| D0h | S.M.A.R.T. Read Data |
| D1h | S.M.A.R.T. Read Attribute Thresholds |
| D2h | S.M.A.R.T. Enable/Disable Autosave |
| D3h | S.M.A.R.T. Save Attribute Values |
| D4h | S.M.A.R.T. Execute Off-Line Immediate |
| D5h | S.M.A.R.T. Read Log |
| D6h | S.M.A.R.T. Write Log |
| D7h | S.M.A.R.T. Write Attribute Thresholds |
| D8h | S.M.A.R.T. Enable Operations |
| D9h | S.M.A.R.T. Disable Operations |
| DAh | S.M.A.R.T. Return Status |

The device aborts any S.M.A.R.T. subcommands with Features register values not listed in the above table.

## 9.2 S.M.A.R.T. Read Data

When the drive receives the S.M.A.R.T. Read Data subcommand, it returns one sector (512 bytes) of data. See the following table for the data structure of this sector.

Table 17: S.M.A.R.T. Data Structure

| Byte(s) | Value | Description |
|---|---|---|
| 0-1 | 0100h | S.M.A.R.T. structure version |
| 2-361 | XXh | Attribute entries 1 to 30 (see Table 19) |
| 362 | 00h | Off-line data collection status (no off-line data collection started) |
| 363 | 00h | Self-test execution status byte (self-test completed) |
| 364-365 | 0000h | Total time, in seconds, to complete off-line data collection |
| 366 | 00h | Vendor specific |
| 367 | 00h | Off-line data collection capability (no off-line data collection) |
| 368-369 | 0002h | S.M.A.R.T. capabilities |
| 370 | 01h | Error logging capability |
| 371 | 00h | Vendor specific |
| 372 | 01h | Short self-test routine recommended polling time, in minutes |
| 373 | 01h | Extended self-test routine recommended polling time, in minutes |
| 374 | 01h | Conveyance self-test routine recommended polling time, in minutes |
| 375-385 | 00h | Reserved |
| 386-395 | XXh | Firmware version in ASCII |
| 396-399 | 00h | Reserved |
| 400-405 | XXh | Controller model in ASCII ("SM2246") |
| 406-510 | 00h | Reserved |
| 511 | XXh | Data structure checksum |

## 9.3 S.M.A.R.T. Attributes

The X-60m2 drives support the S.M.A.R.T. attributes listed in the following table.

Table 18: S.M.A.R.T. Attributes

| ID | Worst | Threshold | Attribute | Description |
|---|---|---|---|---|
| 01h | 100 | 0 | Raw Read Error Rate | Total number of Cyclic Redundancy Check (CRC) errors that occurred over the SATA interface |
| 05h | 100 | 0 | Reallocated Sector Count | Total number of runtime identified (field marked) bad blocks |
| 09h | 100 | 0 | Power-On Hours | Total hours that the device has been powered on and operational (not in Sleep mode) |
| 0Ch | 100 | 0 | Power Cycle Count | Total number of power cycles that have occurred during the life of the drive |
| A0h | 100 | 0 | Uncorrectable Sector Count | Total number of sectors read (active or passive) with UECC errors |
| A1h | 100 | 0* | Spare Blocks | Total number of spare blocks currently available |
| A3h | 100 | 0 | Number of Initial Invalid Blocks | Total number of initially identified (factory marked and pretest) bad blocks |
| A4h | 100 | 0 | Total Erase Count | Total number of erase operations that have ever been performed on all currently valid blocks (excluding the system, bad and reserved blocks) |
| A5h | 100 | 0 | Maximum Erase Count | The maximum number of erase operations that have ever been performed on a single block (excluding the system, bad and reserved blocks) |
| A6h | 100 | 0 | Minimum Erase Count | The minimum number of erase operations that have ever been performed on a single block (excluding the system, bad and reserved blocks) |
| A7h | 100 | 0* | Average Erase Count | The average number of erase operations that have ever been performed on a single block (excluding the system, bad and reserved blocks) |

| ID | Worst | Threshold | Attribute | Description |
|---|---|---|---|---|
| A8h | 100 | 0 | Maximum Specified Erase Count | The specified maximum erase count; equivalent to number of program/erase (P/E) cycles rated for the device |
| A9h | 100 | 0 | Power on UECC Count | The number of uncorrectable errors encountered during a power up event |
| C0h | 100 | 0 | Initial Spare Block Count | Total number of original spare blocks |
| C1h | 100 | 0 | Dynamic Remaps | Total number of dynamic remap operations |
| C2h | 100 | 0 | Temperature | Temperature (minimum, maximum, and current) of the device |
| C3h | 100 | 0 | Flash ECC Recovered | Total number of times the read-retry process was required to recover data |
| C4h | 0 | 0 | Reallocation Event Count | Total count of remapping operations |
| C6h | 100 | 0 | Uncorrectable Sector Count Offline | Total number of sectors read (active only) with UECC errors |
| C7h | 100 | 0 | SATA PHY CRC Error Count | Total count of PHY errors (including CRC) that occurred over the interface cable |
| D7h | 100 | 0 | TRIM Count | Total number of TRIM commands issued by the host |
| EBh | 100 | 0 | Total Flash LBAs Written | The lower 7 bytes of the total number of LBAs (in 32 KByte increments) written to the flash; the higher 5 bytes are located in attribute EDh |
| EDh | 100 | 0 | Total Flash LBAs Written Expanded | The upper 5 bytes of the total number of LBAs (in 32 KByte increments) written to the flash; the lower 7 bytes are located in attribute EBh |
| F1h | 100 | 0 | Total Host LBAs Written | The lower 7 bytes of the total number of LBAs written to the device by the host; the higher 5 bytes are located in attribute F3h |
| F2h | 100 | 0 | Total Host LBAs Read | The lower 7 bytes of the total number of LBAs read from the device by the host; the higher 5 bytes are located in attribute F4h |
| F3h | 100 | 0 | Total Host LBAs Written Expanded | The upper 5 bytes of the total number of LBAs written to the device by the host; the lower 7 bytes are located in attribute F1h |
| F4h | 100 | 0 | Total Host LBAs Read Expanded | The upper 5 bytes of the total number of LBAs read from the device by the host; the lower 7 bytes are located in attribute F2h |
| F8h | 100 | 0 | SSD Remaining Life | Percent of SSD life remaining on the SSD (a value from 0 to 64h), normalized to 100; based upon Average Erase Count (A7h) scaled by the Maximum Specified Erase Count (A8h) |
| F9h | 100 | 0 | Spare Block Remaining Life | Percent of spare blocks remaining |

* These threshold values are changeable using the Write Attribute Thresholds command.

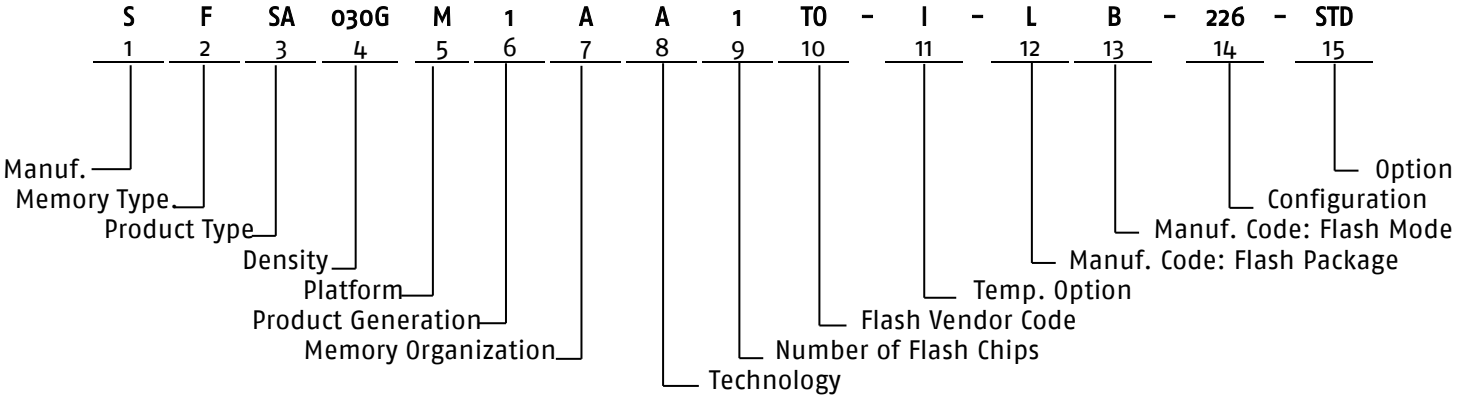
## *9.4 S.M.A.R.T. Attribute Entry Structure*

Each attribute entry consists of 12 bytes. See the following table for the data structure of each entry.

**Table 19: Attribute Entry**

| Byte(s) | Value | Description |
|---|---|---|
| 0 | XXh | Attribute ID (see Table 18) |
| 1-2 | XXXXh | Flags (little-endian) |
| 3 | XXh | Attribute value as a percentage |
| 4 | XXh | Worst value as a percentage |
| 5-8 | XXXXh | Raw value (little-endian) |
| 9-11 | 00h | Reserved |

# 10. Part Number Decoder




## 10.1 Manufacturer

| | |
|---|---|
| Swissbit code | S |

## 10.2 Memory Type

| | |
|---|---|
| Flash | F |

## 10.3 Product Type

| | |
|---|---|
| SATA Interface | SA |

## 10.4 Density

| | |
|---|---|
| 30 GBytes | 030G |
| 60 GBytes | 060G |
| 120 GBytes | 120G |
| 240 GBytes | 240G |
| 480 GBytes | 480G |
| 960 GBytes | 960G |

## 10.5 Platform

| | |
|---|---|
| M.2 SSD | M |

## 10.6 Product Generation

## 10.7 Memory Organization

| | |
|---|---|
| x8 | A |

## 10.8 Technology

| | |
|---|---|
| X-60m2 Series | A |

## 10.9 Number of Flash Chips

| | |
|---|---|
| 1 Flash | 1 |
| 2 Flash | 2 |
| 4 Flash | 4 |
| 8 Flash | 8 |

## 10.10 Flash Code

| | |
|---|---|
| Toshiba | T0 |

## 10.11 Temperature Option

| | |
|---|---|
| Industrial Temperature Range: -40 °C to 85 °C | I |
| Standard Temperature Range: 0 °C to 70 °C | C |

## 10.12 Die Classification

| | |
|---|---|
| MLC MONO (single die package) | G |
| MLC DDP (dual die package) | L |
| MLC QDP (quad die package) | H |
| MLC ODP (octal die package) | O |

## 10.13 Pin Mode

| | TSOP | BGA |
|---|---|---|
| Single nCE and Single R/nB | S | A |
| Dual nCE and Dual R/nB | T | B |
| Quad nCE and Quad R/nB | U | C |
| Octal nCE and Octal R/nB | * | V |
| Sexdec nCE & Sexdec R/nB | * | W |

*Not Available

## 10.14 Drive Configuration XYZ

### X = Dimension and Flash Assembly

| Dimension | Assembly | X |
|---|---|---|
| 2242 | Single-Sided | 1 |
| 2242 | Double-Sided | 2 |
| 2260 | Single-Sided | 3 |
| 2260 | Double-Sided | 4 |
| 2280 | Single-Sided | 5 |
| 2280 | Double-Sided | 6 |

### Y = Firmware Revision

| FW Revision | Y |
|---|---|
| SBR11015 for 30GB up to 480GG | 1 |
| SBR120155 for 30GB up to 480GG | 2 |
| SBR13056 for 960GB | 2 |

### Z = Max Transfer Mode

| Max PIO Mode/CIS | Z |
|---|---|
| UDMA6 (MDMA2, PIO4) | 6 |

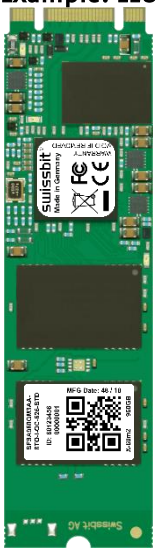
## 10.15 Option

| | |
|---|---|
| Swissbit/Standard | STD |

# 11.Swissbit M.2 SSD Marking Specification

## *11.1 Top View*

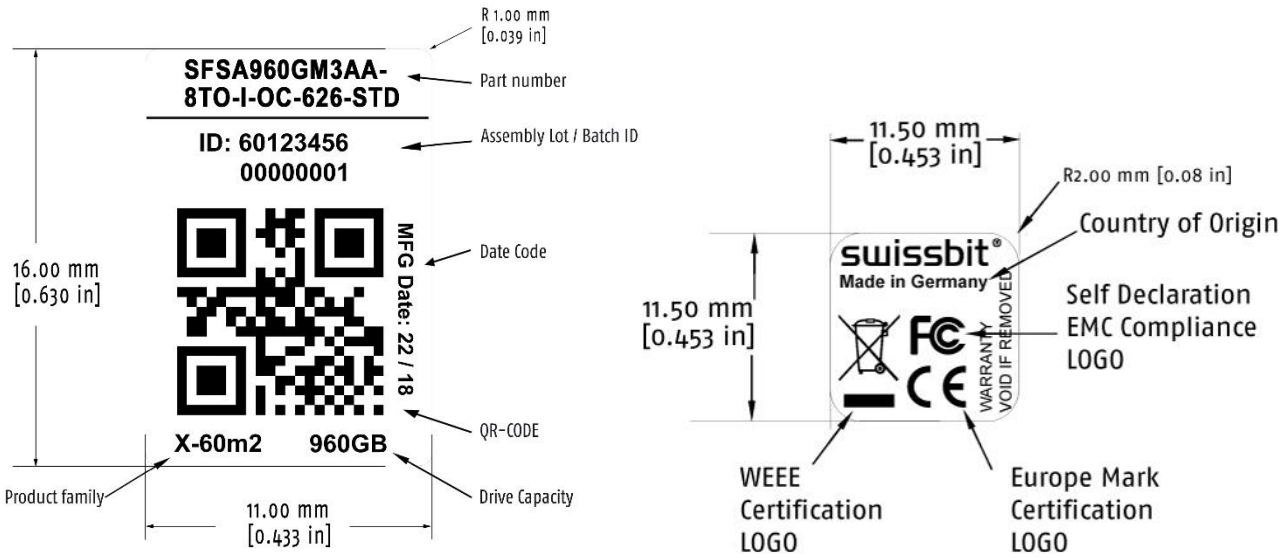
**Example: 2280**



## *11.2 Label Content*

- Part Number
- Lot Code/Identification
- Type Code
- Density
- Manufacturing Date
- Swissbit Logo
- Country of Origin
- CE Logo
- FCC Logo
- WEEE Logo

**M.2 Label**



# 12. Revision History

Table 20: Document Revision History

| Date | Revision | Description | Revision Details |
|---|---|---|---|
| 3-Sept-2015 | 0.90 | First preliminary release | |
| 12-Sept-2015 | 0.91 | Updated connector drawing and spare block attributes. | |
| 24-Sept-2015 | 1.00 | Updated RoHS, ACPEIP and WEEE declaration, product pictures, feature icons and the physical dimensions. | Doc. req. no. 0787 |
| 13-Nov-2015 | 1.01 | Added full X type options in Drive Configuration to include m.2 types, formatted tables, fixed typo and added sector data for some security commands. | Doc. req. no. 0823 |
| 4-Jan-2016 | 1.02 | Removed ATA command byte structure. Updated Identify Device and S.M.A.R.T. information. Updated performance and current values. Added DEVSLP compatible to list of features. Added slumber current. Added Write Thresholds command. Updated storage temperature. Updated copyright date. | Doc. req. no. 0911 |
| 2-Feb-2016 | 1.03 | Fixed formatting issue. | Doc. req. no. 0969 |
| 22-Mar-2016 | 1.04 | Added JEDEC information for endurance workloads. Added FUA command support. Updated part number decoder. Added regulatory information. | Doc. req. no 1022 |
| 27-Jun-2016 | 1.05 | Added available part number table. Added footnote regarding TBW. | Doc. req. no 1147 |
| 31-Aug-2016 | 1.06 | Fixed typo. | Doc. req. no. 1250 |
| 4-Nov-2016 | 1.07 | Corrected endurance values and updated mechanical drawing. | Doc. req. no. 1353 |
| 6-Dec-2016 | 1.08 | Corrected shock and vibration methods. | Doc. req. no. 1417 |
| 8-Feb-2017 | 1.09 | Added 30 µinch gold-plated connector information. Updated copyright date. | Doc. req. no. 1518 |
| 24-May-2018 | 1.10 | Added 960 GByte density (current values TBD). Updated firmware info (chapters device info and S.M.A.R.T. read data), endurance values, test-conditions and part-number decoder (pin mode), changed label illustrations | Doc. req. no. 2224 |
| 28-Nov-2018 | 1.11 | Added measured values for 960 GByte density and updated feature icons. | Doc. req. no. 2641 |
| 11-Jan-2019 | 1.12 | Updated m.2 connector drawing (figure 4). | Doc. req. no. 2700 |
| 23-Jan-2019 | 1.13 | Added new firmware part numbers and updated sections to meet standard data sheet review criteria. | Doc. req. no. 2741 |