HTS221

Capacitive digital sensor for relative humidity and temperature

Datasheet - production data

HLGA-6L
(2 x 2 x 0.9 mm)

Features

- 0 to 100% relative humidity range
- Supply voltage: 1.7 to 3.6 V
- Low power consumption: 2 µA @ 1 Hz ODR
- Selectable ODR from 1 Hz to 12.5 Hz
- High rH sensitivity: 0.004% rH/LSB
- Humidity accuracy: ± 3.5% rH, 20 to +80% rH
- Temperature accuracy: ± 0.5 °C,15 to +40 °C
- Embedded 16-bit ADC
- 16-bit humidity and temperature output data
- SPI and I²C interfaces
- Factory calibrated
- Tiny 2 x 2 x 0.9 mm package
- ECOPACK® compliant

Applications

- Air conditioning, heating and ventilation
- Air humidifiers
- Refrigerators
- Wearable devices
- Smart home automation
- Industrial automation
- Respiratory equipment
- Asset and goods tracking

Description

The HTS221 is an ultra-compact sensor for relative humidity and temperature. It includes a sensing element and a mixed signal ASIC to provide the measurement information through digital serial interfaces.

The sensing element consists of a polymer dielectric planar capacitor structure capable of detecting relative humidity variations and is manufactured using a dedicated ST process.

The HTS221 is available in a small top-holed cap land grid array (HLGA) package guaranteed to operate over a temperature range from -40 °C to +120 °C.

Table 1. Device summary

Order code	Temperature range [°C]	Package	Packing
HTS221TR	-40 to +120	HLGA-6L	Tape and reel

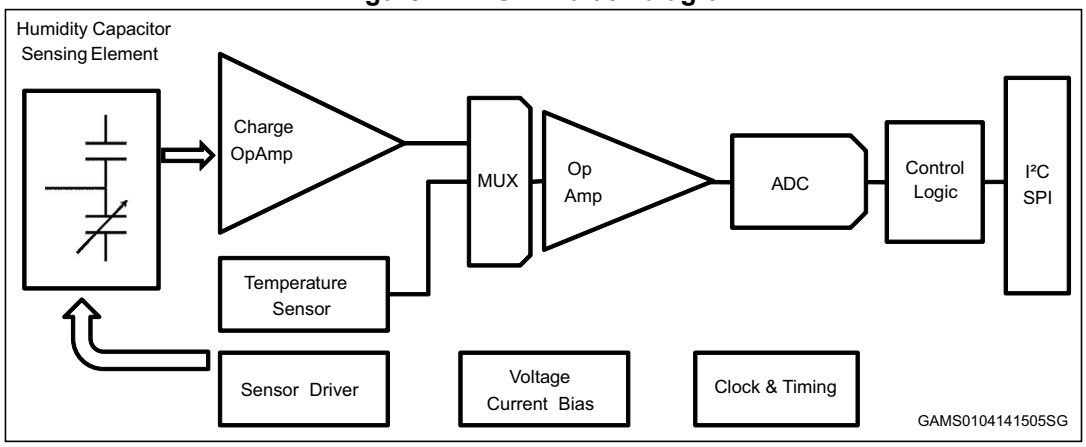
Contents

List of tables

List of figures

1 HTS221 block diagram

Figure 1. HTS221 block diagram



1.1 Pin information

Figure 2. Pin configuration (bottom view)

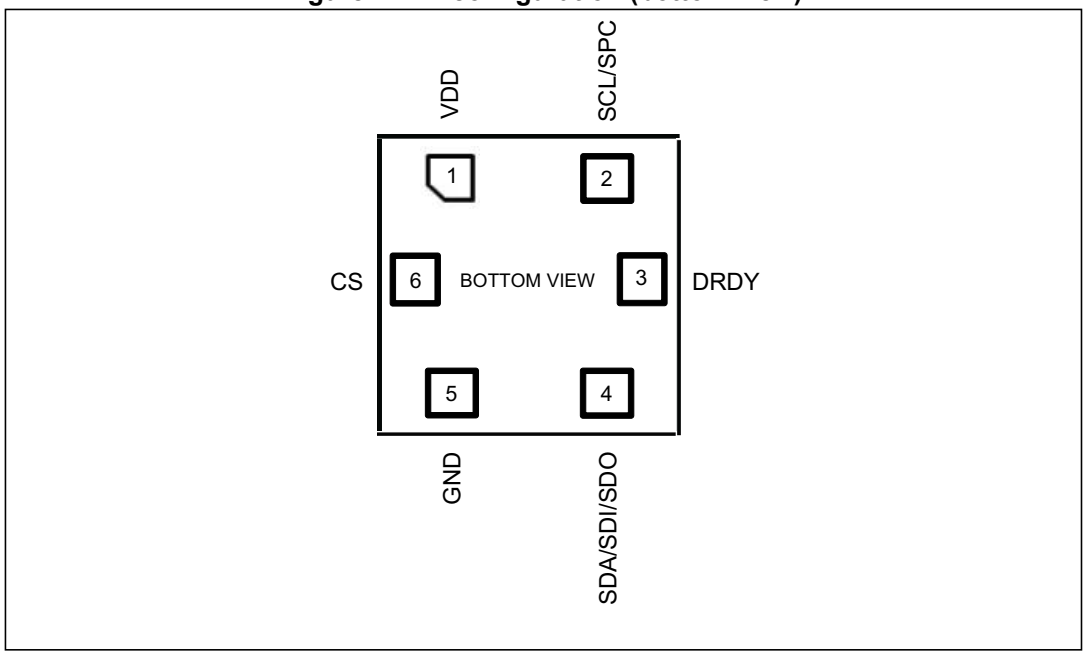


Table 2. Pin description

Pin n°	Name	Function
1	V_{DD}	Power supply
2	SCL/SPC	I²C serial clock (SCL) SPI serial port clock (SPC)
3	DRDY	Data Ready output signal
4	SDA/SDI/SDO	I²C serial data (SDA) 3-wire SPI serial data input /output (SDI/SDO)
5	GND	Ground
6	SPI enable	I²C/SPI mode selection (1: SPI idle mode / I²C communication enabled; 0: SPI communication mode / I²C disabled)

2 Sensor parameters and electrical specifications

Conditions at V_{DD} = 2.5 V, T = 25 °C, unless otherwise noted.

Table 3. Humidity and temperature parameter specifications

Symbol	Parameter	Test condition	Min.	Typ.(1)	Max.	Unit
Hop	Operating humidity range		0	–	100	% rH
Hbit	Humidity output data			16	–	bit
Hs	Humidity sensitivity			0.004		%rH/LSB
				256		LSB/%rH
Hacc	Humidity accuracy(2)	20 to 80% rH		±3.5		% rH
		0 to 100% rH		±5		
Hnoise	Humidity noise(3)			0.03		RMS
Hhys	Humidity hysteresis			±1		% rH
Hstep	Humidity response time(4)	t @ 63%		10		s
Hdrift	Humidity long-term drift	20 to 80% rH		0.5		%rH/yr
Top	Operating temperature range		-40	–	120	°C
Tbit	Temperature output data		–	16	–	bit
Ts	Temperature sensitivity			0.016		°C/LSB
				64		LSB/°C
Tacc	Temperature accuracy	15 to 40 °C		±0.5		°C
		0 to 60 °C		±1		
Tnoise	Temperature noise(3)			0.007		RMS
Tstep	Temperature response time	t @ 63%		15		s
Tdrift	Temperature long-term drift	T = 0 to 80 °C			0.05	°C/yr
ODR	Humidity and temperature digital output data rate			1/7/12.5		Hz

1. Typical specifications are not guaranteed
2. Accuracy in non condensing environment including hysteresis
3. Default value; noise value can be modified by *AV_CONF (10h)*
4. Valid at 25 °C and 1 m/s airflow

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.(1)	Max.	Unit
V_{DD}	Supply voltage		1.7	–	3.6	V
I_{DD}	Supply current (2)	1 Hz, 25 °C, 2.5 V		2		µA
$I_{DD}P_{DN}$	Supply current in power-down mode T = 25 °C	25 °C, 2.5 V	–	0.5	–	µA

1. Typical specifications are not guaranteed
2. Refer to *Table 16*.

2.1 Communication interface characteristics

2.1.1 SPI - serial peripheral interface

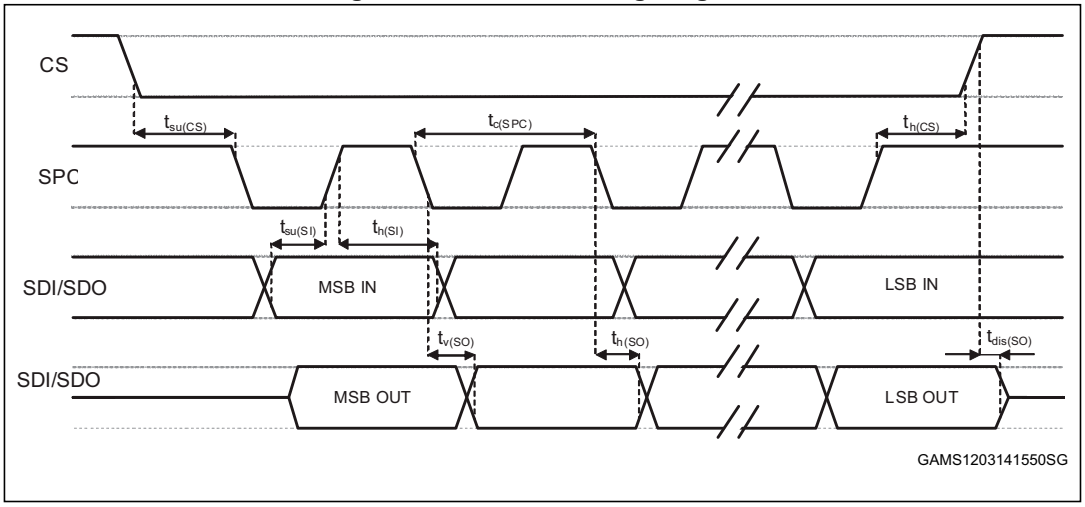
Subject to general operating conditions for V_{DD} and T_{OP}

Table 5. SPI slave timing values

Symbol	Parameter	Value (1)		Unit
		Min.	Max.	
$t_{c(SPC)}$	SPI clock cycle	100		ns
$f_{c(SPC)}$	SPI clock frequency		10	MHz
$t_{su(CS)}$	CS setup time	6		ns
$t_{h(CS)}$	CS hold time	8		
$t_{su(SI)}$	SDI input setup time	5		
$t_{h(SI)}$	SDI input hold time	15		
$t_{v(SO)}$	SDO valid output time		50	
$t_{h(SO)}$	SDO output hold time	9		
$t_{dis(SO)}$	SDO output disable time		50	

1. Values are guaranteed at 10 MHz clock frequency for SPI, based on characterization results, not tested in production.

Figure 3. SPI slave timing diagram



Note: Measurement points are done at $0.2 \cdot V_{DD}$ and $0.8 \cdot V_{DD}$, for both ports.

2.1.2 I²C - control interface

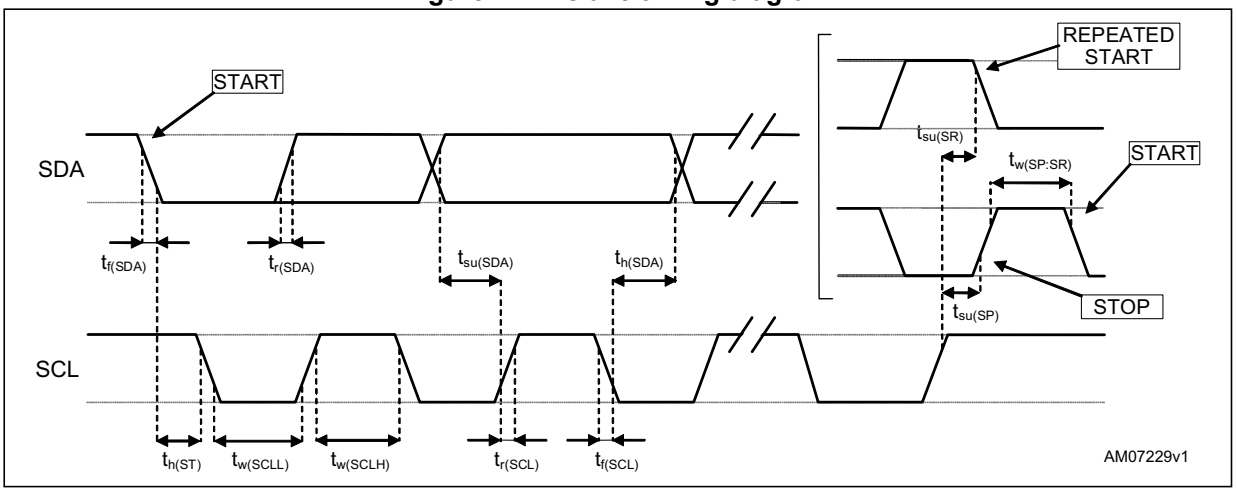
Subject to general operating conditions for V_{DD} and T_{OP}.

Table 6. I²C slave timing values

Symbol	Parameter (1)	I²C standard mode (1)		I²C fast mode (1)		Unit
		Min.	Max.	Min.	Max.	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	kHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0.01	3.45	0	0.9	µs
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000	$20 + 0.1C_b$ (2)	300	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300	$20 + 0.1C_b$ (2)	300	
$t_{h(ST)}$	START condition hold time	4		0.6		µs
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(SP)}$	STOP condition setup time	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		

1. Data based on standard I²C protocol requirement, not tested in production.
2. C_b = total capacitance of one bus line, in pF.

Figure 4. I²C slave timing diagram



Note: Measurement points are done at 0.2·V_{DD} and 0.8·V_{DD}, for both ports.

2.2 Absolute maximum ratings

Stress above those listed as “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 7. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
V_{DD}	Supply voltage	-0.3 to 4.8	V
V_{IN}	Input voltage on any control pin	-0.3 to V_{DD} +0.3	V
T_{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection	2 (HBM)	kV

Note: Supply voltage on any pin should never exceed 4.8 V.

This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.

This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

3 Functionality

The HTS221 is a digital humidity and temperature sensor, packaged in an HLGA holed package.The device includes the sensing element and an IC (integrated circuit) interface able to take information from the sensing element and provide a digital signal to the application, communicating through I²C/SPI interfaces with the host controller.

3.1 IC interface

The complete measurement chain consists of a low-noise capacitive amplifier, which converts the capacitive imbalance of the humidity sensor into an analog voltage signal, and an analog-to-digital converter is used to generate the digital information.

The converter is coupled with a dedicated hardware (HW) averaging filter to remove the high-frequency component and reduce the serial interface traffic.

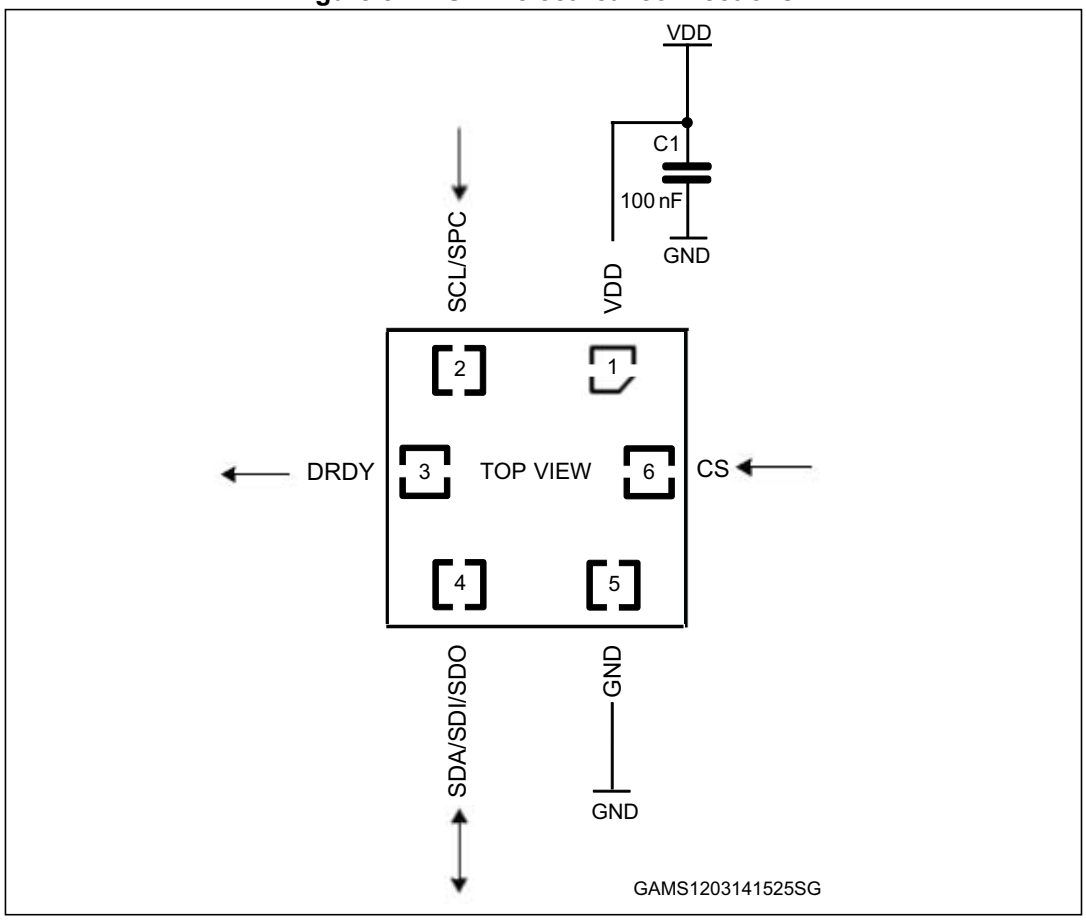
The relative humidity and temperature data can be accessed through an I²C/SPI interface, making the device particularly suitable for direct interfacing with a microcontroller.

3.2 Factory calibration

The IC (integrated circuit) interface is factory calibrated and the coefficients required to convert the ADC 16-bit values into rH% or degrees Celsius can be read through the internal registers of the sensor. Further calibration by the user is not required.

4 Application hints

Figure 5. HTS221 electrical connections



The device is supplied through the V_{DD} line. The power supply decoupling capacitor (100 nF ceramic) should be placed as near as possible to the supply pad of the device (common design practice).

The functionality of the device and the measured data outputs are selectable and accessible through the I²C/SPI interfaces. To select the I²C interface, the CS line must be tied high (i.e. connected to VDD) or left unconnected (thanks to the internal pull-up).

All the voltage and ground supplies must be present at the same time to have proper behavior of the IC (refer to *Figure 5*).

4.1 Soldering information

The HLGA package is compliant with the ECOPACK® standard and it is qualified for soldering heat resistance according to JEDEC J-STD-020. After soldering, the accuracy specification of the sensor can be guaranteed after re-hydration of the sensor element in a stabilized environment (25 °C / 55% rH) for 3 days or at 70% rH for 12 h. Otherwise the sensor may read an offset that slowly disappears if exposed to ambient conditions.

5 Digital interfaces

The registers embedded in the HTS221 may be accessed through both the I²C and SPI 3-wire serial interfaces.

The serial interfaces are mapped onto the same pins.To select the I²C interface, the CS line must be tied high (i.e. connected to V_{DD}) or unconnected (internal pull-up); to select the SPI interface, the CS line must be tied low (i.e. connected to GND).

Table 8. Serial interface pin description

Pin name	Pin description
CS	I²C/SPI mode selection 1: SPI idle mode / I²C communication enabled 0: SPI communication mode / I²C disabled)
SCL/SPC	I²C serial clock (SCL) SPI serial clock (SPC)
SDA/SDI/SDO	I²C serial data (SDA) 3-wire SPI serial data input /output (SDI/SDO)

5.1 I²C serial interface (CS = HIGH or unconnected CS)

The HTS221 I²C is a bus slave. The I²C is employed to write data into registers whose content can also be read back.

The relevant I²C terminology is provided in *Table 9.*

Table 9. I²C terminology

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I²C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bi-directional line used for sending and receiving the data to/from the interface. Both lines must be connected to V_{DD} through pull-up resistors.

The I²C interface is compliant with fast mode (400 kHz) I²C standards as well as with normal mode.

5.1.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A start condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

The 8-bit slave address (SAD) associated to the HTS221 humidity sensor is BEh (write) and BFh (read).

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded in the HTS221 behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit sub-address (SUB) will be transmitted: the 7 LSB represents the actual register address while the MSB enables address auto-increment. If the MSB of the SUB field is ‘1’, the SUB (register address) will be automatically increased to allow multiple data read/write.

The slave address is completed with a Read/Write bit. If the bit was ‘1’ (Read), a repeated START (SR) condition must be issued after the two sub-address bytes; if the bit is ‘0’ (Write) the master will transmit to the slave with direction unchanged. *Table 10* explains how the SAD + read/write bit pattern is composed, listing all the possible configurations.

Table 10. SAD + Read/Write patterns

Command	SAD[6:0]	R/W	SAD+R/W
Read	1011111	1	10111111 (BFh)
Write	1011111	0	10111110 (BEh)

Table 11. Transfer when master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 12. Transfer when master is writing multiple bytes to slave

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 13. Transfer when master is receiving (reading) one byte of data from slave

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 14. Transfer when master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the most significant bit (MSB) first. If a receiver can't receive another complete byte of data until it has performed some other functions, it can hold the clock line, SCL LOW to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver does not acknowledge the slave address (i.e. it is not able to receive because it is performing some real-time function) the data line must be kept HIGH by the slave. The master can then abort the transfer. A LOW to HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

In order to read multiple bytes incrementing the register address, it is necessary to assert the most significant bit of the sub-address field. In other words, SUB(7) must be equal to 1 while SUB(6-0) represents the address of the first register to be read.

In the presented communication format MAK is master acknowledge and NMAK is no master acknowledge.

I²C high speed HS-mode devices can transfer information at bit rates of up to 3.4 Mbit/s, yet they remain fully downward compatible with fast or standard-mode (F/S-mode) devices for bi-directional communication in a mixed-speed bus system. With the exception that arbitration and clock synchronization is not performed during the HS-mode transfer, the same serial bus protocol and data format is maintained as with the F/S-mode system.

HS-mode can only begin after the following conditions (all of which are in F/S-mode):

1. START condition (S)
2. 8-bit master code (00001XXX)
3. not-acknowledge bit (A)

This master code has two main functions:

It allows arbitration and synchronization between competing masters at F/S-mode speeds, resulting in one winning master.

It indicates the beginning of an HS-mode transfer. HS-mode master codes are reserved 8-bit codes, which are not used for slave addressing or other purposes.

The master code indicates to other devices that an HS-mode transfer is to begin and the connected devices must meet the HS-mode specification. As no device is allowed to acknowledge the master code, the master code is followed by a not-acknowledge (A). After the not-acknowledge bit (A), and the SCLH line has been pulled up to a HIGH level, the active master switches to HS-mode and enables (at time t_H, see data transfer in HS mode)

the current-source pull-up circuit for the SCLH signal. As other devices can delay the serial transfer before t_H by stretching the LOW period of the SCLH signal, the active master will enable its current-source pull-up circuit when all devices have released the SCLH line and the SCLH signal has reached a HIGH level, thus speeding up the last part of the rise time of the SCLH signal. The active master then sends a repeated START condition (Sr) followed by a 7-bit slave address (or 10-bit slave address; see previous section) with a R/W bit address, and receives an acknowledge bit (A) from the selected slave.

After a repeated START condition and after each acknowledge bit (A) or not-acknowledge bit (A), the active master disables its current-source pull-up circuit. This enables other devices to delay the serial transfer by stretching the LOW period of the SCLH signal. The active master re-enables its current-source pull-up circuit again when all devices have released and the SCLH signal reaches a HIGH level, and so speeds up the last part of the SCLH signal's rise time. Data transfer continues in HS-mode after the next repeated START (Sr), and only switches back to F/S-mode after a STOP condition (P). To reduce the overhead of the master code, it's possible that a master links a number of HS-mode transfers, separated by repeated START conditions (Sr).

5.2 SPI bus interface (CS = LOW)

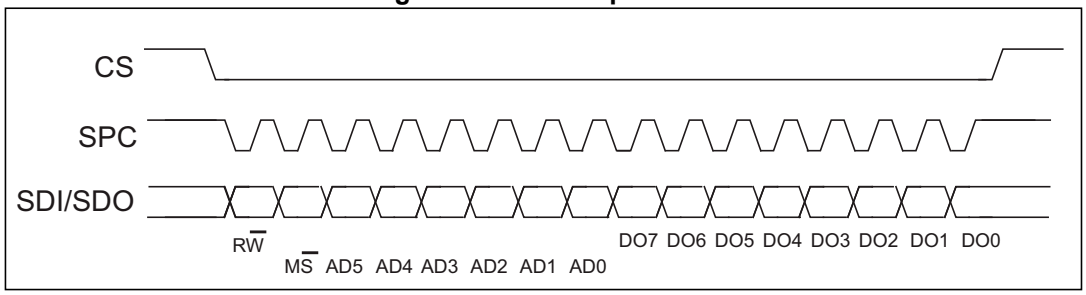
The HTS221 SPI is a slave bus that can operate in 0 and 3 SPI modes. The SPI allows writing to and reading from the registers of the device. The serial interface interacts with the application through 3 wires: **CS**, **SPC**, **SDI/SDO**.

CS is the serial port enable and is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. **SCL** is the serial port clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI/SDO** is the serial port data input and output. This line is driven at the falling edge of **SCL** and should be captured at the rising edge of **SCL**.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in case of multiple read/write bytes. Bit duration is the time between two falling edges of **SCL**. The first bit (bit 0) starts at the first falling edge of **SCL** after the falling edge of **CS** while the last bit (bit 15, bit 23,...) starts at the last falling edge of **SCL** just before the rising edge of **CS**.

5.2.1 SPI write

Figure 6. SPI write protocol



The SPI write command is performed with 16 clock pulses. A multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

bit 0: WRITE bit. The value is 0.

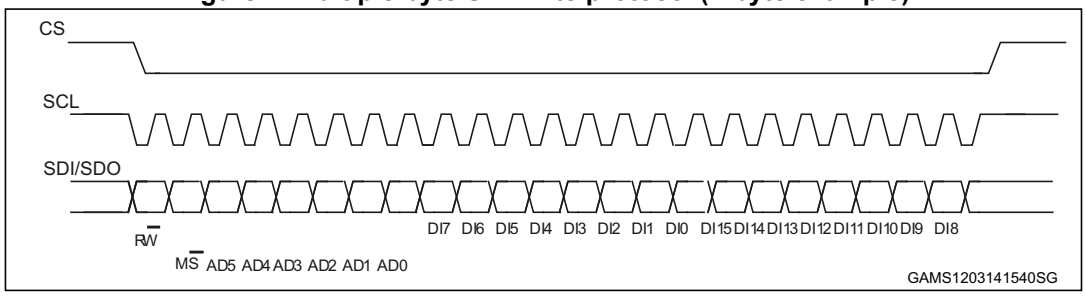
bit 1: MS bit. When 0, does not increment the address; when 1, increments the address in multiple writes.

bit 2 -7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that will be written inside the device (MSB first).

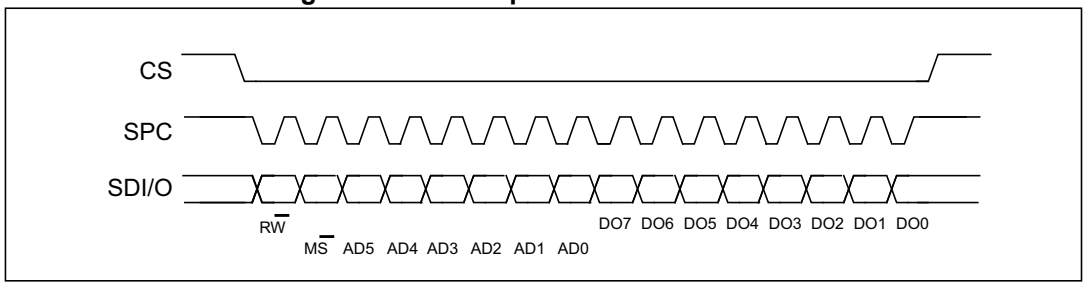
bit 16-...: data DI(...-8). Further data in multiple byte writes.

Figure 7. Multiple byte SPI write protocol (2-byte example)



5.2.2 SPI read

Figure 8. SPI read protocol in 3-wire mode



The SPI read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1: MS bit. When 0, does not increment the address, when 1, increments the address in multiple reads.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSB first).

A multiple read command is also available in 3-wire mode.

6 Register mapping

The table below provides a list of the 8-bit registers embedded in the device and the related addresses.

Table 15. Register address map

Name	Type	Register address (hex)	Default (hex)
Reserved		00-0E	Do not modify
WHO_AM_I	R	0F	BC
AV_CONF	R/W	10	1B
Reserved		11-1C	Do not modify
CTRL_REG1	R/W	20	0
CTRL_REG2	R/W	21	0
CTRL_REG3	R/W	22	0
Reserved		23-26	Do not modify
STATUS_REG	R	27	0
HUMIDITY_OUT_L	R	28	Output
HUMIDITY_OUT_H	R	29	Output
TEMP_OUT_L	R	2A	Output
TEMP_OUT_H	R	2B	Output
Reserved		2C-2F	Do not modify
CALIB_0..F	R/W	30-3F	Do not modify

Registers marked as *Reserved* must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the CALIB_0..F registers that are loaded at power-on from device internal non-volatile memory should never be modified.

7 Register description

The device contains a set of registers which are used to control its behavior and to retrieve humidity and temperature data. The register address, made up of 7 bits, is used to identify and to read/write the data, through the serial interfaces.

7.1 WHO_AM_I (0Fh)

Device identification

7	6	5	4	3	2	1	0
1	0	1	1	1	1	0	0

This read-only register contains the device identifier, set to BCh

7.2 AV_CONF (10h)

Humidity and temperature resolution mode

7	6	5	4	3	2	1	0
Reserved		AVGT2	AVGT1	AVGT0	AVGH2	AVGH1	AVGH0

To configure humidity/temperature average.

[7:6]	Reserved
[5:3]	AVGT2-0: To select the numbers of averaged temperature samples (2 - 256), see *Table 16*.
[2:0]	AVGH2-0: To select the numbers of averaged humidity samples (4 - 512), see *Table 16*.

Table 16. Humidity and temperature average configuration

AVGx2:0	Nr. internal average		Noise (RMS)		I_{DD} 1 Hz
	Temperature (AVGT)	Humidity (AVGH)	Temp (°C)	rH %	µA
000	2	4	0.08	0.4	0.80
001	4	8	0.05	0.3	1.05
010	8	16	0.04	0.2	1.40
011(1)	16	32	0.03	0.15	2.10
100	32	64	0.02	0.1	3.43
101	64	128	0.015	0.07	6.15
110	128	256	0.01	0.05	11.60
111	256	512	0.007	0.03	22.50

1. Default configuration

7.3 CTRL_REG1 (20h)

Control register 1

7	6	5	4	3	2	1	0
PD	Reserved				BDU	ODR1	ODR0

[7]	PD: power-down control (0: power-down mode; 1: active mode)
[6:3]	Reserved
[2]	BDU: block data update (0: continuous update; 1: output registers not updated until MSB and LSB reading)
[1:0]	ODR1, ODR0: output data rate selection (see table 17)

The **PD** bit is used to turn on the device. The device is in power-down mode when PD = ‘0’ (default value after boot). The device is active when PD is set to ‘1’.

The **BDU** bit is used to inhibit the output register update between the reading of the upper and lower register parts. In default mode (BDU = ‘0’), the lower and upper register parts are updated continuously. If it is not certain whether the read will be faster than output data rate, it is recommended to set the BDU bit to ‘1’. In this way, after the reading of the lower (upper) register part, the content of that output register is not updated until the upper (lower) part is read also.

This feature prevents the reading of LSB and MSB related to different samples.

The ODR1 and ODR0 bits permit changes to the output data rates of humidity and temperature samples.The default value corresponds to a “one-shot” configuration for both humidity and temperature output. ODR1 and ODR0 can be configured as described in *Table 17*.

Table 17. Output data rate configuration

ODR1	ODR0	Humidity (Hz)	Temperature (Hz)
0	0	One-shot	
0	1	1 Hz	1 Hz
1	0	7 Hz	7 Hz
1	1	12.5 Hz	12.5 Hz

7.4 CTRL_REG2 (21h)

Control register 2

7	6	5	4	3	2	1	0
BOOT	Reserved					Heater	ONE_SHOT

[7]	BOOT: Reboot memory content (0: normal mode; 1: reboot memory content)
[6:2]	Reserved
[1]	Heater (0: heater disable; 1: heater enable)
[0]	One-shot enable (0: waiting for start of conversion; 1: start for a new dataset)

The **BOOT** bit is used to refresh the content of the internal registers stored in the Flash memory block. At device power-up, the content of the Flash memory block is transferred to the internal registers related to trimming functions to permit good behavior of the device itself. If, for any reason, the content of the trimming registers is modified, it is sufficient to use this bit to restore the correct values. When the BOOT bit is set to ‘1’ the content of the internal Flash is copied inside the corresponding internal registers and is used to calibrate the device. These values are factory trimmed and are different for every device. They permit good behavior of the device and normally they should not be changed. At the end of the boot process, the BOOT bit is set again to ‘0’.

The **ONE_SHOT** bit is used to start a new conversion. In this situation a single acquisition of temperature and humidity is started when the ONE_SHOT bit is set to ‘1’. At the end of conversion the new data are available in the output registers, the STATUS_REG[0] and STATUS_REG[1] bits are set to ‘1’ and the ONE_SHOT bit comes back to ‘0’ by hardware.

The **Heater** bit is used to control an internal heating element, that can effectively be used to speed up the sensor recovery time in case of condensation. The heater can be operated only by an external controller, which means that it has to be switched on/off directly by FW. Humidity and temperature output should not be read during the heating cycle; valid data can be read out once the heater has been turned off, after the completion of the heating cycle. Typical power consumption related to V_{DD} is described in *Table 18*.

Table 18. Typical power consumption with heater ON

V_{DD} [V]	I [mA]
3.3	33
2.5	22
1.8	12

7.5 CTRL_REG3 (22h)

Control register 3

7	6	5	4	3	2	1	0
DRDY_H_L	PP_OD	Reserved			DRDY	Reserved	

Control register for data ready output signal

[7]	DRDY_H_L: Data Ready output signal active high, low (0: active high - default;1: active low)
[6]	PP_OD: Push-pull / Open Drain selection on pin 3 (DRDY) (0: push-pull - default; 1: open drain)
[5:3]	Reserved
[2]	DRDY_EN: Data Ready enable (0: Data Ready disabled - default;1: Data Ready signal available on pin 3)
[1:0]	Reserved

The **DRDY_EN** bit enables the DRDY signal on pin 3. Normally inactive, the DRDY output signal becomes active on new data available: logical OR of the bits STATUS_REG[1] and STATUS_REG[0] for humidity and temperature, respectively. The DRDY signal returns inactive after both HUMIDITY_OUT_H and TEMP_OUT_H registers are read.

7.6 STATUS_REG (27h)

Status register

7	6	5	4	3	2	1	0
Reserved						H_DA	T_DA

Status register; the content of this register is updated every one-shot reading, and after completion of every ODR cycle, regardless of the BDU value in CTRL_REG1.

[7:2]	Reserved
[1]	H_DA: Humidity data available. (0: new data for humidity is not yet available; 1: new data for humidity is available)
[0]	T_DA: Temperature data available. (0: new data for temperature is not yet available; 1: new data for temperature is available) H_DA is set to 1 whenever a new humidity sample is available. H_DA is cleared anytime HUMIDITY_OUT_H (29h) register is read. T_DA is set to 1 whenever a new temperature sample is available. T_DA is cleared anytime TEMP_OUT_H (2Bh) register is read.

7.7 HUMIDITY_OUT_L (28h)

Relative humidity data (LSB)

7	6	5	4	3	2	1	0
HOUT7	HOUT6	HOUT5	HOUT4	HOUT3	HOUT2	HOUT1	HOUT0

Humidity data (see HUMIDITY_OUT_H)

[7:0]	HOUT7 - HOUT0: Humidity data LSB

7.8 HUMIDITY_OUT_H (29h)

Relative humidity data (MSB)

15	14	13	12	11	10	9	8
HOUT15	HOUT14	HOUT13	HOUT12	HOUT11	HOUT10	HOUT9	HOUT8

Humidity data are expressed as HUMIDITY_OUT_H & HUMIDITY_OUT_L in 2's complement. Values exceeding the operating humidity range (see *Table 3*) must be clipped by SW.

[7:0]	HOUT15 - HOUT8: Humidity data MSB

7.9 TEMP_OUT_L (2Ah)

Temperature data (LSB)

7	6	5	4	3	2	1	0
TOUT7	TOUT6	TOUT5	TOUT4	TOUT3	TOUT2	TOUT1	TOUT0

[7:0]	TOUT7 - TOUT0: Temperature data LSB (see TEMPERATURE_OUT_H)

7.10 TEMP_OUT_H (2Bh)

Temperature data (MSB)

15	14	13	12	11	10	9	8
TOUT15	TOUT14	TOUT13	TOUT12	TOUT11	TOUT10	TOUT9	TOUT8

[15:8]	TOUT15 - TOUT8: Temperature data MSB.

Temperature data are expressed as TEMP_OUT_H & TEMP_OUT_L as 2's complement numbers.
The relative humidity and temperature values must be computed by linear interpolation of current registers with calibration registers, according to *Table 19* and scaling as described in *Section 8*.

8 Humidity and temperature data conversion

The Registers in 30h..3Fh address range contain calibration coefficients. Every sensor module has individual coefficients. Before the first calculation of temperature and humidity, the master reads out the calibration coefficients.

Table 19. Decoding the coefficients in the sensor Flash

Addr	Variable	Format	b7	b6	b5	b4	b3	b2	b1	b0
Output registers										
28	H_OUT	(s16)	H7	H6	H5	H4	H3	H2	H1	H0
29			H15	H14	H13	H12	H11	H10	H9	H8
2A	T_OUT	(s16)	T7	T6	T5	T4	T3	T2	T1	T0
2B			T15	T14	T13	T12	T11	T10	T9	T8
Calibration registers										
30	H0_rH_x2	(u8)	H0.7	H0.6	H0.5	H0.4	H0.3	H0.2	H0.1	H0.1
31	H1_rH_x2	(u8)	H1.7	H1.6	H1.5	H1.4	H1.3	H1.2	H1.1	H1.0
32	T0_degC_x8	(u8)	T0.7	T0.6	T0.5	T0.4	T0.3	T0.2	T0.1	T0.0
33	T1_degC_x8	(u8)	T1.7	T1.6	T1.5	T1.4	T1.3	T1.2	T1.1	T1.0
34	Reserved	(u16)								
35	T1/T0 msb	(u2),(u2)	Reserved				T1.9	T1.8	T0.9	T0.8
36	H0_T0_OUT	(s16)	7	6	5	4	3	2	1	0
37			15	14	13	12	11	10	9	8
38	Reserved									
39										
3A	H1_T0_OUT	(s16)	7	6	5	4	3	2	1	0
3B			15	14	13	12	11	10	9	8
3C	T0_OUT	(s16)	7	6	5	4	3	2	1	0
3D			15	14	13	12	11	10	9	8
3E	T1_OUT	(s16)	7	6	5	4	3	2	1	0
3F			15	14	13	12	11	10	9	8

(u8) is the unsigned 8-bit quantity, and (s16) the signed 16-bit quantity using 2's complement format. In the following example, the two steps required to calculate temperature and relative humidity output values are described. The T0 and T1 calibration temperature values are actually composed of 10 bits (unsigned), where the 2 MSB are in reg 35h, and the 8 LSB are in regs 32h and 33h, respectively. T0 and T1 are the actual calibration temperature values multiplied by 8.

Step 1: Temperature conversion from ADC_OUT (LSB) to °C

Data to build the Temperature calibration curve are stored in device registers.

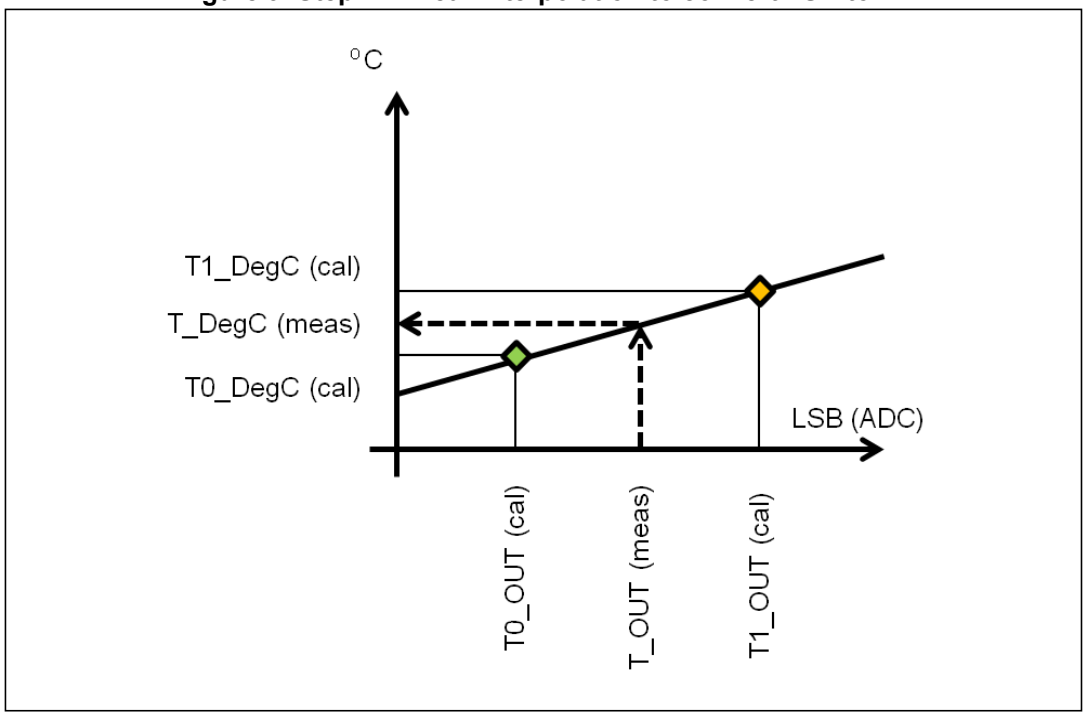
Linear interpolation (example)

Input temperature LSB (ADC)	Output temperature (°C)
T0_OUT = 300	(Msb T0_degC U T0_degC)_x8 = 80 °C => 80/8 = 10.0°C
T1_OUT = 500	(Msb T1_degC U T1_degC)_x8 = 160 °C => 160/8 = 20.0°C

Temperature conversion:

T_OUT = 400	T_degC_x8 =120 °C =>T_degC=120/8 = **15.0 °C**

Figure 9. Step 1: Linear interpolation to convert LSB to °C



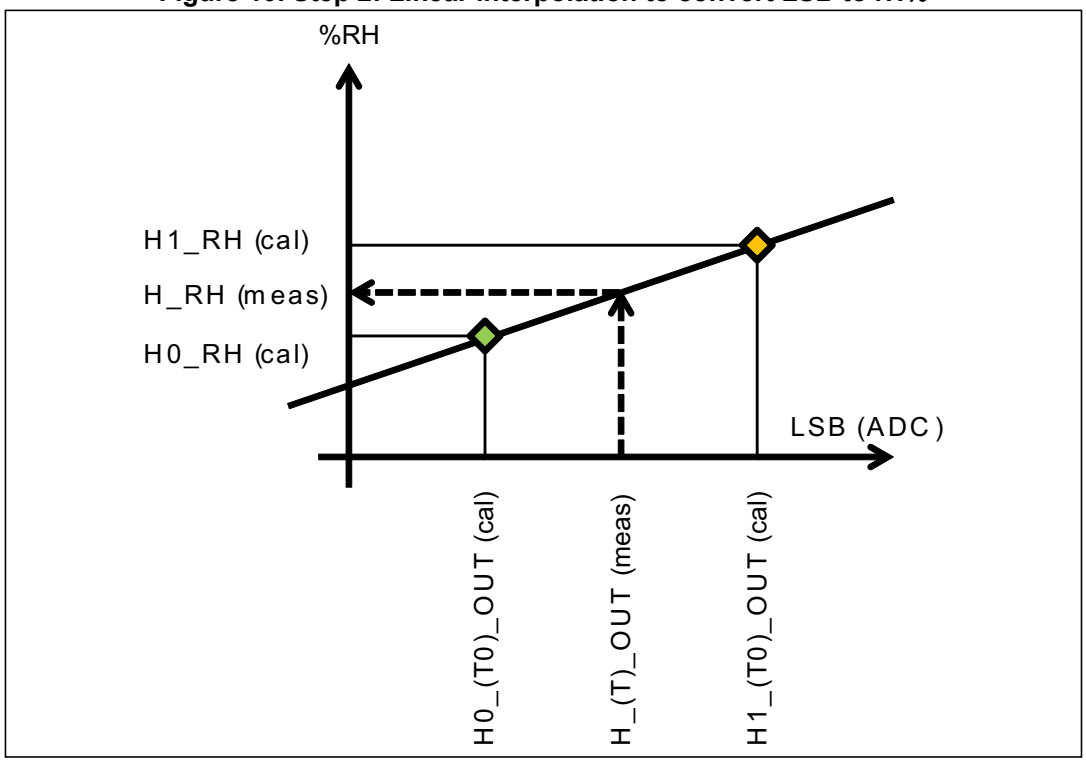
Conclusion: current temperature is 15 °C.

Step 2: Humidity conversion from ADC_OUT (LSB) to rH %

Linear interpolation for relative Humidity (example)

Input: relative Humidity LSB (ADC)	Output: relative Humidity (% rH)
H0_T0_OUT = 0x4000	H0_rH_x2 = 40% rH => 40/2 = 20.0% rH
H1_T0_OUT = 0x6000	H1_rH_x2 = 80% rH => 80/2 = 40% rH
Humidity conversion:	
H_OUT = *0x5000*	H_rH_x2 = 60% [interp.] => 60/2 = **30.0% rH**

Figure 10. Step 2: Linear interpolation to convert LSB to rH%



Conclusion: current relative humidity value is 30%.

9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

9.1 HLGA-6L package information

Figure 11. HLGA-6L (2 x 2 x 0.9 mm) package outline and mechanical data

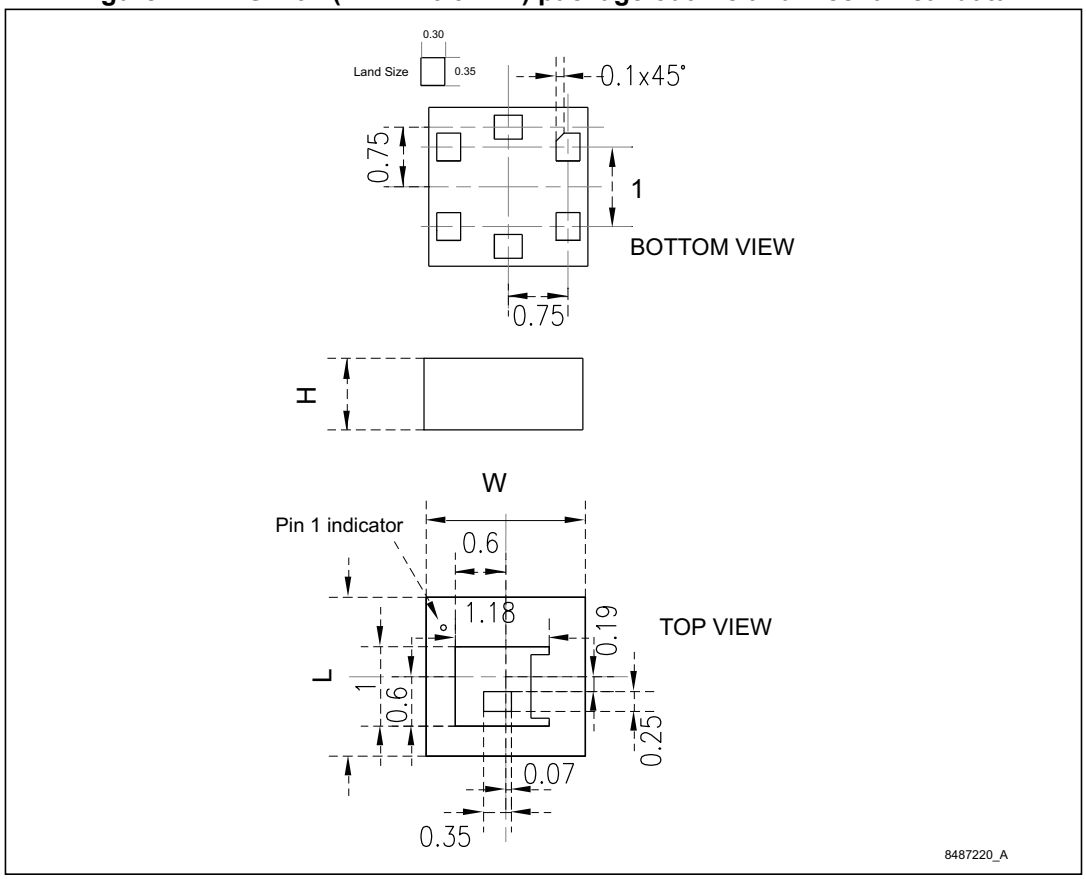


Table 20. HLGA-6L (2 x 2 x 0.9 mm) outer dimensions

Item	Dimension [mm]	Tolerance [mm]
Length [L]	2	± 0.1
Width [W]	2	± 0.1
Height [H]	0.9	± 0.1
Land size	0.30 x 0.35	± 0.05

Dimensions are in millimeters unless otherwise specified.

General tolerance is ± 0.1 mm unless otherwise specified.

9.2 HLGA-6L packing information

Figure 12. Carrier tape information for HLGA-6L package

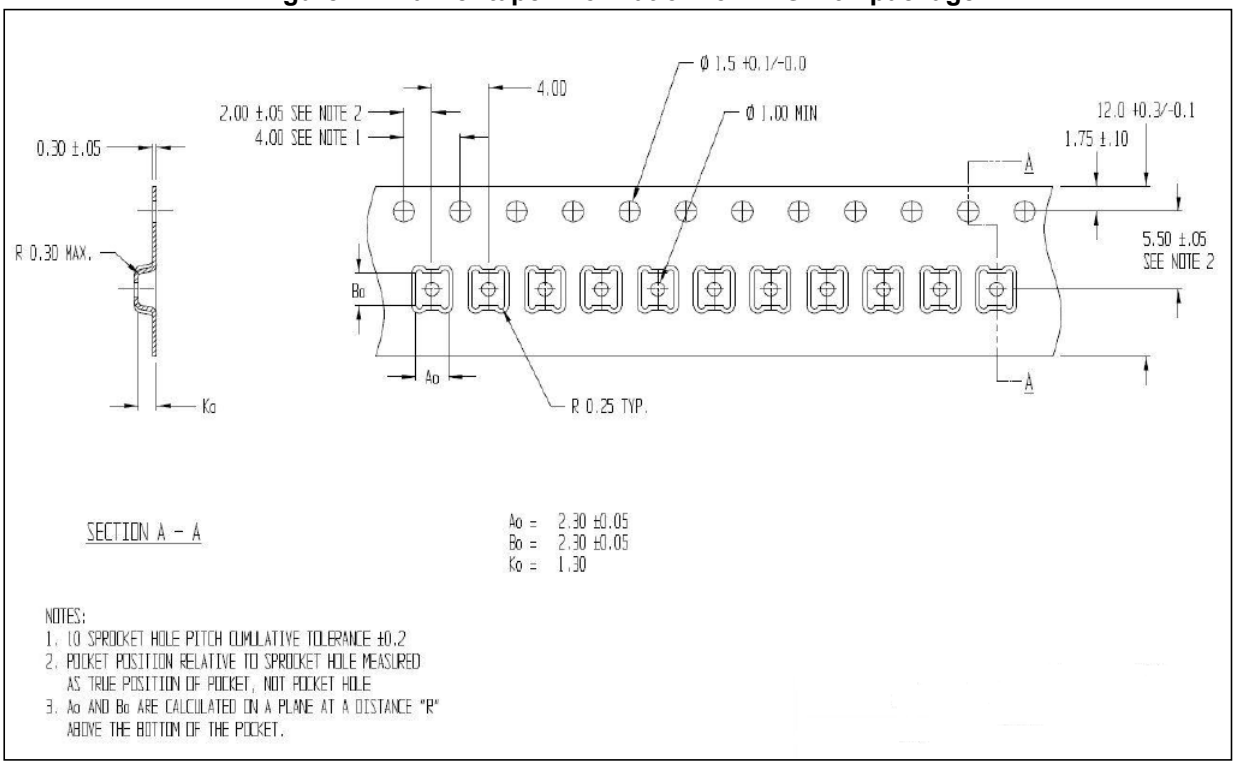


Figure 13. HLGA-6L package orientation in carrier tape

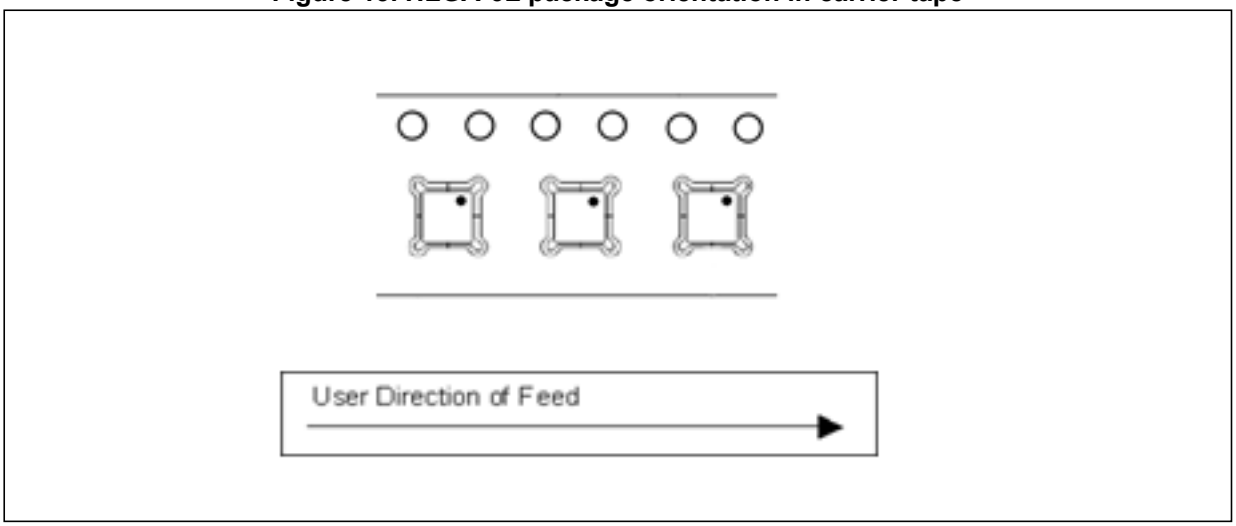


Figure 14. Reel information for carrier tape of HLGA-6L package

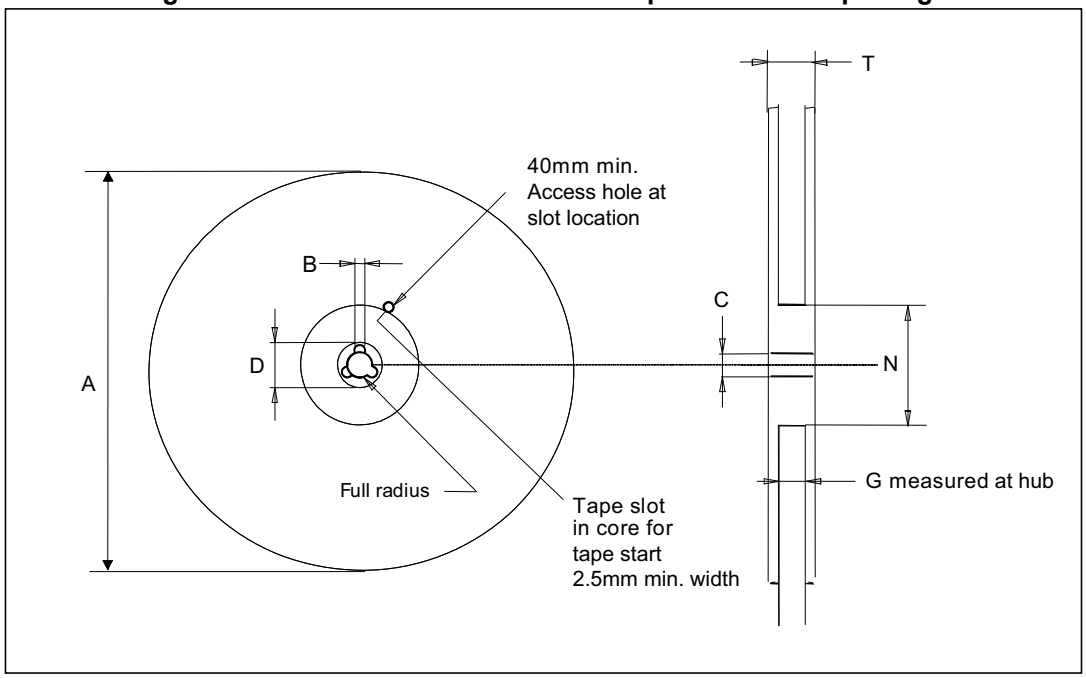


Table 21. Reel dimensions for carrier tape of HLGA-6L package

Reel dimensions (mm)	
A (max)	330
B (min)	1.5
C	13 ±0.25
D (min)	20.2
N (min)	60
G	12.4 +2/-0
T (max)	18.4

10 Revision history

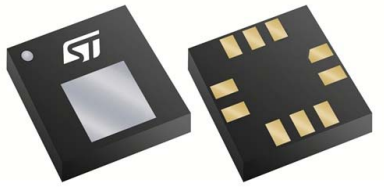
Table 22. Document revision history

Date	Revision	Changes
15-May-2014	1	Initial release
06-Apr-2015	2	Document reformatted to improve readability Updated: *Applications* and *Device summary* in cover page, *Table 2: Pin description*, *Section 4: Application hints*, *Section 5.1: I2C serial interface (CS = HIGH or unconnected CS)*, *Section 7: Register description* and *Section 8: Humidity and temperature data conversion*.
21-Oct-2015	3	Document update to align device performance confirmed in volume production
30-Aug-2016	4	Minor textual changes Added *Section 9.2: HLGA-6L packing information*

LPS22HB

MEMS nano pressure sensor: 260-1260 hPa absolute digital output barometer

Datasheet - production data



HLGA-10L
(2.0 x 2.0 x 0.76 mm)

Features

- 260 to 1260 hPa absolute pressure range
- Current consumption down to 3 µA
- High overpressure capability: 20x full-scale
- Embedded temperature compensation
- 24-bit pressure data output
- 16-bit temperature data output
- ODR from 1 Hz to 75 Hz
- SPI and I²C interfaces
- Embedded FIFO
- Interrupt functions: Data Ready, FIFO flags, pressure thresholds
- Supply voltage: 1.7 to 3.6 V
- High shock survivability: 22,000 *g*
- Small and thin package
- ECOPACK® lead-free compliant

Applications

- Altimeters and barometers for portable devices
- GPS applications
- Weather station equipment
- Sport watches

Description

The LPS22HB is an ultra-compact piezoresistive absolute pressure sensor which functions as a digital output barometer. The device comprises a sensing element and an IC interface which communicates through I^2C or SPI from the sensing element to the application.

The sensing element, which detects absolute pressure, consists of a suspended membrane manufactured using a dedicated process developed by ST.

The LPS22HB is available in a full-mold, holed LGA package (HLGA). It is guaranteed to operate over a temperature range extending from -40 °C to +85 °C. The package is holed to allow external pressure to reach the sensing element.

Table 1. Device summary

Order code	Temperature range [°C]	Package	Packing
LPS22HBTR	-40 to +85°C	HLGA-10L	Tape and reel

Contents

List of tables

List of figures

1 Block diagrams

Figure 1. Device architecture block diagram

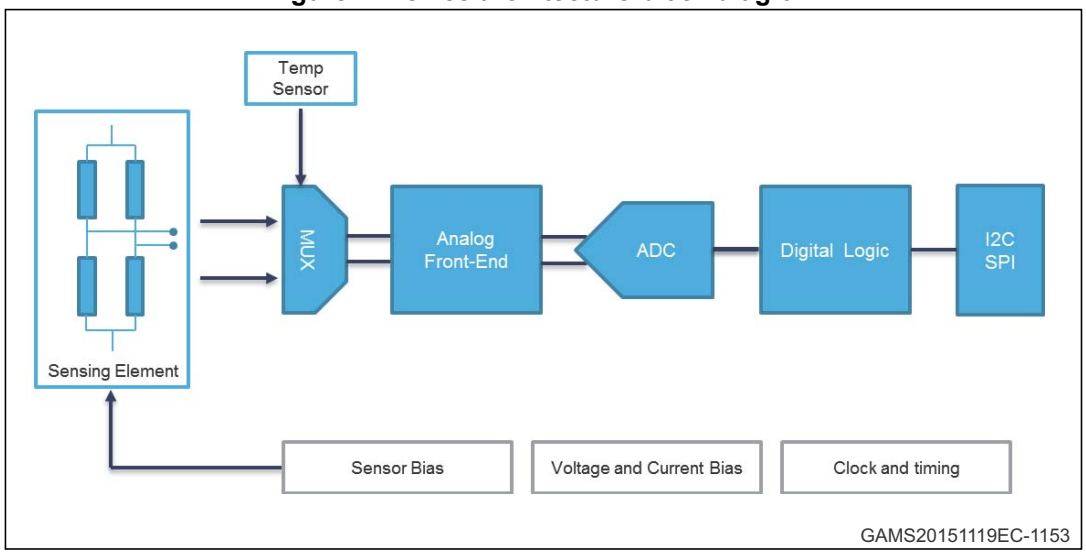
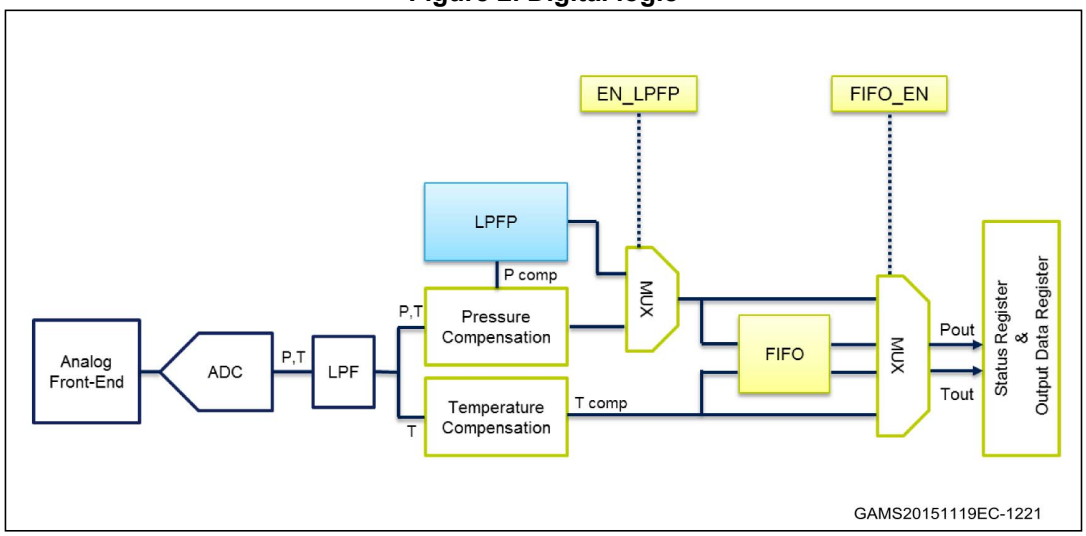


Figure 2. Digital logic



2 Pin description

Figure 3. Pin connections (bottom view)

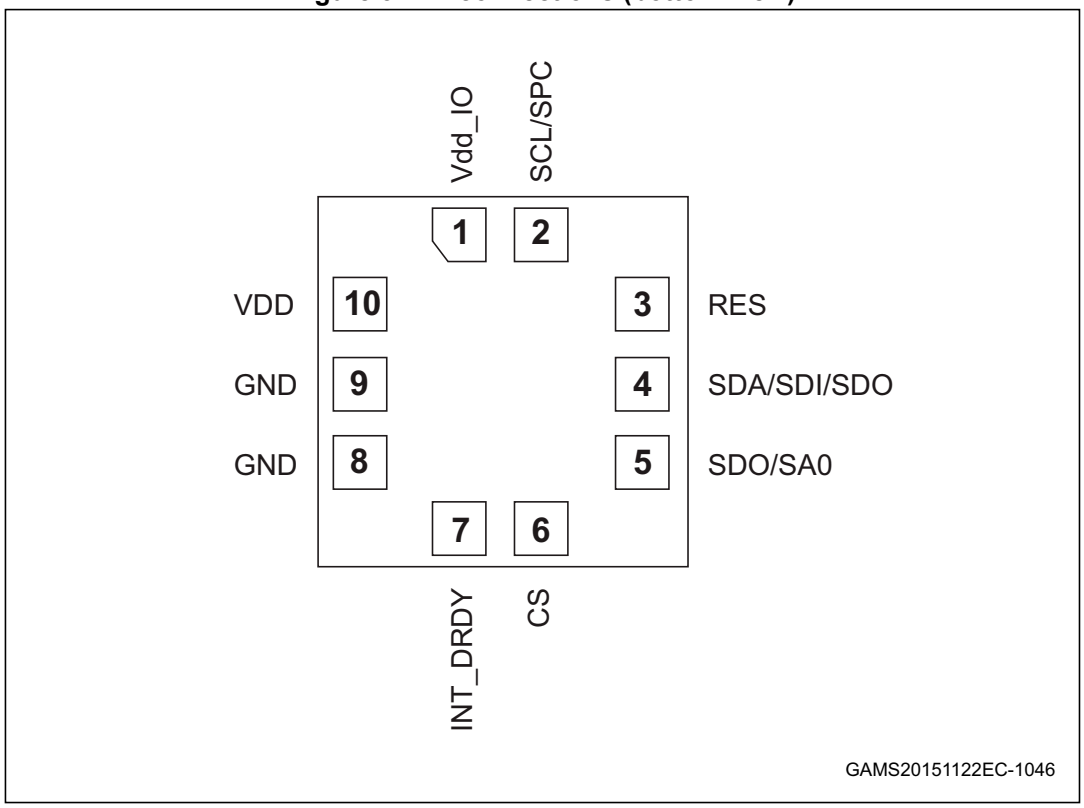


Table 2. Pin description

Pin number	Name	Function
1	Vdd_IO	Power supply for I/O pins
2	SCL SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)
3	Reserved	Connect to GND
4	SDA SDI SDI/SDO	I^2C serial data (SDA) 4-wire SPI serial data input (SDI) 3-wire serial data input/output (SDI/SDO)
5	SDO SA0	4-wire SPI serial data output (SDO) I^2C less significant bit of the device address (SA0)
6	CS	SPI enable I^2C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
7	INT_DRDY	Interrupt or Data Ready
8	GND	0 V supply
9	GND	0 V supply
10	VDD	Power supply

3 Mechanical and electrical specifications

3.1 Mechanical characteristics

VDD = 1.8 V, T = 25 °C, unless otherwise noted.

Table 3. Pressure and temperature sensor characteristics

Symbol	Parameter	Test condition	Min.	Typ.(1)	Max.	Unit
Pressure sensor characteristics						
PT_{op}	Operating temperature range		-40		+85	°C
PT_{full}	Full accuracy temperature range		0		+65	°C
P_{op}	Operating pressure range		260		1260	hPa
P_{bits}	Pressure output data			24		bits
P_{sens}	Pressure sensitivity			4096		LSB/ hPa
P_{AccRel}	Relative accuracy over pressure	P = 800 - 1100 hPa T = 25 °C		±0.1		hPa
P_{AccT}	Absolute accuracy over temperature	P_{op} T = 0 to 65 °C After OPC(2)		±0.1		hPa
		P_{op} T = 0 to 65 °C no OPC (2)		±1		
P_{noise}	RMS pressure sensing noise(3)	with embedded filtering		0.0075		hPa RMS
ODR_{Pres}	Pressure output data rate(4)			1 10 25 50 75		Hz
Temperature sensor characteristics						
T_{op}	Operating temperature range		-40		+85	°C
T_{sens}	Temperature sensitivity			100		LSB/°C
T_{acc}	Temperature absolute accuracy	T = 0 to 65 °C		±1.5		°C
ODR_T	Output temperature data rate(4)			1 10 25 50 75		Hz

1. Typical specifications are not guaranteed.
2. OPC: One-Point Calibration, see *RPDS_L (18h)*, *RPDS_H (19h)*.
3. Pressure noise RMS evaluated in a controlled environment, based on the average standard deviation of 50 measurements at highest ODR and with LC_EN bit = 0, EN_LPFP = 1, LPFP_CFG = 1.
4. Output data rate is configured acting on ODR[2:0] in *CTRL_REG1 (10h)*.

3.2 Electrical characteristics

VDD = 1.8 V, T = 25 °C, unless otherwise noted.

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.(1)	Max.	Unit
VDD	Supply voltage		1.7		3.6	V
Vdd_IO	IO supply voltage		1.7		Vdd+0.1	V
Idd	Supply current	@ ODR 1 Hz LC_EN bit = 0		12		µA
		@ ODR 1 Hz LC_EN bit = 1		3		
IddPdn	Supply current in power-down mode			1		µA

1. Typical specifications are not guaranteed.

Table 5. DC characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
DC input characteristics						
Vil	Low-level input voltage (Schmitt buffer)	-	-	-	0.2 * Vdd_IO	V
Vih	High-level input voltage (Schmitt buffer)	-	0.8 * Vdd_IO	-	-	V
DC output characteristics						
Vol	Low-level output voltage		-	-	0.2	V
Voh	High-level output voltage		Vdd_IO - 0.2	-	-	V

3.3 Communication interface characteristics

3.3.1 SPI - serial peripheral interface

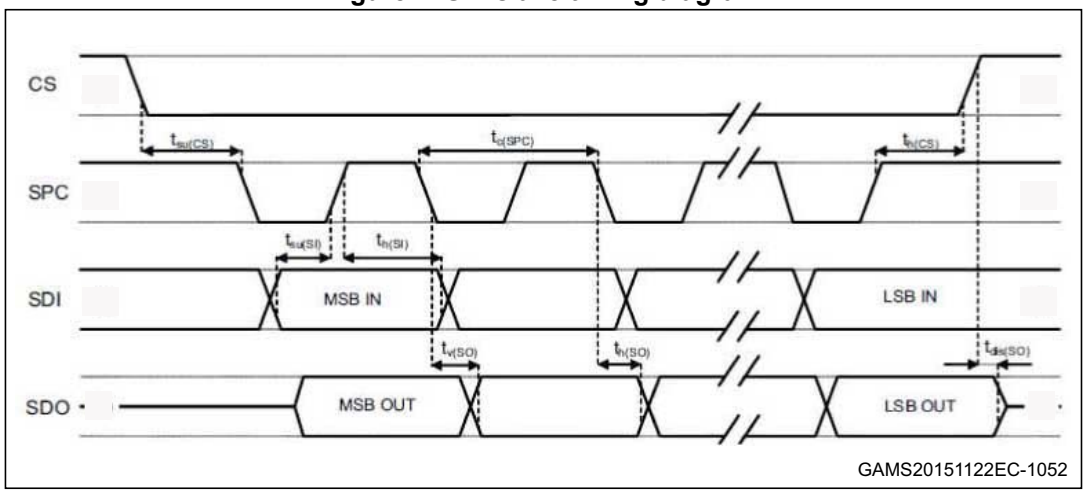
Subject to general operating conditions for Vdd and T_{OP}.

Table 6. SPI slave timing values

Symbol	Parameter	Value(1)		Unit
		Min	Max	
$t_{c(SPC)}$	SPI clock cycle	100		ns
$f_{c(SPC)}$	SPI clock frequency		10	MHz
$t_{su(CS)}$	CS setup time	6		ns
$t_{h(CS)}$	CS hold time	8		
$t_{su(SI)}$	SDI input setup time	5		
$t_{h(SI)}$	SDI input hold time	15		
$t_{v(SO)}$	SDO valid output time		50	
$t_{h(SO)}$	SDO output hold time	9		
$t_{dis(SO)}$	SDO output disable time		50	

1. Values are guaranteed at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production.

Figure 4. SPI slave timing diagram



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports.

3.3.2 I²C - inter-IC control interface

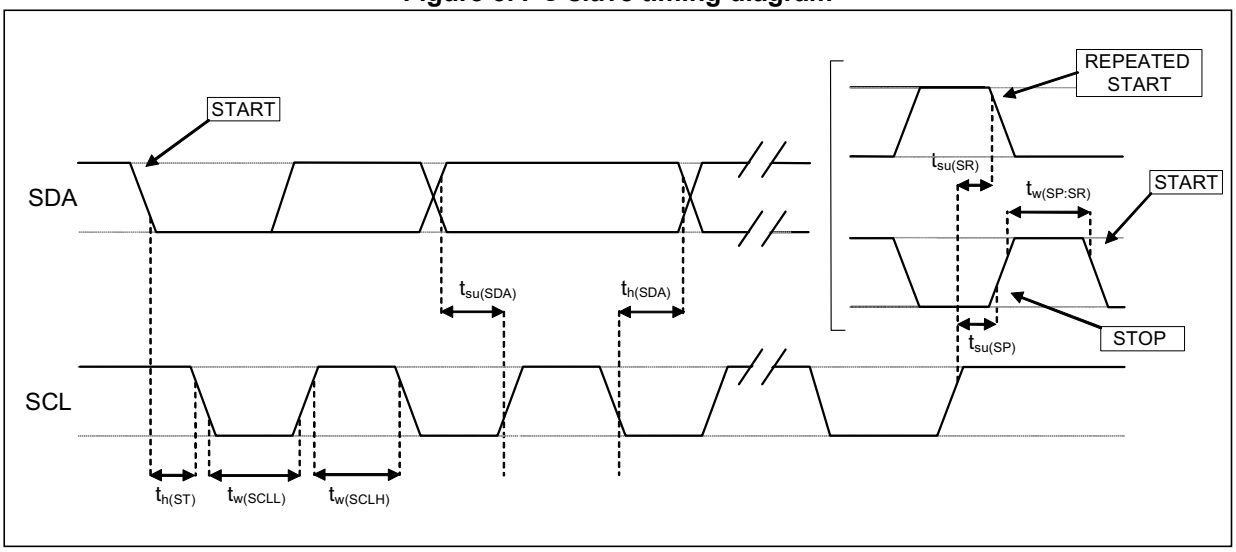
Subject to general operating conditions for Vdd and T_{OP}.

Table 7. I²C slave timing values

Symbol	Parameter (1)	I²C standard mode(1)		I²C fast mode(1)		Unit
		Min	Max	Min	Max	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	kHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0	3.45	0	0.9	µs
$t_{h(ST)}$	START condition hold time	4		0.6		µs
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(SP)}$	STOP condition setup time	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		

1. Data based on standard I²C protocol requirement, not tested in production.

Figure 5. I²C slave timing diagram



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports.

3.4 Absolute maximum ratings

Stress above those listed as “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 4.8	V
Vdd_IO	I/O pins supply voltage	-0.3 to 4.8	V
Vin	Input voltage on any control pin	-0.3 to Vdd_IO +0.3	V
P	Overpressure	2	MPa
T_{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection	2 (HBM)	kV

Note: Supply voltage on any pin should never exceed 4.8 V.

This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.

This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

4 Functionality

The LPS22HB is a high-resolution, digital output pressure sensor packaged in an HLGA full-mold package. The complete device includes a sensing element based on a piezoresistive Wheatstone bridge approach, and an IC interface which communicates a digital signal from the sensing element to the application.

4.1 Sensing element

An ST proprietary process is used to obtain a silicon membrane for MEMS pressure sensors. When pressure is applied, the membrane deflection induces an imbalance in the Wheatstone bridge piezoresistances whose output signal is converted by the IC interface.

4.2 IC interface

The complete measurement chain is composed of a low-noise amplifier which converts the resistance unbalance of the MEMS sensors (pressure and temperature) into an analog voltage using an analog-to-digital converter.

The pressure and temperature data may be accessed through an I²C/SPI interface thus making the device particularly suitable for direct interfacing with a microcontroller.

The LPS22HB features a Data-Ready signal which indicates when a new set of measured pressure and temperature data are available, thus simplifying data synchronization in the digital system that uses the device.

4.3 Factory calibration

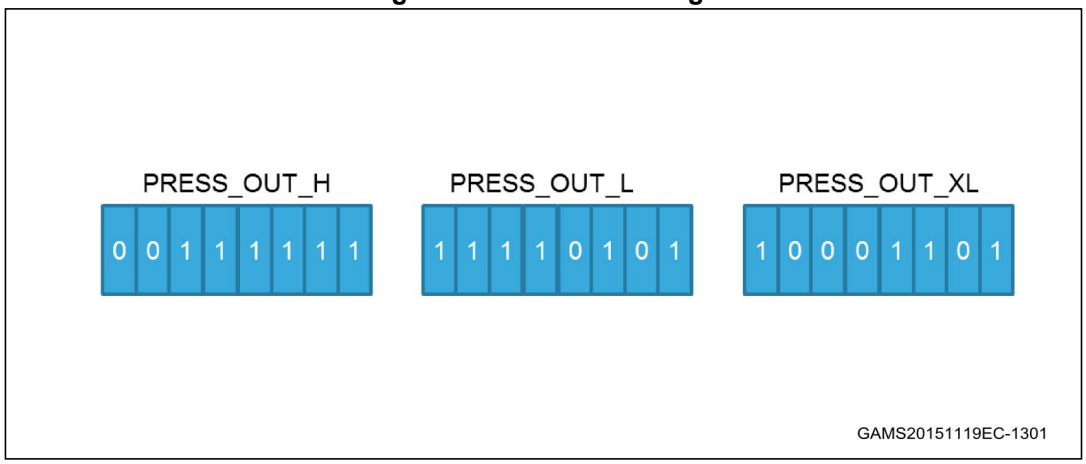
The trimming values are stored inside the device in a non-volatile structure. When the device is turned on, the trimming parameters are downloaded into the registers to be employed during the normal operation which allows the device to be used without requiring any further calibration.

4.4 Interpreting pressure readings

The pressure data are stored in 3 registers: *PRESS_OUT_H (2Ah)*, *PRESS_OUT_L (29h)*, and *PRESS_OUT_XL (28h)*. The value is expressed as 2’s complement.

To obtain the pressure in hPa, take the two’s complement of the complete word and then divide by 4096 LSB/hPa.

Figure 6. Pressure readings



Equation 1

$$\text{Pressure Value (LSB)} = \text{PRESS\_OUT\_H (2Ah) \& PRESS\_OUT\_L (29h) \& PRESS\_OUT\_XL (28h)} = \text{3FF58Dh} = 4191629 \text{ LSB (decimal signed)}$$

Equation 2

$$\text{Pressure (hPa)} = \frac{\text{Pressure Value (LSB)}}{\text{Scaling Factor}} = \frac{4191629 \text{ LSB}}{4096 \text{ LSB/hPa}} = 1023.3\text{hPa}$$

5 FIFO

The LPS22HB embeds 32 slots of 40-bit data FIFO to store the pressure and temperature output values. This allows consistent power saving for the system, since the host processor does not need to continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO. This buffer can work according to seven different modes: Bypass mode, FIFO mode, Stream mode, Dynamic-Stream mode, Stream-to-FIFO mode, Bypass-to-Stream and Bypass-to-FIFO mode. The FIFO buffer is enabled when the FIFO_EN bit in *CTRL_REG2 (11h)* is set to '1' and each mode is selected by the FIFO_MODE[2:0] bits in *FIFO_CTRL (14h)*. Programmable FIFO threshold status, FIFO overrun events and the number of unread samples stored are available in the *FIFO_STATUS (26h)* register and can be set to generate dedicated interrupts on the INT_DRDY pad using the *CTRL_REG3 (12h)* register.

FIFO_STATUS (26h)(FTH_FIFO) goes to '1' when the number of unread samples (*FIFO_STATUS (26h)*(FSS5:0)) is greater than or equal to WTM[4:0] in *FIFO_CTRL (14h)*. If *FIFO_CTRL (14h)*(WTM4:0) is equal to 0, *FIFO_STATUS (26h)*(FTH_FIFO) goes to '0'.

FIFO_STATUS (26h)(OVRN) is equal to '1' if a FIFO slot is overwritten.

FIFO_STATUS (26h)(FSS5:0) contains stored data levels of unread samples; when FSS[5:0] is equal to '000000' FIFO is empty, when FSS[5:0] is equal to '100000' FIFO is full and the unread samples are 32.

To guarantee the switching into and out of FIFO mode, discard the first sample acquired.

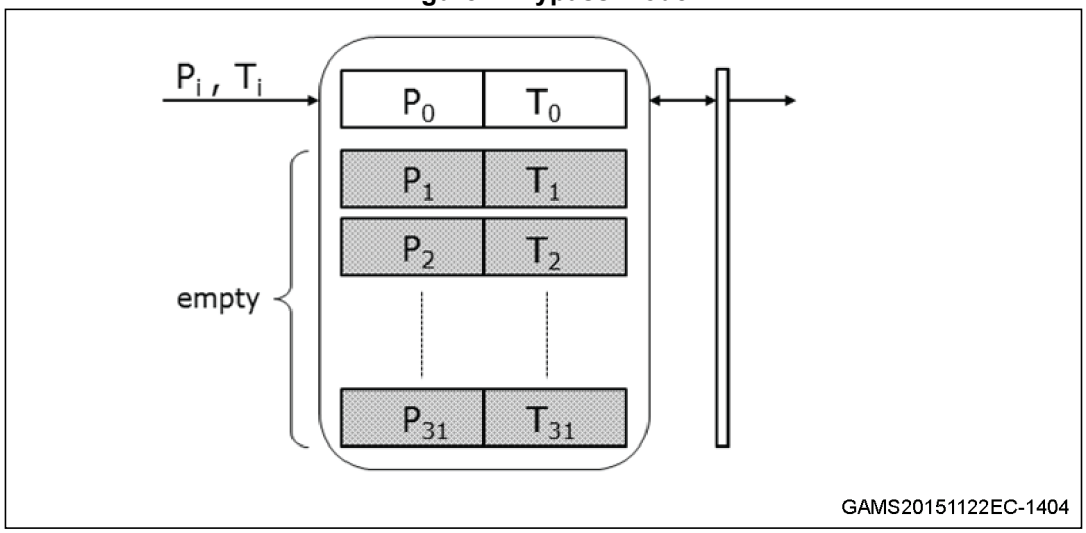
5.1 Bypass mode

In Bypass mode (*FIFO_CTRL (14h)*(FMODE2:0)=000), the FIFO is not operational and it remains empty.

Bypass mode is also used to reset the FIFO when in FIFO mode.

As described in the next figure, for each channel only the first address is used. When new data is available, the older data is overwritten.

Figure 7. Bypass mode



5.2 FIFO mode

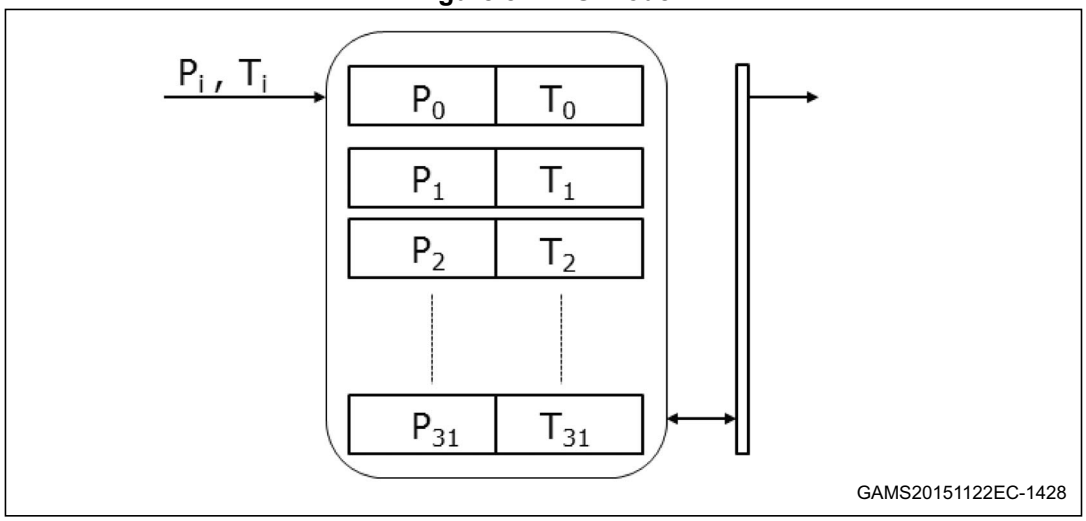
In FIFO mode (*FIFO_CTRL (14h)*(FMODE2:0) = 001) data from the output *PRESS_OUT_XL (28h)*, *PRESS_OUT_L (29h)*, *PRESS_OUT_H (2Ah)* and *TEMP_OUT_L (2Bh)*, *TEMP_OUT_H (2Ch)* are stored in the FIFO until it is overwritten.

To reset FIFO content, in Bypass mode the value '000' must be written in *FIFO_CTRL (14h)*(FMODE2:0). After this reset command, it is possible to restart FIFO mode, writing the value '001' in *FIFO_CTRL (14h)*(FMODE2:0).

FIFO buffer memorizes 32 levels of data but the depth of the FIFO can be resized by setting the *CTRL_REG2 (11h)*(STOP_ON_FTH) bit. If the STOP_ON_FTH bit is set to '1', FIFO depth is limited to *FIFO_CTRL (14h)*(WTM4:0) + 1 data.

A FIFO threshold interrupt can be enabled (F_OVR bit in *CTRL_REG3 (12h)* in order to be raised when the FIFO is filled to the level specified by the WTM4:0 bits of *FIFO_CTRL (14h)*. When a FIFO threshold interrupt occurs, the first data has been overwritten and the FIFO stops collecting data from the input pressure and temperature.

Figure 8. FIFO mode



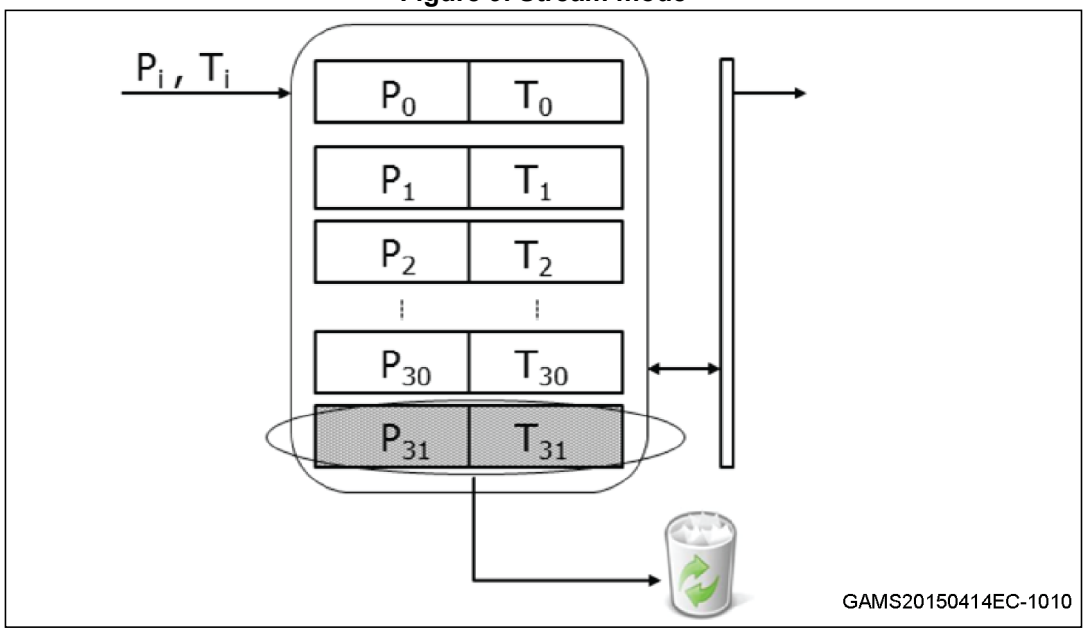
5.3 Stream mode

Stream mode (*FIFO_CTRL (14h)*(FMODE2:0) = 010) provides continuous FIFO update: as new data arrive, the older is discarded.

Once the entire FIFO has been read, the last data read remains in the FIFO and hence once a new sample is acquired, the *FIFO_STATUS (26h)*(FSS5:0) value rises from 0 to 2.

An overrun interrupt can be enabled, *CTRL_REG3 (12h)*(F_OVR) = '1', in order to inform when the FIFO is full and eventually read its content all at once. If an overrun occurs, the oldest sample in FIFO is overwritten, so if the FIFO was empty, the lost sample has already been read.

Figure 9. Stream mode



In the latter case reading all FIFO content before an overrun interrupt has occurred, the first data read is equal to the last already read in the previous burst, so the number of new data available in FIFO depends on the previous reading.

5.4 Dynamic-Stream mode

In Dynamic-Stream mode (*FIFO_CTRL (14h)*(FMODE2:0) = 110) after emptying the FIFO, the first new sample that arrives becomes the first to be read in a subsequent read burst. In this way, the number of new data available in FIFO does not depend on the previous reading.

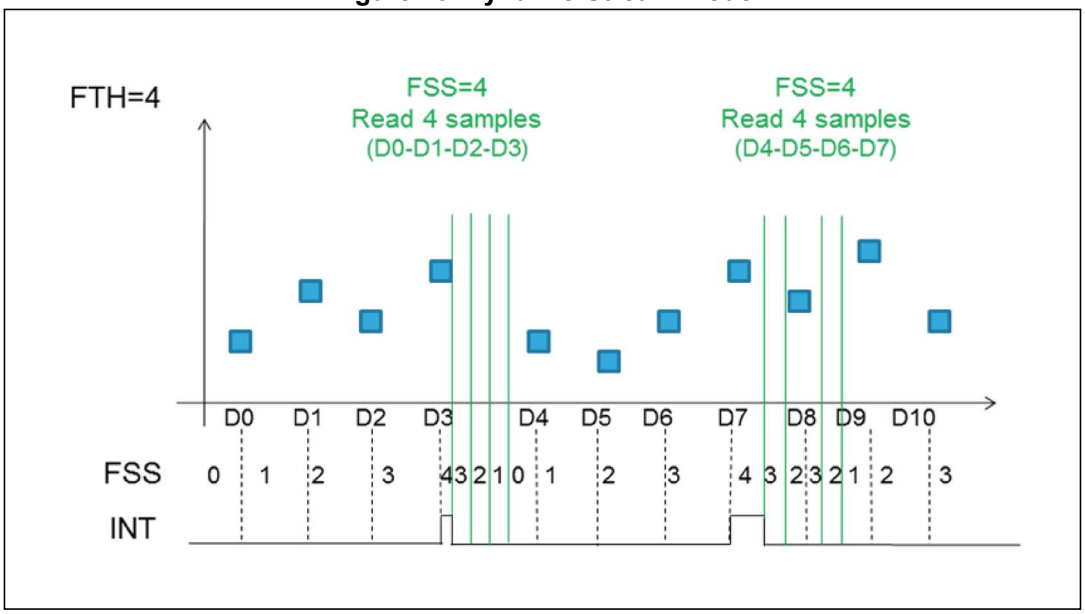
In Dynamic-Stream mode *FIFO_STATUS (26h)*(FSS5:0) is the number of new pressure and temperature samples available in the FIFO buffer.

Stream Mode is intended to be used to read all 32 samples of FIFO within an ODR after receiving an overrun signal.

Dynamic-Stream is intended to be used to read *FIFO_STATUS (26h)*(FSS5:0) samples when it is not possible to guarantee reading data within an ODR.

Also, a FIFO threshold interrupt on the INT_DRDY pad through*CTRL_REG3 (12h)*(F_FTH) can be enabled in order to read data from the FIFO and leave free memory slots for incoming data.

Figure 10. Dynamic-Stream mode



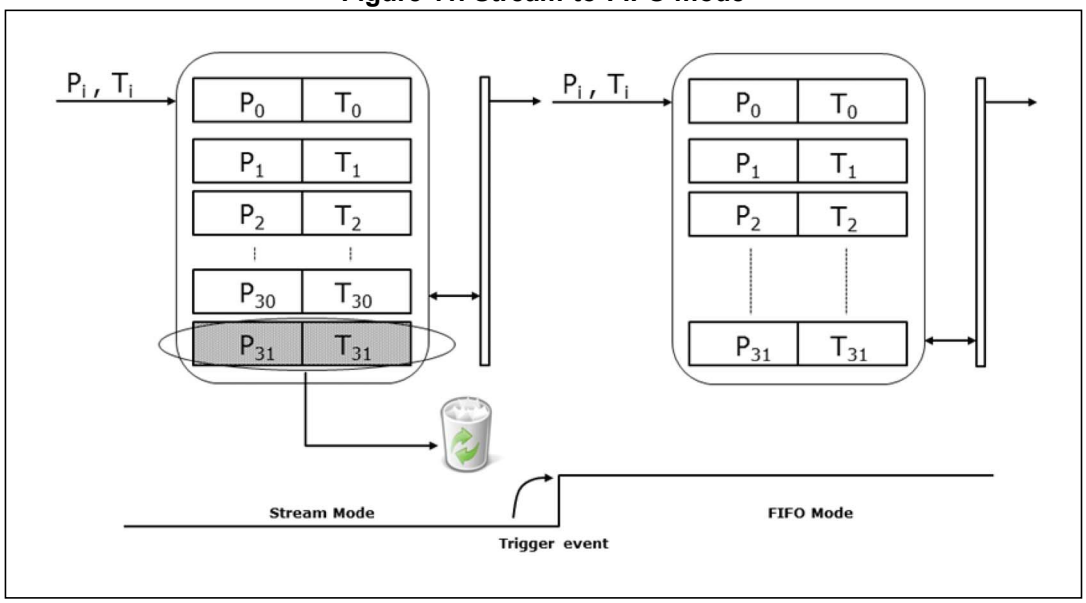
5.5 Stream-to-FIFO mode

In Stream-to-FIFO mode (*FIFO_CTRL (14h)*(FMODE2:0) = 011), FIFO behavior changes according to the INT_SOURCE(IA) bit. When the INT_SOURCE(IA) bit is equal to '1', FIFO operates in FIFO mode. When the INT_SOURCE(IA) bit is equal to '0', FIFO operates in Stream mode.

An interrupt generator can be set to the desired configuration through *INTERRUPT_CFG (0Bh)*.

The *INTERRUPT_CFG (0Bh)*(LIR) bit should be set to '1' in order to have latched interrupt.

Figure 11. Stream-to-FIFO mode



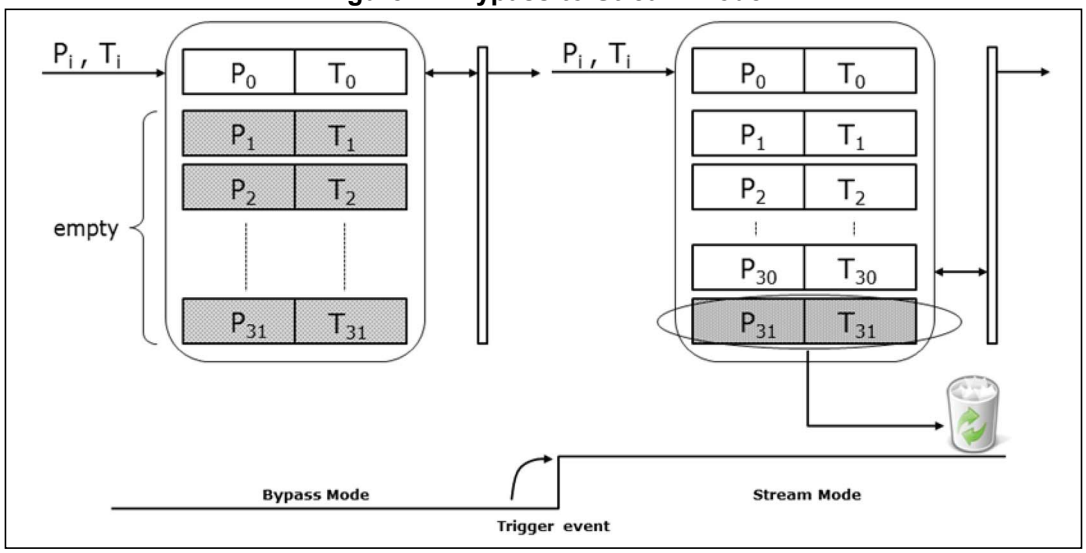
5.6 Bypass-to-Stream mode

In Bypass-to-Stream mode (*FIFO_CTRL (14h)*(FMODE2:0) = '100'), data measurement storage inside FIFO operates in Stream mode when INT_SOURCE(IA) is equal to '1', otherwise FIFO content is reset (Bypass mode).

An interrupt generator can be set to the desired configuration through *INTERRUPT_CFG (0Bh)*.

The *INTERRUPT_CFG (0Bh)*(LIR) bit should be set to '1' in order to have latched interrupt.

Figure 12. Bypass-to-Stream mode



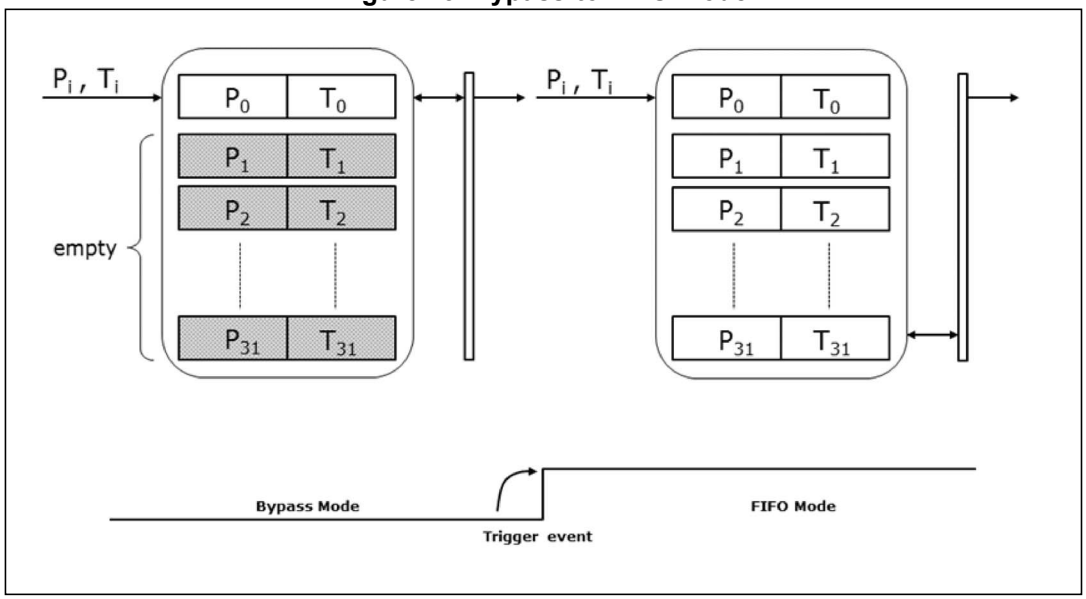
5.7 Bypass-to-FIFO mode

In Bypass-to-FIFO mode (*FIFO_CTRL (14h)*(FMODE2:0) = '111'), data measurement storage inside FIFO operates in FIFO mode when INT_SOURCE(IA) is equal to '1', otherwise FIFO content is reset (Bypass mode).

An interrupt generator can be set to the desired configuration through *INTERRUPT_CFG (0Bh)*.

The *INTERRUPT_CFG (0Bh)* (LIR) bit should be set to '1' in order to have latched interrupt.

Figure 13. Bypass-to-FIFO mode



5.8 Retrieving data from FIFO

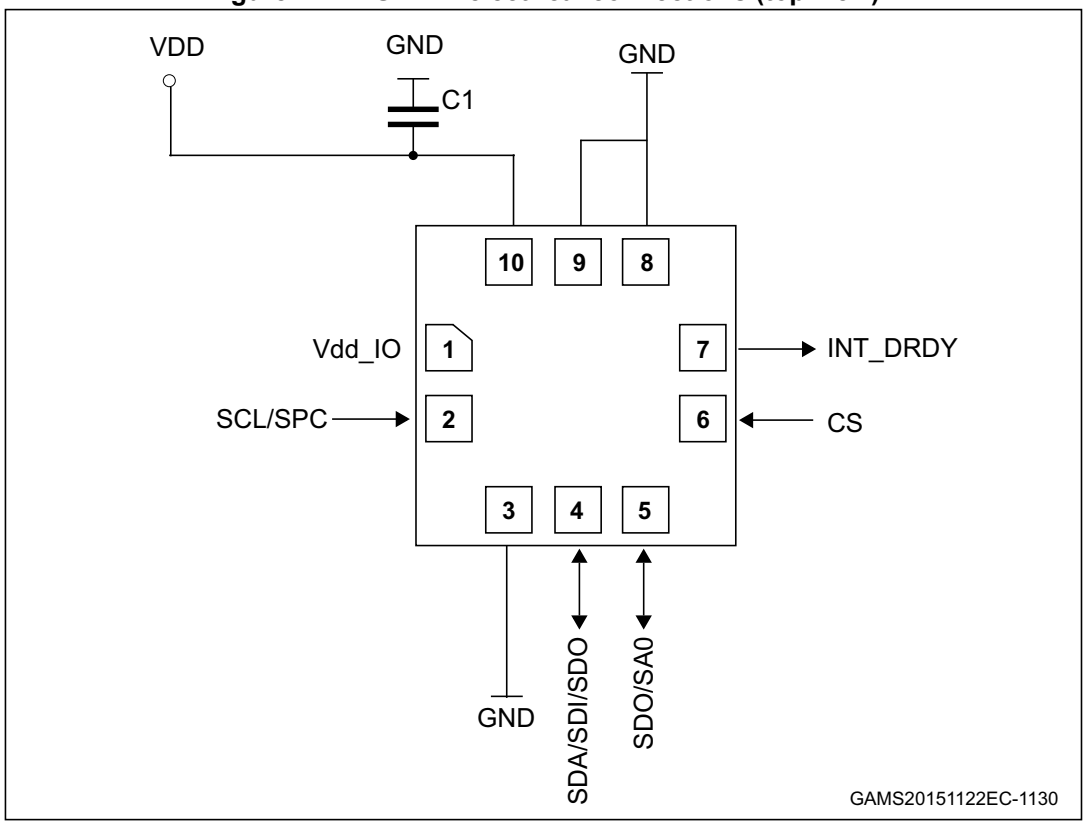
FIFO data is read from PRESS_OUT (Addr. reg 28h,29h,2Ah) and TEMP_OUT (Addr. reg 2Bh,2Ch).

Each time data is read from the FIFO, the oldest data are placed in the *PRESS_OUT_XL (28h)*, *PRESS_OUT_L (29h)*, *PRESS_OUT_H (2Ah)*, *TEMP_OUT_L (2Bh)* and *TEMP_OUT_H (2Ch)* registers and both single-read and read-burst operations can be used.

The device automatically updates the reading address and it rolls back to 28h when register 2Ch is reached. In order to read all FIFO levels in multiple byte reading, 160 bytes (5 output registers by 32 levels) must be read.

6 Application hints

Figure 14. LPS22HB electrical connections (top view)



The device power supply must be provided through the VDD line; a power supply decoupling capacitor C1 (100 nF) must be placed as near as possible to the supply pads of the device. Depending on the application, an additional capacitor of 4.7 µF could be placed on VDD line.

The functionality of the device and the measured data outputs are selectable and accessible through the I²C/SPI interface. When using the I^2C, CS must be tied to Vdd_IO.

All the voltage and ground supplies must be present at the same time to have proper behavior of the IC (refer to *Figure 14*). It is possible to remove VDD while maintaining Vdd_IO without blocking the communication bus, in this condition the measurement chain is powered off.

6.1 Soldering information

The HLGA package is compliant with the ECOPACK® standard, and it is qualified for soldering heat resistance according to JEDEC J-STD-020.

7 Digital interfaces

7.1 Serial interfaces

The registers embedded in the LPS22HB may be accessed through both the I²C and SPI serial interfaces. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped onto the same pads. To select/exploit the I²C interface, the CS line must be tied high (i.e. connected to Vdd_IO).

Table 9. Serial interface pin description

Pin name	Pin description
CS	SPI enable I²C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
SCL/SPC	I²C serial clock (SCL) SPI serial port clock (SPC)
SDA SDI SDI/SDO	I²C serial data (SDA) 4-wire SPI serial data input (SDI) 3-wire serial data input /output (SDI/SDO)
SDO SAO	SPI serial data output (SDO) I²C less significant bit of the device address (SA0)

7.2 I^2C serial interface (CS = High)

The LPS22HB I²C is a bus slave. The I²C is employed to write data into registers whose content can also be read back.

The relevant I²C terminology is given in *Table 10.*

Table 10. I^2C terminology

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I²C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both lines have to be connected to Vdd_IO through pull-up resistors.

The I²C interface is compliant with fast mode (400 kHz) I²C standards as well as with the normal mode.

7.2.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A start condition is defined as a HIGH-to-LOW transition on the data line while the SCL line is held HIGH. After the master has transmitted this, the bus is considered busy. The next data byte transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

The slave address (SAD) associated to the LPS22HB is 101110xb. The **SDO**/**SA0** pad can be used to modify the less significant bit of the device address. If the SA0 pad is connected to voltage supply, LSb is ‘1’ (address 1011101b), otherwise if the SA0 pad is connected to ground, the LSb value is ‘0’ (address 1011100b). This solution permits connecting and addressing two different LPS22HB devices to the same I²C lines.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded inside the ASIC behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge has been returned (SAK), an 8-bit sub-address will be transmitted (SUB): the 7 LSB represent the actual register address while the MSB has no meaning. The IF_ADD_INC bit in *CTRL_REG2 (11h)* enables sub-address auto increment (IF_ADD_INC is '1' by default), so if IF_ADD_INC = '1' the SUB (sub-address) will be automatically increased to allow multiple data read/write.

The slave address is completed with a Read/Write bit. If the bit is ‘1’ (Read), a repeated START (SR) condition must be issued after the two sub-address bytes; if the bit is ‘0’ (Write) the master will transmit to the slave with direction unchanged. *Table 11* explains how the SAD+read/write bit pattern is composed, listing all the possible configurations.

Table 11. SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	101110	0	1	10111001 (B9h)
Write	101110	0	0	10111000 (B8h)
Read	101110	1	1	10111011 (BBh)
Write	101110	1	0	10111010 (BAh)

Table 12. Transfer when master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 13. Transfer when master is writing multiple bytes to slave

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 14. Transfer when master is receiving (reading) one byte of data from slave

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 15. Transfer when master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the most significant bit (MSb) first. If a receiver cannot receive another complete byte of data until it has performed some other functions, it can hold the clock line, SCL LOW to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver does not acknowledge the slave address (i.e. it is not able to receive because it is performing some real-time function), the data line must be kept HIGH by the slave. The master can then abort the transfer. A LOW-to-HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

In order to read multiple bytes incrementing the register address, it is necessary to assert the most significant bit of the sub-address field. In other words, SUB(7) must be equal to 1 while SUB(6-0) represents the address of the first register to be read.

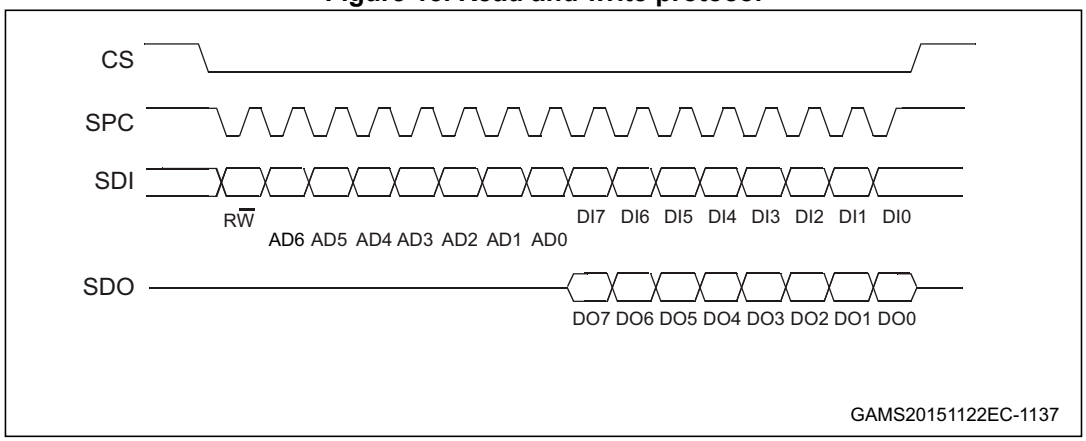
In the presented communication format MAK is Master acknowledge and NMAK is no master acknowledge.

7.3 SPI bus interface

The LPS22HB SPI is a bus slave. The SPI allows writing to and reading from the registers of the device.

The serial interface interacts with the application using 4 wires: **CS**, **SPC**, **SDI** and **SDO**.

Figure 15. Read and write protocol



CS is the serial port enable and it is controlled by the SPI master. It goes low at the start of the transmission and returns to high at the end. **SPC** is the serial port clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are respectively the serial port data input and output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or multiples of 8 in the case of multiple read/write bytes. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23,...) starts at the last falling edge of SPC just before the rising edge of **CS**.

bit 0: R$\overline{W}$ bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In the latter case, the chip will drive **SDO** at the start of bit 8.

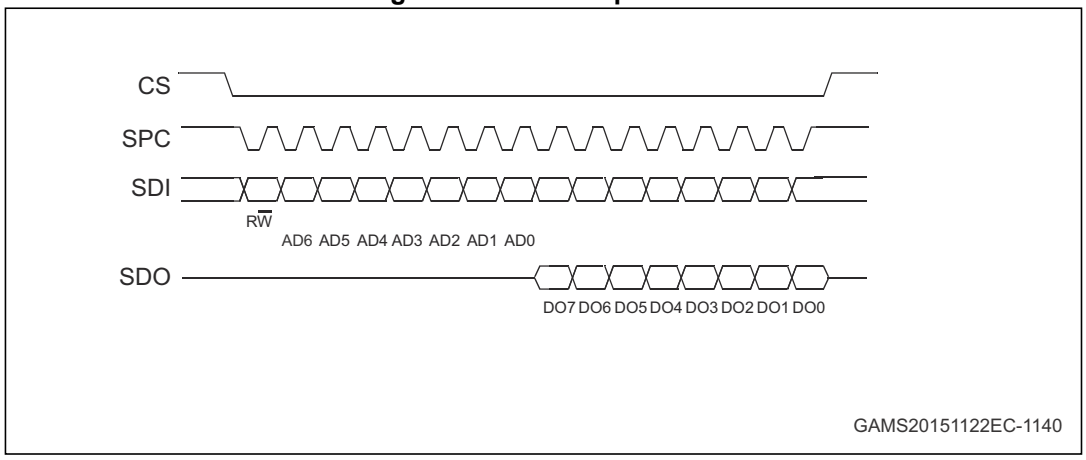
bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written into the device (MSb first).
bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).
In multiple read/write commands further blocks of 8 clock periods are added. When the IF_ADD_INC bit is 0, the address used to read/write data remains the same for every block. When the IF_ADD_INC bit is 1, the address used to read/write data is incremented at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

7.3.1 SPI read

Figure 16. SPI read protocol



The SPI read command is performed with 16 clock pulses. The multiple byte read command is performed by adding blocks of 8 clock pulses to the previous one.

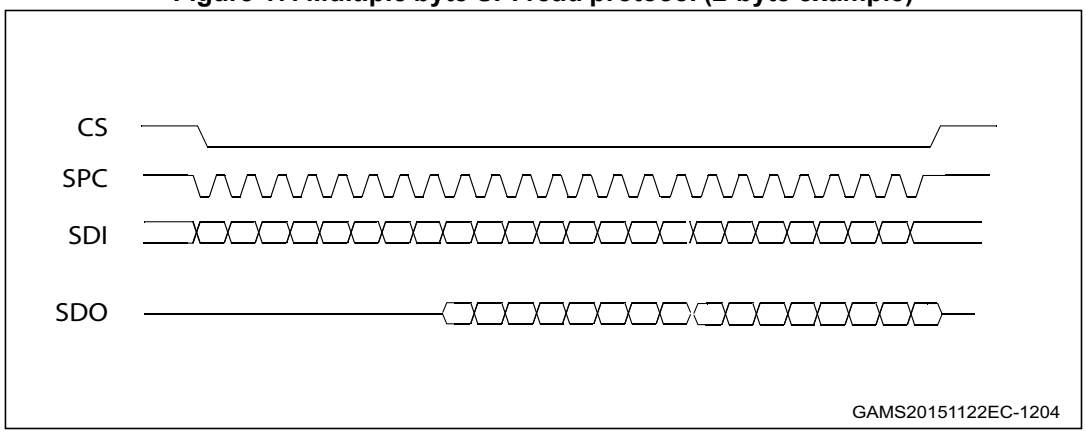
bit 0: READ bit. The value is 1.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

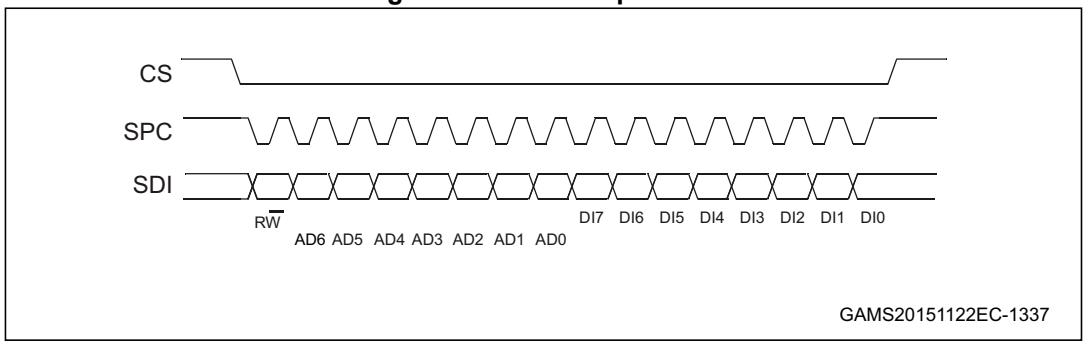
bit 16-...: data DO(...-8). Further data in multiple byte reads.

Figure 17. Multiple byte SPI read protocol (2-byte example)



7.3.2 SPI write

Figure 18. SPI write protocol



The SPI write command is performed with 16 clock pulses. The multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

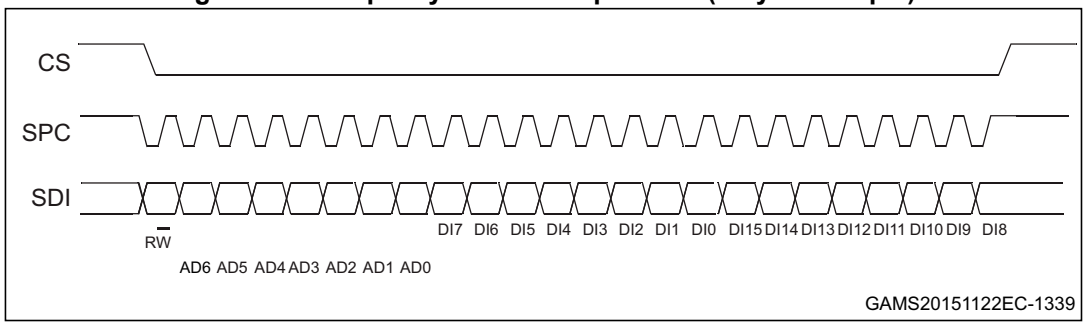
bit 0: WRITE bit. The value is 0.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written in the device (MSb first).

bit 16-...: data DI(...-8). Further data in multiple byte writes.

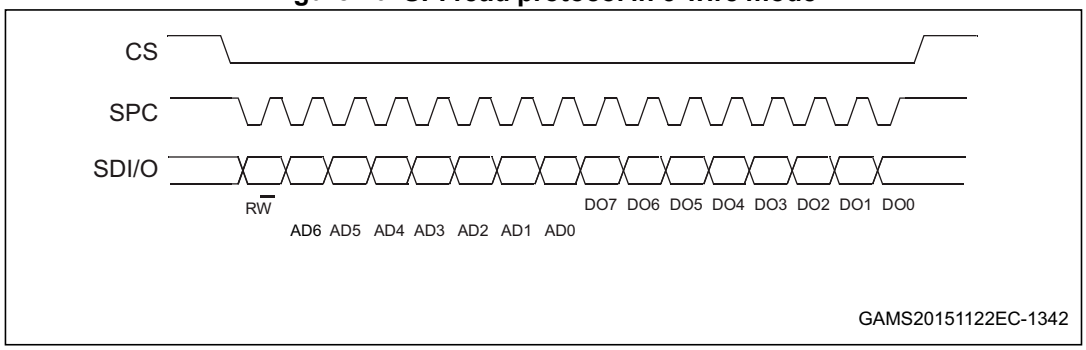
Figure 19. Multiple byte SPI write protocol (2-byte example)



7.3.3 SPI read in 3-wire mode

A 3-wire mode is entered by setting bit SIM to ‘1’ (SPI serial interface mode selection) in *CTRL_REG1 (10h)*.

Figure 20. SPI read protocol in 3-wire mode



The SPI read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).
A multiple read command is also available in 3-wire mode.

8 Register mapping

Table 16 provides a quick overview of the 8-bit registers embedded in the device.

Table 16. Registers address map

Name	Type	Register Address	Default	Function and comment
		Hex	Binary	
Reserved		00 - 0A	-	Reserved
INTERRUPT_CFG	R/W	0B	00000000	Interrupt register
THS_P_L	R/W	0C	00000000	Pressure threshold registers
THS_P_H	R/W	0D	00000000	
Reserved		0E	-	Reserved
WHO_AM_I	R	0F	10110001	Who am I
CTRL_REG1	R/W	10	00000000	Control registers
CTRL_REG2	R/W	11	00010000	
CTRL_REG3	R/W	12	00000000	
Reserved		13	-	Reserved
FIFO_CTRL	R/W	14	00000000	FIFO configuration register
REF_P_XL	R/W	15	00000000	Reference pressure registers
REF_P_L	R/W	16	00000000	
REF_P_H	R/W	17	00000000	
RPDS_L	R/W	18	00000000	Pressure offset registers
RPDS_H	R/W	19	00000000	
RES_CONF	R/W	1A	00000000	Resolution register
Reserved		1B - 24	-	Reserved
INT_SOURCE	R	25	output	Interrupt register
FIFO_STATUS	R	26	output	FIFO status register
STATUS	R	27	output	Status register
PRESS_OUT_XL	R	28	output	Pressure output registers
PRESS_OUT_L	R	29	output	
PRESS_OUT_H	R	2A	output	
TEMP_OUT_L	R	2B	output	Temperature output registers
TEMP_OUT_H	R	2C	output	
Reserved		2D - 32	-	Reserved
LPFP_RES	R	33	output	Filter reset register

Registers marked as Reserved must not be changed. Writing to those registers may cause permanent damage to the device.

To guarantee the proper behavior of the device, all register addresses not listed in the above table must not be accessed and the content stored in those registers must not be changed.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

9 Register description

The device contains a set of registers which are used to control its behavior and to retrieve pressure and temperature data. The register address, made up of 7 bits, is used to identify them and to read/write the data through the serial interface.

9.1 INTERRUPT_CFG (0Bh)

Interrupt mode for pressure acquisition configuration.

7	6	5	4	3	2	1	0
AUTORIFP	RESET_ARP	AUTOZERO	RESET_AZ	DIFF_EN	LIR	PLE	PHE

AUTORIFP	Enable AUTORIFP: function. Default value: 0 (0: normal mode; 1: AutoRifP enabled)
RESET_ARP	Reset AutoRifP function. Default value: 0 (0: normal mode; 1: reset AutoRifP function)
AUTOZERO	Enable Autozero function. Default value: 0 (0: normal mode; 1: Autozero enabled)
RESET_AZ	Reset Autozero function. Default value: 0 (0: normal mode; 1: reset Autozero function)
DIFF_EN	Enable interrupt generation. Default value: 0 (0: interrupt generation disabled; 1: interrupt generation enabled)
LIR	Latch interrupt request to the *INT_SOURCE (25h)* register. Default value: 0 (0: interrupt request not latched; 1: interrupt request latched)
PLE	Enable interrupt generation on pressure low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on pressure value lower than preset threshold)
PHE	Enable interrupt generation on pressure high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on pressure value higher than preset threshold)

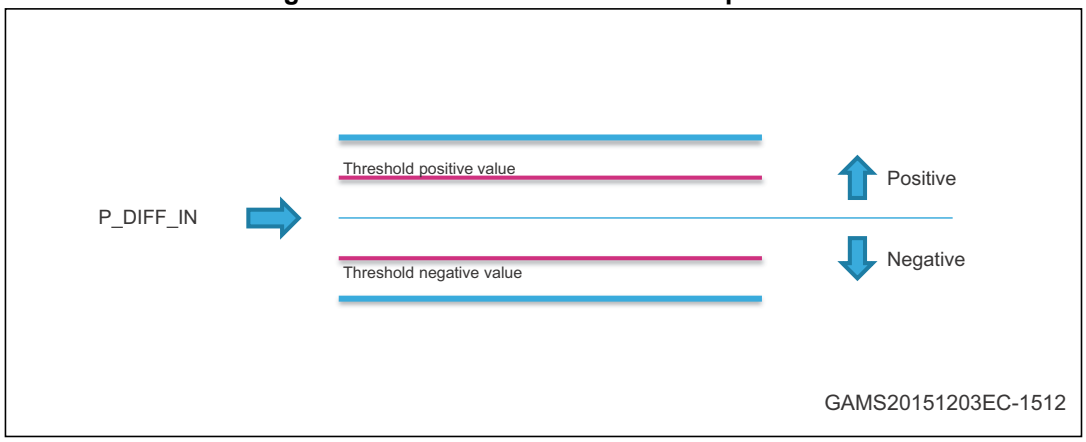
To generate an interrupt event based on a user-defined threshold, the **DIFF_EN** bit must be set to '1' and the threshold values stored in *THS_P_L (0Ch)* and *THS_P_H (0Dh)*.

When DIFF_EN = '1', the **PHE bit or PLE bit (or both bits)** have to be enabled.

When DIFF_EN is enabled and AUTOZERO or AUTORIFP is enabled, the defined pressure threshold values in THS_P (0Ch, 0Dh) is compared with:

P_DIFF_IN = measured pressure - REF_P

Figure 21. “Threshold based” interrupt event



If the **AUTOZERO** bit is set to '1', the measured pressure is used as the reference in the register REF_P (15h, 16h and 17h). From that point on, the output pressure registers **PRESS_OUT (28h, 29h and 2Ah)** are updated and the same value is also used for the interrupt generation:

- PRESS_OUT = measured pressure - REF_P
- P_DIFF_IN = measured pressure - REF_P

After the first conversion, the AUTOZERO bit is automatically set to '0'. To return back to normal mode, **RESET_AZ** bit has to be set to '1'. This resets also the content of the REF_P registers.

If the **AUTORIFP** bit is set to '1', the measured pressure is used as the reference in the register REF_P (15h, 16h and 17h). From that point on, the value used for the interrupt generation is the following:

- P_DIFF_IN = measured pressure - REF_P

The output registers **PRESS_OUT (28h, 29h and 2Ah)** show the difference between the measured pressure and the content of the RPDS registers (18h and 19h):

- PRESS_OUT = measured pressure - RPDS

After the first conversion, AUTORIFP bit is automatically set to '0'. To return back to normal mode, the **RESET_ARP** bit has to be set to '1'.

9.2 THS_P_L (0Ch)

User-defined threshold value for pressure interrupt event (Least significant bits).

7	6	5	4	3	2	1	0
THS7	THS6	THS5	THS4	THS3	THS2	THS1	THS0

THS[7:0]	This register contains the low part of threshold value for pressure interrupt generation.

The threshold value for pressure interrupt generation is a 16-bit unsigned right-justified value composed of *THS_P_H (0Dh)* and *THS_P_L (0Ch)*.The value is expressed as:

Interrupt threshold (hPa) = ±THS_P / 16

To enable the interrupt event based on this user-defined threshold, the DIFF_EN bit in *INTERRUPT_CFG (0Bh)* must be set to '1', the PHE bit or PLE bit (or both bits) in *INTERRUPT_CFG (0Bh)* has to be enabled.

9.3 THS_P_H (0Dh)

User-defined threshold value for pressure interrupt event (Most significant bits).

7	6	5	4	3	2	1	0
THS15	THS14	THS13	THS12	THS11	THS10	THS9	THS8

THS[15:8]	This register contains the high part of threshold value for pressure interrupt generation. Refer to *THS_P_L (0Ch)*.

9.4 WHO_AM_I (0Fh)

Device Who am I

7	6	5	4	3	2	1	0
1	0	1	1	0	0	0	1

9.5 CTRL_REG1 (10h)

Control register 1

7	6	5	4	3	2	1	0
0(1)	ODR2	ODR1	ODR0	EN_LPFP	LPFP_CFG	BDU	SIM

1. This bit must be set to '0' for proper operation of the device.

ODR[2:0]	Output data rate selection. Default value: 000 Refer to *Table 17*.
EN_LPFP	Enable low-pass filter on pressure data when Continuous mode is used. Default value: 0 (0: Low-pass filter disabled; 1: Low-pass filter enabled)
LPFP_CFG	LPFP_CFG: Low-pass configuration register. Default value:0 Refer to *Table 18*.
BDU(1)	Block data update. Default value: 0 (0: continuous update; 1: output registers not updated until MSB and LSB have been read(2))
SIM	SPI Serial Interface Mode selection.Default value: 0 (0: 4-wire interface; 1: 3-wire interface)

1. To guarantee the correct behavior of BDU feature, *PRESS_OUT_H (2Ah)* must be the last address read.
2. When I^2C is used with BDU=1, the IF_ADD_INC bit has to be set to '0' in *CTRL_REG2 (11h)* and only a single-byte read of the output registers is allowed.

Table 17. Output data rate bit configurations

ODR2	ODR1	ODR0	Pressure (Hz)	Temperature (Hz)
0	0	0	Power down / one-shot mode enabled	
0	0	1	1 Hz	1 Hz
0	1	0	10 Hz	10 Hz
0	1	1	25 Hz	25 Hz
1	0	0	50 Hz	50 Hz
1	0	1	75 Hz	75 Hz

When the ODR bits are set to '000', the device is in **Power-down mode**. When the device is in power-down mode, almost all internal blocks of the device are switched off to minimize power consumption. The I^2C interface is still active to allow communication with the device. The content of the configuration registers is preserved and output data registers are not updated, therefore keeping the last data sampled in memory before going into power-down mode.

If the ONE_SHOT bit in *CTRL_REG2 (11h)* is set to '1', **One-shot mode** is triggered and a new acquisition starts when it is required. Enabling this mode is possible only if the device was previously in power-down mode (ODR bits set to '000'). Once the acquisition is completed and the output registers updated, the device automatically enters in power-down mode. ONE_SHOT bit self-clears itself.

When the ODR bits are set to a value different than '000', the device is in **Continuous mode** and automatically acquires a set of data (pressure and temperature) at the frequency selected through the ODR[2:0] bits.

Once the additional low-pass filter has been enabled through the EN_LPFP bit, it is possible to configure the device bandwidth acting on the LPFP_CFG bit. See *Table 18* for low-pass filter configurations.

Table 18. Low-pass filter configurations

EN_LPFP	LPFP_CFG	Additional low-pass filter status	Device bandwidth
0	x	Disabled	ODR/2
1	0	Enabled	ODR/9
1	1	Enabled	ODR/20

The **BDU** bit is used to inhibit the update of the output registers between the reading of upper, middle and lower register parts. In default mode (BDU = '0'), the lower and upper register parts are updated continuously. When the BDU is activated (BDU = '1'), the content of the output registers is not updated until *PRESS_OUT_H (2Ah)* is read, avoiding the reading of values related to different samples.

9.6 CTRL_REG2 (11h)

Control register 2

7	6	5	4	3	2	1	0
BOOT	FIFO_EN	STOP_ON_FTH	IF_ADD_INC	I2C_DIS	SWRESET	0(1)	ONE_SHOT

1. This bit must be set to '0' for proper operation of the device

BOOT	Reboot memory content. Default value: 0 (0: normal mode; 1: reboot memory content). The bit is self-cleared when the BOOT is completed.
FIFO_EN	FIFO enable. Default value: 0 (0: disable; 1: enable)
STOP_ON_FTH	Stop on FIFO watermark. Enable FIFO watermark level use. Default value: 0 (0: disable; 1: enable)
IF_ADD_INC(1)	Register address automatically incremented during a multiple byte access with a serial interface (I^2C or SPI). Default value: 1 (0: disable; 1 enable)
I2C_DIS	Disable I^2C interface. Default value: 0 (0: I^2C enabled;1: I^2C disabled)
SWRESET	Software reset. Default value: 0 (0: normal mode; 1: software reset). The bit is self-cleared when the reset is completed.
ONE_SHOT	One-shot enable. Default value: 0 (0: idle mode; 1: a new dataset is acquired)

1. It is recommend to use a single-byte read (with IF_ADD_INC = 0) when output data registers are acquired without using the FIFO. If a read of the data occurs during the refresh of the output data register, it is recommended to set the BDU bit to '1' in *CTRL_REG1 (10h)* in order to avoid mixing data.

The **BOOT** bit is used to refresh the content of the internal registers stored in the Flash memory block. At device power-up, the content of the Flash memory block is transferred to the internal registers related to the trimming functions to allow correct behavior of the device itself. If for any reason the content of the trimming registers is modified, it is sufficient to use this bit to restore the correct values. When the BOOT bit is set to ‘1’, the content of the internal Flash is copied into the corresponding internal registers and is used to calibrate the device. These values are factory trimmed and they are different for every device. They allow the correct behavior of the device and normally they should not be changed. At the end of the boot process the BOOT bit is set again to ‘0’ by hardware. The BOOT bit takes effect after one ODR clock cycle.

SWRESET is the software reset bit. The following device registers (*INTERRUPT_CFG (0Bh)*, *THS_P_L (0Ch)*, *REF_P_H (17h)*, *CTRL_REG1 (10h)*, *CTRL_REG2 (11h)*, *CTRL_REG3 (12h)*, *FIFO_CTRL (14h)*, *REF_P_XL (15h)*, *REF_P_L (16h)*, *REF_P_H (17h)*) are reset to the default value if the SWRESET bit is set to '1'. The SWRESET bit returns to '0' by hardware.

The **ONE_SHOT** bit is used to start a new conversion when the ODR[2:0] bits in *CTRL_REG1 (10h)* are set to ‘000’. Writing a ‘1’ in ONE_SHOT triggers a single measurement of pressure and temperature. Once the measurement is done, the ONE_SHOT bit will self-clear, the new data are available in the output registers, and the *STATUS (27h)* bits are updated.

9.7 CTRL_REG3 (12h)

Control register 3 - INT_DRDY pin control register

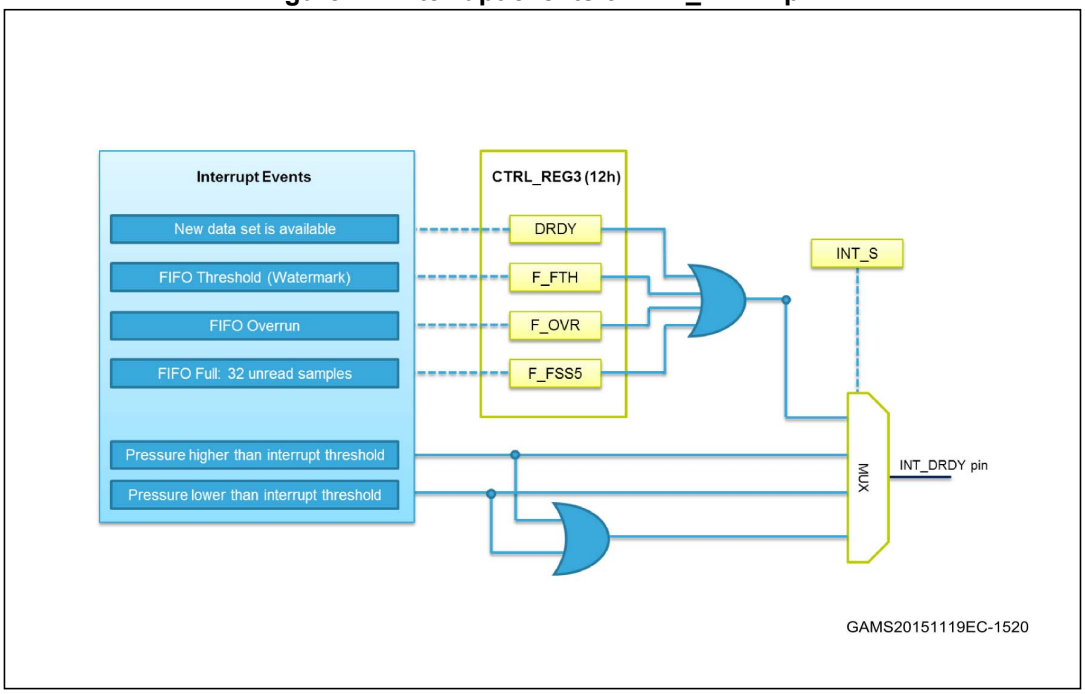
7	6	5	4	3	2	1	0
INT_H_L	PP_OD	F_FSS5	F_FTH	F_OVR	DRDY	INT_S2	INT_S1

INT_H_L	Interrupt active-high/low. Default value: 0 (0: active high; 1: active low)
PP_OD	Push-pull/open drain selection on interrupt pads. Default value: 0 (0: push-pull; 1: open drain)
F_FSS5	FIFO full flag on INT_DRDY pin. Default value: 0 (0: disable; 1: enable)
F_FTH	FIFO watermark status on INT_DRDY pin. Default value: 0 (0: disable; 1: enable)
F_OVR	FIFO overrun interrupt on INT_DRDY pin. Default value: 0 (0: disable; 1: enable)
DRDY	Data-ready signal on INT_DRDY pin. Default value: 0 (0: disable; 1: enable)
INT_S[2:1]	Data signal on INT_DRDY pin control bits. Default value: 00 Refer to *Table 19*.

Table 19. Interrupt configurations

INT_S2	INT_S1	INT_DRDY pin configuration
0	0	Data signal (in order of priority: DRDY or F_FTH or F_OVR or F_FSS5
0	1	Pressure high (P_high)
1	0	Pressure low (P_low)
1	1	Pressure low OR high

Figure 22. Interrupt events on INT_DRDY pin



9.8 FIFO_CTRL (14h)

FIFO control register

7	6	5	4	3	2	1	0
F_MODE2	F_MODE1	F_MODE0	WTM4	WTM3	WTM2	WTM1	WTM0

F_MODE[2:0]	FIFO mode selection. Default value: 000 Refer to *Table 20* and *Section 5* for additional details.
WTM[4:0]	FIFO watermark level selection.

Table 20. FIFO mode selection

F_MODE2	F_MODE1	F_MODE0	FIFO mode selection
0	0	0	Bypass mode
0	0	1	FIFO mode
0	1	0	Stream mode
0	1	1	Stream-to-FIFO mode
1	0	0	Bypass-to-Stream mode
1	0	1	Reserved
1	1	0	Dynamic-Stream mode
1	1	1	Bypass-to-FIFO mode

9.9 REF_P_XL (15h)

Reference pressure (LSB data)

7	6	5	4	3	2	1	0
REFL7	REFL6	REFL5	REFL4	REFL3	REFL2	REFL1	REFL0

REFL[7:0]	This register contains the low part of the reference pressure value.

The Reference pressure value is a 24-bit data and it is composed of *REF_P_H (17h)*, *REF_P_L (16h)* and *REF_P_XL (15h)*. The value is expressed as 2's complement.

The reference pressure value is used when AUTOZERO or AUTORIFP function is enabled. Please refer to *INTERRUPT_CFG (0Bh)* register description.

9.10 REF_P_L (16h)

Reference pressure (middle part)

7	6	5	4	3	2	1	0
REFL15	REFL14	REFL13	REFL12	REFL11	REFL10	REFL9	REFL8

REFL[15:8]	This register contains the mid part of the reference pressure value. Refer to *REF_P_XL (15h)*.

9.11 REF_P_H (17h)

Reference pressure (MSB part)

7	6	5	4	3	2	1	0
REFL23	REFL22	REFL21	REFL20	REFL19	REFL18	REFL17	REFL16

REFL[23:16]	This register contains the high part of the reference pressure value. Refer to *REF_P_XL (15h)*.

9.12 RPDS_L (18h)

Pressure offset (LSB data)

7	6	5	4	3	2	1	0
RPDS7	RPDS6	RPDS5	RPDS4	RPDS3	RPDS2	RPDS1	RPDS0

RPDS[7:0]	This register contains the low part of the pressure offset value.

The pressure offset value is 16-bit data that can be used to implement one-point calibration (OPC) after soldering. This value is composed of *RPDS_H (19h)* and *RPDS_L (18h)*. The value is expressed as 2’s complement.

9.13 RPDS_H (19h)

Pressure offset (MSB data)

7	6	5	4	3	2	1	0
RPDS15	RPDS14	RPDS13	RPDS12	RPDS11	RPDS10	RPDS9	RPDS8

RPDS[15:8]	This register contains the high part of the pressure offset value. Refer to *RPDS_L (18h)*.

9.14 RES_CONF (1Ah)

Low-power mode configuration

7	6	5	4	3	2	1	0
0(1)	0(1)	0(1)	0(1)	0(1)	0(1)	reserved(2)	LC_EN

1. These bits must be set to '0' for proper operation of the device.
2. The content of this bit must not be modified for proper operation of the device

LC_EN(1)	Low current mode enable. Default 0 0: Normal mode (low-noise mode); 1: Low-current mode.

1. The LC_EN bit must be changed only with the device in power down and not during operation. Once LC_EN bit is configured, it affects both One-shot mode and Continuous mode.

9.15 INT_SOURCE (25h)

Interrupt source

7	6	5	4	3	2	1	0
BOOT_STATUS	0	0	0	0	IA	PL	PH

BOOT_STATUS	If '1' indicates that the Boot (Reboot) phase is running.
IA	Interrupt active. (0: no interrupt has been generated; 1: one or more interrupt events have been generated).
PL	Differential pressure Low. (0: no interrupt has been generated; 1: low differential pressure event has occurred).
PH	Differential pressure High. (0: no interrupt has been generated; 1: high differential pressure event has occurred).

9.16 FIFO_STATUS (26h)

FIFO status

7	6	5	4	3	2	1	0
FTH_FIFO	OVR	FSS5	FSS4	FSS3	FSS2	FSS1	FSS0

FTH_FIFO	FIFO watermark status. (0: FIFO filling is lower than treshold level; 1: FIFO filling is equal or higher than treshold level).
OVR	FIFO overrun status. (0: FIFO is not completely full; 1: FIFO is full and at least one sample in the FIFO has been overwritten).
FSS[5:0]	FIFO stored data level. (000000: FIFO empty, 100000: FIFO is full and has 32 unread samples).

Table 21. FIFO_STATUS example: OVR/FSS details

FTH	OVRN	FSS5	FSS4	FSS3	FSS2	FSS1	FSS0	Description
0	0	0	0	0	0	0	0	FIFO empty
--(1)	0	0	0	0	0	0	1	1 unread sample
--								
--(1)	0	1	0	0	0	0	0	32 unread samples
1	1	1	0	0	0	0	0	At least one sample has been written

1. When the number of unread samples in FIFO is greater than the threshold level set in register *FIFO_CTRL (14h)*, the FTH value is ‘1’.

9.17 STATUS (27h)

Status register

7	6	5	4	3	2	1	0
--	--	T_OR	P_OR	--	--	T_DA	P_DA

T_OR	Temperature data overrun. (0: no overrun has occurred; 1: a new data for temperature has overwritten the previous data)
P_OR	Pressure data overrun. (0: no overrun has occurred; 1: new data for pressure has overwritten the previous data)
T_DA	Temperature data available. (0: new data for temperature is not yet available; 1: a new temperature data is generated)
P_DA	Pressure data available. (0: new data for pressure is not yet available; 1: a new pressure data is generated)

This register is updated every ODR cycle.

9.18 PRESS_OUT_XL (28h)

Pressure output value (LSB)

7	6	5	4	3	2	1	0
POUT7	POUT6	POUT5	POUT4	POUT3	POUT2	POUT1	POUT0

POUT[7:0]	This register contains the low part of the pressure output value.

The pressure output value is a 24-bit data that contains the measured pressure. It is composed of *PRESS_OUT_H (2Ah)*, *PRESS_OUT_L (29h)* and *PRESS_OUT_XL (28h)*. The value is expressed as 2's complement.

The output pressure register **PRESS_OUT** is provided as the difference between the measured pressure and the content of the register RPDS (18h, 19h)*.

Please refer to *Section 4.4: Interpreting pressure readings* for additional info.

*DIFF_EN = '0', AUTOZERO = '0', AUTORIFP = '0'

9.19 PRESS_OUT_L (29h)

Pressure output value (mid part)

7	6	5	4	3	2	1	0
POUT15	POUT14	POUT13	POUT12	POUT11	POUT10	POUT9	POUT8

POUT[15:8]	This register contains the mid part of the pressure output value. Refer to *PRESS_OUT_XL (28h)*

9.20 PRESS_OUT_H (2Ah)

Pressure output value (MSB)

7	6	5	4	3	2	1	0
POUT23	POUT22	POUT21	POUT20	POUT19	POUT18	POUT17	POUT16

POUT[23:16]	This register contains the high part of the pressure output value. Refer to *PRESS_OUT_XL (28h)*

9.21 TEMP_OUT_L (2Bh)

Temperature output value (LSB)

7	6	5	4	3	2	1	0
TOUT7	TOUT6	TOUT5	TOUT4	TOUT3	TOUT2	TOUT1	TOUT0

TOUT[7:0]	This register contains the low part of the temperature output value.

The temperature output value is 16-bit data that contains the measured temperature. It is composed of *TEMP_OUT_H (2Ch)*, and *TEMP_OUT_L (2Bh)*. The value is expressed as 2’s complement.

9.22 TEMP_OUT_H (2Ch)

Temperature output value (MSB)

7	6	5	4	3	2	1	0
TOUT15	TOUT14	TOUT13	TOUT12	TOUT11	TOUT10	TOUT9	TOUT8

TOUT[15:8]	This register contains the high part of the temperature output value.

9.23 LPFP_RES (33h)

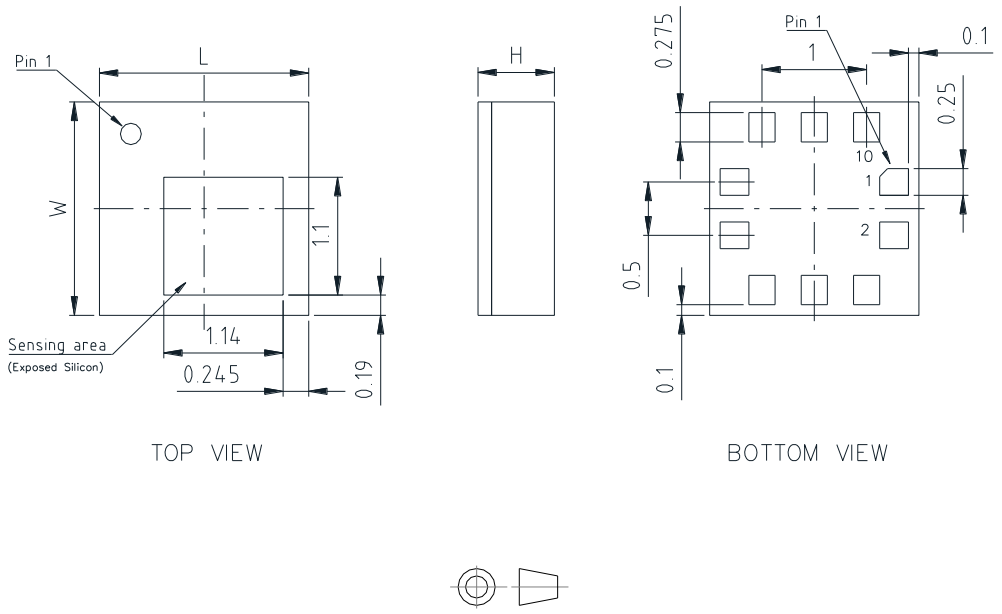
Low-pass filter reset register. If the LPFP is active, in order to avoid the transitory phase, the filter can be reset by reading this register before generating pressure measurements.

10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

10.1 HLGA-10L package information

Figure 23. HLGA-10L (2.0 x 2.0 x 0.76 mm typ.) package outline and mechanical dimensions



Dimensions arein millimeter unless otherwise specified
General Tolerance is +/-0.1mm unless otherwise specified

OUTER DIMENSIONS

ITEM	DIMENSION [mm]	TOLERANCE [mm]
Length [L]	2	±0.1
Width [W]	2	±0.1
Height [H]	0.8 max	/

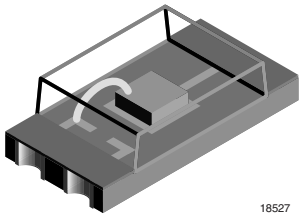
8479831_3

11 Revision history

Table 22. Document revision history

Date	Revision	Changes
29-Oct-2014	1	Initial release.
05-May-2015	2	Datasheet status promoted from “Target specification” to “Preliminary data”. Updated: note 2 in Table 3: Pressure and temperature sensor characteristics, Section 4: FIFO, Table 20: FIFO mode selection and the following registers: FIFO_STATUS (26h), CTRL_REG1 (10h), CTRL_REG2 (11h), Section 9: Package mechanical data.
04-Sep-2015	3	Datasheet status promoted from “Preliminary data” to “Production data”. Updates: *Table 1: Device summary*, Sections: *4.2: IC interface*, *4.3: Factory calibration*, *7.1: Serial interfaces*, *Table 17: Output data rate bit configurations* and *9.17: STATUS (27h)*.
15-Dec-2015	4	Updated: *Section 1: Block diagrams*, *Section 4.4: Interpreting pressure readings*, *Table 16: Registers address map*, *Figure 21*. Added: *TEMP_OUT_H (2Ch)* and *LPFP_RES (33h)*. Minor text changes.
22-Nov-2016	5	Added footnote *2* to *CTRL_REG1 (10h)* Minor textual updates
29-Jun-2017	6	Updated Vol and Voh in *Table 5: DC characteristics* Updated *Table 7: I^2C slave timing values* and *Figure 5: I^2C slave timing diagram* Updated *Table 16: Registers address map* Added footnote *1* to IF_ADD_INC bit in *CTRL_REG2 (11h)*

Ambient Light Sensor



FEATURES

- Package type: surface mount
- Package form: 1206
- Dimensions (L x W x H in mm): 4 x 2 x 1.05
- AEC-Q101 qualified
- High photo sensitivity
- Adapted to human eye responsivity
- Angle of half sensitivity: φ = ± 60°
- Floor life: 168 h, MSL 3, acc. J-STD-020
- Lead (Pb)-free reflow soldering
- Compliant to RoHS Directive 2002/95/EC and in accordance to WEEE 2002/96/EC

AUTOMOTIVE GRADE

Pb-free

e4

RoHS COMPLIANT

GREEN (5-2008)**

Note

** Please see document “Vishay Material Category Policy”: www.vishay.com/doc?99902

DESCRIPTION

TEMT6000X01 ambient light sensor is a silicon NPN epitaxial planar phototransistor in a miniature transparent 1206 package for surface mounting. It is sensitive to visible light much like the human eye and has peak sensitivity at 570 nm.

APPLICATIONS

Ambient light sensor for control of display backlight dimming in LCD displays and keypad backlighting of mobile devices and in industrial on/off-lighting operation.

- Automotive sensors
- Mobile phones
- Notebook computers
- PDA’s
- Cameras
- Dashboards

PRODUCT SUMMARY			
COMPONENT	I_{PCE} (µA)	φ (deg)	$\lambda_{0.5}$ (nm)
TEMT6000X01	50	± 60	440 to 800

Note

- Test condition see table “Basic Characteristics”

ORDERING INFORMATION			
ORDERING CODE	PACKAGING	REMARKS	PACKAGE FORM
TEMT6000X01	Tape and reel	MOQ: 3000 pcs, 3000 pcs/reel	1206

Note

- MOQ: minimum order quantity

ABSOLUTE MAXIMUM RATINGS (T_{amb} = 25 °C, unless otherwise specified)				
PARAMETER	TEST CONDITION	SYMBOL	VALUE	UNIT
Collector emitter voltage		V_{CEO}	6	V
Emitter collector voltage		V_{ECO}	1.5	V
Collector current		I_C	20	mA
Power dissipation		P_V	100	mW

ABSOLUTE MAXIMUM RATINGS (T_{amb} = 25 °C, unless otherwise specified)				
PARAMETER	**TEST CONDITION**	**SYMBOL**	**VALUE**	**UNIT**
Junction temperature		T_j	100	°C
Operating temperature range		T_{amb}	- 40 to + 100	°C
Storage temperature range		T_{stg}	- 40 to + 100	°C
Soldering temperature	Acc. reflow solder profile fig. 8	T_{sd}	260	°C
Thermal resistance junction/ambient	Soldered on PCB with pad dimensions: 4 mm x 4 mm	R_{thJA}	450	K/W

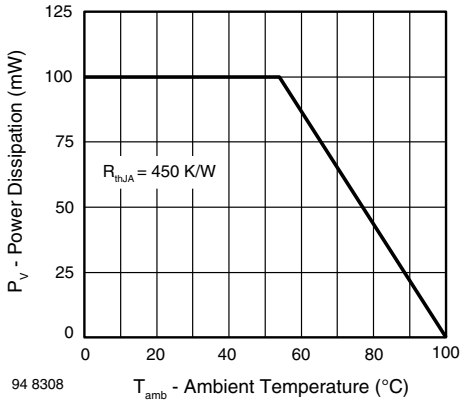


Fig. 1 - Power Dissipation Limit vs. Ambient Temperature

BASIC CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)						
PARAMETER	**TEST CONDITION**	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Collector emitter breakdown voltage	I_C = 0.1 mA	V_{CEO}	6			V
Collector dark current	V_{CE} = 5 V, E = 0	I_{CEO}		3	50	nA
Collector emitter capacitance	V_{CE} = 0 V, f = 1 MHz, E = 0	C_{CEO}		16		pF
Collector light current	E_V = 20 lx, CIE illuminant A, V_{CE} = 5 V	I_{PCE}	3.5	10	16	µA
	E_V = 100 lx, CIE illuminant A, V_{CE} = 5 V	I_{PCE}		50		µA
Temperature coefficient of I_{PCE}	CIE illuminant A	TK_{IPCE}		1.18		%/K
	LED, white	TK_{IPCE}		0.9		%/K
Angle of half sensitivity		φ		± 60		deg
Wavelength of peak sensitivity		λ_p		570		nm
Range of spectral bandwidth		$\lambda_{0.5}$		440 to 800		nm
Collector emitter saturation voltage	E_V = 20 lx, CIE illuminant A, I_{PCE} = 1.2 µA	V_{CEsat}		0.1		V

BASIC CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)

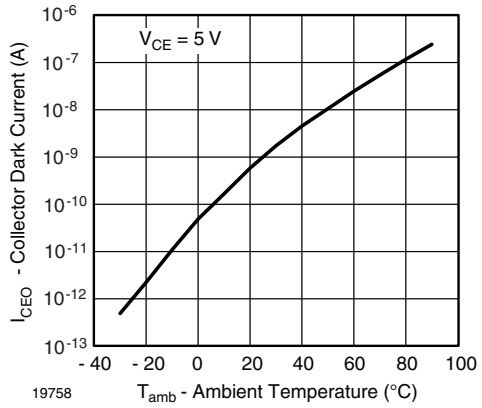


Fig. 1 - Collector Dark Current vs. Ambient Temperature

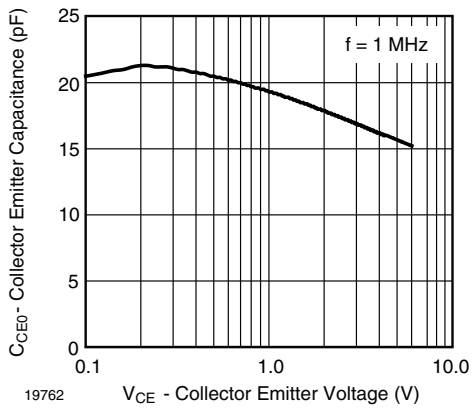


Fig. 4 - Collector Emitter Capacitance vs. Collector Emitter Voltage

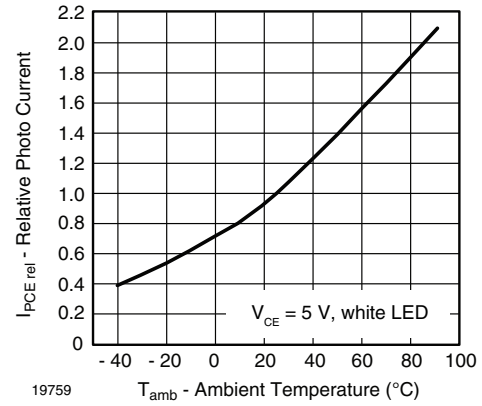


Fig. 2 - Relative Photo Current vs. Ambient Temperature

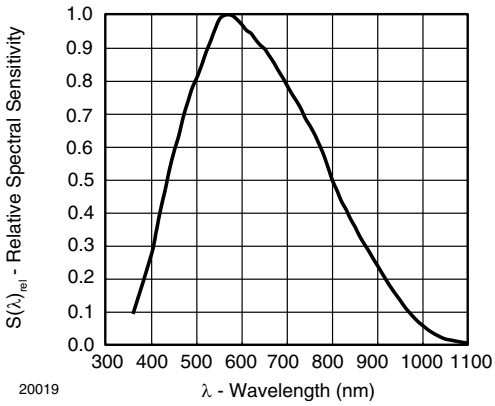


Fig. 5 - Relative Spectral Sensitivity vs. Wavelength

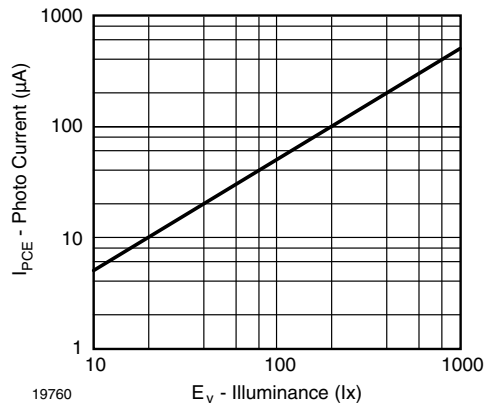


Fig. 3 - Photo Current vs. Illuminance

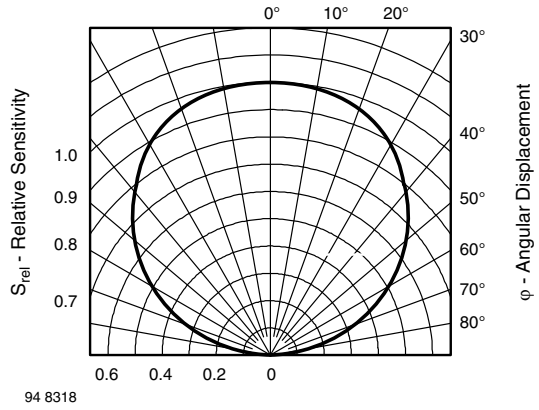


Fig. 6 - Relative Radiant Sensitivity vs. Angular Displacement

REFLOW SOLDER PROFILE

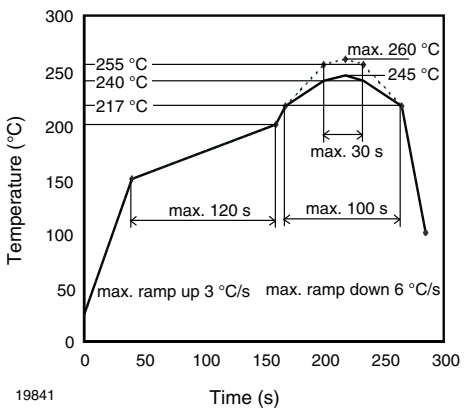


Fig. 7 - Lead (Pb)-free Reflow Solder Profile acc. J-STD-020D

DRYPACK

Devices are packed in moisture barrier bags (MBB) to prevent the products from moisture absorption during transportation and storage. Each bag contains a desiccant.

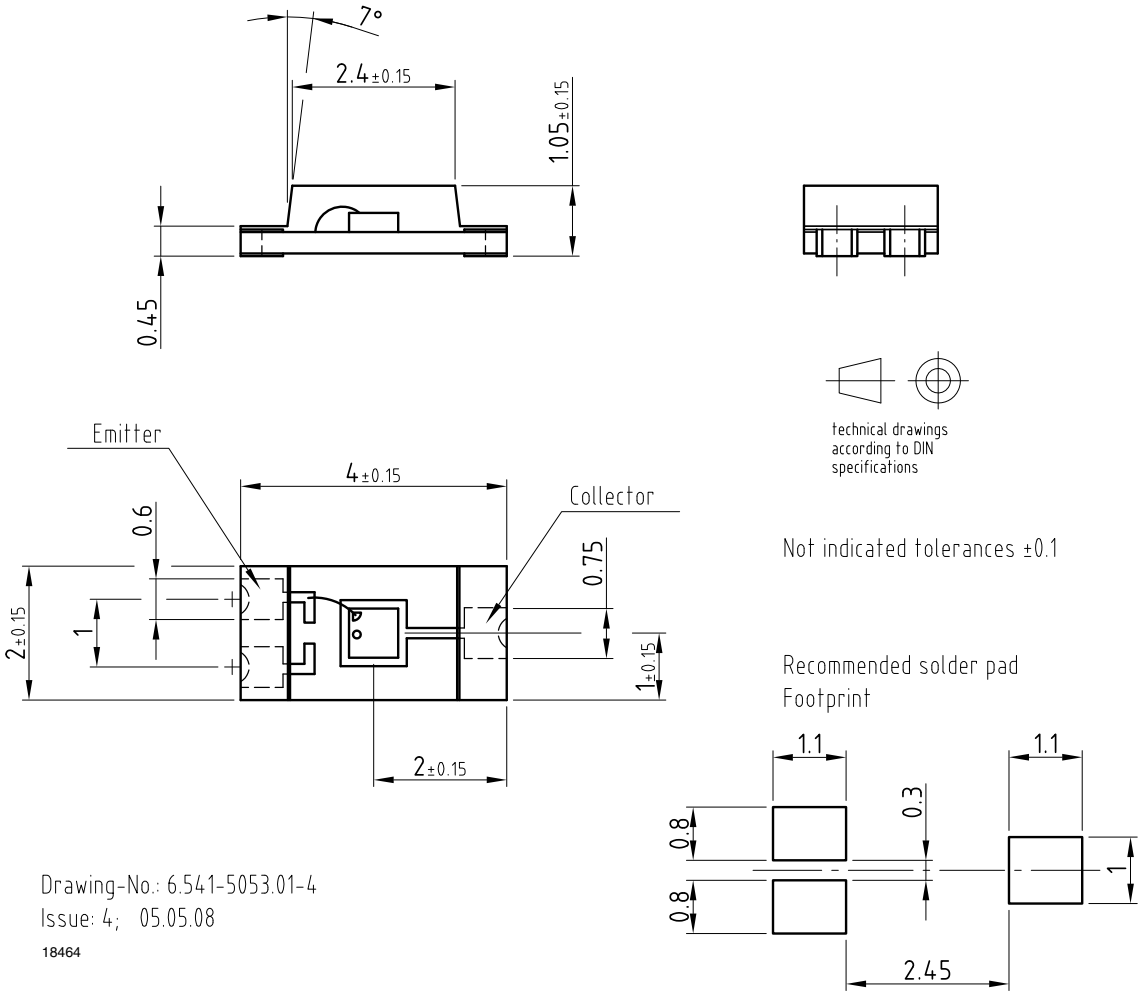
FLOOR LIFE

Time between soldering and removing from MBB must not exceed the time indicated in J-STD-020:
Moisture sensitivity: level 3
Floor life: 168 h
Conditions: T_{amb} < 30 °C, RH < 60 %

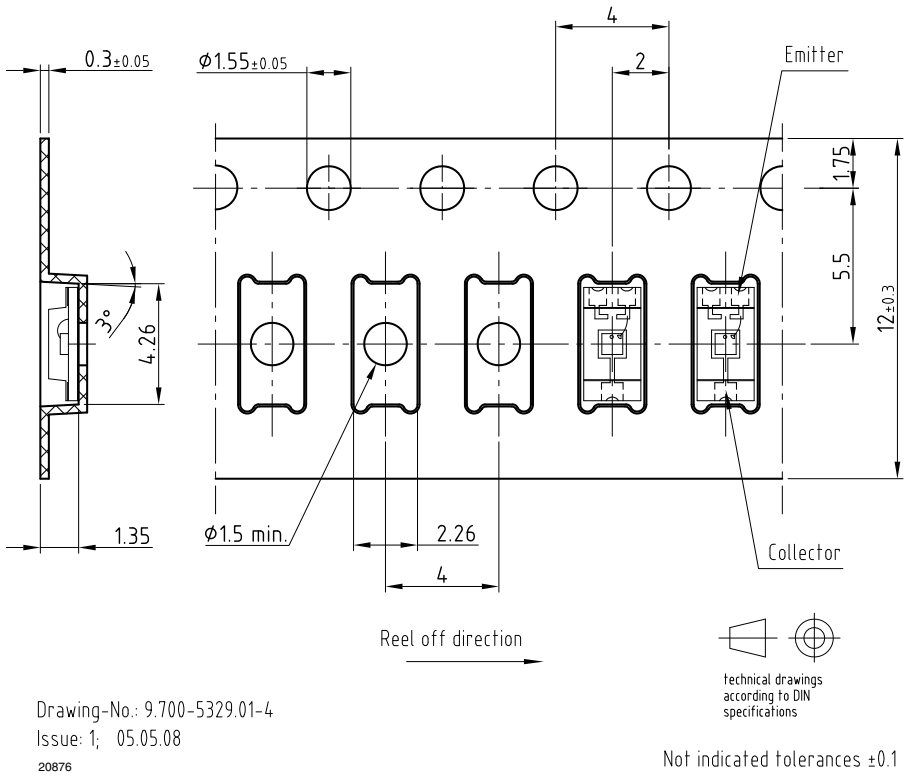
DRYING

In case of moisture absorption devices should be baked before soldering. Conditions see J-STD-020 or label. Devices taped on reel dry using recommended conditions:
192 h at 40 °C (+ 5 °C), RH < 5 %
or
96 h at 60 °C (+ 5 °C), RH < 5 %.

PACKAGE DIMENSIONS in millimeters



BLISTER TAPE DIMENSIONS in millimeters

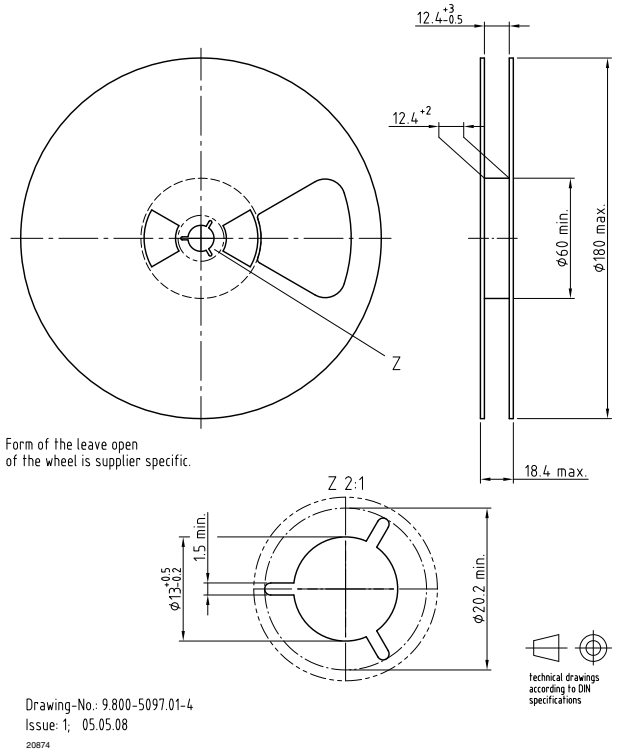


Drawing-No.: 9.700-5329.01-4
Issue: 1; 05.05.08
20876

Not indicated tolerances ±0.1

REEL DIMENSIONS in millimeters

Volume: 3000 pcs/reel



Drawing-No.: 9.800-5097.01-4
Issue: 1; 05.05.08
20874

Disclaimer

ALL PRODUCT, PRODUCT SPECIFICATIONS AND DATA ARE SUBJECT TO CHANGE WITHOUT NOTICE TO IMPROVE RELIABILITY, FUNCTION OR DESIGN OR OTHERWISE.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, “Vishay”), disclaim any and all liability for any errors, inaccuracies or incompleteness contained in any datasheet or in any other disclosure relating to any product.

Vishay makes no warranty, representation or guarantee regarding the suitability of the products for any particular purpose or the continuing production of any product. To the maximum extent permitted by applicable law, Vishay disclaims (i) any and all liability arising out of the application or use of any product, (ii) any and all liability, including without limitation special, consequential or incidental damages, and (iii) any and all implied warranties, including warranties of fitness for particular purpose, non-infringement and merchantability.

Statements regarding the suitability of products for certain types of applications are based on Vishay’s knowledge of typical requirements that are often placed on Vishay products in generic applications. Such statements are not binding statements about the suitability of products for a particular application. It is the customer’s responsibility to validate that a particular product with the properties described in the product specification is suitable for use in a particular application. Parameters provided in datasheets and / or specifications may vary in different applications and performance may vary over time. All operating parameters, including typical parameters, must be validated for each customer application by the customer’s technical experts. Product specifications do not expand or otherwise modify Vishay’s terms and conditions of purchase, including but not limited to the warranty expressed therein.

Except as expressly indicated in writing, Vishay products are not designed for use in medical, life-saving, or life-sustaining applications or for any other application in which the failure of the Vishay product could result in personal injury or death. Customers using or selling Vishay products not expressly indicated for use in such applications do so at their own risk. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay. Product names and markings noted herein may be trademarks of their respective owners.