ZSSC3281

Advanced Dual Channel ARM based Resistive Sensor Signal Conditioner IC

The ZSSC3281 is a dual path sensor signal conditioning IC (SSC) for highly accurate amplification, digitization, and sensor-specific correction of sensor signals. The ZSSC3281 is suitable for bridge and half-bridge sensors, as well as external voltage-source element and single-element sensors (for example, Pt100 and external temperature sensor diodes) powered by an on-chip current source. Digital compensation of the sensor offset, sensitivity, temperature drift, and non-linearity is accomplished via a 32-bit ARM M3 based math core running a correction algorithm with calibration coefficients stored in a non-volatile, reprogrammable memory. The programmable, integrated sensor front-end allows optimally applying various sensors for a broad range of applications.

The ZSSC3281 provides measurement value readouts and programming capabilities via an I2C, SPI, or one-wire interface (OWI). Absolute and ratiometric voltage, current-loop, or interrupt outputs are supported by the ZSSC3281.

Applications

- Calibrated, continuously operating sensors with digital interface and/or analog output: (absolute or ratiometric) voltage or current loop output
- Enables smart, digital sensors for energy-efficient solutions
- (Dual/Diff.) pressure, flow and level sensing
- Industrial applications; for example, process/factory automation
- Consumer / white goods, for example, HVAC, weight scales
- Medical applications, for example, blood pressure, continuous smart health monitors

Features

- Digital communication and calibration interfaces:
  - SPI up to 10MHz
  - I2C (Standard, Fast, Fast+) and I3C SDR
  - One-wire-interface (OWI), up to 100kBit/s
- Accommodates nearly all resistive bridge sensor types (signal spans from 1mV/V up to 500mV/V)
- Supports different sensor element configurations:
  - Resistive bridge or half-bridge
  - Resistive divider string
  - Voltage source
- On-chip temperature sensor
- External temperature sensing supported, for example, sensor-bridge as temperature detector, external diode, etc.
- Programmable 16-bit digital-to-analog-converter and output (supporting “True-0Volt”-output):
  - (0V to 1V) or (0V to 5V) absolute voltage output
  - V_{DD}-ratiometric voltage output
  - 4mA to 20mA current-loop output supported
  - 0V to 10V absolute-voltage output supported
- Wide operational temperature and supply range
- On-chip voltage regulators for sensor supply, and IC operation
- Support for extra regulation by external transistor, for example, JFET (especially for industrial supply voltages >5.5VDC)
- Programmable sensor-signal-conditioning math core
- Reprogrammable, nonvolatile memory (NVM)
- On-chip diagnostics:
  - Sensor connection
  - AFE self-test
  - Memory integrity

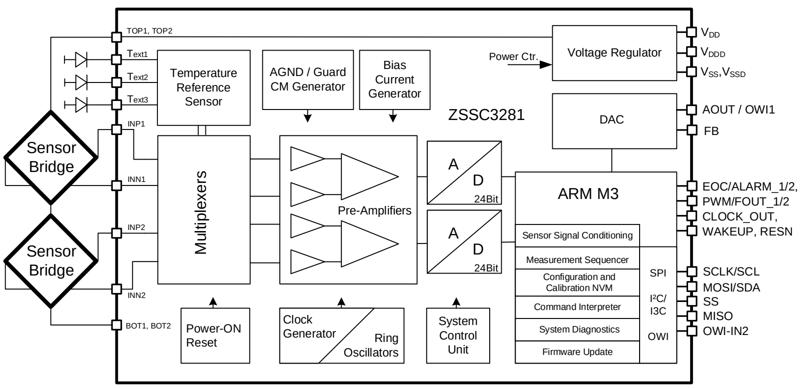

Figure 1. Typical Application Diagram

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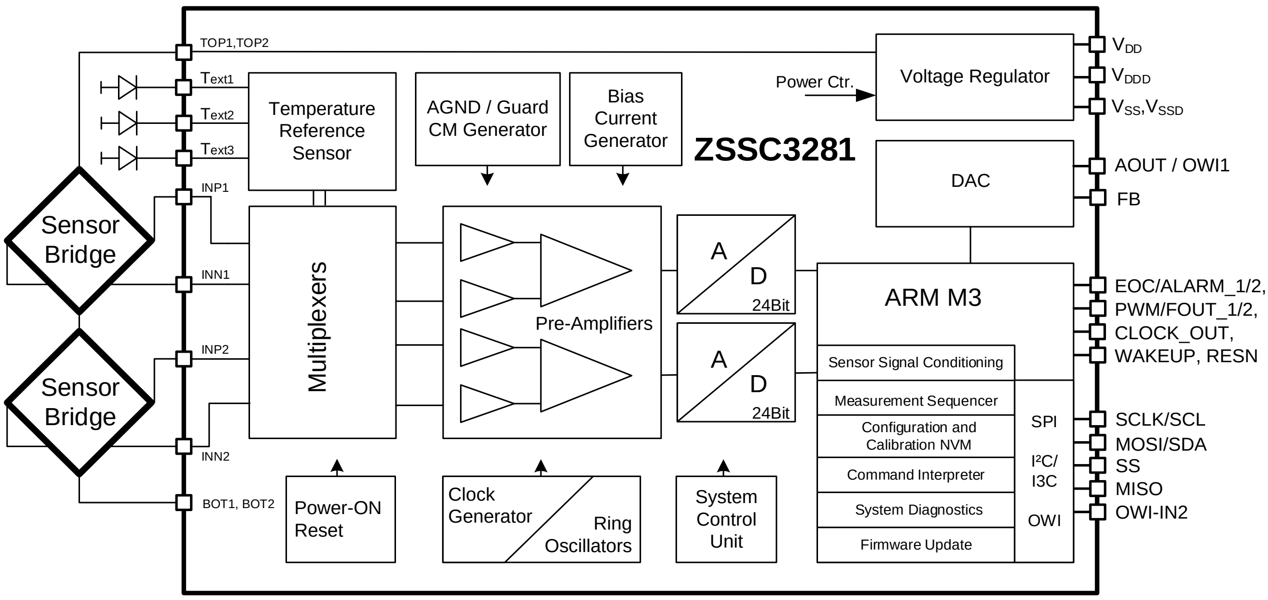
1. Overview

1.1 Block Diagram



1.2 Ordering Information

Orderable Part Number	Description and Package	MSL Rating	Carrier Type	Temperature
ZSSC3281BC1B	DICE on 304µm wafer no inking		Wafer Box	-40 to 85°C
ZSSC3281BC2B	DICE on 725µm wafer no inking		Wafer Box	-40 to 85°C
ZSSC3281BC5B	DICE on 304µm wafer with inking		Wafer Box	-40 to 85°C
ZSSC3281BC6B	DICE on 725µm wafer with inking		Wafer Box	-40 to 85°C
ZSSC3281BC3R	5×5 mm^2 40-QFN	MSL1	13 inch Reel	-40 to 85°C
ZSSC3281BI1B	DICE on 304µm wafer no inking		Wafer Box	-40 to 125°C
ZSSC3281BI2B	DICE on 725µm wafer no inking		Wafer Box	-40 to 125°C
ZSSC3281BI5B	DICE on 304µm wafer with inking		Wafer Box	-40 to 125°C
ZSSC3281BI6B	DICE on 725µm wafer with inking		Wafer Box	-40 to 125°C
ZSSC3281BI3R	5×5 mm^2 40-QFN	MSL1	13 inch Reel	-40 to 125°C
ZSSC3281KIT	Modular ZSSC3281 SSC Evaluation Kit including three interconnecting boards, five ZSSC3281 VFPQFN samples, and cable. Software is available for download on www.renesas.com/ZSSC3281.			

1.3 Pin Configuration

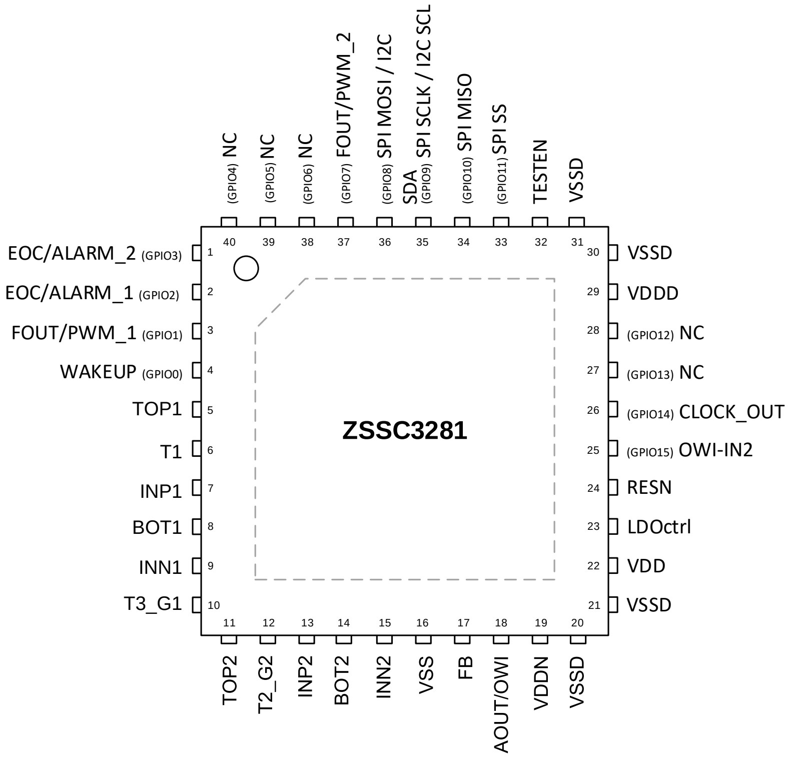


Figure 2. Pin Layout QFN40

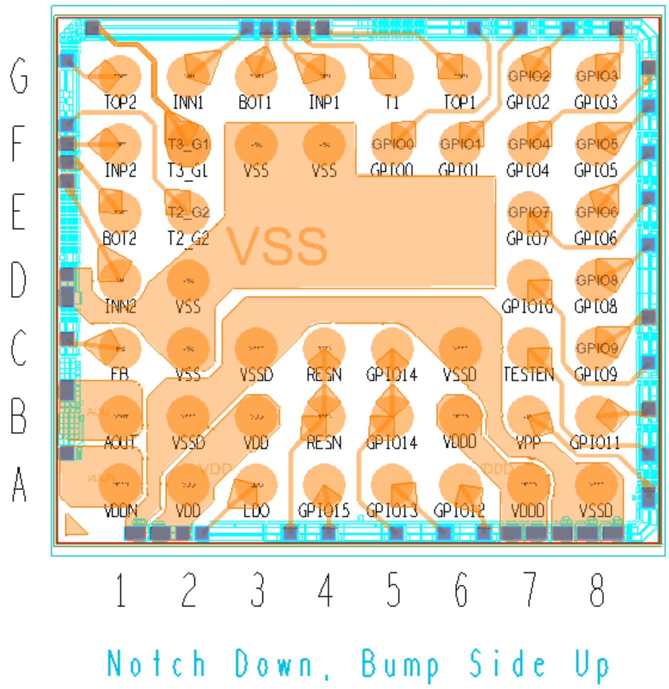


Figure 3. Pin Layout WLCSP

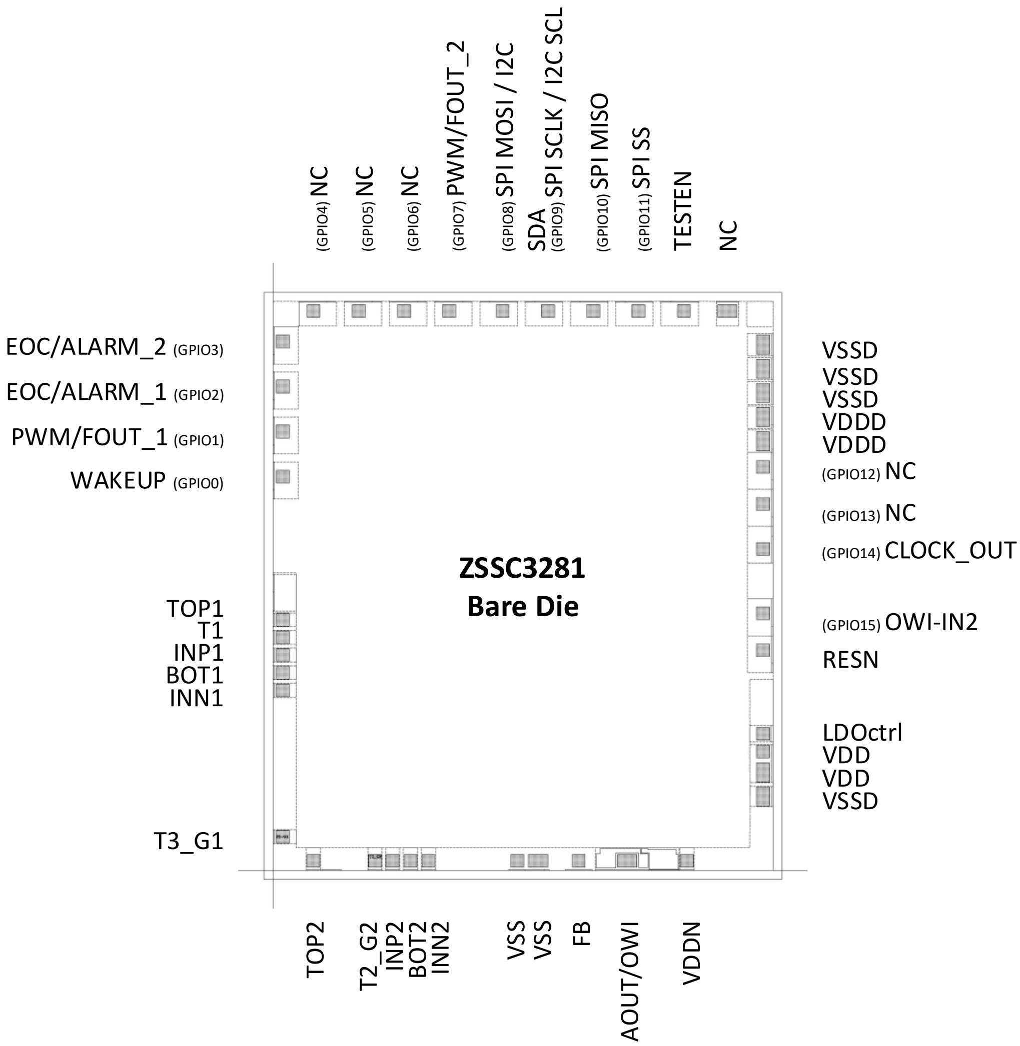


Figure 4. Pad Layout on Die

1.4 Pin Descriptions

Pin Number	Name	Type	Description
1	EOC/ALARM_2	Digital Input/Output	GPIO3: mapped to EOC2 function
2	EOC/ALARM_1	Digital Input/Output	GPIO2: mapped to EOC1 function
3	PWM/FOUT_1	Digital Input/Output	GPIO1: mapped to TIMER2 function
4	WAKEUP	Digital Input/Output	GPIO0: mapped to WAKEUP function
5	TOP1	Analog Input/Output	Positive sensor (bridge 1) supply or sensor-signal input
6	T1	Analog Input/Output	External temperature sensor
7	INP1	Analog Input/Output	Positive sensor (bridge 1) signal
8	BOT1	Analog Input/Output	Sensor (bridge 1) ground or sensor-signal input
9	INN1	Analog Input/Output	Negative sensor (bridge 1) signal
10	T3_G1	Analog Input/Output	External temperature sensor 3
11	TOP2	Analog Input/Output	Positive sensor (bridge 2) supply or sensor-signal input
12	T2_G1	Analog Input/Output	External temperature sensor 2
13	INP2	Analog Input/Output	Positive sensor (bridge 2) signal
14	BOT2	Analog Input/Output	Sensor (bridge 2) ground or sensor-signal input
15	INN2	Analog Input/Output	Negative sensor (bridge 2) signal
16	VSS	Ground	Power supply ground
17	FB	Analog Output	Current-loop application feedback output (level below VSS). No connection if not used.

Pin Number	Name	Type	Description
18	AOUT/OWI	Analog Output; Digital Input/Output	Analog smart-sensor output signal and/or OWI interface input/output line.
19	VDDN	Analog Output	Negative voltage output, charge pump buffer cap
20	VSSD	Ground	Digital power supply ground
21	VSSD	Ground	Digital power supply ground
22	VDD	Supply	Power supply
23	LDOctrl	Analog Output	Control output (reference signal) for (optional) external regulator / supply control loop
24	RESN	Digital Input	Digital IC reset (low active); internal pull-up
25	OWI-IN2	Digital Input/Output	GPIO15: mapped to OWIN-IN2 function
26	CLOCK_OUT	Digital Input/Output	GPIO14: mapped to CLOCK_OUT function
27	N.C.	Digital Input/Output	GPIO13: not mapped
28	N.C.	Digital Input/Output	GPIO12: not mapped
29	VDDD	analog I/O	Buffer cap connection for internal VDDD
30	VSSD	Ground	Digital power supply ground
31	VSSD	Ground	Digital power supply ground
32	TESTEN	–	Renesas internal use only. Connect to VSSD
33	SPI SS	Digital Input/Output	GPIO11: mapped to SPI SS
34	SPI MISO	Digital Input/Output	GPIO10: mapped to SPI MISO
35	SPI SCLK / I2C SCL	Digital Input/Output	GPIO9: mapped to SPI SCLK / I2C SCL
36	SPI MOSI / I2C SDA	Digital Input/Output	GPIO8: mapped to SPI MOSI / I2C SDA
37	PWM/FOUT_2	Digital Input/Output	GPIO7: mapped to TIMER 1
38	N.C.	Digital Input/Output	GPIO6: not mapped
39	N.C.	Digital Input/Output	GPIO5: not mapped
40	N.C.	Digital Input/Output	GPIO4: not mapped
	Exposed PAD	-	QFN-bottom plate, leave pin floating.

2. Specifications

2.1 Absolute Maximum Ratings

Symbol	Parameter	Conditions	Minimum	Maximum	Units
T_J	Junction temperature			135	°C
T_S	Storage temperature		-45	150	°C
	ESD: Human Body Model Tested per JS-001-2017	Pins: INPx, INNx, TOPx, BOTx, Tx, VDDD		2000	V
		Pins: GPIOx, VDD, VDDN, VSS, VSSD, LDOctrl, AOUT/OWI, FB, RESN, NC		4000	V
	ESD: Charged Device Model Tested per JS-002-2014	All Pins		750	V
	Latch-up	Tested per JESD78E; Class 2, Level A	-100	+100	mA
V_{DD_max}	Maximum allowed for voltage supply	Referenced to VSS	-0.3	6.5	V
V_{IF_max}	Voltage at digital I/O	Referenced to VSSD	-0.3	5.5	V
V_{FB_max}	Voltage at FB pin	2-wire Current Loop Mode	-2	2	V

1. CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

Symbol	Parameter	Conditions	Typical	Units
θ_{JA}	Theta JA	40Ld 5x5 QFN Package, 0 m/s air flow	25.8	°C/W
		40Ld 5x5 QFN Package, 1 m/s air flow	22.4	°C/W
		40Ld 5x5 QFN Package, 2 m/s air flow	20.8	°C/W
θ_{JB}	Theta JB	40Ld 5x5 QFN Package	1.3	
θ_{JC}	Theta JC	40Ld 5x5 QFN Package	24.4	

2.3 Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{DD}	Power supply voltage	1.8	–	5.5	V
	Flash write/erase	2.7			
	With optional “true 0V” at analog output	2.7			
T_A	Ambient temperature (depending on the part code)	-40	–	125	°C
C_{VDD}	External capacitance between VDD and VSS, without external supply transistor regulation	–	10	–	µF
	External capacitance between VDD and VSS, with (optional) external supply transistor regulation	–	10	–	
C_{VDDD}	External capacitance between VDDD and VSS		1		µF
C_{VDDN}	External capacitance between VDDN and VSS, with optional “true 0V” at analog output		1		µF
$C_{TOP,EMC}$	Recommended, external capacitance between TOP and VSS for electro-magnetic immunity (EMI)	0	6.8	8	nF
$C_{AOUT,EMC}$	Recommended, external capacitance between AOUT versus VDD and VSS for EMI suppression [1]	0	22	33	nF
I_{Sensor}	Load current through external sensor element [1]	0.005	0.5	2	mA
$V_{DioDrop}$	External temperature diode and RTD input range, drop over external element referenced to T1, T2_G2, T3_G1 pin	0.2	–	1.2	V
V_{Sens_in}	Absolute sensor signal input level, INN, INP pins	0.2	–	1.2	V
$I_{max\_AOUT\_V}$	Maximum current load at AOUT pin for voltage outputs	0	5	–	mA
SR_{VDD_POR}	Recommended V_{DD} rise slew rate for power-on-reset (POR)	1.5	–	–	V/ms
I_{max_GPIO}	Maximum overall GPIO driver strength			120	mA

1. For applications with OWI interface or analog voltage-output.
2. With ratiometric sensor supply configuration; for example, a ratiometric bridge or bridge as temperature sensor with internal or external temperature sensitive resistor

2.4 Electrical Specifications

All parameter values are valid only under operating conditions specified in section 2.3. All voltages are referenced to V_{SS}.

Table 1: Electrical Operating Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
IC Supply						
I_{IC}	Current consumption, active mode:	Excluding connected sensor elements (external LDO enabled)				mA
	• low power (current loop)		–	3.3	3.5	
	• high power (depending on settings)		–	8	15	

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
$V_{DD,LDO}$	VDD generated with external depletion - NMOS	Programmable in 4 steps: • 3V	2.85	3	3.15	V
		• 4V	3.80	4	4.20	
		• 5V	4.75	5	5.25	
		• 5.25V	5.00	5.25	5.50	
VDDA	Internally generated analog supply		1.6	1.65	1.85	V
Sensor Supply						
TOP	Sensor bias voltage in ratiometric supply mode	Ratiometric sensor voltage supply		VDDA		
I_{bias_TOP}	Sensor bias current used in Source Mode	Programmable in 10 steps: 0µA, 5µA, 10µA, 20µA, 40µA, 80µA, 100µA, 160µA, 200µA, 500µA	0		500	µA
I_{biasN_BOT}	Sensor current used in sink mode	Programmable in 2 steps: 20µA, 100µA	20		100	µA
I_{ERR}	Relative bias current (I_{bias_TOP} and I_{biasN_BOT}) error	Overall	-10		10	%
		Over-temperature	-1		1	%
R_{TH}, R_{TL}	TOP/BOT bias resistor	Programmable in 12 steps: open, 1kΩ.33kΩ, 2kΩ, 4kΩ, 8kΩ, 10kΩ, 14kΩ, 18kΩ, 20kΩ, 24kΩ, 28kΩ, 40kΩ	1.3		40	kΩ
dR_{TH}, dR_{TL}	TOP/BOT bias resistor process variation		-30		30	%
TK of R_{TH}, R_{TL}	TOP/BOT bias resistor temperature variation	T = -55°C to125°C			1.3	%
Analog-to-Digital Converter (ADC, A2D)						
r_{ADC}	Resolution		10	16	24	Bit
V_{ADCmid} (AGND)	Differential ADC input Common Mode	With internal regulator supplying TOP pin, typical: $V_{TOP}/2$ = 875mV (=PGA output Common Mode level)	–	0.5	–	V_{TOP}
$\Delta_{ADC,c}$	Differential input offset shift	Sensor signal offset versus maximum sensor signal. Programmable in 8 steps.	0	–	7/8	V_{shift}/V_{fs}
ENOB [1]	Effective number of bits, $3\sigma_{Noise}$ based	Gain = 1.32, r_{ADC} = 24-bit, no oversampling	–	17	–	Bit
		Gain = 28, r_{ADC} = 16-bit, no oversampling	–	12	–	Bit
		Gain = 495, r_{ADC} = 24-bit, no oversampling	–	11	–	Bit
Digital-to-Analog Converter (DAC) and Analog Output						
VDD	VDD operating range	AOUT modes using 1V buffer	1.8		5.5	V
		AOUT modes using 5V buffer	2.7		5.5	
$t_{AOUTsettle}$	Time from digital value applied at DAC and voltage at VOUT	10% to 90% input step: V_{AOUT} at 90% of final value			100	µs
V_{OUT_START}	voltage at AOUT during startup			0		V
V_{AOUT}	Output voltage at pin AOUT	Ratiometric Voltage Mode	0		VDD	V
		1V absolute Voltage Mode	0		1	V

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
		5V absolute Voltage Mode			5[1]	
		10V absolute Voltage Mode			5[1]	
I_{OUTMAX}	Short current limit at pin AOUT	AOUT modes using 5V Buffer • short to VDD or VSS • programmable in 4 steps	3 8 15 20	5 12 19 25	9 20 23 30	mA mA mA mA
C_{load}	Load capacitance at AOUT	• 2-Wire Current Loop Mode			2	nF
		• all other modes (for example. cap for EMC: 33nF, ECU load: 10nF)			50	
r_{DAC}	Resolution		–	16	–	Bit
Programmable-Gain Amplifier (PGA)						
G_{amp}	Gain	120 steps	1.32	–	495	V/V
G_{err}	Gain error	Referenced to nominal gain Gain = 1.32…5 Gain = 6…125 Gain = 126…495	-2.5 -5 -10	0	2.5 5 10	%
$G_{errTemp}$	Gain error over-temperature	Temperature compensated sensors do not require calibration over-temperature.	-0.2		0.2	%
V_{CMin}	Supported input common mode		0.2	0.5	0.7	V_{TOP}
V_{ioffsc}	Differential input offset shift	Programmable in 30 steps Gain1 < 240 Gain1 > 240	-28 -22	0 0	28 22	mV
Sensor Signal Conditioning (SSC) Performance						
f_{SSCout}	Output (update) rate	• 3 measurements: signal+, signal-, diagnosis • r_{ADC} = 16bit • SSC-corrected digital output	–	1.3	–	kHz
		• 3 measurements: signal+, signal-, diagnosis • r_{ADC} = 14bit • SSC-corrected digital output	–	2.245	–	kHz
		• 2 measurements: signal+, diagnosis • r_{ADC} = 14bit • SSC-corrected digital output	–	3.36	–	kHz
$t_{stepresp}$	Step response	• 3 measurements: signal+, signal-, diagnosis • r_{ADC} = 16bit • SSC-corrected digital output		1.38		ms
		• 3 measurements: signal+, signal-, diagnosis • r_{ADC} = 14bit • SSC-corrected digital output		0.84		ms
Analog Inputs						
V_{INP}, V_{INN}	Absolute sensor input	Voltages at INP and INN pin; resulting minimum/maximum differential voltages: -800mV < V_{INdiff} < 800mV	0.2	–	1.2	V

[1] VDD must be ≥ 5.25V

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{TEXT}	External temperature diode or RTD input range	at T1, T2_G2, T3_G1 pin (see Sensor Supply section of this table and chapter 4.3.2 for available configuration options)	0.3	–	1.2	V
R_{SENSOR}	External sensor (bridge) resistance	TOP = 1.65V	0.825	–	60	kΩ
		2-wire Current Loop Mode	3.3	–	60	kΩ
$\|V_{DIFFin}\|$	Differential input signal range	Referenced to sensor supply ($VDDA_{int}$)	–	–	800	mV
Diagnostics						
R_{open}	Broken sensor: values $>R_{open}$ set a failure flag	• INP1 vs. INN1 • INP2 vs. INN2	100	120	150	kΩ
R_{short}	Shorted sensor: values $<R_{short}$ set a failure flag	• INP1 vs. INN1 • INP2 vs. INN2 • INP1 vs. INP2 • INP2 vs. INN1	120	–	220	Ω
I_{leak}	Sensor leakage check	Sensor leakage current from INP/INN to VSS: values $>I_{leak}$ set a failure flag	0.8	1	2	µA
V_{common}	Sensor Common Mode check (measurement V_{INP}-V_{AGND}, V_{INN}-V_{AGND})	Detects sensor connection failure: • open TOP or BOT • short INP or INN to TOP or BOT	0.4	–	0.6	V_{TOP}
V_{drift}	AFE gain check, run measurement with dedicated gain, compare with stored values	Input value from R-DAC is applied	–	–	–	–
V_{RDAC}	R-DAC differential output voltage	VDDAx = 1.65V:	–		–	mV
		• S = 00		2		
		• S = 01		10		
		• S = 10		100		
		• S = 11		200		
R_{T_OPEN}	T1, T2_G2, T3_G1 connection check: open	Broken Tx sensor: values $>R_{T\_OPEN}$ set a failure flag: • 3 level can be configured • INN is drawn to VSS! --> is not applicable in sensor configuration with one bridge at both frontends!	1.6	2	3	MΩ
			0.4	0.5	0.6	
			0.07	0.1	0.13	
t_{T_OPEN}	Diagnosis time; depends on C_{ts} and R_{T_OPEN}	Time from diagnose enable to valid output	0.1		10	ms
R_{T_SHORT}	T1, T2_G2, T3_G1 connection check: short to TOP, BOT, INP, INN	Shorted Tx sensor: values $<R_{T\_SHORT}$ set a failure flag:				Ω
		• configuration for Pt1000	320	500	650	
VDD	• Programmed (expected) VDD level • VDD drop below the programmed level signalizes a VDD drop	Programmable in 6 steps: 2.2V, 2.7V, 3V, 4V, 5V, 5.25V	2.2		5.25	V
$V_{dropVDD}$	Voltage level, where the VDD drop is detected		70	85	95	%VDD

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
$VDDX_{BOD}$	VDDA, VDDD brown out detection	VDDX < $VDDX_{BOD}$ set a failure flag	67	90	97.5	%VDDX
V_{LOSS}	Power/ground loss with respect to AOUT	• V_{AOUT} – VDD > V_{LOSS} • V_{AOUT} – VSS < V_{LOSS}		0.2		V
Power-Up						
t_{STA1}	Start-up time	V_{DD} ramp up to interface communication	–	–	5	ms
t_{STA2}		V_{DD} ramp up to analog operation	–	–	5	ms
t_{WUP1}	Wake-up time	Sleep to Active State interface communication	–	2	10	µs
Oscillator						
f_{CLK_HF}	Internal HF-oscillator frequency	At T=27°C	15.8	16	16.2	MHz
		Across temperature range	15.4		16.6	
f_{CLK_LF}	Internal LF-oscillator frequency		25	32	41	kHz
Internal Temperature Sensor						
r_{Temp}	Internal temperature sensor resolution	Differential output voltage	–	220	–	µV/K
Digital IO Pins						
V_{IL}	Input low voltage	voltage level where the input is recognized as low level	–		30	%VDD
V_{IH}	Input high voltage	voltage level where the input is recognized as high level	70		–	%VDD
V_{Ihys}	Input hysteresis		10		35	%VDD
V_{OL}	Output low voltage				8	%VDD
V_{OH}	Output high voltage		92			%VDD
I_{OL}	Output drive low current	V_{PAD} = V_{OL}				mA
		VDD = 1.7V	1		2.4	
		VDD = 2.6V	2.7		6.6	
		VDD = 5V	9		20	
I_{OH}	Output drive high current	V_{PAD} = V_{OH}				mA
		VDD = 1.7V	1.2		2.3	
		VDD = 2.6V	3.2		6.4	
		VDD = 5V	10.9		20.2	
I_{pullup}	Weak pull-up current at pin RESN	V_{PAD} = 0V				µA
		VDD = 1.7V	5		13	
		VDD = 2.6V	17		50	
		VDD = 5V	84		250	
$I_{pulldown}$	Weak pull-down current at pin WAKEUP	V_{PAD} = VDD				µA
		VDD = 1.7V	5		11	
		VDD = 2.6V	17		35	
		VDD = 5V	80		160	
Serial Interfaces						
$f_{C,SPI}$	SPI clock frequency		–	–	12	MHz
$f_{C,I2C}$	I2C clock frequency		–	–	1	MHz
$f_{C,I3C}$	I3C clock frequency		–	–	12.5	MHz
CD_{OWI}	OWI data rate		0.25	–	100	kBit/s

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
Flash Memory						
t_{PROG}	NVM program time	Programming time for complete configuration and calibration page:	–		–	ms
		• f_{CLK_HF} = 16Mhz		360		
		• f_{CLK_HF} = 1Mhz		740		
n_{NVM}	NVM endurance	Number of reprogramming cycles	20000	–	–	Numeric
$t_{RET,NVM}$	Data retention		10	–	–	Years

1. ENOB = LOG2($2^{r_{ADC}}$ / $3\sigma_{Noise}$) with for example, r_{ADC}[Bit] = 24.

3. Basic System Configuration

3.1 System Modes/System Start

The ZSSC3281 can operate in three different main operating modes:

Cyclic Mode — This is the default mode for continuously operating sensors. In this mode autonomous, cyclically repeated sensor measurements are performed and related digital and/or analog output updates are provided. The cyclic sequences for sensor measurements and system diagnostic measurements are configurable and allow to define the output update rate of the conditioned sensor signals. Cyclic Mode supports only a subset of the defined serial interface commands to guarantee deterministic input-output behavior (especially latencies) and to prevent accidental interruption of the conditioned sensor data stream.

Command Mode — This is the most appropriate mode for evaluation, test, and calibration purposes. In this mode, all supported serial interface commands are available. Command Mode can be used for applications requiring re-occurring digital interaction on functions that are not available in Cyclic Mode or certain system configuration changes.

Sleep Mode — This is reserved for future firmware releases which will specifically support power consumption critical applications.

ZSSC3281 provides a fourth operation mode which is not a user accessible operation mode:

Boot/Diagnosis Mode — This is immediately active after power-on or reset of ZSSC3281, while the firmware is still in boot-up phase and the Command Interpreter is not functional yet. The mode is also reached in case the system self-supervision detected a dangerous system fault, which could lead to unreliable or unpredictable behavior of the IC. The serial interfaces are only partly operational in Boot/Diagnosis Mode to allow an external host to read the system status for ZSSC3281. Write access and command execution is not supported.

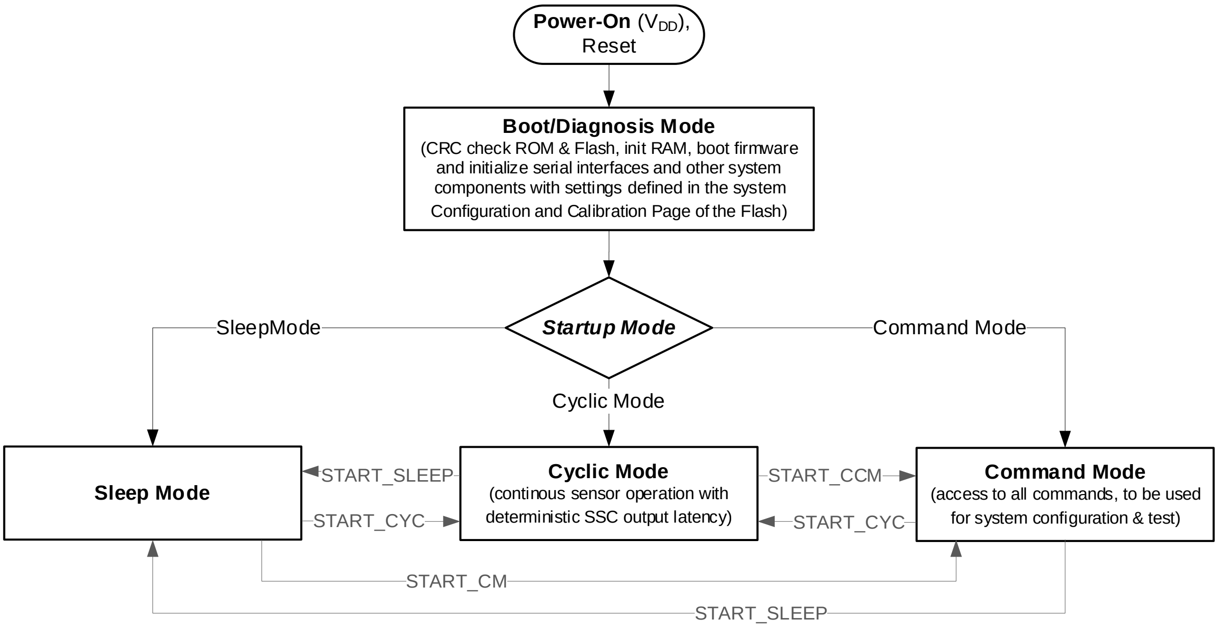


Figure 5: Main Operating Modes

After power-on (reset) the ZSSC3281 always enters the programmed System Startup Mode (GUI path: *Configure\System Control\System Startup*) as soon as the firmware boot process is finished.

Each of the three operating modes can be set up as the default start-up mode. Changing the ZSSC3281 to another operating mode is possible via the mode change and start commands: *START_CM, START_CYC, START_SLEEP* (see section 11.2.1 for details).

The ZSSC3281 supports three different types of digital interfaces: I2C/I3C, SPI, and OWI. All three interface types are available in the different main operating modes, if they were enabled via GUI.

3.2 Power Supply

3.2.1. Power Supply Modes

ZSSC3281 supports two different main supply modes (Direct VDD Supply and Pre-Regulated High Voltage Supply) and an optional negative voltage supply for the Analog Output Driver. Respective application schematics are shown in sections 3.2.2 and 3.2.3.

Table 2: Power Supply Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
VDD	Low voltage supply		1.8	2.8	5.25	V
VDDHV	High voltage supply	Requires external pre-regulator JFET	VDD+0.5		48	V
VDDN	Negative voltage supply for analog output (AOUT)	Internally generated, requires activation of VDDN Charge Pump		$V_{ExtShottky}$		V
		Externally supplied	0	-0.3V	-0.5V	V
VSS	Analog ground reference			0		V
VSSD	Digital ground reference			0		V
C_{VDD}	External supply buffer cap			10		µF
C_{V3D}	Regulated internal supply buffer cap			1		µF
C_{VDDN}	Negative supply buffer cap	Internally generated VDDN		1		µF
		Externally supplied VDDN				
C_{HV}	External high voltage buffer cap	All applications except 2-wire Current Loop		10		µF

3.2.2. Direct VDD Supply

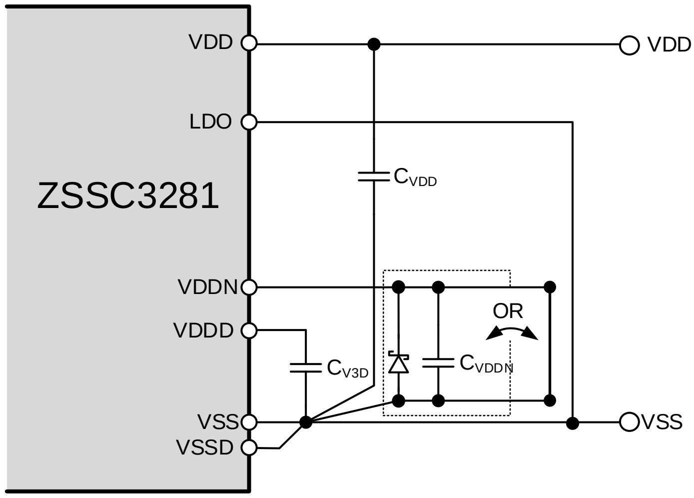


Figure 6: Application with Direct IC Supply

The Direct VDD Supply configuration requires the LDO pin to be connected to VSS on PCB level. To minimize power consumption in all operation modes, the LDO driver circuit is turned off as soon as the user selects 'Direct VDD Supply' mode during device configuration (see GUI Tab: Configure\PowerSupply & Oscillator\Supply Mode).

3.2.3. Pre-Regulated High Voltage Supply

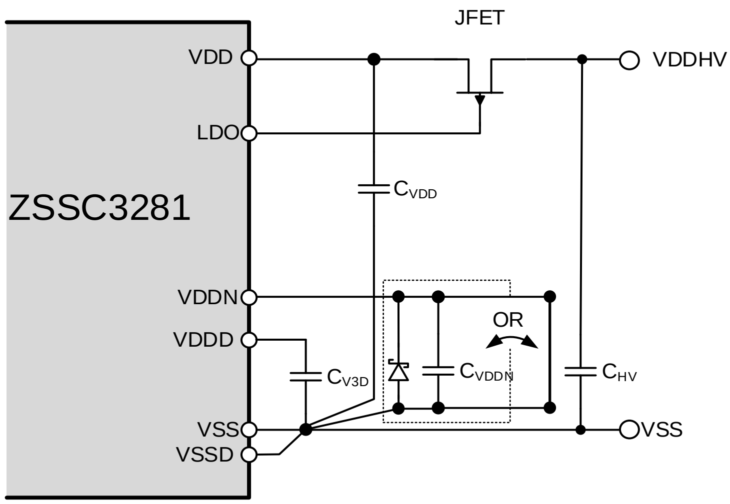


Figure 7: Application with External Regulator

Higher supply voltages than 5.25V require an external JFET as pre-regulation device. The LDO output pin of ZSSC3281 is able to drive the JFET devices listed in Table 3 in a circuit configuration as shown in Figure 7.

Table 3: Supported JFET Devices

Manufacturer	Type	VTH	ID/A
Supertex inc.	DN3545	-3.5 to -1.5V	0.2
Infineon	BSP149	-1.8 to -1V	0.66
Infineon	BSS169	-2.9 to -1.8V	0.17

The output voltage of the JFET assisted pre-regulator is configurable as shown in Table 4. In the GUI it can be configured through the field Configure\PowerSupply & Oscillator\Regulated VDD.

Table 4: JFET Assisted VDD Pre-Regulator Parameters

Configurable Pre-Regulator Output Voltage (VDD)	VDDHV Min	VDDHV Max	Unit
3V	3.5	48	V
4V	4.5	48	V
5V	5.5	48	V
5.25V	5.75	48	V

Besides the VDD buffer capacitor C_{VDD} another buffer capacitor C_{HV} is recommended on the high voltage supply VDDHV for stability reasons.

3.2.4. Negative Voltage Supply for AOUT

To support True-0V signals on the Analog Output (AOUT), ZSSC3281 provides an option to externally supply a negative voltage rail for the AOUT buffer at VDDN. VDDN supply specifications are shown in Table 2.

The negative VDDN voltage can also be generated by an internal charge pump circuit. The internal charge pump can be activated through GUI field: Configure\AOUT\VDDN Charge Pump.

The charge pump function is only available for all AOUT Operation Modes with Voltage Output. The charge pump circuit requires an external buffer capacitor C_{VDDN} and a Shottky Diode to work properly.

If no True-0V signals are required at AOUT, the user must directly connect VDDN with VSS on PCB level.

3.3 System Clocks

3.3.1. Internal Oscillators and Specifications

ZSSC3281 is equipped with two internal oscillators:

- Calibrated, first order temperature compensated 16MHz system clock oscillator
- Un-calibrated, first order temperature compensated 32kHz ultra low power oscillator

Table 5: Oscillator Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
f_{CLK_HF}	Internal HF-oscillator frequency	At T = 27°C	15.8	16	16.2	MHz
		Across temperature range	15.4		16.6	
f_{CLK_LF}	Internal LF-oscillator frequency		25	32	41	kHz

3.3.2. Main System Clock

The Main System Clock, which drives the MCU, the memories (ROM, Flash, SRAM), and the peripherals is derived from the internal System Clock Oscillator. By default, the oscillator frequency (16MHz) is directly applied across the entire system without further down division. Hardware and software driven clock gating are applied to maintain a low power consumption.

For applications where power consumption of ZSSC3281 is a concern, the Main System Clock can be reduced by choosing a system clock source divider other than the value of div1. The maximum divider factor can be 16 (div16), which sets the Main System Clock to 1MHz.

The system clock divider can be changed via GUI field: Configure\PowerSupply and Oscillator\System Clock Source Divider.

If the ZSSC3281 is operated in a 2-Wire Current Loop setup (and respective GUI configurations are made) a reduction of the Main System Clock to 1 MHz is mandatory to meet the maximum system current consumption specification (<4 mA) over the entire temperature range. In this case the ‘System Clock Source Divider’ is not selectable by the user.

3.3.3. Always-On Clock

The 32kHz always-on clock is used by the System Management Unit to control the power-up-sequence of the ZSSC3281 device, as well as by the internal watchdog and the low speed timer.

3.4 System Reset

The ZSSC3281 becomes reset at following scenarios:

Power On Reset — Voltage at VDD or VDDD is below limits as specified in section 2.4.

External Reset — RESN Pin of ZSSC3281 is set to LOW.

Self-Reset — Self supervision via system diagnosis detected a critical system state and sets system in safe reset state.

Table 6: VDDD Power-On-Reset Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
$V_{riseVDDD}$	reset release voltage	VDDD level where reset is released	1.35		1.8	V
$V_{fallVDDD}$	reset voltage	VDDD level where reset is generated	1.1		1.6	V
$V_{hysVDDD}$	reset hysteresis voltage		50		500	mV

4. Analog Front End (AFE)

4.1 AFE Signal Path

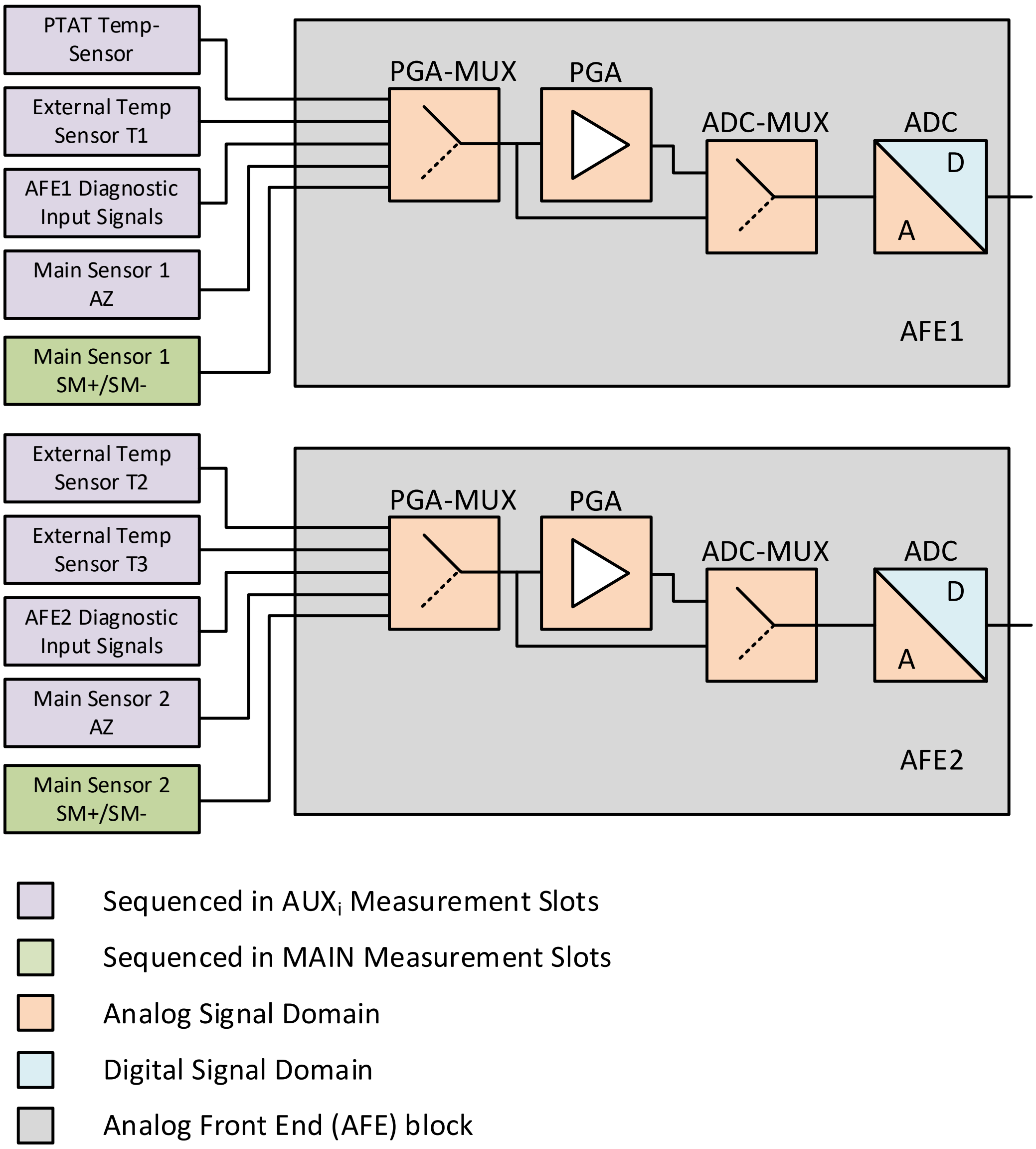


Figure 8: Block Diagram Analog Front End

4.2 Bridge Sensor Inputs

4.2.1. Resistive Bridge Sensors

Table 7: Resistive Bridge Parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{br}	Bridge resistor	Constant Voltage Mode	0.825		60	kΩ
		Constant current mode	0.1			
C_{br}	Bridge capacitance, depends on the required resolution: $\tau = R_{br} \times C_{br}$ defines the settle time.	Filter capacitances C_{br} between INNx/INPx and VSS		1		nF
V_{sig}	Signal span	mV/V is related to the bridge supply			500	mV/V
V_{off}	Signal offset	For example, V_{sig} = 1mV --> V_{off} = 20mV			2000 20	% off V_{sig} 1/ V_{sig}

Table 8: Resistive Bridge Application Configurations

Type #	Application Case	AFE1	AFE2	Comment
1	One resistive sensor	Resistive sensor 1	-	
2	Two resistive sensors	Resistive sensor 1	Resistive sensor 2	Not available with 2-wire current loop operation
3	One resistive sensor at both inputs	Resistive sensor 1 (normal speed)	Resistive sensor 1 (low speed)	Not available with 2-wire current loop operation

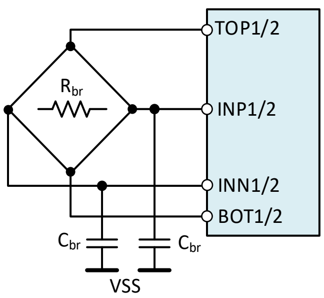


Figure 9: Bridge Sensor Type 1

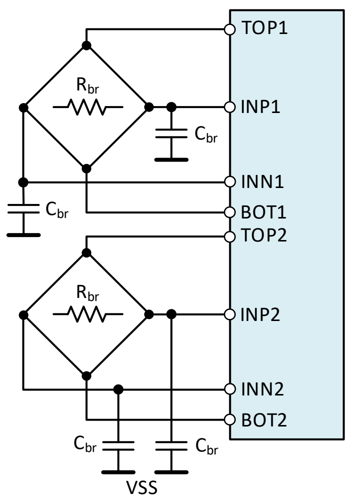


Figure 10: Bridge Sensor Type 2

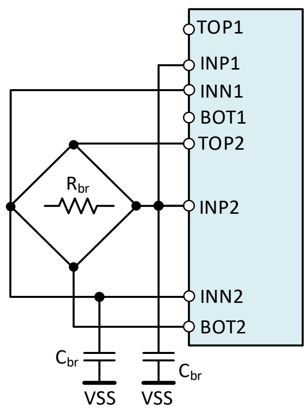
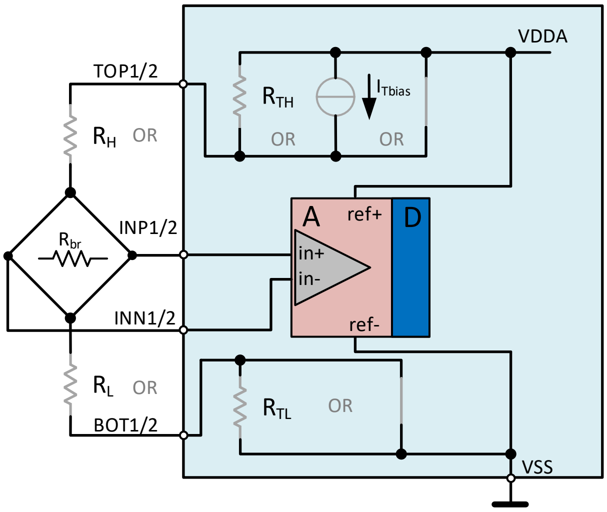


Figure 11: Bridge Sensor Type 3

The resistive bridge can be sourced in either Constant Voltage mode (V-source) or in Constant Current mode (I-source), requires low resistance.



Legend:

Gray components: can be activated "either-or" via the GUI.

Figure 12: Resistive Bridge Bias Configurations

In constant current mode the bridge output must be set into the common input range of the PGA. This can be done with a low side external resistor R_L or with the internal resistor R_{TL}.

In constant Voltage Mode the bridge current can be reduced by inserting the internal high and low side resistors R_{TH}, R_{TL} or by adding external resistors R_H and R_L.

Table 9: Resistive Bridge Supply Parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{TOP1/2}$	Output voltage at TOP1/2	Direct voltage output		VDDA		V
C_{load}	Load capacitance				2.2	nF
I_{load}	Load current				2	mA
I_{Tbias}	Current out of TOP1/2		5		500	µA
R_{TH}, R_{TL}	Bias resistor		1.3		40	kΩ

4.2.2. Thermocouple and Thermopile Sensors

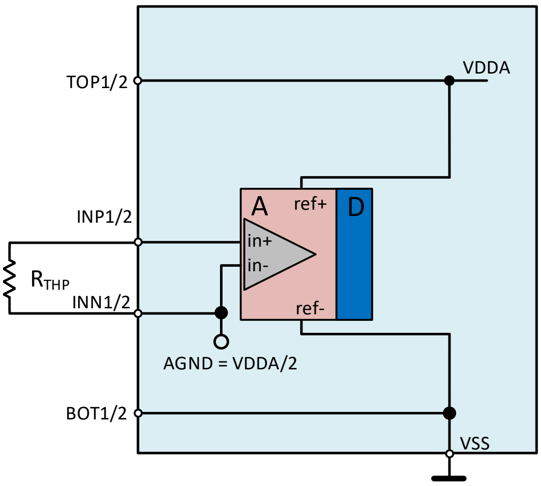


Figure 13: Thermocouple/Thermopile Input and Bias Configuration

Table 10: Thermopile/Thermocouple Parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{in}	Differential input voltage signal range at INP1/2, INN1/2		0.01		10	mV
I_{leak}	Input leakage current at INP1/2, INN1/2			200		nA
R_{THP}	Thermocouple/Thermopile resistance			100		kΩ
ADC_{res}	Resolution	Programmable ADC resolution	10		24	bit
ENOB	Effective resolution	±1.5sigma	10			bit

4.3 Auxiliary Temperature Sensor Inputs

4.3.1. Internal PTAT Temperature Sensor

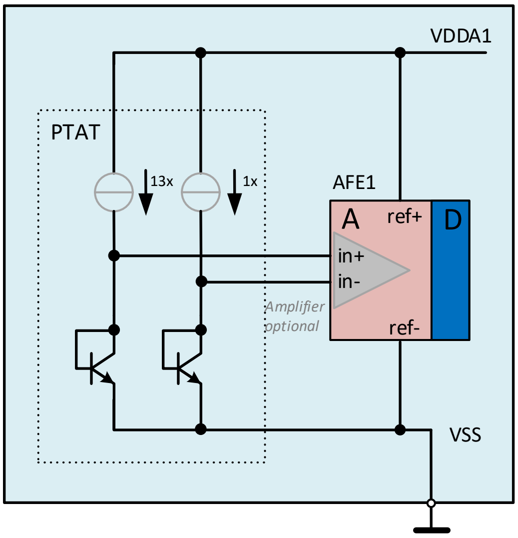


Figure 14: PTAT Sensor Configuration

Table 11: Internal PTAT Parameters

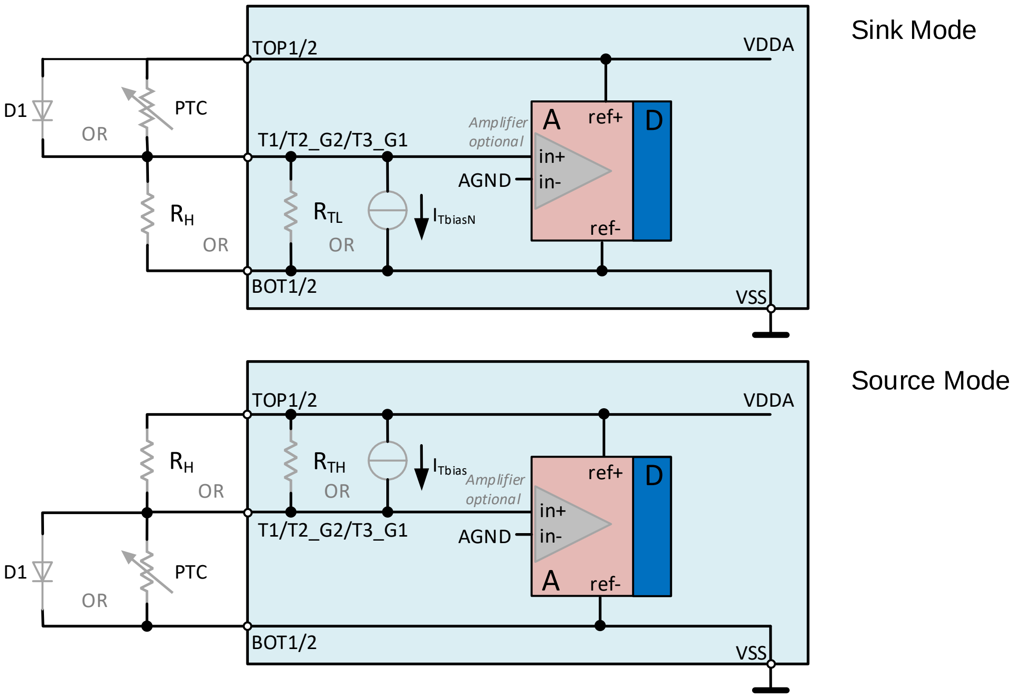
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{meas}	Measurement range		-55		125	°C
E_T	Measurement error	Calibrated	-5		5	K
ADC_{res}	Resolution	Programmable ADC resolution	10		15	bit
T_{res}	Effective resolution	±1.5sigma	2			LSB/°C
S	Sensitivity	Differential output voltage	218		230	µV/K

4.3.2. External Temperature Sensors

Three different external sensor types can be used to measure the temperature of the main sensor or a media temperature in the auxiliary signal path of the AFEs:

- PTC
- Diode
- TC Bridge Sensor

The PTC and Diode Sensors can be supplied either in Sink Mode or in Source Mode as shown in Figure 15. The gray marked components can be activated "either-or" via the GUI. The AGND potential is at VDDA/2.

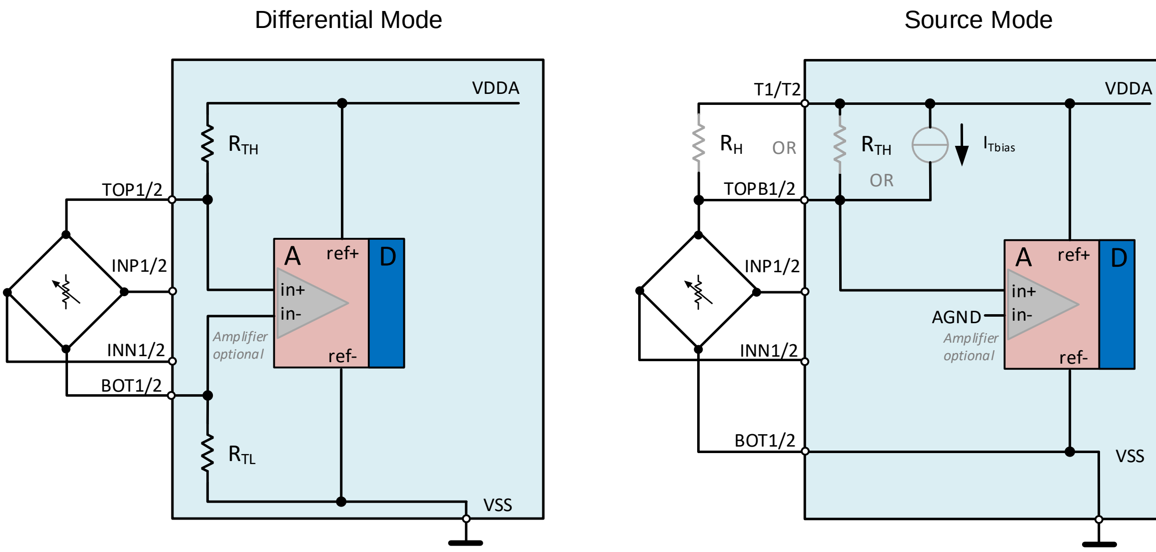


Legend:

Gray components: can be activated "either-or" via the GUI. The AGND potential is at VDDA/2.

Figure 15: PTC, Diode Sensor Bias Configurations

TC Bridge Sensor configurations can be supplied in Differential Mode or Source Mode as shown in Figure 16.



Legend:

Gray components: can be activated "either-or" via the GUI. The AGND potential is at VDDA/2.

Figure 16: TC Bridge Sensor Bias Configurations

Table 12: External Temperature Sensor Parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{sensor}	Sensor resistance (PTC/TC Bridge Sensor)		50		1M	Ω
ADC_{res}	ADC resolution	Programmable ADC resolution	10		15	bit
ENOB	Effective resolution	±1.5sigma	14			bit

4.4 Programmable Gain Amplifier (PGA)

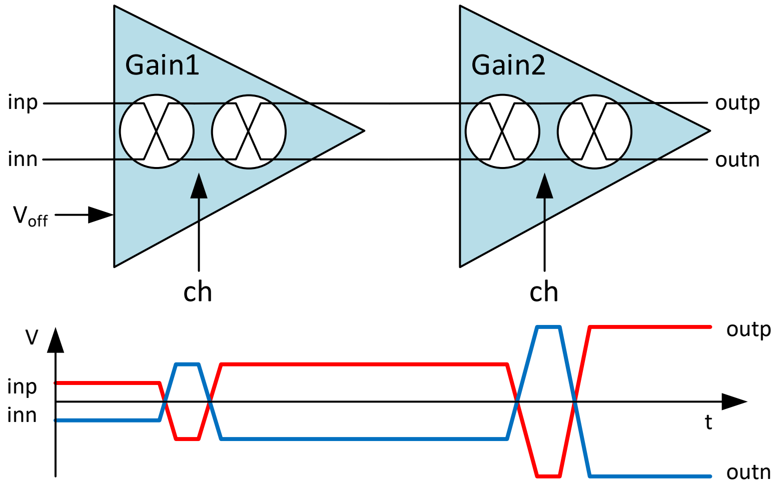


Figure 17: PGA Architecture

The first amplifier (gain1) has a built in PGA offset compensation (auto-zero) that is refreshed at the beginning of every measure cycle. The second stage has no offset compensation. The second stage amplifier offset is present at the PGA output with offset × gain2. Both PGA amplifier stages have built-in chopper functionality to suppress 1/f noise.

The gain settings that can be selectively programmed for both PGA stages are listed in Table 13.

Table 13: PGA Gain Steps

Gain1	Gain2
1.2	1.1
2	1.2
4	1.3
6	1.4
11.9	1.5
19.8	1.6
29.6	1.7
39.2	1.8
58.1	
76.6	
112	
143	
187	
223	
275	

Certain bridge sensors show noticeable DC offsets in their differential output voltage (usable differential voltage range is offset from zero). The sensor DC offset limits the maximum PGA gain, which can be applied without putting the PGA into saturation. In order to compensate for such sensor offsets, the PGA can be programmed to shift the input signal by a certain offset voltage before it gets gained up. The default shift is 0mV, the offset can be compensated by 15 steps in positive and negative direction as shown in Table 14. The PGA offset shift function is offered only for PGA Gain1 ≥ 11.9.

Table 14: PGA Input Offset Compensation Steps

11.9 ≤ Gain1 ≤223 [mV]	Gain1 = 275 [mV]
0	0
±1.9	±1.5
±3.8	±3
±5.6	±4.5
±7.5	±6
±9.4	±7.5
±11.3	±9
±13.1	±10.5
±15	±12
±16.9	±13.5
±18.8	±15
±20.6	±16.5
±22.5	±18
±24.4	±19.5
±26.3	±21
±28.1	±22.5

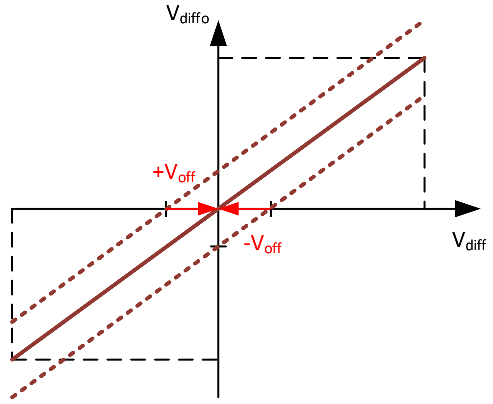


Figure 18: PGA Input Offset Compensation

PGA gain and the Input Offset Compensation value can be programmed separately for the two Main bridge sensors and for the three External auxiliary temperature sensors that can be connected to the ZSSC3281. The PGA Input offset compensation feature is limited to SM+/SM- and SM+ sequencer configurations which are described in section 4.6.

Table 15: PGA Parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Gain	Total PGA gain	Programmable in 15/8 steps: • stage1: 15 steps, 1.2 to 275 • stage2: 8 steps, 1.1 to 1.8	1.32		495	V/V
Egain	Gain error absolute		-5		5	%
Egain	Gain error over-temperature	Temperature compensated sensors do not require calibration over-temperature.	-0.2		0.2	%
V_{diff}	Differential input voltage		-0.8		0.8	V
V_{cmi}	Input common mode voltage			VDDA/2		V
V_{in}	Absolute input voltage at INN, INP		0.2		1.2	V
V_{off}	Input offset compensation	Gain1 ≤223	-28.1		28.1	mV
		Gain1 =275	-22.5		22.5	mV
BW	Bandwidth			5		kHz
t_{az}	Auto-zero time		10			µs
f_{ch}	Chopper frequency			100		kHz

4.5 Analog-to-Digital Converter (ADC)

An incremental delta-sigma analog-to-digital converter (ADC) is used to digitize the PGA signal. To allow optimizing the trade-off between conversion time and resolution, the resolution can be programmed from 10-bit to 24-bit. The ADC processes differential input signals around its input common mode level VDDA/2. Table 16 lists the ADC resolution, signal ranges, conversion times for a single analog-to-digital conversion.

Table 16: ADC Configuration Parameters

ADC Resolution [Bits]	Full Scale Input Voltage V_{fs} [V]	LSB Size V_{LSB} [µV]	Conversion Time, Typical, T_{Conv} [µs]	Conversion Rate, Typical, F_{Conv} [kHz]
10	±1.375	2768.638	32.54	30.73
11	±1.382	1391.718	43.75	22.86
12	±1.387	698.499	59.59	16.78
13	±1.391	350.189	81.99	12.20
14	±1.394	175.428	113.68	8.80
15	±1.395	87.832	158.49	6.31
16	±1.397	43.958	221.86	4.51
17	±1.398	21.994	311.48	3.21
18	±1.398	11.002	438.22	2.28
19	±1.399	5.503	617.46	1.62
20	±1.399	2.752	870.94	1.15
21	±1.399	1.376	1229.41	0.81
22	±1.400	0.688	1736.38	0.58
23	±1.400	0.344	2453.33	0.41
24	±1.400	0.172	3467.25	0.29

The ADC can perform an additional offset shift (independent of the PGA shifting) in order to adapt input signals with offsets to the ADC input range. Enabling the offset shift causes the ADC to perform an additional amplification of the ADC's input signal by factor x2. This must be considered for a correct PGA configuration setup.

The ADC offset shift feature is limited to SM+/SM- and SM+ sequencer configurations which are described in section 4.6.

The shift values in Table 17 are related to the input voltages at INP, INN:

- Full scale differential input voltage: $V_{INdiff\_fs} = \frac{V_{fs}}{Gain}$
- Differential input shift voltage: V_{INdiff_shift}
- Maximum, minimum differential input voltage: V_{INdiff_max} , V_{INdiff_min}

Table 17: ADC Input Offset Shift Steps

PGA Polarity	ADC Shift Enable	ADC Gain	ADC shift	$V_{INdiff\_shift}/V_{INdiff\_fs}$	$V_{INdiff\_min}/V_{INdiff\_fs}$	$V_{INdiff\_max}/V_{INdiff\_fs}$
Positive	0	x1	0	no shift	-1	+1
Negative			0	no shift	+1	-1
Positive	1	x2	1	7/8	-1/16	+15/16
			2	6/8	-2/16	+14/16
			3	5/8	-3/16	+13/16
			4	4/8	-4/16	+12/16
			5	3/8	-5/16	+11/16
			6	2/8	-6/16	+10/16
			7	1/8	-7/16	+9/16
			0	no shift	-1/2	+1/2
Negative			0	no shift	+1/2	-1/2

PGA Polarity	ADC Shift Enable	ADC Gain	ADC shift	$V_{INdiff\_shift}/V_{INdiff\_fs}$	$V_{INdiff\_min}/V_{INdiff\_fs}$	$V_{INdiff\_max}/V_{INdiff\_fs}$
Negative			1	1/8	-9/16	+7/16
			2	2/8	-10/16	+6/16
			3	3/8	-11/16	+5/16
			4	4/8	-12/16	+4/16
			5	5/8	-13/16	+3/16
			6	6/8	-14/16	+2/16
			7	7/8	-15/16	+1/16

4.6 AFE Sequencer

The measurement flow, especially the frequency of Main bridge measurements vs. Auxiliary measurements can be configured by the user. Once started by the ARM M3 MCU, the measurement flow runs autonomously controlled by the AFE. The AFE Sequencer state machine ensures predictable measurement timing in the continuous cyclic operation of ZSSC3281.

The AFE Sequencer carries out AFE measurements based on a measurement slot mechanism. There can be up to eight measurement slots assigned per AFE, which form a single measurement sequence. A measurement sequence can be executed only once (for example, initiated by a dedicated command request) or continuously cycled in Cyclic Mode operation of ZSSC3281.

Each of the measurement slots can be individually configured for the following measurement types:

- Sensor Measurement SM+: bridge inputs INP/INN directly converted (non-inverted)
- Sensor Measurement SM-: bridge inputs INP/INN flipped (inverted)
- Auxiliary Measurement $aux_{i:}$ cycles through the Auxiliary measurement vector

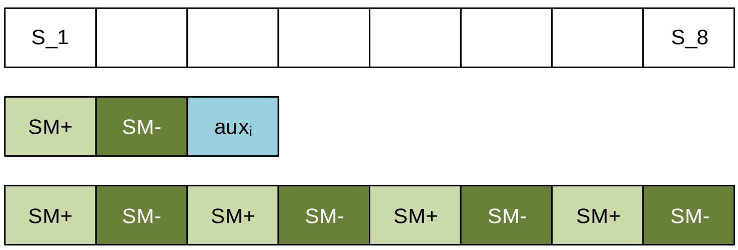


Figure 19: Measurement Slot Configuration with Two Example Configurations

The actual number of measurement slots per measurement sequence can be defined by the user and may vary between 1 and 8. The hardware allows to configure any combination based on the above definitions, but not all combinations lead to reasonable measurement schemes. The GUI supports the user in selecting proper measurement schemes. Figure 19 shows to reasonable example configurations. The measurement schemes are explained in further detail in subsequent chapters 4.6.3 to 4.6.5.

Auxiliary measurements usually have lower response time requirements than measurements on the main sensor bridge. The auxiliary measurements are therefore cycled orthogonal to the main loop of the sequencer. Activated auxiliary measurements become listed in the so called Auxilary measurement vector. The vector index ‘i’ gets increased after each executed aux_i slot and starts over after the entire set of active measurements was completed. The configuration options for of auxiliary measurements are further detailed in section 4.6.2

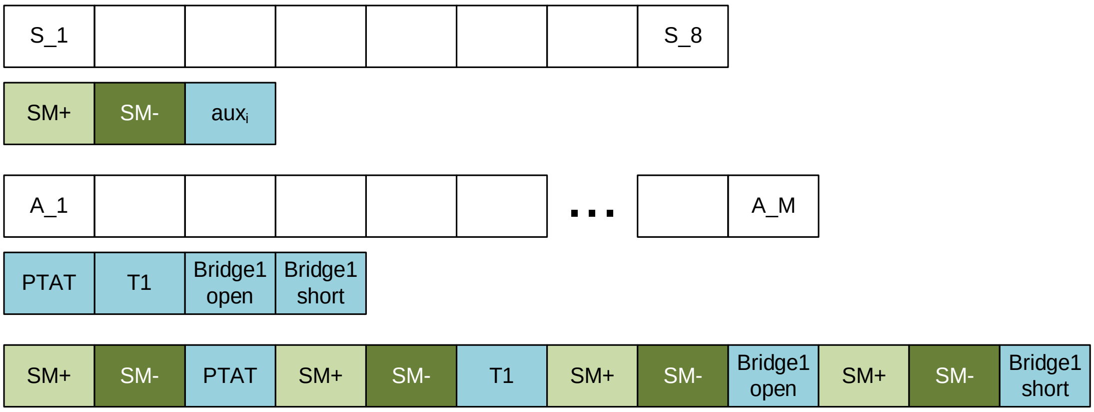


Figure 20: Auxiliary Measurement Configuration, and Corresponding Measurement Flow

Figure 20 illustrates the sequencer operation with an example configuration. During the 3rd measurement slot (configured as aux_i), the first enabled auxiliary measurement is executed ("PTAT", internal temperature sensor). When the measurement sequence (SM+/SM-/aux_i) is executed again in Cyclic Mode, the next enabled auxiliary measurement is executed ("T1", external temperature sensor). Similarly, "Bridge1 open" and "Bridge1 short" diagnostics measurements are carried out in following measurement sequence cycles. During the 5th execution of the measurement sequence, the PTAT auxiliary measurement is carried out again.

4.6.1. Bridge Sensor Measurement Configuration

The main bridge sensor signals can be measured in three ways:

- SM+/SM- (or SM-/SM+) measurement
- SM+/AZ measurement
- SM+ without AUX_AZ measurement

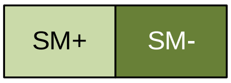


Figure 21: SM+/SM- (or SM-/SM+) Measurement

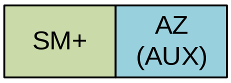


Figure 22: SM+/AZ Measurement

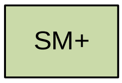


Figure 23: SM+ Without AZ Measurement

Configurations in Figure 21 and Figure 22 provide digital offset compensation of the entire signal path in the Analog front end. The respective calculations that need to be done are shown in Figure 35 in section 5.1. The configuration in Figure 23 only provides analog offset compensation in the first stage of the PGA. The offsets of the second PGA stage and the ADC offset are not compensated.

In the SM+/SM- configuration, the bridge inputs INP/INN are first converted straight forward in the SM+ measurement slot and second with an internally flipped INP/INN input signal in SM- slot. For the SM+/AZ configuration, the second measurement (AZ) is performed without applied input signal. INP/INN become disconnected form the sensor and internally shorted for AZ measurements.

Since signal integration time the SM+/SM- configuration is twice as long as in in the SM+/AZ configuration (same ADC resolution settings assumed), the SM+/SM- configuration achieves approx. 0.5 bit better noise performance than the SM+/AZ configuration. However, the longer input signal integration time of the SM+/SM- configuration leads to an increased measurement latency as described in section 4.6.3 and 4.6.4.

The Auto-zero measurement (AZ) belongs to the group of auxiliary measurements and is cycled less often if further auxiliary measurements are defined in the Auxiliary measurement vector. Since the offset in the internal signal path varies rather slowly, the Auto-zero compensation still remains very accurate, even for a long Auxiliary measurement vector.

Because most sensor applications also require other auxiliary measurements, the assignment of the AZ measurement to the group of auxiliary measurements helps to reduce the worst case measurement latency on the main bridge sensor. This is because the SM- slot as needed in configuration of Figure 21, can be omitted.

The lowest measurement latency is achieved with the "SM- only" configuration in Figure 23. However, this is only true if no other auxiliary measurements are needed for the desired sensor application.

A further influence on the overall measurement time has the input settling time, which is required depending on the output resistance of the external sensors, respective capacitive loads on the signal lines and the ADC resolution selected by the user. The input settling time is always inserted before an ADC conversion starts and can be configured in the GUI for main bridge measurements via Configure\AFE\Bridge\SetTime[µs] and for auxiliary temperature measurements via Configure\AFE\Temperature\SetTime[µs].

Considering achievable measurement latencies and noise performance, configuration in Figure 21 is better when higher ADC resolutions are required or for sensor configurations with fast input settling, while configuration in Figure 22 and Figure 23 are preferable when lower ADC resolutions become selected or for sensor configurations requiring long input settling times (bridge settling time has a considerable impact on the timing budget).

4.6.2. Auxiliary Measurement Configuration

The supported auxiliary measurements are:

- Auto-zero for internal signal path
- Temperature on sensor input T1
- Temperature on sensor input T2
- Temperature on sensor input T3
- Internal PTAT
- AFE diagnostic checks
  - Sensor connection checks for all external sensors (Short to TOPx pin or BOTx pin and Open)
  - Bridge sensor leakage to VSS in Thermocouple/Thermopile operation mode of the AFE
  - Bridge signal range check
  - AFE gain and offset drift supervision via internal reference DAC

They can be activated in the GUI via tabs Configure\AFE\Sequencer, Configure\AFE\Temperature Selection and Diagnostic\Sensor/AFE.

4.6.3. Deterministic Input Step Response with SM+/SM- Configuration

As described in section 4.6.1, sensor configurations with fast input settling or applications requiring higher ADC resolutions are better served with the SM+/SM- scheme for the main bridge measurement. For the following step response consideration, the below application example is used:

- Sensor Measurement (non-inverted)
- Sensor Measurement (inverted)
- Auxiliary Measurement (e.g. for sensor temperature)
- Note: SM+ and SM- can be exchanged yielding to the same result

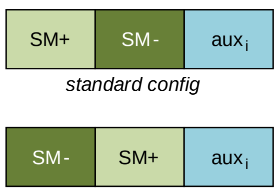


Figure 24: SM+/SM- Configuration

The worst-case input to output latency consists of:

- 4 sensor A2D-conversion times (duration depending on selected ADC resolution)
- 1 auxiliary conversion time (fixed duration, based on longest auxiliary conversion timing)
- 1 SSC calculation

- 1 settling time at AOUT, if AOUT is enabled

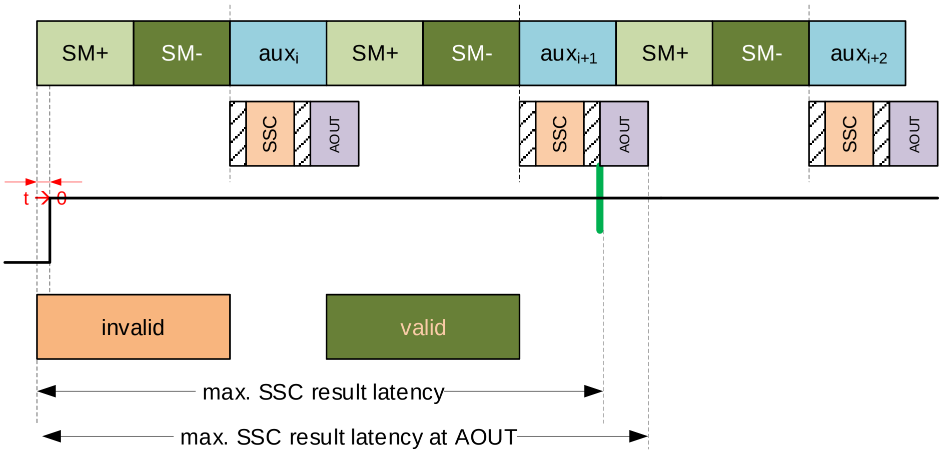


Figure 25: Measurement Flow and Latency for SM+/SM- Configuration

4.6.4. Deterministic Input Step Response with SM+/AZ Configuration

Since the SM+/SM- configuration samples the input signal twice as long as the SM+/AZ configuration and it suffers a noticeable timing overhead for sensor configurations with slow sensor input signal settling, a second SM+/AZ measurement scheme with deterministic step response times is available. For the following step response consideration, the below application example is used:

- Sensor measurement (non-inverted)
- Auxiliary measurement (for example, for sensor path Auto-zero and/or Sensor Temperature) within the auxiliary measurement vector

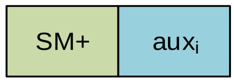


Figure 26: SM+/AZ Configuration

As shown in Figure 27, the worst-case latency consists of:

- 2 sensor AD-conversion times (duration depending on selected ADC resolution)
- 1 auxiliary conversion time (fixed duration, based on longest auxiliary conversion timing)
- 1 SSC calculation
- 1 settling time at AOUT, if AOUT is enabled

Assuming equal ADC resolution settings for the SM+/SM- configuration as described in section 4.6.3 and the SM+/AZ configuration described in this section, the worst case input to output latency is shorter by two sensor AD-conversion times in case of the SM+/AZ setup. The auxiliary measurement duration in the SM+/AZ setup may become slightly longer than for the SM+/SM- configuration, since it is determined by the AZ measurement time if the selected resolution of the main bridge is larger than the resolutions of all other active auxiliary measurements. This is because the resolution of the AZ measurement is set by the resolution of the SM+ measurement and the longest measurement of the Auxiliary measurement vector determines the duration of the aux_i slot(s)

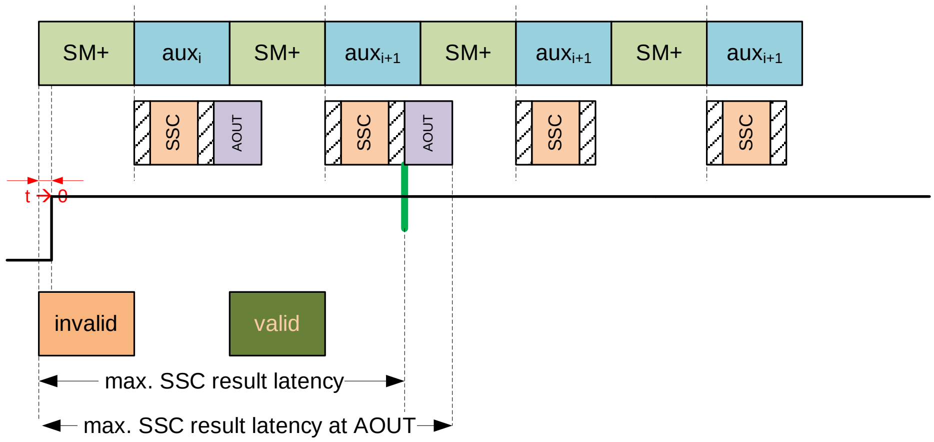


Figure 27: Measurement Flow and Latency for SM+/AZ Configuration

4.6.5. Accelerated Bridge Measurements with Sparsely Inserted Auxiliary Measurements

For applications which focus on highest conversion rates at the bridge sensor input but do not require a deterministic maximum input to output latency of the corrected sensor signal, auxiliary measurements can be sparsely inserted to occur only after a certain number of measurement sequences were executed by the AFE sequencer. This way, auxiliary measurements become executed even more seldom, giving the main sensor bridge measurements priority.

The AFE sequencer can be configured such that an aux_i measurement is only executed (inserted) after every Px measurement sequence. P can be selected as 2, 4, or 8. Figure 28 shows an example of a measurement flow with P = 2.

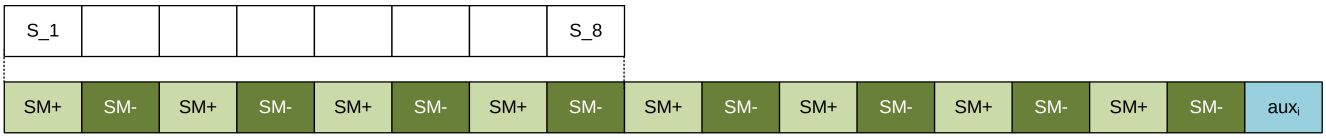


Figure 28: Auxiliary Measurement Executed after Every Second Measurement Cycle

Figure 29: Sequencer Setup for Highest Update Rate on Bridge Sensor – aux_i Executed after Eighth Measurement Cycle

4.7 AFE Dual Speed Mode

The AFE Dual Speed Mode operation is intended for single bridge sensor applications that require a fast transient step response combined with a high resolution steady state signal at analog and serial interface outputs. It can be activated in the GUI via Configure\AFE\Sequencer\AFE Selection and Configurability\Dual speed AFE with AOUT.

In AFE Dual Speed Mode the sensor bridge is measured by both frontends (AFE1 and AFE2) in parallel, see Figure 30 for the required input configuration. AFE Dual Speed Mode allows the operation of one external temperature sensor (T1) or the internal temperature sensor (PTAT).

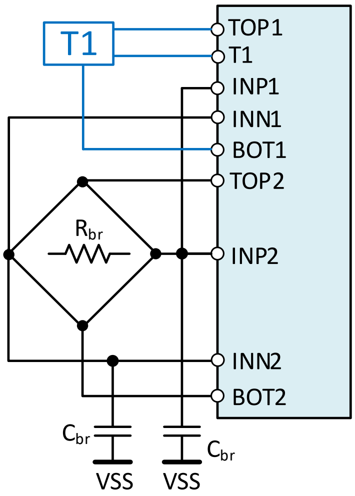


Figure 30: Input Configuration in AFE Dual Speed Mode

The fast reaction of the bridge sensor input is achieved through AFE1, which runs at low resolution (10 bit) and highest update rate. AFE2 runs on high resolution (SM+/SM- sequencer, 16bit) and a slower update rate.

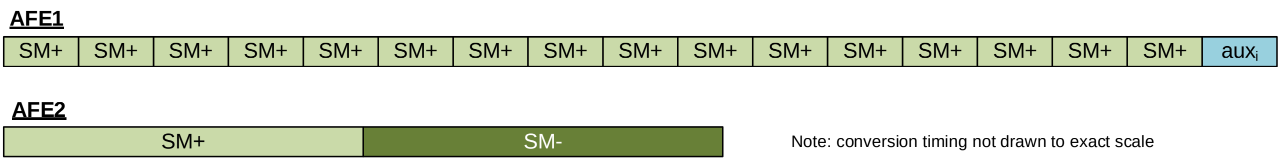


Figure 31: Sequencer Illustration for AFE1 and AFE2

A digital algorithm decides whether the SSC conditioned results of AFE1 or AFE2 are forwarded to the outputs. By default, the more precise data of AFE2 is forwarded. As soon as a significant signal step occurs at the bridge sensor inputs, the algorithm switches from the slower AFE2 to the fast AFE1. After the transition to AFE1, the outputs follow the AFE1 results with its speed, accuracy, and noise properties.

AFE1 stays active for at least the duration of approximately two slow AFE2 conversions. If no further significant input signal variation is detected within this time, the algorithm switches back from AFE1 to AFE2. See Figure 32 for a graphical explanation of the algorithm.

An input step is detected if the signal difference between AFE1 and AFE2 crosses Threshold 1 (can be setup via GUI Configure\AFE\Sequencer\Dual Speed AFE with AOUT). Once an input step was detected and outputs were switched to AFE1, a count down timer is started to let AFE1 process a number of approximately 60 samples. The actual sample number is between 57 and 61, depending on the configured AFE2 bridge settling time and is automatically calculated by the GUI. Once the count down timer expired, the outputs are switched back from AFE1 to AFE2 if no further step was detected.

To judge the signal variation after the initial step detection, all new AFE1 measurement results are compared against an AFE1 reference result that was stored at the preceding threshold crossing. A further step is detected when the comparison difference is larger than Threshold 2 (can also be setup via GUI). In this case a new AFE1 reference value is stored and the count down timer is reset.

The algorithm detects signal changes which span over multiple AFE1 conversions (see Figure 32), it compares the current measurement result with a reference value from several conversion periods back in time. The user can modify the dynamic behavior of the algorithm be modifying the Threshold 1 and Threshold 2 settings.

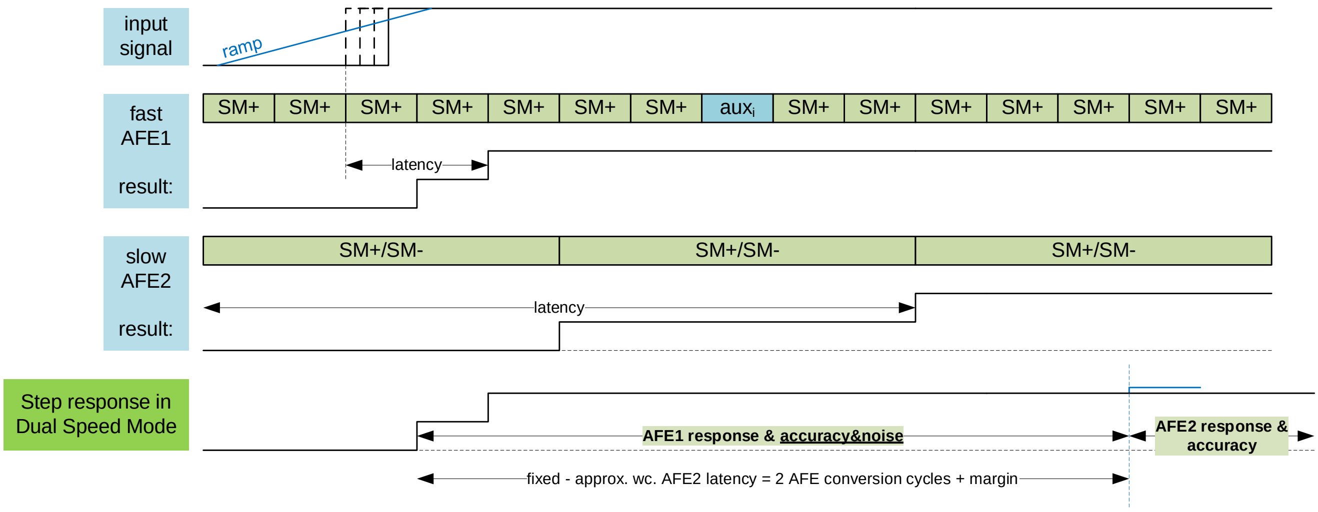


Figure 32: Step Response in Dual Speed Mode for a Significant Single Input Step

The AFE Dual Speed Mode is available for following SSC outputs:

- all Analog Output (AOUT) Modes with exception of 2-wire current loop mode
- all Serial interface outputs

AFE Dual Speed Mode is not available for:

- 2-wire current loop operation
- PMW/FOUT output modes
- Signal Post processing features: EOC, ALARM, Output Filtering.
- AFE diagnosis features

The dynamic Sensor Bridge configuration is fixed to:

- AFE1: 10bit, SM+ only
- AFE2: 16bit, SM+/SM-
- The aux$_i$ cycle in the sequencer becomes automatically activated if T1 or PTAT are selected. If no temperature sensor is selected, the aux$_i$ cycle shown in Figure 31 is removed.

With the dynamic AFE configuration setup a worst case input step latency of 0.35ms is achievable at AOUT. The precise signal settles maximum 5ms after stable input signal.

5. Sensor Signal Conditioning

5.1 Signal Conditioning Data Path

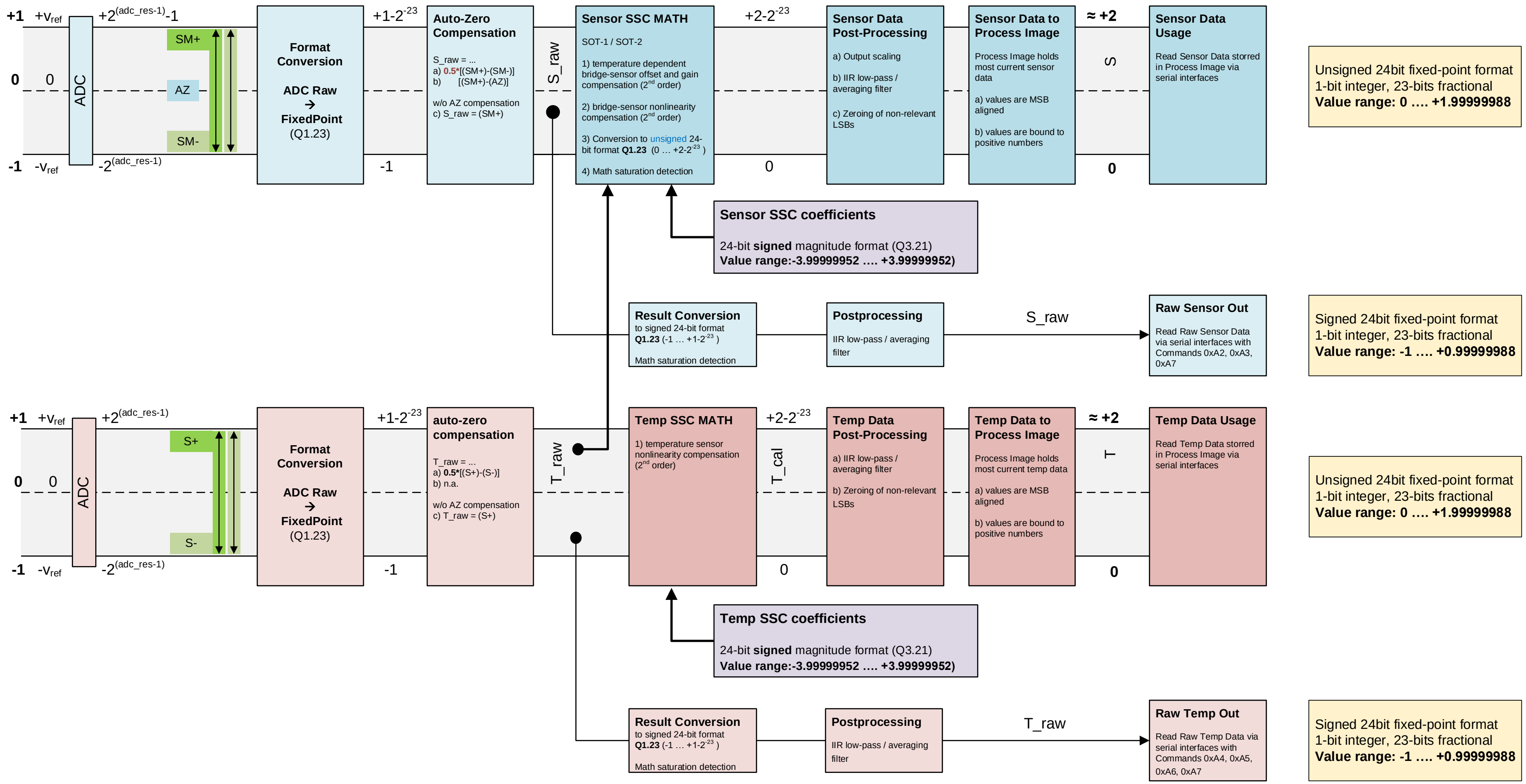


Figure 33: SSC Signal Data Path

5.2 Basic SSC Math options

ZSSC3281 supports basic second-order compensation of sensor nonlinearities. The following basic SSC math options are available:

- Sensor signal correction
  - SOT Curve-0: Parabolic compensation curve
  - SOT Curve-1: S-shaped compensation curve
- Temperature signal correction

The parabolic compensation is recommended for most sensor types. The applied SSC math option can be selected in the GUI through the field Calibration\Curve.

5.2.1. Main Sensor Signal Correction

The available SSC capabilities for SOT Curve-0 and SOT Curve-1 are described below. The used equation terms are as follows:

S Corrected sensor reading output via I2C, OWI, or SPI; range [0_{HEX} to $FFFFFF_{HEX}$]

S_Raw Raw sensor reading from ADC (after AZ correction, if selected); range [$-7FFFFF_{HEX}$ to $7FFFFF_{HEX}$]

Gain_S Sensor gain term; range [$-7FFFFF_{HEX}$ to $7FFFFF_{HEX}$]

Offset_S Sensor offset term; range [$-7FFFFF_{HEX}$ to $7FFFFF_{HEX}$]

Tcg Temperature coefficient gain term; range [$-7FFFFF_{HEX}$ to $7FFFFF_{HEX}$]

Tco Temperature coefficient offset term; range [$-7FFFFF_{HEX}$ to $7FFFFF_{HEX}$]

T_Raw Raw temperature reading (after AZ correction); range [$-7FFFFF_{HEX}$ to $7FFFFF_{HEX}$]

SOT_tcg Second-order term for Tcg non-linearity; range [$-7FFFFF_{HEX}$ to $7FFFFF_{HEX}$]

SOT_tco Second-order term for Tco non-linearity; range [$-7FFFFF_{HEX}$ to $7FFFFF_{HEX}$]

SOT_sens Second-order term for sensor non-linearity; range [$-7FFFFF_{HEX}$ to $7FFFFF_{HEX}$]

SENS_shift Post-calibration, post-assembly offset shift; range [$-7FFFFF_{HEX}$ to $7FFFFF_{HEX}$]

$|\dots|$ Absolute value

$[\dots]_{ll}^{ul}$ Bound/saturation number range from ll to ul, over-flow/under-flow is reported as saturation in the status byte

All raw data and compensation coefficients supplied to the formulas are required in the following 24-bit data format:

Table 18: Data Format of Raw ADC Readings

Bit-Number	23	22	21	20	…	2	1	0
Meaning, Weighting	-2^{0}	2^{-1}	2^{-2}	2^{-3}	…	2^{-21}	2^{-22}	2^{-23}

Table 19: Data Format of 24-bit SSC Coefficients

Bit-Number:	23	22	21	20	…	2	1	0
Meaning, Weighting	0 = positive 1 = negative	2^{1}	2^{0}	2^{-1}	…	2^{-19}	2^{-20}	2^{-21}

The compensated result data is supplied in the following 24-bit data format:

Table 20: Data Format of Corrected SSC Results (*S* and *T*)

Bit-Number:	23	22	21	20	…	2	1	0
Meaning, Weighting	2^{0}	2^{-1}	2^{-2}	2^{-3}	…	2^{-21}	2^{-22}	2^{-23}

5.2.1.1. SOT Curve-0 (Parabolic Compensation)

Simplified:

$$K_1 = 2^{23} + \frac{T\_Raw}{2^{23}} \cdot \left(\frac{4 \cdot SOT\_tcg}{2^{23}} \cdot T_{Raw} + 4 \cdot Tcg\right)$$ **Equation 1**

$$K_2 = 4 \cdot Offset\_S + S\_raw + \frac{T\_Raw}{2^{23}} \cdot \left(\frac{4 \cdot SOT\_tco}{2^{23}} \cdot T_{Raw} + 4 \cdot Tco\right)$$ **Equation 2**

$$Z_{SP} = \frac{4 \cdot Gain\_S}{2^{23}} \cdot \frac{K_1}{2^{23}} \cdot K_2 + 2^{23} \quad \text{(delimited to positive number range)}$$ **Equation 3**

$$S = \frac{Z_{SP}}{2^{23}} \cdot \left(\frac{4 \cdot SOT\_sens}{2^{23}} \cdot Z_{SP} + 2^{23}\right) + SENS\_shift \quad \text{(delimited to positive number range)}$$ **Equation 4**

Complete:

$$K_1 = \left[2^{23} + \left[\frac{T\_Raw}{2^{23}} \cdot \left[\left[\frac{SOT\_tcg}{2^{21}} \cdot T_{Raw}\right]_{-2^{25}}^{2^{25}-1} + 4 \cdot Tcg\right]_{-2^{25}}^{2^{25}-1}\right]_{-2^{25}}^{2^{25}-1}\right]_{-2^{25}}^{2^{25}-1}$$ **Equation 5**

$$K_2 = \left[4 \cdot Offset\_S + \left[S\_raw + \left[\frac{T\_Raw}{2^{23}} \cdot \left[\left[\frac{SOT\_tco}{2^{21}} \cdot T_{Raw}\right]_{-2^{25}}^{2^{25}-1} + 4 \cdot Tco\right]_{-2^{25}}^{2^{25}-1}\right]_{-2^{25}}^{2^{25}-1}\right]_{-2^{25}}^{2^{25}-1}\right]_{-2^{25}}^{2^{25}-1}$$ **Equation 6**

$$Z_{SP} = \left[\left[\frac{Gain\_S}{2^{21}} \cdot \left[\frac{K_1}{2^{23}} \cdot K_2\right]_{-2^{25}}^{2^{25}-1}\right]_{-2^{25}}^{2^{25}-1} + 2^{23}\right]_{0}^{2^{25}-1}$$ **Equation 7**

$$S = \left[\left[\frac{Z_{SP}}{2^{23}} \cdot \left[\left[\frac{SOT\_sens}{2^{21}} \cdot Z_{SP}\right]_{-2^{25}}^{2^{25}-1} + 2^{23}\right]_{-2^{25}}^{2^{25}-1}\right]_{-2^{25}}^{2^{25}-1} + SENS\_shift\right]_{0}^{2^{24}-1}$$ **Equation 8**

5.2.1.2. SOT Curve-1 (S-shaped Compensation)

Simplified:

$$Z_{SS} = \frac{4 \cdot Gain\_S}{2^{23}} \cdot \frac{K_1}{2^{23}} \cdot K_2 \quad \text{(} K_1 \text{ and } K_2 \text{ according to Equation 1 and Equation 2)}$$ **Equation 9**

$$S = \frac{Z_{SS}}{2^{23}} \cdot \left(\frac{4 \cdot SOT\_sens}{2^{23}} \cdot |Z_{SS}| + 2^{23}\right) + 2^{23} + SENS\_shift \quad \text{(delimited to positive number range)}$$ **Equation 10**

Complete:

$$Z_{SS} = \left[\frac{Gain\_S}{2^{21}} \cdot \left[\frac{K_1}{2^{23}} \cdot K_2\right]_{-2^{25}}^{2^{25}-1}\right]_{-2^{25}}^{2^{25}-1}$$ **Equation 11**

$$S = \left[\left[\left[\frac{Z_{SS}}{2^{23}} \cdot \left[\left[\frac{SOT\_sens}{2^{21}} \cdot |Z_{SS}|\right]_{-2^{25}}^{2^{25}-1} + 2^{23}\right]_{-2^{25}}^{2^{25}-1}\right]_{-2^{25}}^{2^{25}-1} + 2^{23}\right]_{-2^{25}}^{2^{25}-1} + SENS\_shift\right]_{0}^{2^{24}-1}$$ **Equation 12**

5.2.2. Temperature Signal Correction

Temperature is measured either internally by the ZSSC3281, through an additional external element, or by means of a combination of ZSSC3281 internal and external temperature sensing capabilities. Temperature correction contains both linear gain and offset terms as well as a second-order term to correct for any nonlinearities. For temperature, second-order compensation is always parabolic.

The correction equation terms are as follows:

- *T* — Corrected temperature sensor reading output via digital interface; range [0_{HEX} to $FFFFFF_{HEX}$]
- *Gain_T* — Gain coefficient for temperature; range [$-7FFFFF_{HEX}$ to $7FFFFF_{HEX}$]
- *T_Raw* — Raw temperature reading after AZ correction; range [$-7FFFFF_{HEX}$ to $7FFFFF_{HEX}$]
- *Offset_T* — Offset coefficient for temperature; range [$-7FFFFF_{HEX}$ to $0x7FFFFF_{HEX}$]
- *SOT_T* — Second-order term for temperature source nonlinearity; range [$-7FFFFF_{HEX}$ to $7FFFFF_{HEX}$]
- *T_Shift* — Shift for post-calibration/post-assembly offset compensation [$-7FFFFF_{HEX}$ to $7FFFFF_{HEX}$]

The correction formula is best represented as a two-step process as follows:

Simplified:

$$Z_T = \frac{4 \cdot Gain\_T}{2^{23}} \cdot (T\_Raw + 4 \cdot Offset\_T) + 2^{23}$$ (delimited to positive number range) **Equation 13**

$$T = \frac{Z_T}{2^{23}} \cdot \left(\frac{4 \times SOT\_T}{2^{23}} \cdot Z_T + 2^{23}\right) + T\_shift$$ (delimited to positive number range) **Equation 14**

Complete:

$$Z_T = \left[\left[\frac{Gain\_T}{2^{21}} \cdot [T\_Raw + 4 \cdot Offset\_T]_{-2^{25}}^{2^{25}-1}\right]_{-2^{25}}^{2^{25}-1} + 2^{23}\right]_{0}^{2^{25}-1}$$ **Equation 15**

$$T = \left[\left[\frac{Z_T}{2^{23}} \cdot \left[\left[\frac{SOT\_T}{2^{21}} \cdot Z_T\right]_{-2^{25}}^{2^{25}-1} + 2^{23}\right]_{-2^{25}}^{2^{25}-1}\right]_{-2^{25}}^{2^{25}-1} + T\_shift\right]_{0}^{2^{24}-1}$$ **Equation 16**

6. Post Processing Options for Conditioned Sensor Signals

6.1 Signal Post Processing Flow Chart

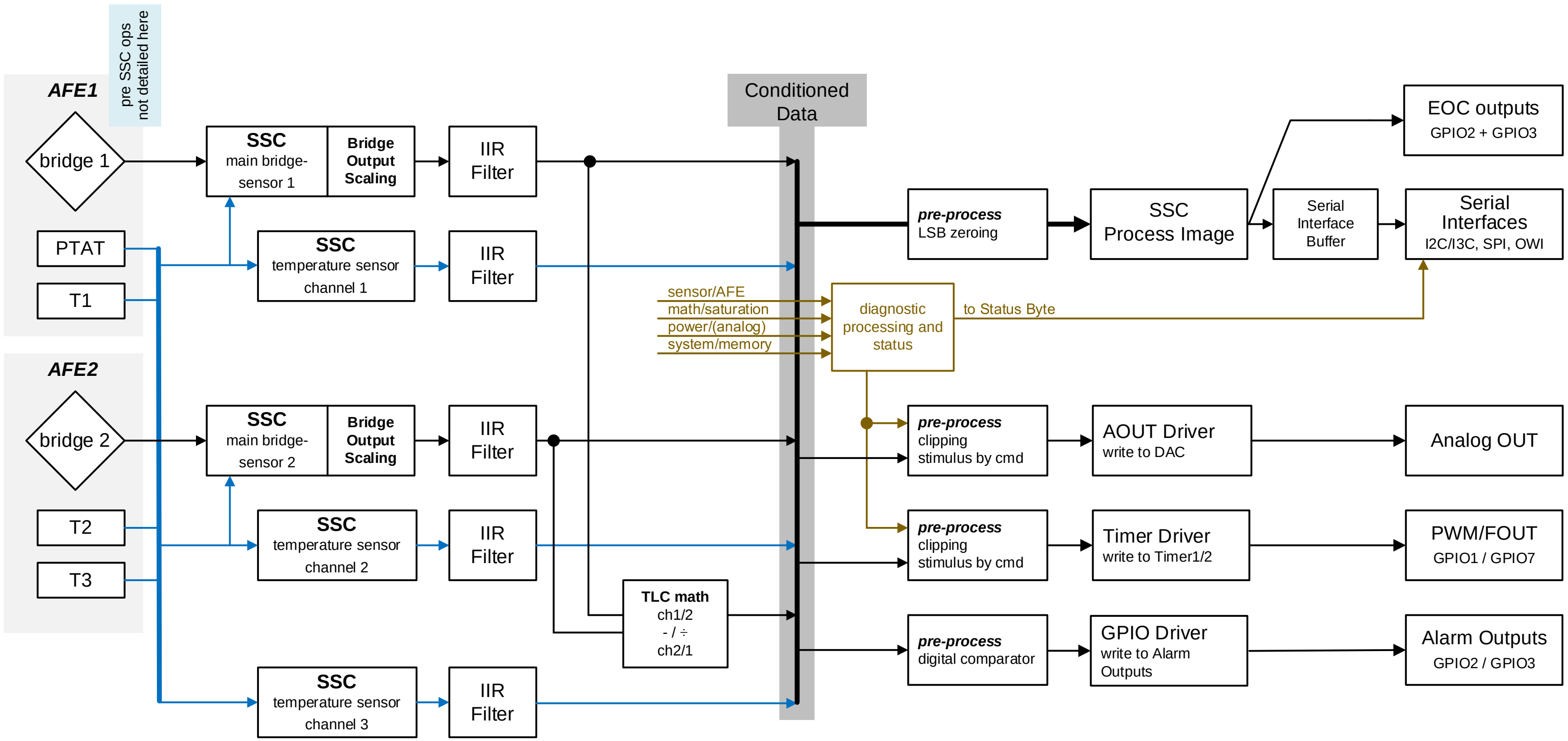


Figure 34: Sensor Signal Flow Chart from Input to Output

6.2 Bridge Output Scaling

ZSSC3281 offers a linear rescaling function to amplify or compress a partial region of the sensor input range to the desired signal output range. The feature is intended for customers who need to separate product derivatives after a common sensor calibration step.

The rescaling feature applies the following formula to the SSC conditioned outputs of the main bridge sensor:

$$y = \left[\frac{8 \cdot OutScaleGain}{2^{23}} \cdot (x + 8 \cdot OutScaleOffset)\right]_{0}^{2^{24}-1}$$ **Equation 17**

The Coefficients *OutScaleGain* and *OutScaleOffset* are stored in the CCP (Configuration and Calibration Page) of ZSSC3281 in signed magnitude format. *OutScaleGain* is limited to a maximum gain of x4. The *OutScaleOffset* can vary from -1.5 to 0 related to the SSC result number range 0 to ~2.

Table 21: Data Format of Output Scaling Coefficients in CCP

Bit-Number:	23	22	21	20	…	2	1	0
Meaning, Weighting	0 = positive 1 = negative	2^2	2^1	2^0	2^{-1}	…	2^{-19}	2^{-20}

The GUI supports the calculation of *OutScaleGain* and *OutScaleOffset* based on provided relative input and output range specifications (Can be set on the GUI tab Configure\Output Scaling).

6.3 IIR Filtering

The conditioned outputs of the two Main sensor bridge channels CH1 and CH2 and the conditioned outputs of the Temperature channels TCh1 to TCh3 can be low pass filtered for noise reduction. Each channel is equipped with an independent configurable IIR Filter. The mathematical filter description is as follows

$$y_0 = x_0$$ **Equation 18**

$$y_i = y_{i-1} + \frac{(x_i - y_{i-1}) \cdot \text{Diff}}{\text{Avg}}$$ **Equation 19**

where:

$$\text{Diff} = \text{FiltDiff} + 1$$ **Equation 20**

$$\text{Avg} = 2^{\text{FiltAvg}}$$ **Equation 21**

FiltDiff and *FiltAvg* represent the filter coefficients which are stored as unsigned 3-bit values per filter channel in the CCP of ZSSC3281. They are determined by the GUI (Configure\Filter) depending on the filter Tau-selections made by the user. For a stable system, the Diff ≤ Avg must be true.

The filter Tau can be calculated by:

$$\frac{\text{Diff}}{\text{Avg}} = \alpha \approx \frac{1}{\tau_{dig}} = \frac{\Delta T}{\tau_{(ana)}}$$ **Equation 22**

$$\tau_{dig} = -\frac{1}{\ln(1-\alpha)}$$ **Equation 23**

τ_{dig} is given in number of digital samples.

6.4 Third Logic Channel Combination

The potentially pre-scaled and filtered two Main sensor bridge channels Ch1 and Ch2 of ZSSC3281 can be mathematically combined to calculate the output of a third logic channel Ch3. Channel Ch3 is only available in the synchronized AFE mode which is enabled via the GUI menu Configure\AFE\Sequencer\AFE Selection and Configurability\selection: “AFE1+AFE2, config equally”.

The calculation result on Ch3 is available through serial interface read out only. The digital output format is signed 32-bit (two's complement), see Table 22. Outputting the Ch3 result at AOUT and FOUT/PWM will be made available in a future release of the ZSSC3281 firmware.

The Third Logic Channel (TLC) can be configured via the GUI menu Configure\TLC menu.

Following mathematical operations are available:

- Subtraction: (Ch1 – Ch2) or (Ch2 – Ch1)
- Division: (Ch1 / Ch2) or (Ch2 / Ch1)

Calibration of the sensor channels Ch1 and Ch2 must still be done independently applying the single channel calibration routines.

Table 22: Data Format of Logic Output Channel Ch3 at Serial Interface

Bit-Number	31	30	…	24	23	22	21	20	…	2	1	0
Meaning, Weighting	-2^{8}	2^{7}	…	2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	…	2^{-21}	2^{-22}	2^{-23}

6.5 EOC/Alarm Functions

The Pins EOC/ALARM 1 (GPIO2) and EOC/ALARM 2 (GPIO3) can be configured to operate either as an end-of-conversion (EOC) transducer or as a configurable switch/alarm transducer for the respective SSC conditioned outputs of the main bridge sensors.

To support different external logic, the polarity of the EOC/ALARM outputs can be configured as active high or active low (can be setup via GUI Configure\EOC/ALARM\Output Polarity).

6.5.1. EOC Function

If the EOC output mode is active (can be setup via GUI Configure\EOC/ALARM\Selected Mode\EOC), an EOC event is signalled at the GPIO pin as soon as a new SSC-corrected measurement result of the bridge sensor is available for read out by the host system. The EOC signal pulse is approximately 5µs wide (see Figure 36).

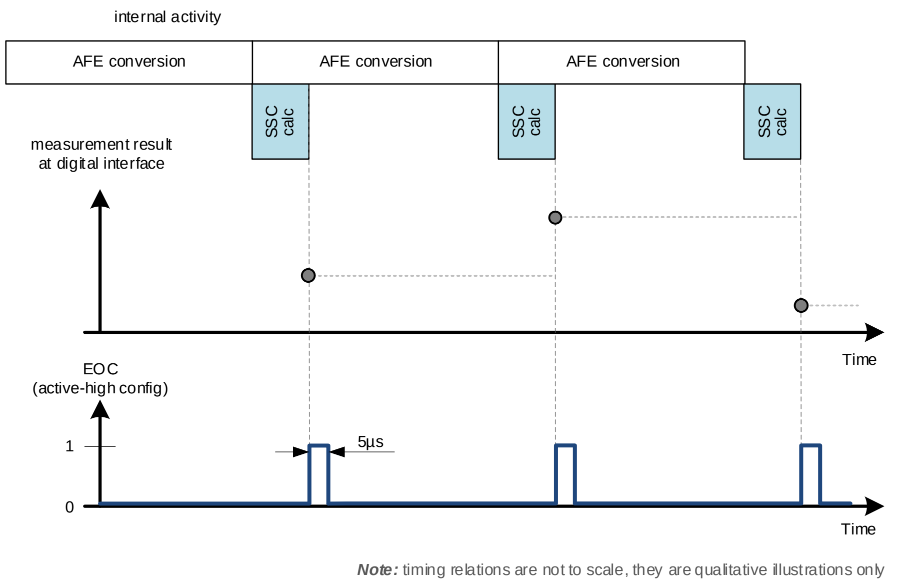


Figure 35: EOC Behavior - Signalization of End-of-Conversion

Important Notes:

- The EOC Output Mode is not available in AFE Dual Speed Mode.
- The EOC Output Mode is not available in PWM/FOUT Mode
- The EOC1 Output Mode is not available if the serial OWI interface is activated

6.5.2. ALARM Function

If the ALARM output mode is active (can be setup via GUI Configure\EOC/ALARM\Selected Mode\Alarm) further configuration options exist:

- Single threshold comparison vs. Window comparison
- Range definition for ALRAM (above/below vs. inside/outside)
- Hysteresis setting
- Persistence setting

Figure 37 shows the ALARM output signalling in the possible four different modes. The doted black lines reflect the behavior for zero hysteresis, while the doted blue lines take a configured threshold hysteresis into account.

The lower charts of Figure 37 feature a special signal transient example. If the measurement result jumps from one sample to another from above the upper to below the lower alarm threshold (or vice versa), the alarm state remains the same since the logic conditions of the Window comparison mode permit this.

The configured hysteresis value (GUI tab Configure\ EOC/ALARM \ Hysteresis) defines the hysteresis half width or “offset”. The total hysteresis width is effectively twice the configured hysteresis value.

The ALARM persistence can be set between 0 and 255. A persistence value >0 requires the signal to remain above or below the threshold for the selected number of consecutive pulses before the ALARM output state is changed. The value of 0 effectively disables the persistence feature and the logic checks for a single occurrence of the threshold condition only.

If AFE1 and AFE2 are running asynchronously, the EOC/ALARM outputs are also evaluated independently after the SSC operation was completed. In case of synchronous setup, the evaluations happen at about the same time but AFE1 is evaluated first.

The alarm thresholds and hysteresis values are stored in the respective CCP registers using the data format as shown in Table 23.

Table 23: Data Format of Alarm Thresholds and Hysteresis

Bit-Number:	23	22	21	20	…	2	1	0
Meaning, Weighting	2^{0}	2^{-1}	2^{-2}	2^{-3}	…	2^{-21}	2^{-22}	2^{-23}

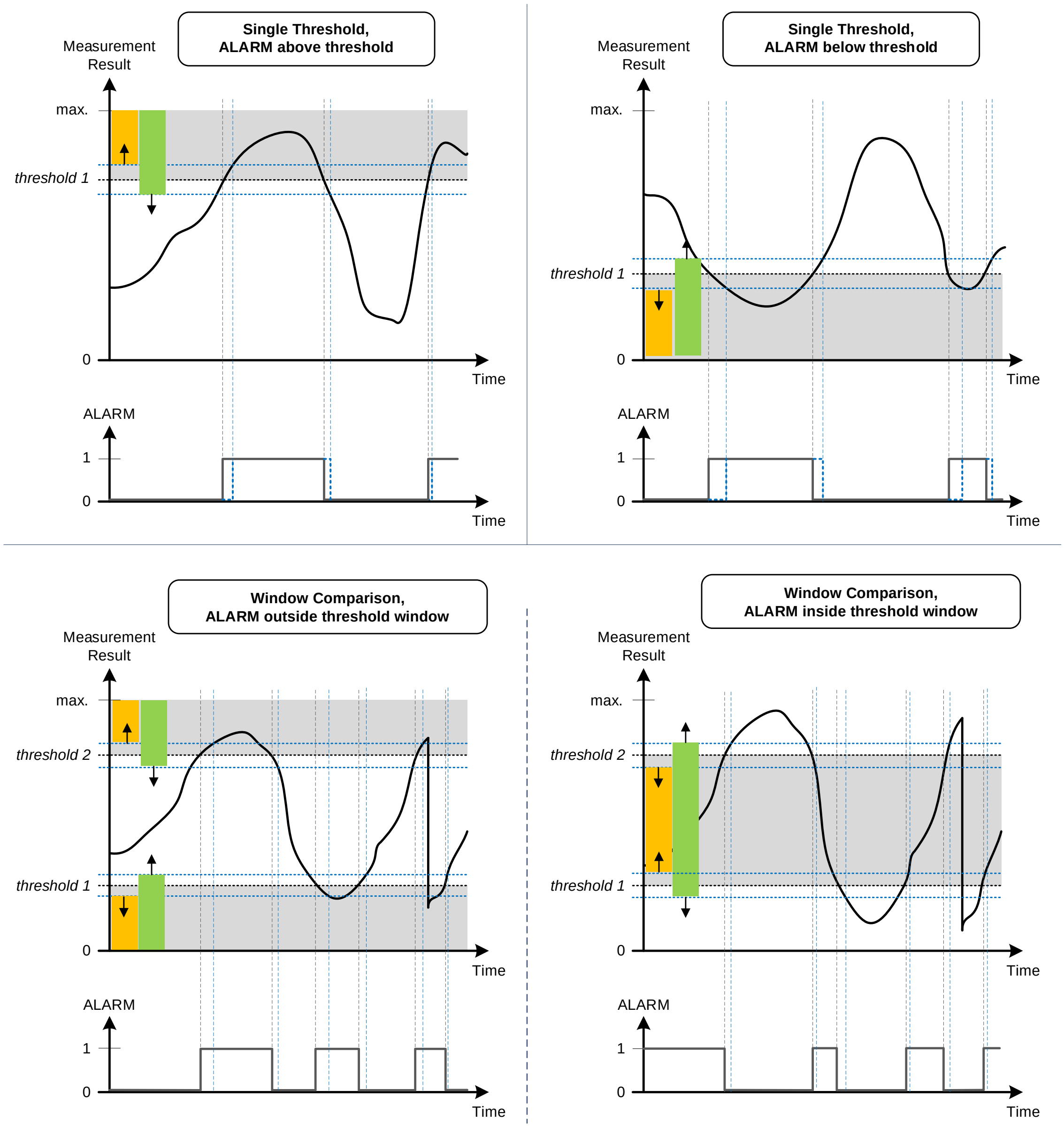


Figure 36: Behaviour of ALARM Feature in Four Different Modes

7. Output Memories

7.1 SSC Process Image

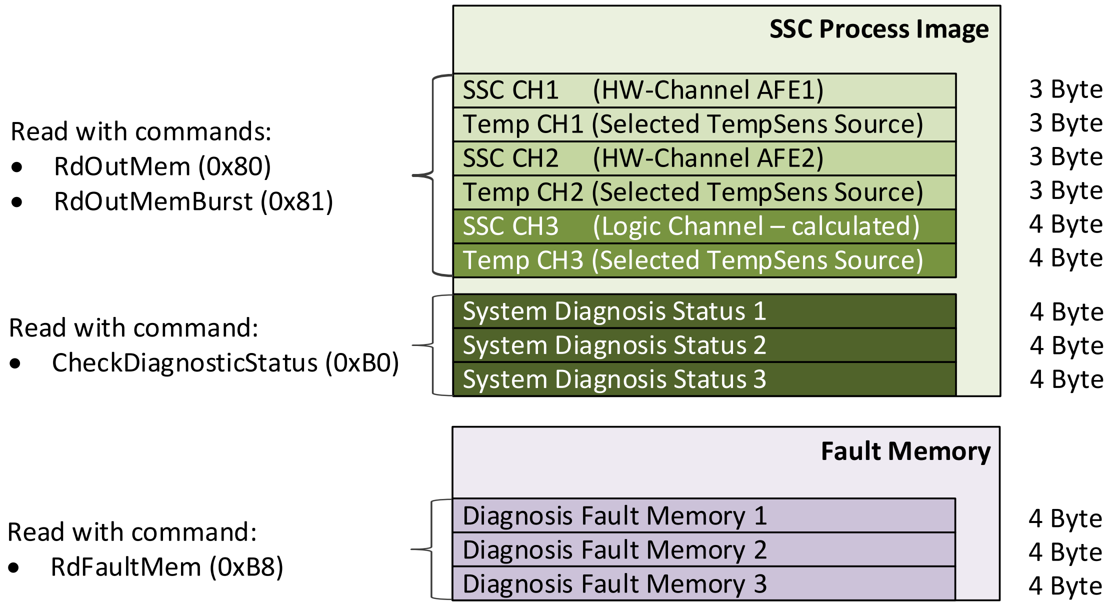


Figure 37: SSC Process Image and Fault Memory Map

ZSSC3281 handles all continuous process data communication with a host system through a memory interface, called SSC Process Image. The data in the Process Image is updated as soon as respective AFE measurements are completed, and the related sensor signal conditioning operations are carried out. It always reflects the most up-to-date known status of the connected sensor system.

The SSC Process Image holds data of the main sensor and temperature signals for all three available channels (AFE1, AFE2, Logic Channel). It contains detailed status information from all activated system diagnosis checks. This detailed status data allows the host system to check for the source of system failure states that were reported in the status byte of a previously received command response. The structure of the system diagnosis status words is shown in Table 26 in section 8.2.

8. Sensor and System Diagnosis

The ZSSC3281 Sensor and System Diagnosis function can detect several false conditions on externally connected sensors and monitor long term gain and offset drifts of the Analog front end. This makes ZSSC3281 well suited for sensing applications that require increased system reliability as well as for predictive maintenance supervision done by the host system.

8.1 Sensor and AFE Diagnostic Features

The supported Sensor and AFE Diagnostic features are summarized in Table 24.

Table 24: Sensor and AFE Diagnosis Functions

Monitored Input or Component	Failure Category	Failure Condition
Main sensor bridge 1	INP or INN open	INP to INN resistance >125kΩ
	INP or INN shorted	INP to INN resistance <170Ω
Main sensor bridge 2	INP or INN open	INP to INN resistance >125kΩ
	INP or INN shorted	INP to INN resistance <170Ω
Temperature sensor T1	Short to Top (TOP)	T1 to TOP resistance <500Ω
	Short to Bottom (BOT)	T1 to BOT resistance <500Ω
	Open	T1 resistance >2MΩ, 500kΩ, 100kΩ
Temperature sensor T2	Short to Top (TOP)	T2 to TOP resistance <500Ω
	Short to Bottom (BOT)	T2 to BOT resistance <500Ω
	Open	T2 resistance >2MΩ, 500kΩ, 100kΩ
Temperature sensor T3	Short to Top (TOP)	T3 to TOP resistance <500Ω
	Short to Bottom (BOT)	T3 to BOT resistance <500Ω
	Open	T3 resistance >2MΩ, 500kΩ, 100kΩ
AFE1	Gain Drift	Gain check deviates by provided percentage from previously stored reference value
	Offset Drift	Offset check deviates by provided permillage from previously stored reference value
AFE1	Gain Drift	Gain check deviates by provided percentage from previously stored reference value
	Offset Drift	Offset check deviates by provided permillage from previously stored reference value

For all active sensor inputs and AFEs, the checks can be enabled selectively on the GUI tab Diagnostic\Sensor AFE.

The AFE gain drift check employs an internally connected resistive DAC to create itself a defined input signal. The internal DAC can generate four different input voltages: 2mV, 20mV, 100mV, 200mV. The GUI proposes the most suitable setting based on other configurations made for the AFE. The selected voltage level is stored in the CCP.

In order to make proper use of the long-term AFE gain and offset drift checks, a device dependent reference value must be acquired and stored during the sensor calibration process. The GUI supports this via the 'Get' button which is located in front of the GainRef and OffsetRef fields.

Command $B4_{HEX}$, allows the test of all enabled sensor checks.

Table 25: Self Diagnostic Measurement Command

Command Code	Return	Description	Sleep Mode	Command Mode	Cyclic Mode

B4HEX followed by 0XYYHEX	2 bytes	**Self-Diagnostic Measure** for AFE1 & AFE2
		• 0XHEX
		  ○ AFE1: 00HEX
		  ○ AFE2: 01HEX
		• YYHEX – see table below
			No	Yes	No

YY	Measurement	Return
05 HEX	External temperature sensor, T1, check short to top	0000_0000_0000_000X BIN
06 HEX	External temperature sensor, T1, check short to bottom	0000_0000_0000_000X BIN
07 HEX	External temperature sensor, T1, check open	0000_0000_0000_000X BIN
0A HEX	External temperature sensor, T2, check short to top	0000_0000_0000_000X BIN
0B HEX	External temperature sensor, T2, check short to bottom	0000_0000_0000_000X BIN
0C HEX	External temperature sensor, T2, check open	0000_0000_0000_000X BIN
0F HEX	External temperature sensor, T3 (pin GUARD), check short to top	0000_0000_0000_000X BIN
10 HEX	External temperature sensor, T3 (pin GUARD), check short to bottom	0000_0000_0000_000X BIN
11 HEX	External temperature sensor, T3 (pin GUARD), check open	0000_0000_0000_000X BIN
1B HEX	Main bridge sensor connection check open	0000_0000_0000_000X BIN
1C HEX	Main bridge sensor connection check short	0000_0000_0000_000X BIN
27HEX	Offset drift (calculated diagnosis result)	0000_0000_0000_000X BIN
28HEX	Gain drift (calculated diagnosis result)	0000_0000_0000_000X BIN

8.2 Sensor and System Diagnosis Status

Table 26: System Diagnosis Status Mapping to Status Byte

	Meaning	Class	Representation in Status Byte of Command Response: bit[1] Sensor Fault	bit[0] Math Saturation	bit[6] Power Supply OK	bit[2] Memory Error	@AFE1	@AFE2	System Diagnosis Status: Word#	Bit#
	reserved									0
bridge sensor connection check	AFE1 sensor broken connection check → INP1 or INN1 open: R > R_{broken}	S	X				x			1
	AFE1 sensor shorted connection check → INP1 - INN1 shorted: R < R_{short}	S	X				x			2
	AFE1 sensor leakage check: INP1 to VSS	S	X				x			3
	AFE1 sensor leakage check: INN1 to VSS	S	X				x			4
	AFE1 sensor signal range check: INP1	S	X				x			5
	AFE1 sensor signal range check: INN1	S	X				x			6
	AFE2 sensor broken connection check → INP2 or INN2 open: R > R_{broken}	S	X					x		7
	AFE2 sensor shorted connection check → INP2 - INN2 shorted: R < R_{short}	S	X					x		8
	AFE2 sensor leakage check: INP2 to VSS	S	X					x		9
	AFE2 sensor leakage check: INN2 to VSS	S	X					x		10
	AFE2 sensor signal range check: INP2	S	X					x		11
	AFE2 sensor signal range check: INN2	S	X					x		12
	Reserved for ZSSC3285 / ZSSC3286									13
	Reserved for ZSSC3285 / ZSSC3286								0	14
	Reserved									15
(external) temperature sensor connection check	AFE1 temperature sensor broken connection check → T1 open: R > RT_OPEN	S	X				x			16
	AFE1 temperature sensor shorted connection check → T1 - TOP shorted: R < RT_SHORT	S	X				x			17
	AFE1 temperature sensor shorted connection check → T1 - BOT shorted: R < RT_SHORT	S	X				x			18
	AFE2 temperature sensor broken connection check → T2 open: R > RT_OPEN	S	X					x		19
	AFE2 temperature sensor shorted connection check → T2 - TOP shorted: R < RT_SHORT	S	X					x		20
	AFE2 temperature sensor shorted connection check → T2 - BOT shorted: R < RT_SHORT	S	X					x		21
	AFE2 temperature sensor broken connection check → T3 open: R > RT_OPEN	S	X					x		22
	AFE2 temperature sensor shorted connection check → T3 - TOP shorted: R < RT_SHORT	S	X					x		23
	AFE2 temperature sensor shorted connection check → T3 - BOT shorted: R < RT_SHORT	S	X					x		24
	Reserved									25…31

			Representation in Status Byte of command response						System Diagnosis Status	
			bit[1]	bit[0]	bit[6]	bit[2]				
	Meaning	Class	Sensor Fault	Math Saturation	Power Supply *OK*	Memory Error	@AFE1	@AFE2	Word#	Bit#
parametric checks in analog sensor path	AFE1 Gain Drift	S	X				x		1	0
	AFE1 Offset Drift	S	X				x			1
	AFE2 Gain Drift	S	X					x		2
	AFE2 Offset Drift	S	X					x		3
	Reserved									4 to 31
parametric checks in digital data path	SSC calculation unit OR raw output data saturation channel 1, bridge sensor data	S		X					2	0
	SSC calculation unit OR raw output data saturation channel 1, temperature sensor data	S		X						1
	SSC calculation unit OR raw output data saturation channel 2, bridge sensor data	S		X						2
	SSC calculation unit OR raw output data saturation channel 2, temperature sensor data	S		X						3
	math saturation: channel 3, bridge sensor data	S		X						4
	math saturation OR raw output data saturation channel 3, temperature sensor data	S		X						5
	Reserved									6 to 31

Failure classification:

S	Safe Failure, system response via digital interfaces still reliable
D	Dangerous Failure, system response via digital interfaces unreliable

Since the SSC Process Image data is continuously updated as soon as new measurement data becomes available, it may happen that Diagnosis Faults disappear before the host has read them via the CheckDiagnosticStatus command 0xB0.

To allow system failure detection at a later point in time, ZSC3281 additionally stores all appeared system diagnosis failures in a separate volatile fault memory. The fault memory has the same organization as the system diagnosis status memory and becomes cleared only via ClearFaultMem (0xB9) command or a system reset. The fault memory can be read via RdFaultMem (0xB8) command.

8.3 Output Data Clipping

The signaling of a diagnosis failure state can also be activated on the analog output AOUT or the digital outputs PWM/FOUT via GUI tab Diagnostic\General. If the signalization of Diagnostic state at AOUT and PWM/FOUT is enabled, discovered diagnostic failure states can be either mapped to the Upper or the Lower Diagnostic Range (UDR and LDR) of the output span (GUI tab Diagnostic \ Sensor/AFE).

The boundaries of the upper and lower diagnostic ranges are configurable via the GUI tab Configure\Output Preprocess. They are typically set to 95% and 5% of the full-scale output level but can be modified to the application needs.

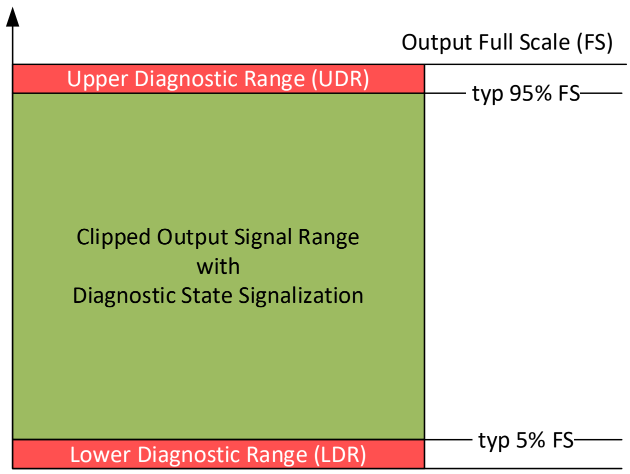


Figure 38: AOUT and PWM/FOUT Output Ranges with Active Diagnostic State Signalization

To prevent false interpretation of very large or very low output signals (UDR and LDR ranges), the conditioned data is clipped to fit into the remaining output range between UDR and LDR, before it is forwarded to the AOUT and PWM/FOUT outputs.

Important Notes:

- There is no rescaling of the conditioned data performed at this stage.
  If rescaling of the conditioned data to the clipped output signal range is required, use the Bridge Output Scaling feature (see section 6.2.) or use different target values during the SSC calibration process.
- The digital output data which is accessible on the serial interfaces (read from the process image) is not clipped since a diagnosis failure condition is signaled there within the status byte.

9. Analog Output

The conditioned and post processed output data of one of following channels can be made available as analog output signal at the Analog Output AOUT

- Bridge Sensor Channel 1
- Bridge Sensor Channel 2
- Third Logic Channel
- Temperature Channel 1
- Temperature Channel 2
- Temperature Channel 3

Depending on the configuration of the Analog Output Driver, different output modes, like ratiometric voltage output, absolute voltage output and current mode output are supported.

9.1 Analog Output Driver Modes

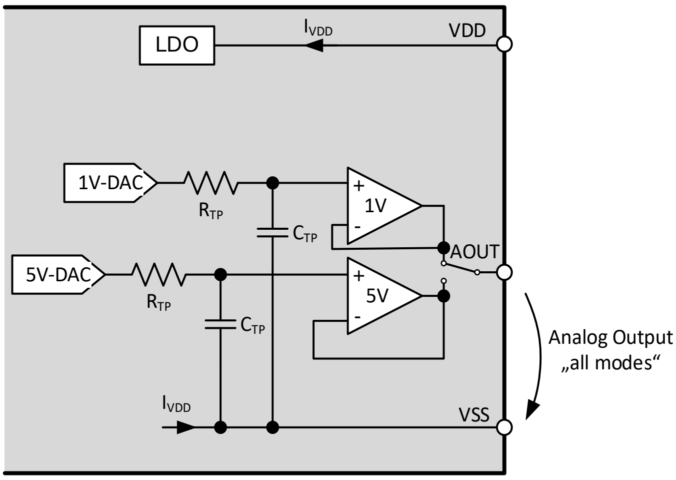


Figure 39: Block Schematic AOUT Driver

The Analog Output Driver contains two separate output buffers, one for a full-scale voltage of 1V and another one for full scale voltages ranging up to VDD. The following functional assignments apply:

- 1V buffer: 1V absolute Voltage Mode
  2-wire current loop mode
  3-wire current loop mode
- 5V buffer: Ratiometric Voltage Mode
  5V absolute Voltage Mode
  10V absolute Voltage Mode

The 5V buffer offers a programmable output current limiting function which is not available for the 1V buffer. The 5V buffer requires the VDD to be in the range between 2.7V and 5.5V for proper operation.

Table 27: AOUT Parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	VDD operating range	AOUT modes using 1V buffer AOUT modes using 5V buffer	1.7 2.7		5.5 5.5	V V
t_{settle}	Time from digital value applied at DAC and voltage at VOUT	10% to 90% input step: V_{AOUT} at 90% of final value			100	µs
V_{OUT_START}	Voltage at AOUT during startup			0		V
V_{AOUT}	Output voltage at pin AOUT	Ratiometric Voltage Mode	0		VDD	V
		1V Absolute Voltage Mode			1	
		5V Absolute Voltage Mode	0		5[2]	V
		10V Absolute Voltage Mode			5[3]	
I_{OUTMAX}	Short current limit at pin AOUT	AOUT modes using 5V Buffer • short to VDD or VSS • programmable in 4 steps	3 8 15 20	5 12 19 25	9 20 23 30	mA mA mA mA
C_{load}	Load capacitance at AOUT	• 2-wire current loop mode			2	nF nF

2 VDD must be ≥ 5.25V
3 VDD must be ≥ 5.25V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		• all other modes (for example, cap for EMC: 33nF, ECU load: 10nF)			50	
RES_{DAC}	DAC resolution			16		bit

9.2 Analog Output Configuration

9.2.1. Negative Voltage Generation for AOUT

As described in section 3.2.4, an internal charge pump can be activated to support True-0V signals in all voltage output modes of the Analog Output (AOUT).

The activation of the internal charge pump at VDDN considerably increases the power consumption of ZSSC3281 and needs to be carefully considered in applications where current consumption of the sensor device (sensor + ZSSC3281) is a critical parameter. The VDDN charge pump can only be used for VDD ≥ 2.7V.

ZSSC3281 supports to keep the internal charge pump disabled but to provide a negative VDDN voltage through an external circuity. The external circuity must ensure to not generate a VDDN voltage of less than -0.5V to prevent latchup conditions for the internal circuity.

If no True-0V signals are required at AOUT, the user must disable the VDDN charge pump in the GUI and directly connect VDDN with VSS on PCB level.

The internal charge pump can be activated or deactivated through the GUI field Configure\AOUT\VDDN Charge Pump. The field Configure\AOUT\VDDN Load allows to set a maximum current that the internal charge pump can supply. Lower values lead to less power consumption of the charge pump than high values.

Table 28: Parameter Negative Voltage for AOUT

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDD_{CP}	VDD operating range of internal charge pump		2.7		5.5	V
I_{VDDN}	Available charge pump load current	Programmable in 4 steps.			0.5 1 3 5	mA
I_{VDD}	Charge pump current consumption at VDD	Load current:	0.5	4.5	5	mA
			1	9	10	
			3	15.5	17	
			5	25	30	
C_{VDDN}	Buffer capacitance at pin VDDN			1		µF
$V_{FW\text{-}Schottky}$	Forward voltage of external Shottky diode			0.3		V
$V_{VDDN\text{-}ext}$	Voltage range for externally supplied VDDN		-0.5V		0.05	V

9.2.2. Ratiometric Voltage Mode

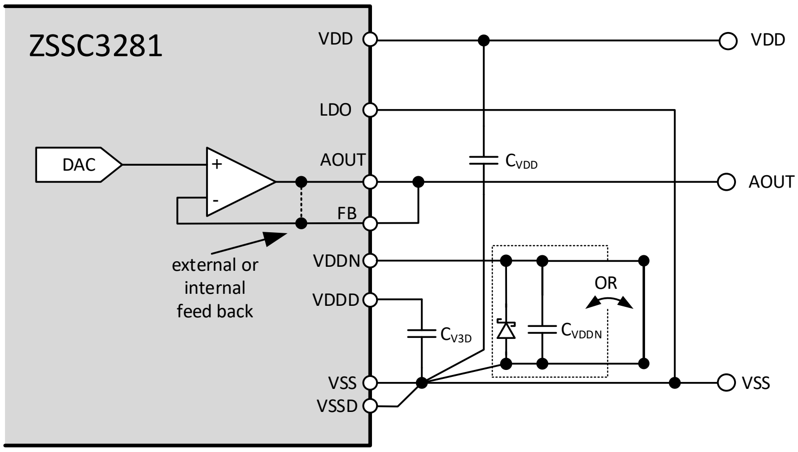


Figure 40: Ratiometric Output Mode Configuration at AOUT

The SSC output can be ratiometric mapped to 0 to VDD range with the application circuit shown in Figure 40 and activation of the Ratiometric Voltage Mode in the GUI via Configure\AOUT\Operation Mode\Ratiometric Voltage.

In Ratiometric Output Mode the reference voltage for the AOUT DAC is identical to the VDD level.

9.2.3. 5V Absolute Voltage Mode

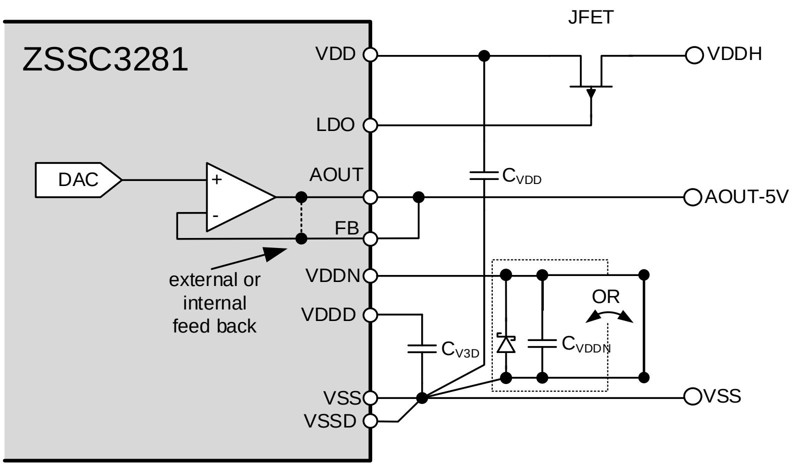


Figure 41: 5V Absolute Output Voltage Configuration at AOUT

The SSC output can be mapped to 0 to 5V voltage range with the application circuit shown in Figure 41 and activation of the 5V Absolute Voltage Mode in the GUI via Configure\AOUT\Operation Mode\Absolute Voltage 0V – 5V. This AOUT mode requires the external regulator supply configuration to be active in the GUI with the regulated VDD set to 5.25V. The GUI cross-checks for this requirement.

The applied reference voltage for the AOUT DAC is directly derived from VDD through a digital factory calibration coefficient.

9.2.4. 10V Absolute Voltage Mode

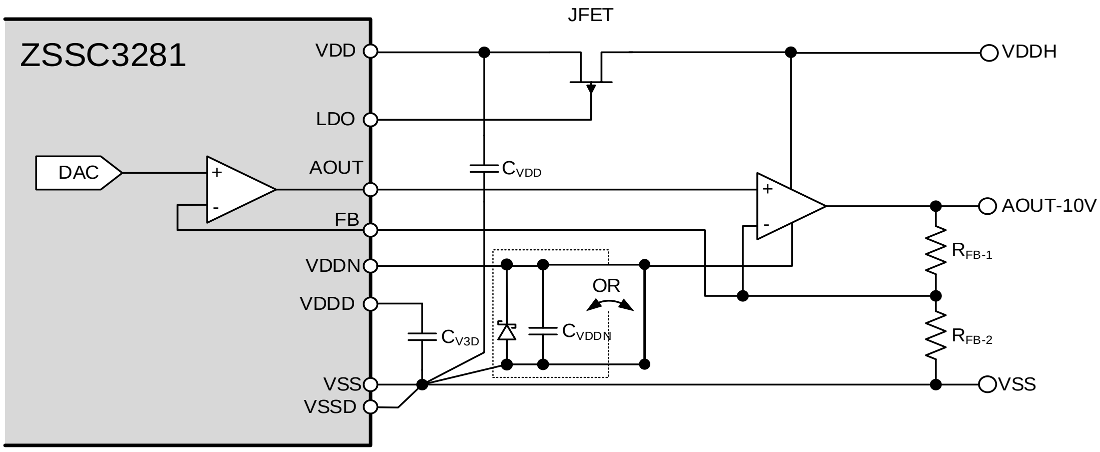


Figure 42: 10V Absolute Output Voltage Configuration at AOUT

The SSC output can be mapped to 0 to 10V voltage range with the application circuit shown in Figure 42 and activation of the 10V Absolute Voltage Mode in the GUI via Configure\AOUT\Operation Mode\Absolute Voltage 0V – 10V. This AOUT mode requires the external regulator supply configuration to be active in the GUI with the regulated VDD set to 5.25V. The GUI cross-checks for this requirement.

The applied reference voltage for the AOUT DAC is similar to the 5V Absolute Voltage Mode directly derived from VDD through a digital factory calibration coefficient. In order to obtain a 0 to 10V output signal at AOUT-10V the following condition must be met: $R_{FB-1} = R_{FB-2}$. The external Operational Amplifier should be offset compensated.

9.2.5. 1V Absolute Output Voltage Mode

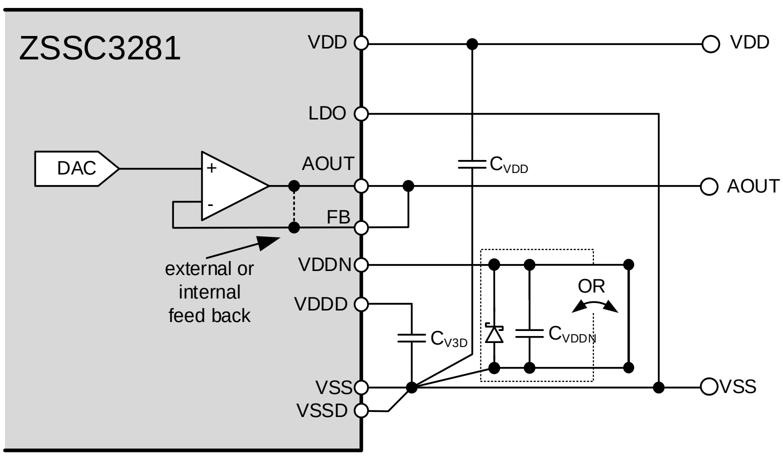


Figure 43: 1V Absolute Output Voltage Configuration at AOUT

The SSC output can be mapped to 0 to 1V voltage range with the application circuit shown in Figure 43 and activation of the 1V Absolute Voltage Mode in the GUI via Configure\AOUT\Operation Mode\Absolute Voltage 0V – 1V.

The applied reference voltage for the AOUT DAC is generated from an internal factory calibrated bandgap source.

9.2.6. 2-Wire Current Loop Mode

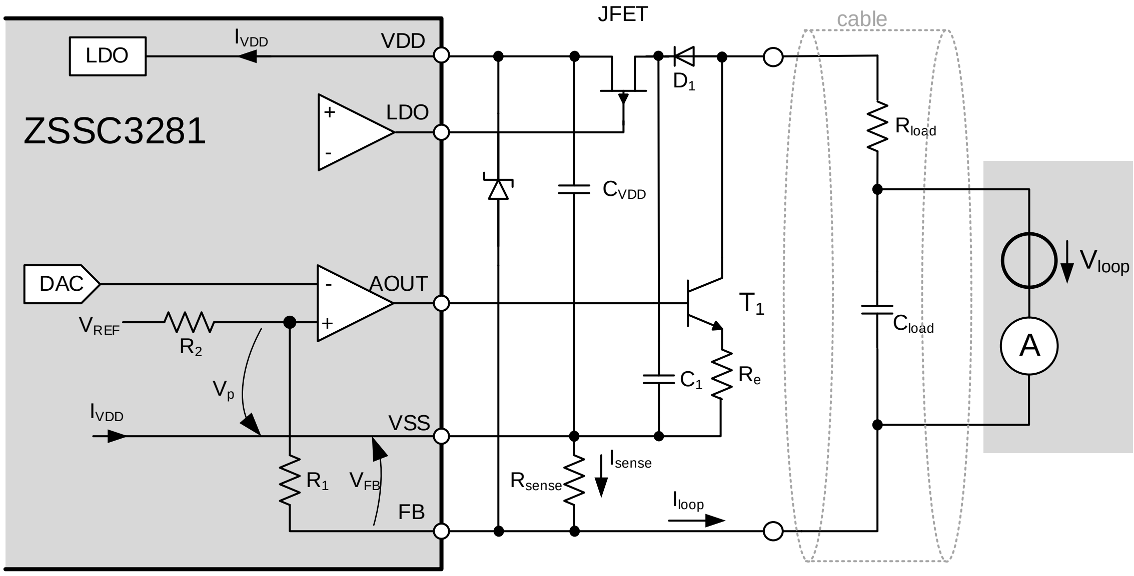


Figure 44: 2-Wire Current Loop Configuration at AOUT

Table 29: External Components in 2-Wire Current Loop Mode

Symbol	Parameter	Min	Typ	Max	Unit
R_{sense}	Feedback resistor		42		Ω
R_e	Emitter resistor		150		Ω
T_1	Bipolar Transistor	For example, BCX56-16			

The ZSSC3281 can be operated in two wire current loop configuration as shown in Figure 44. It requires the activation of 2-Wire Current Loop Mode in the GUI via Configure\AOUT\Operation Mode\2-Wire Current Loop. Because the signal current is typically expected to range from 4 to 20mA on the 2-wire cable, the total operating current of the ZSSC3281 IC and the connected resistive bridges must stay below 4.0mA. To achieve this, the clock frequency of ZSCC3281 needs to be reduced to 1MHz, which impacts input to output signal latency and selectable AFE resolutions. 2-Wire Current Loop Mode also requires the activation of the external JFET pre-regulator. This, as well as the system clock frequency reduction are ensured by the GUI when 2-Wire Current Loop is selected at AOUT tab.

Besides production calibrated parameters of ZSSC3281, the value of the external resistor R_{sense} also determines the available min/max signal current range on the cable. To compensate for tolerances of R_{sense}, the GUI offers a post calibration option to calibrate the current loop current to the required absolute accuracy. The function recalculates the default CCP parameters 'CL2_Offset' and 'CL2_Delta' based on the entered R_{sense} (typical value), required and measured I_{min} and I_{max} values. To activate the optimized values, a Write Memory operation needs to be triggered by the user. 'CL2_Offset' and 'CL2_Delta' determine the swing of the AOUT voltage to cover the 4mA to 20mA current output signal.

The user can select the signal which shall be mapped to the 2-Wire Current Loop output via the drop-down menu Configure\AOUT\AOUT Pin Mapping.

9.2.7. 3- Wire Current Loop Mode

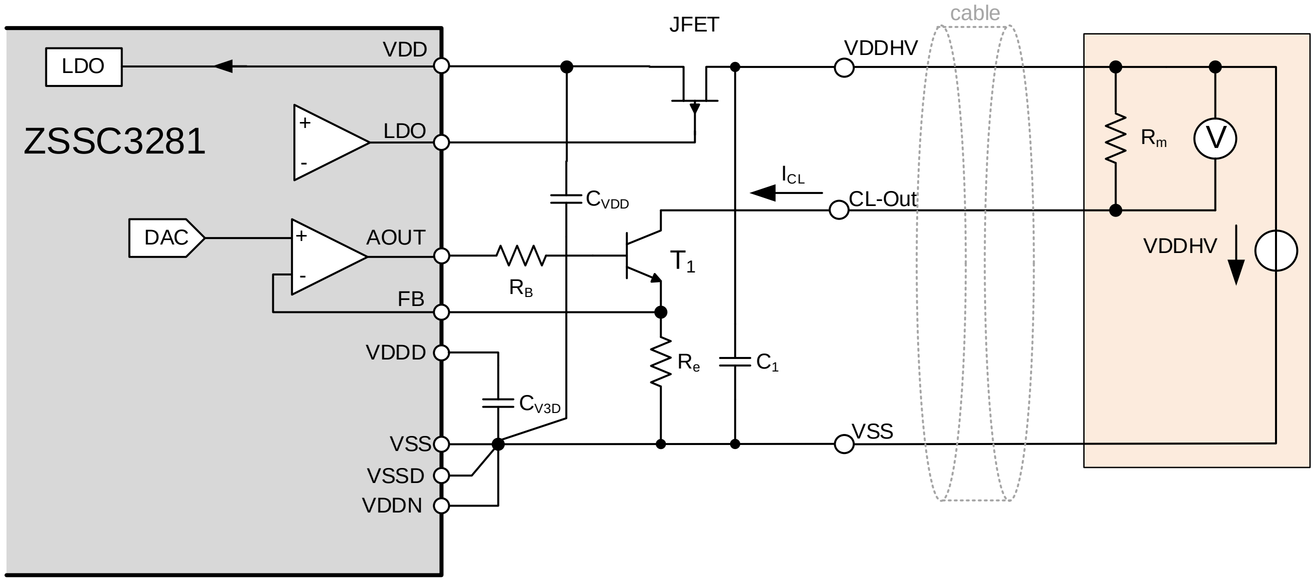


Figure 45: 3-wire NPN Current Loop Configuration at AOUT

Table 30: External Components in 3-Wire Current Loop Mode

Symbol	Parameter	Min	Typ	Max	Unit
R_e	Emitter resistor		43		Ω
R_b	Base resistor		5000		Ω
T_1	Bipolar Transistor	For example, BCX56-16			

The SSC output can be mapped to an input current at CL-Out in the application circuit shown in Figure 45 and by activation of the 3-Wire Current Loop Mode in the GUI via Configure\AOUT\Operation Mode\3-Wire Current Loop.

The signal current at CL-Out is typically required to range from 4 to 20mA. The available min/max signal current range at CL-Out depends on the actual value of the external emitter resistor R_e.

To compensate for tolerances of R_e, the GUI offers a post calibration option to calibrate the current loop current to the required absolute accuracy. The function recalculates the default CCP parameters 'CL3_Offset' and 'CL3_Delta' based on the entered R_e (typical value), required and measured I_{min} and I_{max} values. To activate the optimized values, a Write Memory operation needs to be triggered by the user. 'CL3_Offset' and 'CL3_Delta' determine the swing of the AOUT voltage to cover the 4mA to 20mA current output signal.

The user can select the signal to map to the 3-Wire Current Loop output via the drop-down menu Configure\AOUT\AOUT Pin Mapping.

10. Digital Outputs

The conditioned and post processed output data of two of the following channels can be made available as modulated digital output signal at the pins FOUT/PWM_1 (GPIO1) and FOUT/PWM_2 (GPIO7)

- Bridge Sensor Channel 1
- Bridge Sensor Channel 2
- Third Logic Channel
- Temperature Channel 1
- Temperature Channel 2
- Temperature Channel 3

The channel assignment to the output pins and the type of output modulation can be selected in the GUI via Configure\DOUT tab. There will be two types of output modulation supported:

- Frequency Modulation – available in FW rev 1.0.0
- Pulse Width Modulation – reserved for a future release of the ZSSC3281 firmware

10.1 Frequency Modulation

The minimum and maximum frequencies of the frequency modulation output can be configured via GUI on the Configure\DOUT tab.

The frequency accuracy of the Frequency Modulation Output is determined by the frequency accuracy of the internal oscillator. An option to switch to an external clock or crystal oscillator will be provided in a future release of ZSSC3281 firmware.

Table 31: FOUT Parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$FOUT_{MIN}$	Minimum output frequency		100		255	Hz
$FOUT_{MAX}$	Maximum output frequency		1,000		10,000	Hz
$FOUT_{ERR}$	Frequency error	FOUT feature operated with internal oscillator clock	-5%		5%	

11. Digital Interfaces

11.1 Serial Interfaces

For sensor data read out, ZSSC3281 supports three digital interface protocols in slave mode operation:

- I2C/I3C
- SPI
- OWI (One-Wire-Interface)

Digital slave interfaces do not initiate data communication with the host system themselves but have to quickly react on arbitrary received read/write requests from the host.

To maintain short response times in continuous Cyclic Mode operation, ZSSC3281 is equipped with a dedicated DMA controller, which can read the content of the Process Image (see section 7.1) without interaction of the ARM MCU. The DMA controller is alternatively called Interface Bridge (IFB).

The Interface Bridge supports one active digital interface at the time. After reset, the IFB activates and locks the serial interface for further communication that first received a valid telegram. A telegram is valid if:

- the address match was pass for I2C/I3C or OWI and the first 8 bit of telegram data were received
- the Slave Select (SS) was activated for SPI and first 8 bit of telegram data were received on MOSI

As soon as one of the three interfaces was locked by IFB, potential data streams from the other interfaces are blocked. A different interface can only be selected after reset of ZSSC3281.

11.1.1. Command/Response Format

All three interfaces operate on the same command request and response format. The number of Data Bytes which need to follow the command byte in the command request or are returned after the status byte in command response, assuming the command execution was completed, is specific to the command code.

Table 32: Command Request Format

<table>
<tr><th rowspan="2">Command</th><th colspan="8">Command Byte</th><th>Data Bytes</th></tr>
<tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th><th></th></tr>
<tr><td>Valid Command</td><td colspan="8">8-bit command</td><td>[Data Bytes]</td></tr>
</table>

Table 33: Command Response Format

<table>
<tr><th rowspan="2">Command Response</th><th colspan="10">Status Byte</th><th>Data Bytes</th></tr>
<tr><th colspan="2">7</th><th>6</th><th colspan="2">5</th><th colspan="2">4</th><th>3</th><th>2</th><th>1</th><th>0</th><th></th></tr>
<tr><td>Previously received command in execution, response pending,
New command not accepted, retry later</td><td rowspan="2">Telegram Error Flag</td><td>0</td><td rowspan="2">Power Supply OK</td><td rowspan="2">Busy Flag</td><td>1</td><td rowspan="2" colspan="2">SSC Mode
00: Command Mode
01: Cyclic Mode
10: Sleep Mode
11: Boot/Diagnosis Mode</td><td rowspan="2">Memory Error</td><td rowspan="2">Sensor Connection Fault</td><td rowspan="2">Math Saturation</td><td>NONE</td></tr>
<tr><td>Command successfully processed</td><td>0</td><td>0</td><td>[Data Bytes]</td></tr>
</table>

A list of supported command codes, the number of command and response Data Bytes and the command function description can be found in section 11.2.1.

If a command is still processed by the ZSSC3281 when the response read starts, the BusyFlag of the status byte is set and no response data is returned. The response data stream only contains a repeated StatusByte until the transaction is ended. The BusyFlag within the StatusByte changes as soon as the command execution is completed.

11.1.2. I2C/I3C

ZSSC3281 supports I2C communication in StandardMode, FastMode, FastMode+, and it supports high speed communication in I3C Single Data Rate (SDR) Mode on I2C SCL and I2C SDA pins. The I2C/I3C interface is listening to receive a telegram after system startup or system reset as long as the SPI Slave Select (pin SPI SS) signal is not active.

I2C/I3C communication mode is selected and locked after I2C/I3C address match was pass and the first 8 bit of telegram data were received.

The interface settings, and a selection whether to use the traditional I2C or the advanced I3C communication mode, can be made in the GUI at the tab Configure\Serial Interfaces in section I2C/I3C.

I3C is an MIPI standard (https://www.mipi.org/specifications/i3c-sensor-specification) which is based on the traditional I2C protocol but extends the physical layer and the protocol layer towards higher communication speeds and improved management of the slave communication parameters by the I3C master. It allows In-Band Interrupts through which an I3C slave can signal an interrupt request to the I3C master via the SCL/SDA lines. Inband Interrupts will be supported in a future release of the ZSSC3281 firmware.

Table 34: I2C/I3C Interface Parameter

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SlvAddr	I"C slave address Static I3C address	ZSSC3281 delivery default		0x3C		
f_{SCL}	Interface clock	I2C Mode	0.1		1.0	MHz
		I3C Mode	0.1		12.5	MHz
D_{I2C}	Duty cycle		33	–	50	%

Timing and protocol details of the I2C communication in Standard Mode, Fast Mode, and Fast Mode+ are given in I2C-Bus Specification, Rev.6, UM10204. SCL Clock Stretching is not supported by ZSSC3281.

In I2C/I3C Mode, each Command Request follows the structure shown in Figure 46. Only the number of Data Bytes needed by the command must be sent.

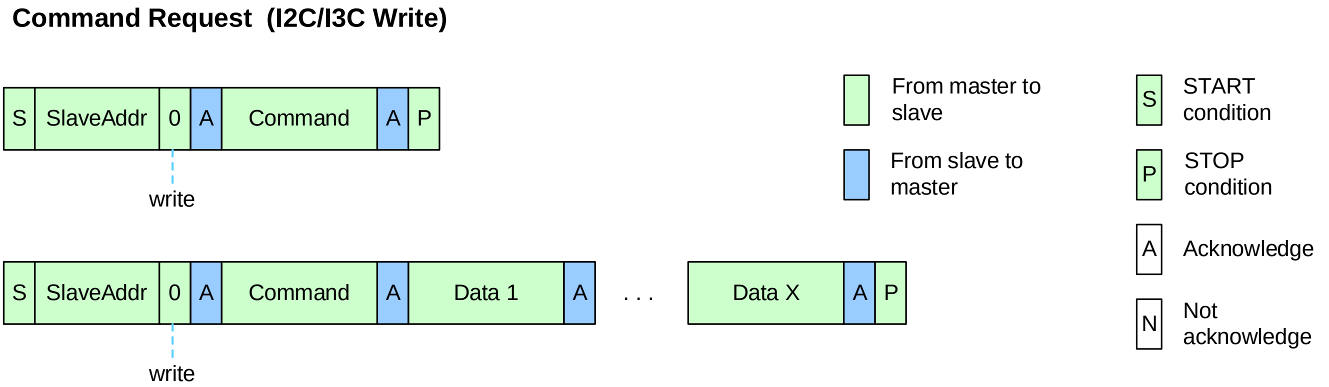


Figure 46: I2C/I3C Command Request

The different options for a response request are shown in Figure 47.

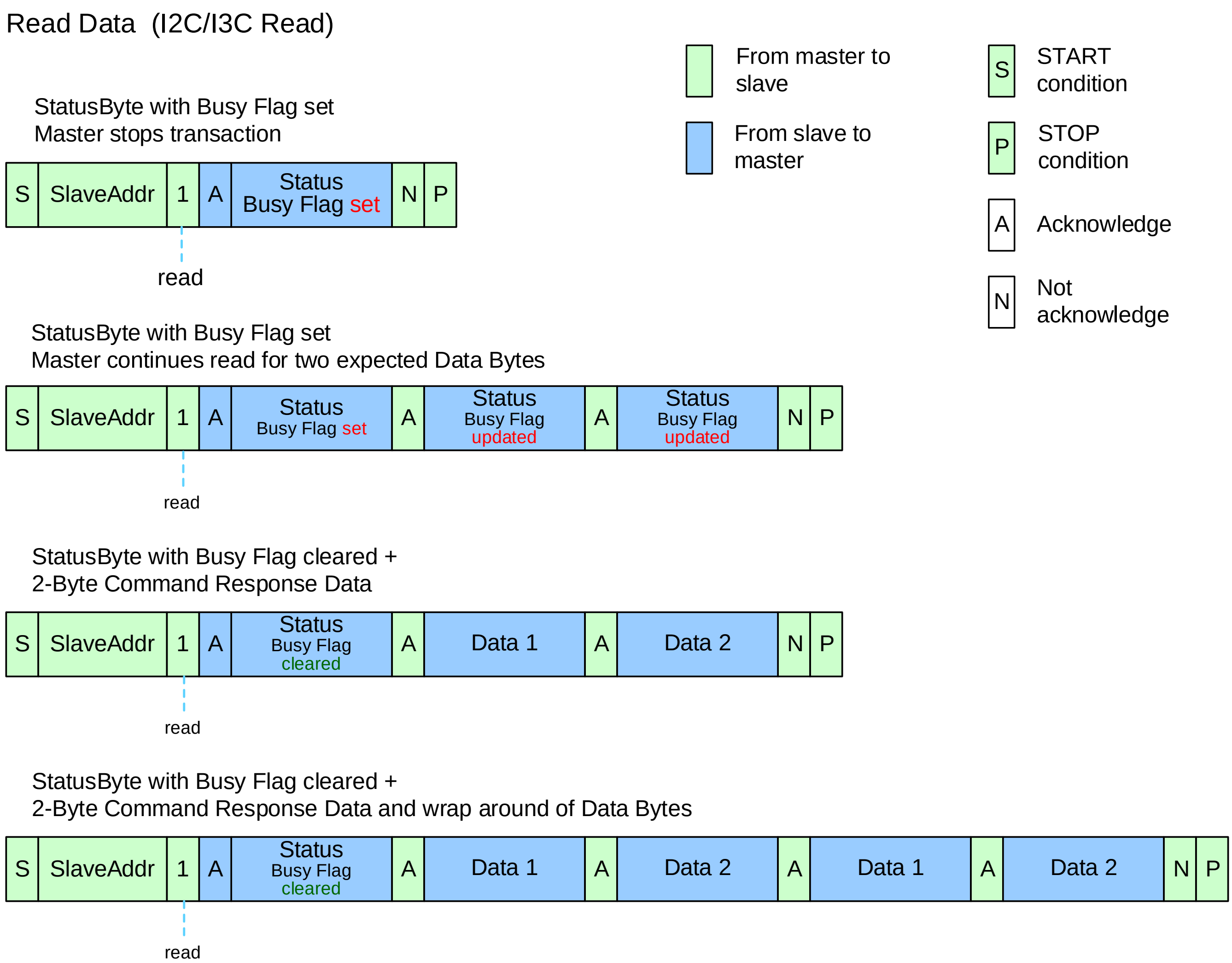


Figure 47: I2C/I3C Response Request

11.1.3. SPI

ZSSC3281 supports SPI communication on the SPI SCLK, SPI MOSI, and SPI MISO pins if the SPI slave select signal is active at the SPI SS pin and no other serial interface was locked yet after reset or power-on.

An active SPI SS signal connects the SPI SCLK and SPI MOSI pins to the SPI slave interface at the Interface Bridge (IFB) and disconnects the I2C/I3C slave. As soon as the first 8 bit of data received on MOSI line, the SPI interface is locked as communication interface until the next reset or power-on of the ZSSC3281.

The polarity of the SPI slave select signal is active low by delivery default. It can be changed to active high at the Serial Interfaces tab of the GUI Configure\Serial Interfaces\SPI Slave Select Polarity. The polarity and the phase of the SPI clock can be changed via ‘CPHA’ and ‘CPOL’ selection fields at the same GUI tab.

The different combinations of polarity and phase are illustrated in Figure 48 and Figure 49. See Table 35 for the timing parameters.

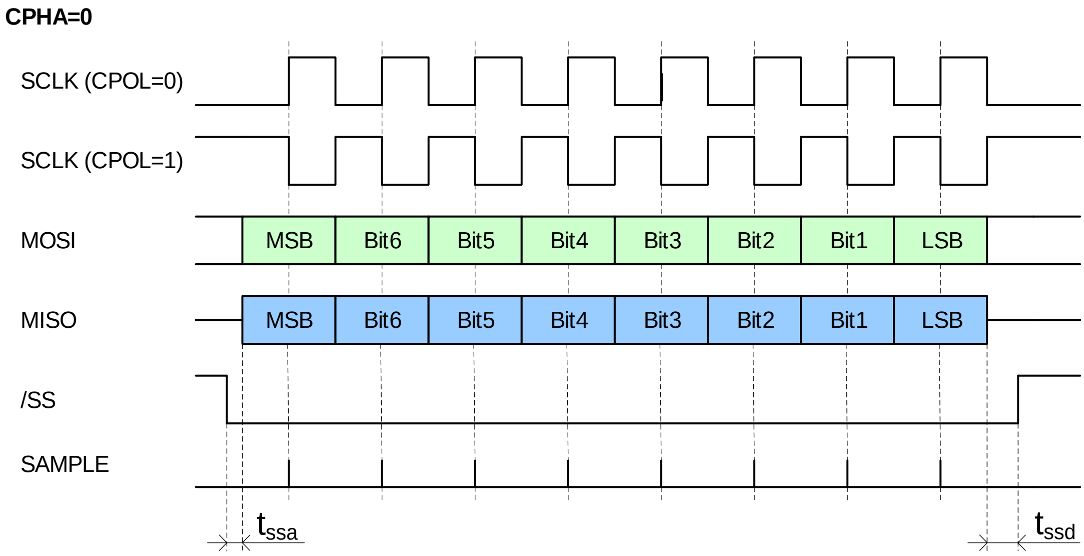


Figure 48: SPI Configuration CPHA=0

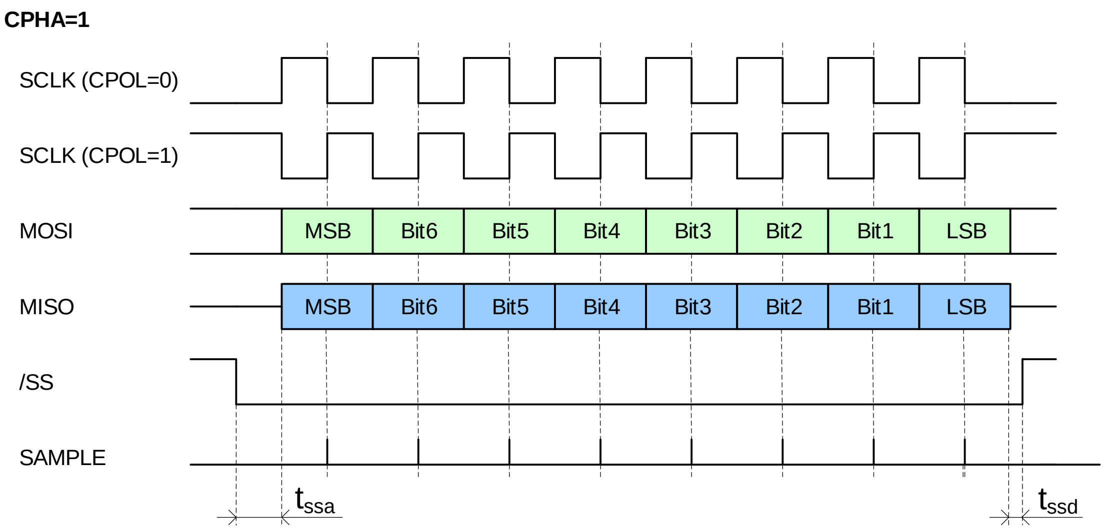


Figure 49: SPI Configuration CPHA=1

Table 35: SPI Interface Parameter

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCLK}	Interface clock		0.05	1	12	MHz
D_{SPI}	Duty cycle		40	50	60	%
SR_{SPI}	Input rising and falling edge slew rate		0.26	–	1	V/ns
t_{ssa}	Delay time between SS-activation edge and first edge of SLCK, MOSI or MISO	"Typical" is for $f_{SCLK} \leq$ 3MHz operation	62.5	–	–	ns
t_{ssd}	Delay time between SS-deactivation edge and last edge of SLCK, MOSI or MISO			50(tbd)	–	ns
t_{ss}	Delay between SS-deactivation edge of last command and of SS-activation edge for next command		10	–	–	µs

In SPI Mode, each command request follows the structure shown in Figure 50. Only the number of data bytes needed by the command must be sent.

A SPI transaction is started with activation of SPI SS and it is ended with deactivation of SPI SS. A new command request can only be sent at the start of a new transaction, which begins after SPI SS changed from inactive to active state.

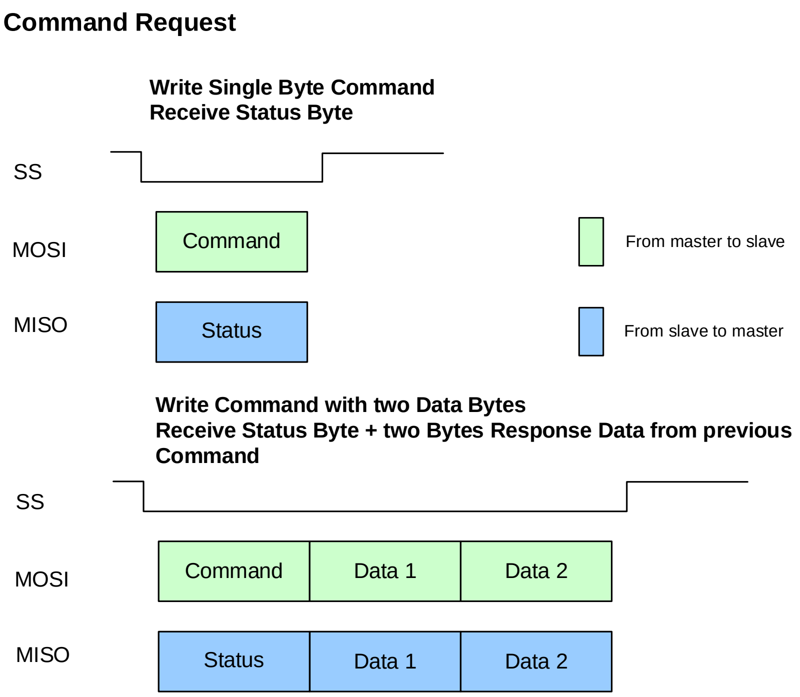


Figure 50: SPI Command Request

In contrast to the I2C/I3C interface the SPI interface supports full duplex communication. Hence, a new command request can already be sent on the MOSI line while response data from the previous command request is returned on the MISO line.

If the response data from the previous call is read without triggering a new command request in parallel, the NOP command must be sent on the MOSI line in the first telegram byte of the transaction as shown in Figure 51.

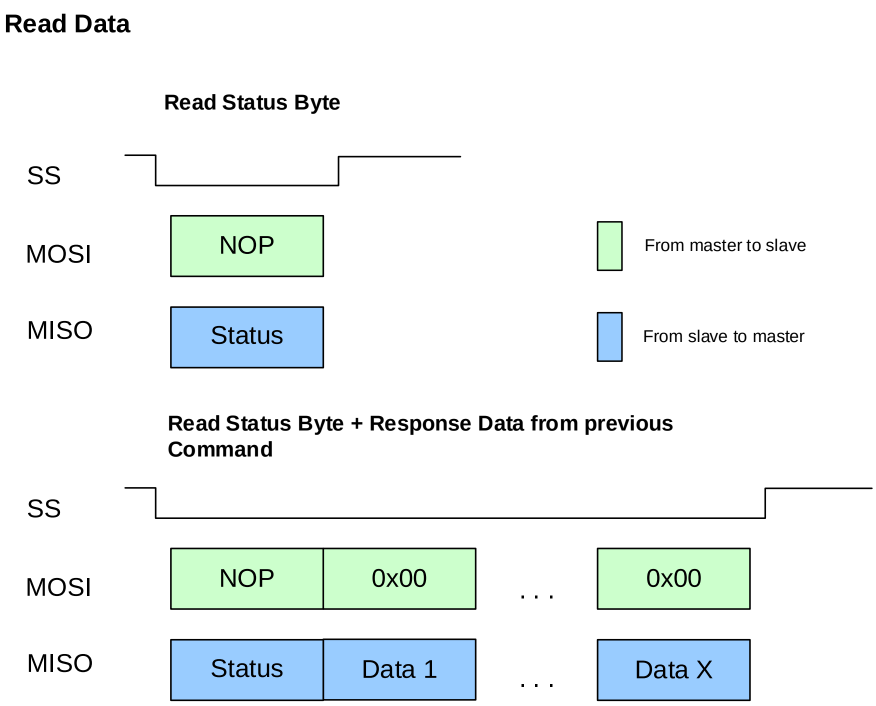


Figure 51: SPI Read Data

11.1.4. One-Wire-Interface

ZSSC3281 employs a one-wire digital interface concept (OWI). The communication principle of the OWI interface is derived from the I2C protocol.

An advantage of the OWI is that it enables “end of line” calibration, no additional pins are required to digitally calibrate a finished assembly. Although the OWI is integrated mainly for calibration, it can also be used to read out the calibrated sensor signal continuously or retrieve diagnostic detail information.

The OWI Driver and the OWI receiver are usually connected both to the analog output signal pin AOUT. The mode switching at AOUT between Analog Output Mode and OWI Communication Mode is controlled via different selectable OWI operation modes that are described in section 11.1.4.1.

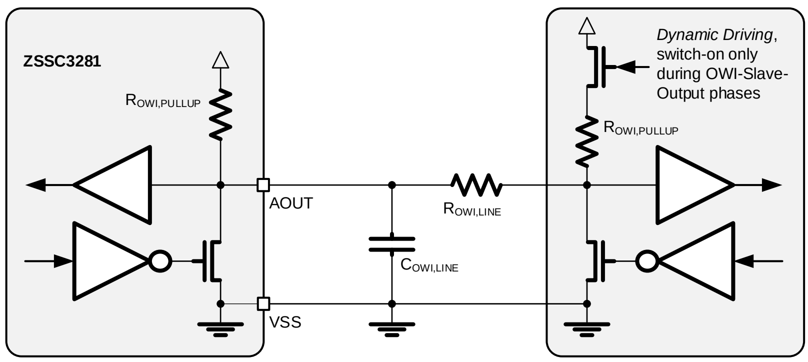


Figure 52: General Block Schematic of the OWI Interface

Some Analog Output configurations, like 2-Wire and 3-Wire Current Loop Mode and the 10V Absolute Voltage Mode require a second OWI input pin (OWI-IN2) because the external AOUT circuitry does not allow to drive a digital signal from an external OWI master into the AOUT pin. A respective application schematic is provided in section 14.3.

The OWI protocol is defined as follows:

- Idle state

  During inactivity of the bus, the OWI line is pulled up to the supply voltage V_{DD} by an external resistor.

- Start condition

  When the OWI line is in idle mode, a low pulse with a minimum width of $t_{OWI,START} \geq 10\mu s$ and then a return to high indicates a start condition. Every request must be initiated by a start condition sent by a master. A master can generate a start condition only when the OWI line is in idle mode.

- Stop condition

  A constant level at the OWI line (no transition from low to high or from high to low) for at least twice the period of the last transmitted valid bit indicates a stop condition. Without considering the last bit-time (secure stop condition), a stop condition is generated with a constant level at the OWI line for at least 20ms.

  The master finishes a transmission by changing back to the high level (idle mode). Every command must be closed by a stop condition to start the processing of the command. The master must interrupt a sending slave after it has completed a data request by clamping the OWI line to the low level for generating a stop condition.

- Valid data

  Data is transmitted in bytes (8 bits) starting with the most significant bit (MSB). Transmitted bits are recognized after a start condition at every transition from low to high at the OWI line. The value of the transmitted bit depends on the duty ratio between the high phase and high/low period (bit period, $t_{OWI,BIT}$ in Table 37). A duty ratio greater than 1/8 and less than 3/8 is detected as 0; a duty ratio greater than 5/8 and less than 7/8 is detected as 1. The bit period of consecutive bits must not increase to more than 1.5 times the previous bit period or decrease to less than half of the previous bit period because a stop condition is detected in this case.

- Write operation

  During transmission from master to slave (WRITE), the address byte including a set data direction bit (0 for WRITE) is followed by a command byte and, depending on the transmitted command, by an optional number of data bytes. The internal microcontroller evaluates the received command and processes the requested routine. Figure 53 illustrates the writing of a command with two data bytes and a command without data bytes.

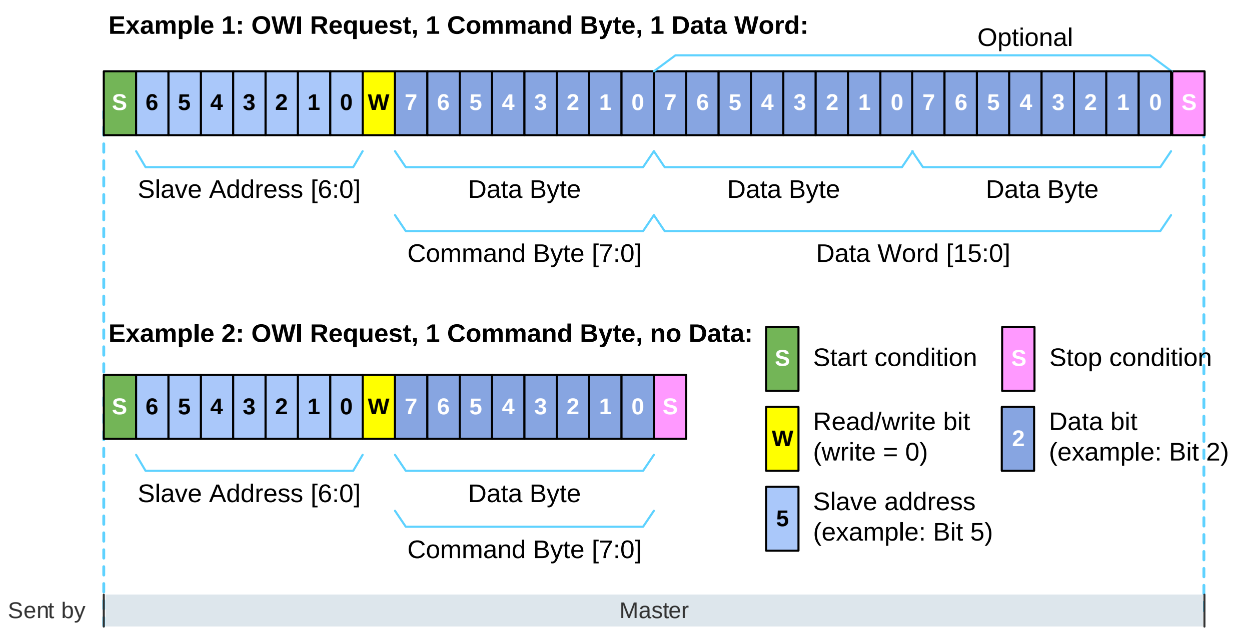


Figure 53: OWI Write Operation/Command Request

- Read operation

  After a data read request from the master to the slave (matching address byte and data direction bit = 1 for READ), the slave answers by sending data from the interface output registers. The master must generate a stop condition after receiving the requested data (see Figure 54).

  The data in the output registers is sent continuously until a stop condition is detected. After transmitting all available date, the slave starts repeating the data. The data of an ongoing OWI transaction is fixed. It does not get updated with newly available conditioned results. To receive new output data a new OWI read transaction must be started.

Example: OWI Read Operation, Status Byte (+n) Data Bytes*:

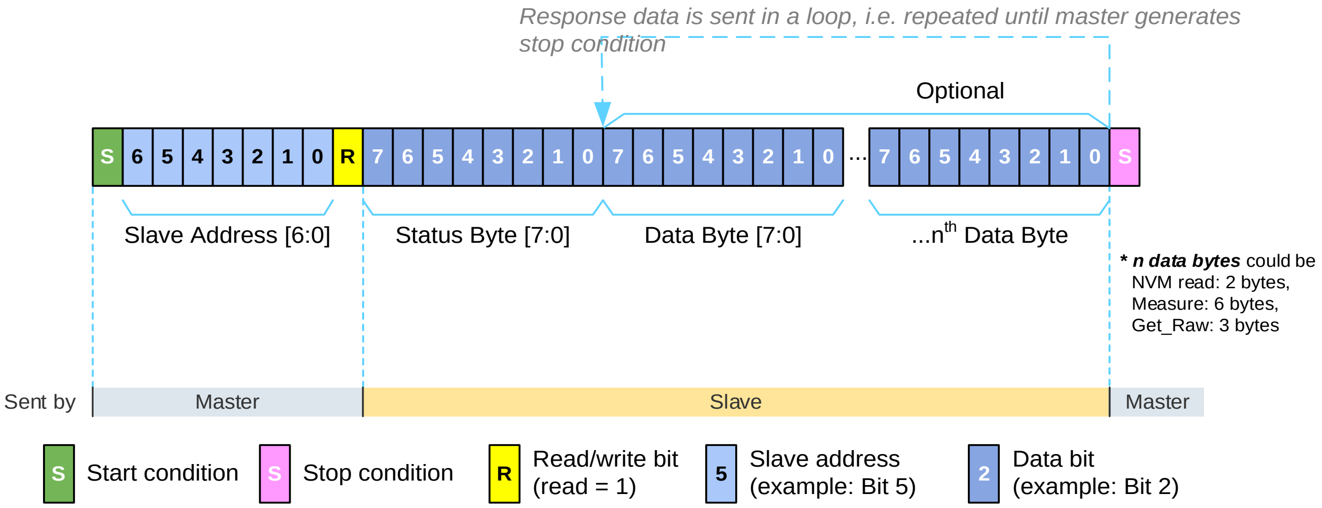


Figure 54: OWI Read Operation

The length of the OWI-line and the size of $R_{OWI,PULL}$ (if it is statically connected to AOUT), and consequently the resistive and capacitive loads, influence the maximum possible interface speed and minimum Bit period. Additional capacitance on the OWI1 (AOUT) line can improve RF disturbance robustness und harsh EMC conditions. Table 36 shows practical OWI-interface dimensioning examples and the resulting maximum signal frequencies (minimum possible Bit periods).

The ZSSC3281's OWI interface properties and timing capabilities are given in Table 37.

Table 36: OWI Dimensioning Examples

$R_{OWI,PULL}$ (+ $R_{OWI,LOAD}$) / $C_{OWI,LOAD}$ [1]	1.8 kΩ	2.5 kΩ	3.3 kΩ	5.5 kΩ	10.0 kΩ
1nF	20µs	20µs	21µs	35µs	63µs
10nF	113µs	157µs	207µs	345µs	628µs
22nF	249µs	345µs	456µs	760µs	1381µs
33nF	373µs	518µs	684µs	1140µs	2070µs
44nF	497µs	691µs	912µs	1520µs	2762µs
51nF	576µs	801µs	1057µs	1760µs	3205µs

1. Examples are shown with statically connected $R_{OWI,PULL}$, and with minimum bit period: $t_{OWI,BIT}$.

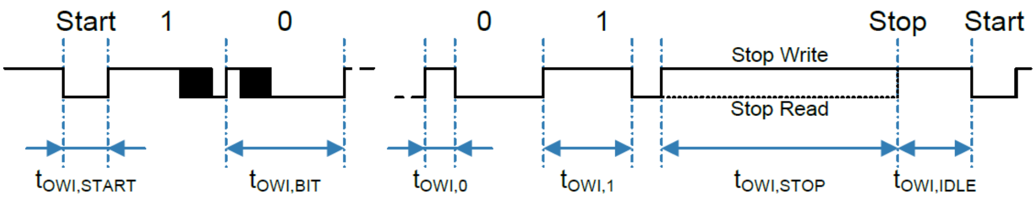


Figure 55: OWI Telegram

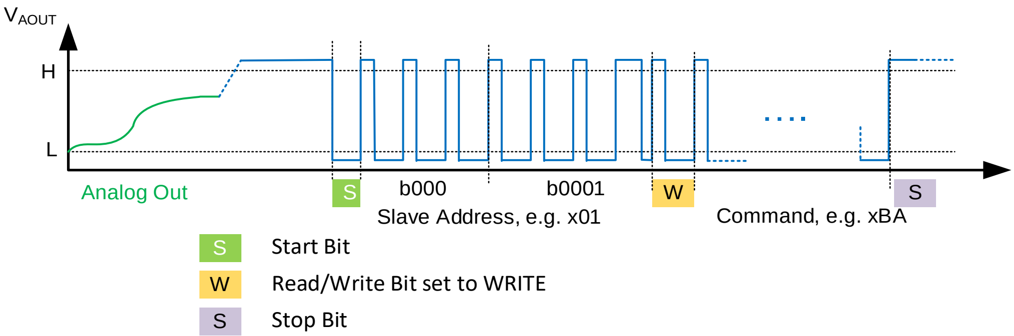


Figure 56: Typical OWI Communication on AOUT in Voltage Out Mode

Table 37: OWI Timing Parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{OWI,WINDOW}$	OWI-Start-UP “Listening” Window	Time after power-on in which the OWI can be enabled by a valid OWI-Start-Condition and command				ms
		OWI Window Mode		400		
		OWI Analog Mode		200		
$t_{OWI,IDLE}$	Bus free time between start and stop condition		1		30	us
$t_{OWI,START}$	Hold time start condition		10			us
$t_{OWI,BIT}$	Bit time		10	40	4000	us
$t_{OWI,0}$	Duty ratio bit ‘0’		0.125	0.25	0.375	t_{OWI_BIT}
$t_{OWI,1}$	Duty ratio bit ‘1’		0.625	0.75	0.875	t_{OWI_BIT}
$t_{OWI\_BIT\_DEV}$	Bit time deviation	Tolerated variation of Bit time from bit to bit	0.55	1.0	1.45	t_{OWI_BIT}
$t_{OWI,STOP}$	Hold time stop condition	$t_{OWI\_BIT\_L}$ is the bit time of the last valid bit	1.5	250		$t_{OWI\_BIT\_L}$
$C_{OWI,LOAD}$	Capacitive load at OWI line		–	2.2	50	nF
$R_{OWI,PULL}$	Pull-up resistance – master		0.3	0.47	3.3	kΩ
$R_{OWI,LOAD}$	Resistive OWI line load		20	0.01 x $R_{OWI,PULL}$	–	Ω

An enabled OWI interface is checked after power-on or reset of ZSSC3281 for incoming telegrams. The OWI interface is locked for further communication if it is the first which received a telegram with a matching slave address and at least 8bit of telegram data. The OWI communication mode can only be left by power-on or reset of the ZSSC3281.

11.1.4.1. OWI operation modes

The ZSSC3281 allows utilization of the OWI interface in different application configurations. The respective configuration settings can be made in the GUI via Configure\Serial Interfaces\OWI Mode.

- OWI Disable/OWI Off

  This mode deactivates the OWI interface. For example, this could be applied in cases when an analog-output smart sensor is configured and calibrated using the OWI interface and the OWI is not available for end user access after calibration and final setup/programming.

- OWI Digital (no analog output)

  In this mode AOUT does not provide any analog outputs and is only used as OWI pin. There is no start-up window limitation for activation of the OWI interface, but if the ZSSC3281 was started in Command Mode or Sleep Mode and no *OWI Startup* (BA_{HEX}) command was received within a window time of 200ms, the system state machine automatically moves to Cyclic Mode.

- OWI Window

  The OWI Window Mode disables the analog output signal driving at AOUT after power-on or reset of ZSSC3281 for a start-up window time of 2 x 200ms. During the first 200ms window ZSSC3281 listens on OWI-IN1 (=AOUT) for incoming OWI telegrams. As soon as it receives an OWI Startup (BA_{HEX}) command on OWI-IN1 it locks the AOUT channel for OWI communication. The OWI channel can only be locked if the I2C/I3C and SPI channels remained silent and do not lock the InterfaceBridge (IFB) first.

  If no OWI Startup command was received during the first 200ms start-up window, a second 200ms window is started and ZSSC3281 listens on OWI-IN2 for incoming OWI telegrams. If it detects an OWI Startup (BA_{HEX}) command within the second 200ms start-up window, it locks the OWI channel to the OWI-IN2 + AOUT communication path.

  If no OWI Startup command was received even during the second 200ms start-up window, the OWI interface is disabled automatically and the AOUT resumes to its configured analog output function. OWI Window Mode is the factory default OWI mode for AOUT.

- OWI Analog Voltage

  The OWI Analog Voltage mode allows to start OWI communication even while the configured voltage output function is already active on AOUT. During a start-up window of 200ms after power-on or reset ZSSC3281 listens on OWI-IN1 for incoming OWI telegrams. As soon as it receives an OWI Startup (BA_{HEX}) command on OWI-IN1 it locks the AOUT channel for OWI communication.

  The difference to the OWI Window Mode is, that the OWI master has to overdrive the analog output voltage signal at AOUT. To prevent self-locking of the OWI channel without external overdrive from the OWI master (for example, if the conditioned analog output waveform at AOUT matches an OWI telegram by accident), the OWI slave also checks for the occurrence of at least one overdrive drive condition at AOUT (either short to VSS or short to VDD) before it releases a received OWI telegram to the IFB.

  If no OWI Startup command was received during the 200ms start-up window, the OWI interface is disabled automatically and the AOUT remains in its configured analog output function. OWI activation is not possible until new power-on on reset of ZSSC3281.

11.2 Command Interpreter

11.2.1. Command Table

The availability of commands depends on the active main operating mode: Command, Sleep, or Cyclic Mode.

Table 38: Command Table

Command Code (Byte)	Return	Description	Command Mode	Cyclic Mode	Sleep Mode	Since FW Release
80_{HEX}	StatusByte + 20-byte SCC data	**Read output memory** Reads content of output memory which contains following information: • Conditioned Bridge Sensor1 (24 bit) • Conditioned Temperature Channel1 (24 bit) • Conditioned Sensor2 (24 bit) • Conditioned Temperature Channel2 (24 bit) • Logic Bridge Sensor Channel3 (32 bit) • Conditioned Temperature Channel3 (32 bit) Note: If more than 20 data bytes are read by the host, the response data rolls over. In Command Mode/Sleep Mode the last valid output data is provided.	Yes	Yes	Yes	1.0.0
81_{HEX} followed by data $XXYY_{HEX}$	YY_{HEX} bytes	**Read output memory burst** Reads content of output memory in burst mode: • XX_{HEX} selects the byte in output memory which is read first • YY_{HEX} defines the number of bytes which is read from output memory Note: If more than YY_{HEX} data bytes are read by the host, the response data rolls over. In Command Mode/Sleep Mode the last valid output data is provided.	Yes	Yes	Yes	1.0.0
82_{HEX} followed by data $XXWW_{HEX}$	WW_{HEX} * 4 bytes	**Read configuration data in burst** Reads content of Configuration and Calibration Page (CCP) in burst mode: • XX_{HEX} selects the 32-bit word in CCP which is read first • WW_{HEX} defines the number of words which is read from output memory Note: Maximum supported WW_{HEX} is 0x20	Yes	No	No	1.0.0
83_{HEX} followed by data $XXWW_{HEX}$	–	**(Over-) Write configuration data in burst** [1] Writes content of Configuration and Calibration Page (CCP) in burst mode into Shadow RAM: • XX_{HEX} selects the word in CCP which is written first • WW_{HEX} defines the number of words which is written in output memory Note: Maximum supported WW_{HEX} is 0x20	Yes	No	No	1.0.0
84_{HEX} followed by data $XXWW_{HEX}$	WW_{HEX} * 4 bytes	**Read device info data in burst** Reads content of InfoPage in burst mode • XX_{HEX} selects the word in CCP which is read first • WW_{HEX} defines the number of words which is read from output memory Note: Maximum supported XX_{HEX} is 0x1F Maximum supported WW_{HEX} is 0x20 If XX_{HEX} + WW_{HEX} is > 0x20 the command fails.	Yes	No	No	1.0.0

Command Code (Byte)	Return	Description	Command Mode	Cyclic Mode	Sleep Mode	Since FW Release
88_{HEX}	–	**Write CCP RAM shadow to flash** Writes Configuration and Calibration Page in flash with content from Shadow RAM	Yes	No	No	1.0.0
$8A_{HEX}$	2 bytes Chip Hardware Version	**Read chip hardware version**	Yes	No	Yes	1.0.0
$8B_{HEX}$	3 bytes IAP Firmware Version	**Read IAP firmware version**	Yes	No	Yes	1.0.0
$8C_{HEX}$ followed by data $XXXX_{HEX}$	No answer is returned *(Execution jumps directly to the FW update routines)*	**Start firmware update** Triggers Firmware update procedure. $XXXX_{HEX}$ represent the two Authentication Key bytes	Yes	No	No	1.0.0
$8D_{HEX}$	–	**Restart device** Device is immediately restarted	Yes	No	No	1.0.0
$8E_{HEX}$	3 bytes	**Read RCA firmware version**	Yes	No	Yes	1.0.0
$8F_{HEX}$	3 bytes	**Read application firmware version**	Yes	No	Yes	1.0.0
$A0_{HEX}$		**Reserved** for future use				
$A2_{HEX}$	3 bytes raw data	**Raw sensor measurement AFE1** [2] Returns unconditioned raw data of Bridge Sensor1	Yes	No	Yes	1.0.0
$A3_{HEX}$	3 bytes raw data	**Raw sensor measurement AFE2** [2] Returns unconditioned raw data of Bridge Sensor2	Yes	No	Yes	1.0.0
$A4_{HEX}$	3 bytes raw data	**Raw temperature measurement Sensor1** [2] Returns unconditioned temperature data for Temperature Channel 1	Yes	No	Yes	1.0.0
$A5_{HEX}$	3 bytes raw data	**Raw temperature measurement Sensor2** [2] Returns unconditioned temperature data for Temperature Channel 2	Yes	No	Yes	1.0.0
$A6_{HEX}$	3 bytes raw data	**Raw temperature measurement Sensor3** [2] Returns unconditioned temperature data for Temperature Channel 3	Yes	No	Yes	1.0.0
$A7_{HEX}$ followed by data $XXYY_{HEX}$	20 bytes raw data	**Snapshot calibration all sensors** [2] Returns unconditioned raw sensor and temperature data of all AFE channels that are activated in CCP. • XX_{HEX} minimum average count for AFE1 data • YY_{HEX} minimum average count for AFE2 data The output data format is as follows: • Raw Data Bridge Sensor1 (24 bit) • Raw Data Temperature Channel1 (24 bit) • Raw Data Bridge Sensor2 (24 bit) • Raw Data Temperature Channel2 (24 bit) • 0x00000000 (4 bytes 0x0) (32 bit) • Raw Data Temperature Channel3 (32 bit)	Yes	No	Yes	1.0.0
$A8_{HEX}$	–	**START_SLEEP** Exit Command Mode or Cyclic Mode and transition to Sleep Mode Sleep Mode is currently no different than Command Mode	Yes	Yes	No	1.0.0

Command Code (Byte)	Return	Description	Command Mode	Cyclic Mode	Sleep Mode	Since FW Release
A9HEX	–	**START_CM** Exit Sleep Mode or Cyclic Mode and transition to Command Mode	No	Yes	Yes	1.0.0
AAHEX		**Reserved**				
ABHEX	–	**START_CYC** Enter the Cyclic Mode: continuous measurement cycles, SSC corrections, and automatic, continuous digital and/or analog output updates	Yes	No	Yes	1.0.0
ACHEX		**Reserved** for future use				
ADHEX		**Reserved** for future use				
AEHEX		**Reserved** for future use				
AFHEX		**Reserved** for future use				
B0HEX	12 bytes diagnostic result data	**Check diagnosis status** Responds with the detailed diagnosis status	Yes	No	Yes	1.0.0
B1HEX	–	**Reset diagnosis status** Resets the contents of the diagnosis status register to 00HEX	Yes	No	Yes	1.0.0
B2HEX	–	**Update diagnosis status** Executes a all activated sensor and system diagnosis checks Note: If a measurement cycle is running concurrently, the diagnostic update happens after completion of the measurement cycle and SSC calculations.	Yes	No	Yes	1.0.0
B3HEX followed by data (0000HEX to FFFFHEX)	–	**DAC diagnosis** Set the DAC output register with the data in the command and enable/output the respective analog signal through AOUT (according to the AOUT_setup) Note: The DAC output can be switched off by the RESN pin, POR, or a change in the main operating mode	Yes	No	No	1.0.0
B4HEX followed by parameters 0x0X + 0xYY	2 bytes	**Self-diagnostic measure** for AFE1 and AFE2 Parameter 0x0X: • AFE1: 00HEX • AFE2: 01HEX Parameter 0xYY • See description in section 7	Yes	No	No	1.0.0
B5HEX		**Reserved** for future use				
B6HEX		**Reserved** for future use				
B7HEX		**Reserved** for future use				
B8HEX	12 bytes diagnostic result data	**Read fault memory** Responds with the detailed fault-memory status	Yes	No	Yes	1.0.0
B9HEX	–	**Reset fault memory** Resets the contents of the fault memory to 00HEX	Yes	No	Yes	1.0.0
BAHEX	–	**Startup OWI** Initialization command to enter OWI interface operation; only valid for OWI (see section 11.1.4)	Yes	Yes	Yes	1.0.0
D4HEX		**Reserved** for future use				
D5HEX		**Reserved** for future use				
D6HEX		**Reserved** for future use				

Command Code (Byte)	Return	Description	Command Mode	Cyclic Mode	Sleep Mode	Since FW Release
D7HEX		**Reserved** for future use				
FFHEX	Status followed by last output buffer data	**NOP** Output of read results; only valid for SPI	Yes	Yes	Yes	1.0.0

1. The Overwrite CCP data command 83HEX can be used to optimize evaluation and test routine execution time for analog front-end setup or to configure measurement setups without changing the ZSSC3281's Flash content. Without adding command 88HEX the changes made by 83HEX command are lost after reset of ZSSC3281 reset via the RESN pin or Power On Reset

2. These commands can be used to conduct a measurement without SSC conditioning, e.g., during the smart sensor calibration procedure. No digital correction is performed on the measurement result. The setup and configuration for the raw measurement is the content in the shadow registers that can be pre-loaded (automatically loaded during power-on) from the Flash or by means of the Overwrite command 83HEX
   Use Oversample measurements to obtain noise-minimized measurement results in Sleep or Command Mode. With higher oversampling factors, the command execution time increases proportionally.

12. Firmware Update

ZSSC3281 offers a firmware update function via the serial I2C interface for Renesas provided code (RCA code).

Figure 57 shows the high-level firmware flow. Initiating the firmware update is done by a "start firmware update" command in command mode. This command stores a magic sequence in a dedicated register and performs a reset of the device. Due to the stored magic sequence, the device starts to the update procedure during system boot and performs the firmware update.

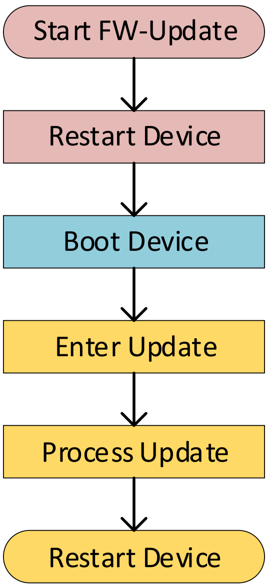


Figure 57 High-level Firmware Update Flow

A firmware update is meant to be executed exclusively via the ZSSC3281 GUI. It can be initiated at the FW Update Tab, where the respective new firmware file can be selected, and the update process can be triggered.

13. Production Configuration

13.1 Configuration and Calibration Page (CCP) Memory Map

13.1.1. Serial Interfaces

Address:	0x00	Register Name:	IfbParamCfg	Default:	0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
1	EnCrc	0	CRC Checking of Serial Interface Communication 0: Disabled 1: Enabled
2	EnErrResp	0	Extended Error Response Mode in Serial Communication 0: Inactive 1: Active
4	BypassCmdInterp	0	Bypass of IFB Command Interpreter in Cyclic Mode 0: Inactive 1: Active

Address:	0x01	Register Name:	I3cslvRegCtrl	Default:	0x000000C0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
3:0	InstanceId	0	I3C Instance ID 4bit hex value
6	Enable	1	I2C/I3C Interface Activation 0: Disabled 1: Enabled
7	ModeI2c	1	Operation Mode of I2C/I3C Interface 0: I3C Mode 1: I2C Mode

Address:	0x02	Register Name:	I3cslvRegStatAddrCtrl	Default:	0x0000003C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
6:0	Addr	0x3C	I2C/I3C Static Slave Address 7bit hex value

Address:	0x03	Register Name:	I3cslvInBandIrqSupport	Default:	0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
0	InBandIrq	0x0	I2C/I3C Inband Interrupt Support 0: Disabled 1: Enabled

Address:	0x04	Register Name:	SpislvParamCfg	Default:	0x00000001

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
0	Enable	0x1	SPI Interface Activation 0: Disabled 1: Enabled
1	ClockPhase	0x0	SPI Clock Phase 0: CPHA=0 1: CPHA=1
2	ClockPolar	0x0	SPI Clock Polarity 0: CPOL =0; Default Low 1: CPOL=1; Default High
3	SsPolar	0x0	SPI Slave Select Polarity 0: Active Low 1: Active High

Address:	0x05	Register Name:	OwislvCtrReg	Default:	0x00000008

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
1	FixedLenEn	0x0	Apply fixed bit length as defined in register **OwislvFixedlenReg** for transmission instead of the bit length measured for the last received bit. 0: Disabled 1: Enabled
2	FamAddrEn	0x0	OWI Family Address Checking 0: Disabled 1: Enabled
3	SlvAddrEn	0x1	OWI Slave Address Checking 0: Disabled 1: Enabled
5	In1PolarBit	0x0	OWI-IN1 Input Polarity 0: Active Low 1: Active High
6	In2PolarBit	0x0	OWI-IN1 Input Polarity 0: Active Low 1: Active High
7	OutPolarBit	0x0	OWI-OUT Output Polarity 0: Active Low 1: Active High

Address:	0x06	Register Name:	OwislvSlvaddrReg	Default:	0x00000028

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
6:0	SlvAddr	0x28	OWI Static Slave Address 7bit hex value

Address:	0x07	Register Name:	OwislvFixedlenReg	Default:	0x00000140

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
6:0	FixedLen	0x140	Bit length of a single OWI bit in 8MHz clock cycles, relevant only if **OwislvCtrReg.FixedLenEn** = 1 16bit hex value

Address:	0x08	Register Name:	OwiModeParam	Default:	0x00000001

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
2:0	OwiSlvMode	0x1	OWI Slave Operation Mode 0x0: Off 0x1: Window Mode 0x2: Digital Mode 0x3: Analog Voltage Mode

Address:	0x09	Register Name:	CntCommParam	Default:	0x0000000A

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
31:0	CntCommParam	0x4	Internal parameter of ZSSC3281 Firmware. **Must not be changed.**

Address:	0x0A	Register Name:	CommParamCrc	Default:	0x685AD4EB

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
31:0	CommParamCrc	0x685AD4EB	Internal parameter of ZSSC3281 Firmware. **Must not be changed.**

13.1.2. Clocks

Address:	0x0B	Register Name:	Clkout	Default:	0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
1:0	ClkOutMode	0x0	Clock Output Signal at CLK_OUT Pin (GPIO14) 0x0: Inactive 0x1: Internal High Speed Clock (16MHz) 0x2: Internal Low Speed Clock (32kHz) 0x3: Main System Clock, depends on stetting in Register **MiscctrlParamCfg.Divfclk**

Address:	0x0C	Register Name:	Divafeaout	Default:	0x00000008

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
1:0	FreqDivClkAfe	0x0	Clock Divider HighSpeedClock to AFE Clock 0x0: div4 (4MHz AFE clock) 0x1: div8 (2MHz AFE clock) 0x2: div16 (1MHz AFE clock)
4:2	FreqDivClkAout	0x2	Clock Divider HighSpeedClock to AOUT Clock 0x0: div1 (16MHz AOUT clock) 0x1: div2 (8MHz AOUT clock) 0x2: div4 (4MHz AOUT clock) 0x3: div8 (2MHz AOUT clock) 0x4: div16 (1MHz AOUT clock)
5	Afe2LowSpeedMode	0x0	AFE2 clock speed with respect to AFE1 0: Normal (equal) Speed 1: Quarter Speed

Address:	0x0D	Register Name:	Divfclk	Default:	0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
2:0	Divfclk	0x0	Clock Divider HighSpeedClock to System Clock 0x0: div1 (16MHz System clock) 0x1: div2 (8MHz System clock) 0x2: div4 (4MHz System clock) 0x3: div8 (2MHz System clock) 0x4: div16 (1MHz System clock)

Address:	0x0E	Register Name:	Anacfg	Default:	0x00000100

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
0	ExtldoDisable	0x0	External JFET LDO Activation 0: Enabled 1: Disabled
8:4	ExtldoVolt	0x10	External JFEL LDO Voltage 0x10 = 5.25V

Address:	0x0F	Register Name:	Extclkcfg	Default:	0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
1	EnExtclk	0x0	External Clock Input Activation 0: Disabled 1: Enabled

13.1.3. Basic AFE Setup

Address:	0x10	Register Name:	AfeBaseCfgParam	Default:	0x00000003

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
7:0	AfeActive	0x3	AFE Activation configuration 0x0: None 0x1: AFE1 only 0x2: AFE2 only 0x3: AFE1 and AFE2 0x7: DualSpeed
15:8	Afe1SmConfig	0x0	AFE1 Sequencer Configuration 0x0: SM- and SM+ 0x1: SM+ and AUX_AZ 0x2: SM+ only; 0x3: No Main Sensor-Bridge Measurement
23:16	Afe2SmConfig	0x0	AFE2 Sequencer Configuration 0x0: SM- and SM+ 0x1: SM+ and AUX_AZ 0x2: SM+ only; 0x3: No Main Sensor-Bridge Measurement
31:24	AfeSyncStatus	0x0	AFE1 / AFE2 Synchronization 0x0: Asynchronous measurement 0x1: Synchronized measurement

Address:	0x11	Register Name:	AfeDsCfg.Reg1	Default:	0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
23:0	Thresh1	0x0	Dual Speed Mode Threshold 1
31:24	ConvCnt	0x0	Internal Dual Speed Mode parameter – **Must not be changed.**

Address: 0x12						Register Name:									AfeDsCfg.Reg2												Default: 0x00000000				
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
23:0	Thresh2	0x0	Dual Speed Mode Threshold 2

13.1.4. Sensor Bridge

Address:	0x13 0x15	Register Name:	Bm1Cfg1 – Sensor Bridge 1 setting Bm2Cfg1 – Sensor Bridge 2 setting	Default:	0x04000655 0x04000656

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
3:0	BmPgaGain1	0x5 0x6	PGA1 Gain 0x0: 1.2 0x8: 58.1 0x1: 2 0x9: 76.6 0x2: 4 0xA: 112 0x3: 6 0xB: 143 0x4: 11.9 0xC: 187 0x5: 19.8 0xD: 223 0x6: 29.6 0xE: 275 0x7: 39.2
6:4	BmPgaGain2	0x5	PGA2 Gain 0x0: 1.1 0x4: 1.5 0x1: 1.2 0x5: 1.6 0x2: 1.3 0x6: 1.7 0x3: 1.4 0x7: 1.8
7	BmPgaPolarity	0x0	PGA Polarity 0: Positive 1: Negative
11:8	BmAdcReso	0x6	ADC Resolution 0x0: 10 bit 0x8: 18 bit 0x1: 11 bit 0x9: 19 bit 0x2: 12 bit 0xA: 20 bit 0x3: 13 bit 0xB: 21 bit 0x4: 14 bit 0xC: 22 bit 0x5: 15 bit 0xD: 23 bit 0x6: 16 bit 0xE: 24 bit 0x7: 17 bit
14:12	BmAdcShift	0x0	ADC Shift V_{shift}/ V_{fs} 0x0: 0 0x4: 0.500 0x1: 0.125 0x5: 0.625 0x2: 0.250 0x6: 0.750 0x3: 0.375 0x7: 0.875
15	BmBrdgType	0x0	Bridge Supply via TOPx, BOTx 0: Voltage Source 1: Resistor or Current Source
17:16	BmSetTime	0x0	Bridge Settling Time before ADC conversion starts 0x0: 20 us 0x1: 40 us 0x2: 60 us 0x3: 80 us

Address:	0x13 0x15	Register Name:	Bm1Cfg1 – Sensor Bridge 1 setting Bm2Cfg1 – Sensor Bridge 2 setting	Default:	0x04000655 0x04000656

Bits: 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Bits	Field Name	Default	Description
21:18	BmBrdgRth	0x0	Rth resistor, applicable if BmBrdgType = 1 0x0: Open; 0x1: 1333 ohms; 0x2: 2000 ohms; 0x3: 4000 ohms; 0x4: 8000 ohms; 0x5: 10000 ohms 0x6: 14000 ohms; 0x7: 18000 ohms; 0x8: 20000 ohms; 0x9: 24000 ohms; 0xA: 28000 ohms; 0xB: 40000 ohms
25:22	BmBrdgRtl	0x0	Rtl resistor, applicable if BmBrdgType = 1 0x0: Open; 0x1: 1333 ohms; 0x2: 2000 ohms; 0x3: 4000 ohms; 0x4: 8000 ohms; 0x5: 10000 ohms 0x6: 14000 ohms; 0x7: 18000 ohms; 0x8: 20000 ohms; 0x9: 24000 ohms; 0xA: 28000 ohms; 0xB: 40000 ohms
28:26	BmAdcMux	0x1	ADC Input MUX Setting 0x0: ADC inputs shorted to AGND 0x1: ADC input connected to PGA 0x2: ADC input connected to input (Gain = 1, PGA bypassed)
29	BmTest	0x0	Reserved, must remain 0
30	BmTestDac	0x0	Reserved, must remain 0
31	BmType	0x0	Sensor Type 0x0: Resistive Bridge 0x0: Thermopile / Thermocouple

Address:	0x14 0x16	Register Name:	Bm1Cfg2 – Sensor Bridge 1 setting Bm2Cfg2 – Sensor Bridge 2 setting	Default:	0x00000210 0x00000210

Bits: 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Bits	Field Name	Default	Description
4:0	BmPgaOffset	0x10	PGA Offset Shift 0x1: -1.9 mV; 0x2: -3.8 mV; 0x3: -5.6 mV; 0x4: -7.5 mV; 0x5: -9.4 mV; 0x6: -11.3 mV; 0x7: -13.1 mV; 0x8: -15.0 mV; 0x9: -16.9 mV; 0xA: -18.8 mV; 0xB: -20.6 mV; 0xC: -22.5 mV; 0xD: -24.4 mV; 0xE: -26.2 mV; 0xF: -28.1 mV 0x10: 0mV; 0x11: 1.9 mV; 0x12: 3.8 mV; 0x13: 5.6 mV; 0x14: 7.5 mV; 0x15: 9.4 mV; 0x16: 11.3 mV; 0x17: 13.1 mV; 0x18: 15.0 mV; 0x19: 16.9 mV; 0x1A: 18.8 mV; 0x1B: 20.6 mV; 0x1C: 22.5 mV; 0x1D: 24.4 mV; 0x1E: 26.2 mV; 0x1F: 28.1 mV
8:5	BmBrdgIBias	0x0	Sensor Supply Current, applicable if BmBrdgType = 1 0x0: Open/Off; 0x1: 5 uA; 0x2: 10 uA; 0x3: 20 uA; 0x4: 40 uA 0x5: 80 uA; 0x6: 100 uA; 0x7: 160 uA; 0x8: 200 uA; 0x9: 500 uA
9	BmAdcEnShift	0x1	ADC Shift & Gain x2 Enable, activates **BmAdcShift** setting 0x0: ADC Gain x1, ADC Shift disabled 0x1: ADC Gain x2, ADC Shift enabled

11:10	BmBias	0x0	AFE Bias Current Setting 0x0: normal operation 0x3: reduced AFE bias current

13.1.5. External Temperature Sensor

Address:	**0x17 0x19 0x1B**	**Register Name:**	**ExtTemp1Cfg1 – T1 Sensor setting ExtTemp2Cfg1 – T2 Sensor setting ExtTemp3Cfg1 – T3 Sensor setting**	**Default:**	**0x0011C5F1 0x00118502 0x00118502**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	**Field Name**	**Default**	**Description**
3:0	ExtTempPgaGain1	0x1 0x2 0x2	PGA1 Gain 0x0: 1.2 — 0x8: 60 0x1: 2 — 0x9: 80 0x2: 4 — 0xA: 120 0x3: 6 — 0xB: 150 0x4: 12 — 0xC: 200 0x5: 20 — 0xD: 240 0x6: 30 — 0xE: 300 0x7: 40
6:4	ExtTempPgaGain2	0x7 0x0 0x0	PGA2 Gain 0x0: 1.1 — 0x4: 1.5 0x1: 1.2 — 0x5: 1.6 0x2: 1.3 — 0x6: 1.7 0x3: 1.4 — 0x7: 1.8
7	ExtTempPgaPolarity	0x1 0x0 0x0	PGA Polarity 0: Positive 1: Negative
11:8	ExtTempAdcReso	0x5 0x5 0x5	ADC Resolution 0x0: 10 bit — 0x3: 13 bit 0x1: 11 bit — 0x4: 14 bit 0x2: 12 bit — 0x5: 15 bit
14:12	ExtTempAdcShift	0x4 0x0 0x0	ADC Shift value V_{shift}/V_{fs} 0x0: 0 — 0x4: 0.500 0x1: 0.125 — 0x5: 0.625 0x2: 0.250 — 0x6: 0.750 0x3: 0.375 — 0x7: 0.875
18:15	ExtTempType	0x3 0x3 0x3	External Temperature Type 0x0: Reserved 0x1: Diode/NTC/PTC sink mode, internal bias 0x2: Diode/NTC/PTC, external bias 0x3: Diode/NTC/PTC source mode, internal bias 0x4: Reserved 0x5: Bridge single ended, internal bias 0x6: Bridge single ended, external bias 0x7: Bridge differential
19	ExtTempInput	0x0 0x0 0x0	External Temperature Sensor Input MUX 0x0: Input connected to PGA 0x1: Input connected to ADC

Address:	0x17 0x19 0x1B	Register Name:	ExtTemp1Cfg1 – T1 Sensor setting ExtTemp2Cfg1 – T2 Sensor setting ExtTemp3Cfg1 – T3 Sensor setting	Default:	0x0011C5F1 0x00118502 0x00118502

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description	
23:20	ExtTempBrdgRth	0x1 0x1 0x1	Rth resistor, applicable depending on ExtTempType setting 0x0: Open 0x1: 1333 ohms 0x2: 2000 ohms 0x3: 4000 ohms 0x4: 8000 ohms 0x5: 10000 ohms	 0x6: 14000 ohms 0x7: 18000 ohms 0x8: 20000 ohms 0x9: 24000 ohms 0xA: 28000 ohms 0xB: 40000 ohms
27:24	ExtTempBrdgRtl	0x0 0x0 0x0	Rtl resistor, applicable depending on ExtTempType setting 0x0: Open 0x1: 1333 ohms 0x2: 2000 ohms 0x3: 4000 ohms 0x4: 8000 ohms 0x5: 10000 ohms	 0x6: 14000 ohms 0x7: 18000 ohms 0x8: 20000 ohms 0x9: 24000 ohms 0xA: 28000 ohms 0xB: 40000 ohms

Address:	0x18 0x1A 0x1C	Register Name:	ExtTemp1Cfg2 – T1 Sensor setting ExtTemp2Cfg2 – T2 Sensor setting ExtTemp3Cfg2 – T3 Sensor setting	Default:	0x00000210 0x00000010 0x00000010

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description	
4:0	ExtTempPgaOffset	0x10 0x10 0x10	PGA Offset Shift 0x1: -1.9 mV 0x2: -3.8 mV 0x3: -5.6 mV 0x4: -7.5 mV 0x5: -9.4 mV 0x6: -11.3 mV 0x7: -13.1 mV 0x8: -15.0 mV 0x9: -16.9 mV 0xA: -18.8 mV 0xB: -20.6 mV 0xC: -22.5 mV 0xD: -24.4 mV 0xE: -26.2 mV 0xF: -28.1 mV	0x10: 0mV 0x11: 1.9 mV 0x12: 3.8 mV 0x13: 5.6 mV 0x14: 7.5 mV 0x15: 9.4 mV 0x16: 11.3 mV 0x17: 13.1 mV 0x18: 15.0 mV 0x19: 16.9 mV 0x1A: 18.8 mV 0x1B: 20.6 mV 0x1C: 22.5 mV 0x1D: 24.4 mV 0x1E: 26.2 mV 0x1F: 28.1 mV
8:5	ExtTempBrdgIBias	0x0 0x0 0x0	External Temp Sensor Supply Current, applicable depending on ExtTempType setting 0x0: Open/Off; 0x1: 5 uA 0x2: 10 uA 0x3: 20 uA 0x4: 40 uA 0x5: 80 uA	 0x6: 100 uA 0x7: 160 uA 0x8: 200 uA 0x9: 500 uA 0xA: -20 uA 0xB: -100 uA
9	ExtTempAdcEnShift	0x1 0x0 0x0	ADC Shift & Gain x2 Enable, activates ExtTempAdcShift setting 0x0: ADC Gain x1, ADC Shift disabled 0x1: ADC Gain x2, ADC Shift enabled	
11:10	ExtTempBias	0x0 0x0 0x0	AFE Bias current Setting 0x0: normal operation 0x3: reduced AFE bias current	
13:12	ExtTempSetTime	0x0 0x0 0x0	Tx Input Settling Time before ADC conversion starts 0x0: 20 us 0x1: 40 us	

			0x2: 60 us 0x3: 80 us

Address:	0x1D	Register Name:	CmConfig[0]	Default:	0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
23:0	Reserved	0x0	tbd

Address:	0x1E	Register Name:	CmConfig[1]	Default:	0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
23:0	Reserved	0x0	Tbd

Address:	0x1F	Register Name:	CmConfig[2]	Default:	0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
23:0	Reserved	0x0	tbd

13.1.6. PTAT Sensor

Address:	0x20	Register Name:	PtatCfg1 – PTAT Sensor setting	Default:	0x00008413

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
3:0	PgaGain1	0x3	PGA1 Gain 0x0: 1.2 0x1: 2 0x2: 4 0x3: 6 0x4: 12 0x5: 20 0x6: 30 0x7: 40 0x8: 60 0x9: 80 0xA: 120 0xB: 150 0xC: 200 0xD: 240 0xE: 300
6:4	PgaGain2	0x1	PGA2 Gain 0x0: 1.1 0x1: 1.2 0x2: 1.3 0x3: 1.4 0x4: 1.5 0x5: 1.6 0x6: 1.7 0x7: 1.8
7	PgaPolarity	0x0	PGA Polarity 0: Positive 1: Negative
11:8	AdcReso	0x4	ADC Resolution 0x0: 10 bit 0x1: 11 bit 0x2: 12 bit 0x3: 13 bit 0x4: 14 bit 0x5: 15 bit

Address:	0x20	Register Name:	PtatCfg1 – PTAT Sensor setting	Default:	0x00008413

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
14:12	AdcShift	0x0	ADC Shift value V_{shift}/V_{fs} 0x0: 0 0x1: 0.125 0x2: 0.250 0x3: 0.375 0x4: 0.500 0x5: 0.625 0x6: 0.750 0x7: 0.875
17:15	AdcMux	0x1	ADC Input MUX Setting 0x0: ADC input connected to PGA 0x1: ADC input connected to input (Gain = 1, PGA bypassed)

Address:	0x21	Register Name:	PtatCfg2 – PTAT Sensor setting	Default:	0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
4:0	PgaOffset	0x0	PGA Offset Shift 0x1: -1.9 mV 0x2: -3.8 mV 0x3: -5.6 mV 0x4: -7.5 mV 0x5: -9.4 mV 0x6: -11.3 mV 0x7: -13.1 mV 0x8: -15.0 mV 0x9: -16.9 mV 0xA: -18.8 mV 0xB: -20.6 mV 0xC: -22.5 mV 0xD: -24.4 mV 0xE: -26.2 mV 0xF: -28.1 mV 0x10: 0mV 0x11: 1.9 mV 0x12: 3.8 mV 0x13: 5.6 mV 0x14: 7.5 mV 0x15: 9.4 mV 0x16: 11.3 mV 0x17: 13.1 mV 0x18: 15.0 mV 0x19: 16.9 mV 0x1A: 18.8 mV 0x1B: 20.6 mV 0x1C: 22.5 mV 0x1D: 24.4 mV 0x1E: 26.2 mV 0x1F: 28.1 mV
5	AdcEnShift	0x0	ADC Shift & Gain x2 Enable, activates AdcShift setting 0x0: ADC Gain x1, ADC Shift disabled 0x1: ADC Gain x2, ADC Shift enabled
7:6	Bias	0x0	AFE Bias current Setting 0x0: normal operation 0x3: reduced AFE bias current

13.1.7. AFE Sequencer

Wrong setting of this parameter can corrupt firmware execution. Leave the computation of necessary setup for this register to the GUI.

Address:	0x22 0x26	Register Name:	Afe1MeasCfg1 – AFE1 setting Afe2MeasCfg1 – AFE2 setting	Default:	0x01020036 0x01020036

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
1:0	MeasTypeSlot1	0x2	AFE Measurement Type for Slot_x 0x0: None 0x1: SM- 0x2: SM+ 0x3: AUX_i
3:2	MeasTypeSlot2	0x1	
5:4	MeasTypeSlot3	0x3	
7:6	MeasTypeSlot4	0x0	
9:8	MeasTypeSlot5	0x0	
11:10	MeasTypeSlot6	0x0	
13:12	MeasTypeSlot7	0x0	
15:14	MeasTypeSlot8	0x0	

16	EocIrqSlot1	0	End of Conversion Interrupt after Slot_x 0: Disabled 1: Enabled
17	EocIrqSlot2	1	
18	EocIrqSlot3	0	
19	EocIrqSlot4	0	
20	EocIrqSlot5	0	
21	EocIrqSlot6	0	
22	EocIrqSlot7	0	
23	EocIrqSlot8	0	
24	BurstModeSlot1	1	AFE DMA Burst Mode Data Transfer after Slot_x 0: Disabled 1: Enabled
25	BurstModeSlot2	0	
26	BurstModeSlot3	0	
27	BurstModeSlot4	0	
28	BurstModeSlot5	0	
29	BurstModeSlot6	0	
30	BurstModeSlot7	0	
31	BurstModeSlot8	0	

Wrong setting of this parameter can corrupt firmware execution. Leave the computation of necessary setup for this register to the GUI.

Address:	**0x23 0x27**	**Register Name:**	**Afe1MeasCfg2 – AFE1 setting Afe2MeasCfg2 – AFE2 setting**	**Default:**	**0x00000013 0x00000013**
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0					

Bits	**Field Name**	**Default**	**Description**
3:0	NrOfSlots	0x3	Number of active measurement slots 0x0 … 0x8 selectable
5:4	CyclicMode	0x1	Sequencer Run Mode 0x0: Single measurement 0x1: Continuous cyclic measurement 0x2: Discontinuous cyclic measurement, started by trigger
7:6	AuxInsertRate	0x0	Insertion Rate of an AUX_i measurement in “Accelerated main measurement” setup 0x0: Disabled 0x1: Every 2nd 0x2: Every 4th 0x3: Every 8th
23:8	AuxMaxTime	0x0	Maximum lenght of AUX_i measurement slots within a sequence 0x0000 … 0xFFFF AFE clock cycles The parameter is calculated based on the relevant timing setups of all active AUX_i measurements to secure all AUX_i measurements have the same duration. This is mainly required for synchronized AFE operation.

Wrong setting of this parameter can corrupt firmware execution. Leave the computation of necessary setup for this register to the GUI.

Address:	0x24 0x28	Register Name:	Afe1MeasCfg3 – AFE1 setting Afe2MeasCfg3 – AFE2 setting	Default:	0x00000018 0x00000300

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default		Description
31:0	AuxMeasEnable0Aux1	0	0	Activation of Auxiliary measurements Bit 0: Auto-zero (AZ) measurement on Sensor Bridge Bit 1: PTAT Sensor S- Bit 2: PATAT Sensor S+ Bit 3: T1 Sensor S- Bit 4: T1 Sensor S+ Bit 5: T1 Sensor, check short to top Bit 6: T1 Sensor, check short to bottom Bit 7: T1 Sensor, check open Bit 8: T2 Sensor S- Bit 9: T2 Sensor S+ Bit 10: T2 Sensor, check short to top Bit 11: T2 Sensor, check short to bottom Bit 12: T2 Sensor, check open Bit 13: T3 Sensor S- Bit 14: T3 Sensor S+ Bit 15: T3 Sensor, check short to top Bit 16: T3 Sensor, check short to bottom Bit 17: T3 Sensor, check open Bit 18: AFE gain diagnosis S+ Bit 19: AFE gain diagnosis S- Bit 22: AFE offset diagnosis Bit 27: Bridge Sensor connection check, INP or INN open Bit 28: Bridge Sensor connection check, INP and INN shorted All other bits reserved Bit Value Meaning 0: Aux measurement Skipped 1: Aux measurement Executed
	AuxMeasEnable0Aux2	0	0	
	AuxMeasEnable0Aux3	0	0	
	AuxMeasEnable0Aux4	1	0	
	AuxMeasEnable0Aux5	1	0	
	AuxMeasEnable0Aux6	0	0	
	AuxMeasEnable0Aux7	0	0	
	AuxMeasEnable0Aux8	0	0	
	AuxMeasEnable0Aux9	0	1	
	AuxMeasEnable0Aux10	0	1	
	AuxMeasEnable0Aux11	0	0	
	AuxMeasEnable0Aux12	0	0	
	AuxMeasEnable0Aux13	0	0	
	AuxMeasEnable0Aux14	0	0	
	AuxMeasEnable0Aux15	0	0	
	AuxMeasEnable0Aux16	0	0	
	AuxMeasEnable0Aux17	0	0	
	AuxMeasEnable0Aux18	0	0	
	AuxMeasEnable0Aux19	0	0	
	AuxMeasEnable0Aux20	0	0	
	AuxMeasEnable0Aux21	0	0	
	AuxMeasEnable0Aux22	0	0	
	AuxMeasEnable0Aux23	0	0	
	AuxMeasEnable0Aux24	0	0	
	AuxMeasEnable0Aux25	0	0	
	AuxMeasEnable0Aux26	0	0	
	AuxMeasEnable0Aux27	0	0	
	AuxMeasEnable0Aux28	0	0	
	AuxMeasEnable0Aux29	0	0	
	AuxMeasEnable0Aux30	0	0	
	AuxMeasEnable0Aux31	0	0	
	AuxMeasEnable0Aux32	0	0	

Address:	0x25 0x29	Register Name:	Afe1MeasCfg4 – AFE1 setting Afe2MeasCfg4 – AFE2 setting	Default:	0x00400000 0x00400000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default		Description
4:0	AuxMeasEnable0Aux33	0	0	Activation of Auxiliary measurements Reserved
	AuxMeasEnable0Aux34	0	0	
	AuxMeasEnable0Aux35	0	0	
	AuxMeasEnable0Aux36	0	0	
	AuxMeasEnable0Aux37	0	0	
20:5	IdleTime	0x0		In continuous cyclic measurement mode idle times up to 10ms can be asserted between two sequences. IdleTime represents a number of AFE clocks – 4MHz by default
21	IrqEnableEoauxins	0		End of Inserted AUX Measurement 0: IRQ disabled 1: IRQ enabled
22	IrqEnableEoauxseq	1		End of Aux Sequence 0: IRQ disabled 1: IRQ enabled
23	IrqEnableEoauxaz	0		End of AZ Measurement 0: IRQ disabled 1: IRQ enabled
24	SensBufDepth	0		Bridge Sensor data buffer depth in SRAM 0: data buffer depth 1 1: data buffer depth 8

13.1.8. Diagnosis

Address:	0x2A	Register Name:	DiagCfg	Default:	0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
0	Afe1GainChkResDacEn	0	Resistive Diagnosis DAC activation at AFE1 0: Disabled 1: Enabled
2:1	Afe1GainChkResDacVal	0x0	Resistive Diagnosis DAC value at AFE1 0x0: 2mV 0x1: 10mV 0x2: 100mV 0x3: 200mV
3	Afe2GainChkResDacEn	0	Resistive Diagnosis DAC activation at AFE2 0: Disabled 1: Enabled
5:4	Afe2GainChkResDacVal	0x0	Resistive Diagnosis DAC value at AFE2 0x0: 2mV 0x1: 10mV 0x2: 100mV 0x3: 200mV
6	Extt1Pt100	0	Reference for temperature sensor short measurement on T1 0: RT_SHORT < 500Ω 1: RT_SHORT < 10Ω
8:7	Extt1Range	0x0	Reference for Temp Sensor open check on T1 0x0: 2MΩ 0x1: 0.5MΩ 0x3: 0.1MΩ
10	Extt2Pt100	0	Reference for temperature sensor short measurement on T2 0: RT_SHORT < 500Ω

Bits	Field Name	Default	Description
			1: RT_SHORT < 10Ω
12:11	Extt2Range	0x0	Reference for Temp Sensor open check on T2 0x0: 2MΩ 0x1: 0.5MΩ 0x3: 0.1MΩ
14	Extt3Pt100	0	Reference for temperature sensor short measurement on T3 0: RT_SHORT < 500Ω 1: RT_SHORT < 10Ω
16:15	Extt3Range	0x0	Reference for Temp Sensor open check on T3 0x0: 2MΩ 0x1: 0.5MΩ 0x3: 0.1MΩ

Address:	0x2B 0x2D	Register Name:	DiagSen.Range[0].Inp – AFE1 setting DiagSen.Range[1].Inp – AFE2 setting	Default:	0x00000000 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
15:0	Min	0x0	Reserved
31:16	Max	0x0	Reserved

Address:	0x2C 0x2E	Register Name:	DiagSen.Range[0].Inn – AFE1 setting DiagSen.Range[1].Inn – AFE2 setting	Default:	0x00000000 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
15:0	Min	0x0	Reserved
31:16	Max	0x0	Reserved

Address:	0x2F 0x30	Register Name:	DiagSen.GainChk[0] – AFE1 setting DiagSen.GainChk[1] – AFE2 setting	Default:	0x00000000 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
15:0	RefVal	0x0	Gain Reference Value for Gain Drift Diagnosis During sensor calibration an initial AFE Gain Check measurement with a properly defined AFExGainCheckResDacVal setting must be done and the obtained RAW output value shall be stored in this register for later reference.
31:16	TolVal	0x0	Gain Tolerance Value for Gain Drift Diagnosis A tolerance value in ADC counts for acceptable gain drift over lifetime shall be stored in this register A gain failure is signaled after the Gain Drift Check if the determined AFE Gain Value is either < (RefVal - TolVal) or > (RefVal + TolVal)

Address:	0x31 0x32	Register Name:	DiagSen.OfstChk[0] – AFE1 setting DiagSen.OfstChk[1] – AFE2 setting	Default:	0x00000000 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
15:0	RefVal	0x0	Offset Reference Value for Offset Drift Diagnosis During sensor calibration an initial AFE Offset Check measurement must be done and the obtained RAW output value shall be stored in this register for later reference.
31:16	TolVal	0x0	Offset Tolerance Value for Offset Drift Diagnosis

			A tolerance value in ADC counts for acceptable offset drift over lifetime shall be stored in this register An offset failure is signaled after the Offset Drift Check if the determined AFE Offset Value is either < (RefVal - TolVal) or > (RefVal + TolVal)

13.1.9. Temperature Channel Mapping

Address:	0x33	Register Name:	TempMapChId	Default:	0x0000001A

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
2:0	Tch1	0x2	Temperature Sensor Source for Temperature Channels 1, 2, 3 0x0: None 0x1: PTAT 0x2: T1 0x3: T2 0x4: T3
5:3	Tch2	0x3	
8:6	Tch3	0x0	

13.1.10. SSC Algorithm Selection

Address:	0x34	Register Name:	MathSbrAlgoSel	Default:	0x00000011

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
3:0	Sensor1	0x1	SSC Algorithm for Bridge Sensors 1 & 2 0x0: None 0x1: SOT Parabolic 0x2: SOT S-Shaped
7:4	Sensor2	0x1	
10:8	TlcOp	0x0	Third Logic Channel Operation 0x0: Subtraction 0x1: Division
11	TlcChOrder	0x0	Third Logic Channel Operand Order 0x0: CH1 op CH2 0x1: CH2 op CH1

13.1.11. EOC / Alarm

Address:	0x35 0x38	Register Name:	EocAlarmPin[0].Reg1 – Pin EOC/ALARM_1 EocAlarmPin[1].Reg1 – Pin EOC/ALARM_2	Default:	0x00000000 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
23:0	Thresh1	0x0	Alarm Threshold 1 24 bit value, matches SSC output number format
24	En	0	EOC / Alarm Activation 0: Disabled 1: Enabled
25	Pol	0	Output Polarity 0: Active High 1: Active Low
27:26	NrThresh	0x0	Number of Alarm Thresholds 0x0: None (EOC Mode) 1: Single Threshold 2: Window (2 Thresholds)
28	Range	0	Alarm Range 0: Above / Outside 1: Below / Inside

Address:	0x36 0x39	Register Name:	EocAlarmPin[0].Reg2 – Pin EOC/ALARM_1 EocAlarmPin[1].Reg2 – Pin EOC/ALARM_2	Default:	0x00000000 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
23:0	Thresh2	0x0	Alarm Threshold 2 24 bit value, matches SSC output number format

Address:	0x37 0x3A	Register Name:	EocAlarmPin[0].Reg3 – Pin EOC/ALARM_1 EocAlarmPin[1].Reg3 – Pin EOC/ALARM_2	Default:	0x00000000 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
23:0	Hyst	0x0	Alarm Hysteresis 24bit value, matches SSC output number format
31:24	Persist	0x0	Alarm Condition Persistence before Alarm State is changed 8bit value (0 … 255)

13.1.12. Analog Output (AOUT)

Address:	0x3B	Register Name:	AoutSelParam	Default:	0x00000001

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
2:0	SelAfeForDac	0x1	Source Signal for Analog Output 0x0: None 0x1: Bridge Sensor Channel 1 0x2: Bridge Sensor Channel 2 0x3: Third Logic Channel 0x4: Temperature Channel 1 0x5: Temperature Channel 2 0x6: Temperature Channel 3
5:3	AoutModSel	0x0	Analog Output Driver Mode 0x0: Disabled 0x1: Absolute Voltage Output 0-10V 0x2: Absolute Voltage Output 0-5V 0x3: Absolute V 0-1V 0x4: Ratiometric Voltage Output 0x5: 2-Wire Current Loop 0x6: 3-Wire Current Loop

Address:	0x3C	Register Name:	AoutRegCtrl	Default:	0x0000001B

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
0	AoutEn	1	Analog Output Activation 0: Disabled 1: Enabled
2:1	AoutMode	0x1	Analog Output Mode 0x0: Current Loop 5V-R-DAC 0x1: VOUT 5V 0x2: VOUT 1V 0x3: Current Loop 1V-R-DAC
3	AoutHighPowEn	1	AOUT Driver Output Power 0: Low Power 1: High Power
4	AoutFeedBackEn	1	AOUT Driver Feedback 0: External 1: Internal

6:5	AoutCurrLim	0x0	AOUT Driver Output Current Limitation 0x0: 6 mA 0x1: 12 mA 0x2: 18 mA 0x3: 25 mA
7	AoutOffsetCompOff	0	AOUT Driver Offset Compensation 0: Disabled 1: Enabled
8	AoutVddnEn	0	VDDN Charge Pump for Negative Supply 0: Disabled 1: Enabled
10:9	AoutVddnLoad	0x0	VDDN Charge Pump Load Current 0x0: 0.5 mA 0x1: 1 mA 0x2: 3 mA 0x3: 5 mA

Address: 0x3D	Register Name: AoutRegDiag		Default: 0x00000000
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0			
Bits	**Field Name**	**Default**	**Description**
0	AoutDiagOutEn	0	Diagnosis Level Output at AOUT 0: Normal Operation Mode 1: Diagnosis Output Mode
2:1	AoutDiagOutValue	0x0	Analog Output Mode 0x0: V_{AOUT} = VSS 0x1: V_{AOUT} = 5% VDD 0x2: V_{AOUT} = 96% VDD 0x3: V_{AOUT} = VDD
3	AoutDiagVddaEn	0	VDDA Diagnosis if VDDA regulator for AOUT is turned on 0: Disabled 1: Enabled

Address: 0x3E	Register Name: AoutCl2Coeff		Default: 0x00000000
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0			
Bits	**Field Name**	**Default**	**Description**
15:0	ClOffset	0x0000	2-Wire Current Loop Calibration Coefficient CL2_Offset 16 bit Value
31:16	ClDelta	0x0000	2-Wire Current Loop Calibration Coefficient CL2_Delta 16 bit Value

Address: 0x3F	Register Name: AoutCl3Coeff		Default: 0x00000000
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0			
Bits	**Field Name**	**Default**	**Description**
15:0	ClOffset	0x0000	3-Wire Current Loop Calibration Coefficient CL3_Offset 16 bit Value
31:16	ClDelta	0x0000	3-Wire Current Loop Calibration Coefficient CL3_Delta 16 bit Value

13.1.13. System Startup

Address:	0x40	Register Name:	StartupParamCfg	Default:	0x00000001

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
0	StartInCmMode	1	System Startup in Command Mode 0: Disabled 1: Enabled

13.1.14. IIR Filter

Address:	0x41	Register Name:	IirFiltCoeffReg	Default:	0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
2:0	FiltSbr1Avg	0x0	IIR Avg Value Sensor Bridge 1
5:3	FiltSbr1Diff	0x0	IIR Diff Value Sensor Bridge 1
8:6	FiltSbr2Avg	0x0	IIR Avg Value Sensor Bridge 2
9:11	FiltSbr2Diff	0x0	IIR Diff Value Sensor Bridge 2
14:12	FiltTemp1Avg	0x0	IIR Avg Value Temperature Channel 1
17:15	FiltTemp1Diff	0x0	IIR Diff Value Temperature Channel 1
20:18	FiltTemp2Avg	0x0	IIR Avg Value Temperature Channel 2
23:21	FiltTemp2Diff	0x0	IIR Diff Value Temperature Channel 2
26:24	FiltTemp3Avg	0x0	IIR Avg Value Temperature Channel 3
29:18	FiltTemp3Diff	0x0	IIR Diff Value Temperature Channel 3

13.1.15. General AFE Configuration

Address:	0x42	Register Name:	AfeConfig	Default:	0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
1:0	BM1ChpMode	0x0	PGA Chopper Mode Bridge Sensor 1 0x0: 100 kHz 0x1: 200 kHz 0x2: 50 kHz 0x3: Chopper Off
3:2	BM2ChpMode	0x0	PGA Chopper Mode Bridge Sensor 2 0x0: 100 kHz 0x1: 200 kHz 0x2: 50 kHz 0x3: Chopper Off
5:4	ExtTemp1ChpMode	0x0	PGA Chopper Mode External Temperature Sensor T1 0x0: 100 kHz 0x1: 200 kHz 0x2: 50 kHz 0x3: Chopper Off
7:6	ExtTemp2ChpMode	0x0	PGA Chopper Mode External Temperature Sensor T2 0x0: 100 kHz 0x1: 200 kHz 0x2: 50 kHz 0x3: Chopper Off
9:8	ExtTemp3ChpMode	0x0	PGA Chopper Mode External Temperature Sensor T3 0x0: 100 kHz 0x1: 200 kHz 0x2: 50 kHz 0x3: Chopper Off
11:10	TChpMode	0x0	PGA Chopper Mode PTAT Temperature Sensor 0x0: 100 kHz 0x1: 200 kHz 0x2: 50 kHz 0x3: Chopper Off
12	BM1NoiseInt1	0	ADC 10µV Noise Reduction 0: Disabled 1: Enabled
13	BM2NoiseInt1	0	
14	ExtTemp1NoiseInt1	0	

15	ExtTemp2NoiseInt1	0	
16	ExtTemp3NoiseInt1	0	
17	TNoiseInt1	0	
18	CMNoiseInt1	0	Reserved
19	CMDitheringEnable	0	Reserved
20	Vdda1Brownout	0	AFE1 Vdda Brownout Diagnosis 0: Disabled 1: Enabled
21	Vdda2Brownout	0	AFE2 Vdda Brownout Diagnosis 0: Disabled 1: Enabled
22	Vdda3Brownout	0	AOUT Vdda Brownout Diagnosis 0: Disabled 1: Enabled
23	CM1En	0	Reserved
24	CM2En	0	Reserved

Address: 0x42	**Register Name: AfeConfig**		**Default: 0x00000000**
31 30 29 28 27 26	**25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8**		**7 6 5 4 3 2 1 0**
Bits	**Field Name**	**Default**	**Description**
25	Afe2LowSpeed	0	AFE2 clock speed with respect to AFE1 0: Normal (equal) Speed 1: Quarter Speed
20:26	AfeMisc	0x0	Reserved
31	CLMode	0	AFE Operation Mode for 2-Wire Current Loop application 0: Disabled 1: Enabled

13.1.16. Output Modulation

Address: 0x43	**Register Name: OutModConf**		**Default: 0x27106400**
31 30 29 28 27 26	**25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8**		**7 6 5 4 3 2 1 0**
Bits	**Field Name**	**Default**	**Description**
1:0	Sel	0x0	Output Modulation Type 0x0: No Output Modulation 0x1: Frequency Modulation 0x2: reserved
4:2	ChGpio1	0x0	Source Signal for FOUT/PWM_1 0x0: Not Used 0x1: Bridge Sensor 1 0x2: Bridge Sensor 2 0x3: Third Logic Channel 0x4: Temperature Channel 1 0x5: Temperature Channel 2 0x6: Temperature Channel 3
7:5	ChGpio2	0x0	Source Signal for FOUT/PWM_2 0x0: Not Used 0x1: Bridge Sensor 1 0x2: Bridge Sensor 2 0x3: Third Logic Channel 0x4: Temperature Channel 1 0x5: Temperature Channel 2 0x6: Temperature Channel 3
15:8	FmMinFreqPwmDc	0x64	Frequency Modulation – Minimum Frequency in Hz 8bit value in range 100 to 255

31:16	FmMaxFreqPwmBaseFreq	0x2710	Frequency Modulation – Maximum Frequency in Hz 16bit value in range 10,000 to 65,535

13.1.17. Output Clipping and Diagnostic Range Assignment

Address:	0x44	Register Name:	DiagClipOutCfg.SysDiagCfg	Default:	0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
0	DiagOutEn	0	Output Signalization of Diagnostic State at AOUT and FOUT 0: Disabled 1: Enabled
1	ClipOutEn	0	Two-Sided Clipping to Upper and Lower Diagnostic Limit 0: Disabled 1: Enabled

Address:	0x45	Register Name:	DiagClipOutCfg.DiagOutLvl[0]	Default:	0x00007FFE

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
31:0	DiagOutLvl[0]	0x7FFE	Select register for UDR / LDR assignment of diagnostic checks

Address:	0x46	Register Name:	DiagClipOutCfg.DiagOutLvl[1]	Default:	0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
31:0	DiagOutLvl[1]	0x0	Select register for UDR / LDR assignment of diagnostic checks

Address:	0x47	Register Name:	DiagClipOutCfg.DiagOutLvl[2]	Default:	0x0000003F

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
31:0	DiagOutLvl[2]	0x0	Reserved

Address:	0x48	Register Name:	DiagClipOutCfg.ClipOutLvl	Default:	0xF3330CCC

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
15:0	ClipOutLow	0xCCC	Lower Clipping Limit 0xCCC: 5% FS
31:16	ClipOutHigh	0xF333	Upper Clipping Limit 0xF333: 95% FS

13.1.18. SSC Coefficients

Address:	0x4D 0x57	Register Name:	Bs1Coeff.SOffset – Bridge Sensor 1 Bs2Coeff.Soffset – Bridge Sensor 2	Default:	0x00000000 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
23:0	SOffset	0x0	Sensor offset term *Offset_S*

Address:	0x4E 0x58	Register Name:	Bs1Coeff.SGain – Bridge Sensor 1 Bs2Coeff.SGain – Bridge Sensor 2	Default:	0x00200000 0x00200000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description

23:0	SGain	0x200000	Sensor gain term *Gain_S*

Address:	0x4F 0x59	Register Name:	Bs1Coeff.SSot – Bridge Sensor 1 Bs2Coeff.SSot – Bridge Sensor 2	Default:	0x00000000 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
23:0	SSot	0x0	Second-order term for sensor non-linearity *SOT_sens*

Address:	0x50 0x5A	Register Name:	Bs1Coeff.SShift – Bridge Sensor 1 Bs2Coeff.SShift – Bridge Sensor 2	Default:	0x00000000 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
23:0	SShift	0x0	Post-calibration term *SENS_shift*

Address:	0x51 0x5B	Register Name:	Bs1Coeff.STco – Bridge Sensor 1 Bs2Coeff.STco – Bridge Sensor 2	Default:	0x00000000 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
23:0	STco	0x0	Temperature coefficient offset term *Tco*

Address:	0x52 0x5C	Register Name:	Bs1Coeff.SSotTco – Bridge Sensor 1 Bs2Coeff.SSotTco – Bridge Sensor 2	Default:	0x00000000 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
23:0	SSotTco	0x0	Second-order term for Tco nonlinearity *SOT_tco*

Address:	0x53 0x5D	Register Name:	Bs1Coeff.STcg – Bridge Sensor 1 Bs2Coeff.STcg – Bridge Sensor 2	Default:	0x00000000 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
23:0	STcg	0x0	Temperature coefficient gain term *Tcg*

Address:	0x54 0x5E	Register Name:	Bs1Coeff.SSotTcg – Bridge Sensor 1 Bs2Coeff.SSotTcg – Bridge Sensor 2	Default:	0x00000000 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
23:0	SSotTcg	0x0	Second-order term for Tcg non-linearity *SOT_tcg*

Address:	0x55 0x5F	Register Name:	Bs1Coeff.OutScaleGain – Bridge Sensor 1 Bs2Coeff.OutScaleGain – Bridge Sensor 2	Default:	0x00100000 0x00100000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
23:0	OutScaleGain	0x100000	Post SSC Output Scaling Gain

Address:	0x56 0x60	Register Name:	Bs1Coeff.OutScaleOfst – Bridge Sensor 1 Bs2Coeff.OutScaleOfst – Bridge Sensor 2	Default:	0x00000000 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
23:0	OutScaleOfst	0x0	Post SSC Output Scaling Offset

Address:	0x61 0x65 0x69	Register Name:	Tch1Coeff.TOffset – Temp Channel 1 Tch2Coeff.TOffset – Temp Channel 2 Tch3Coeff.TOffset – Temp Channel 3	Default:	0x00000000 0x00000000 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
23:0	TOffset	0x0	Offset coefficient for temperature *Offset_T*

Address:	0x62 0x66 0x6A	Register Name:	Tch1Coeff.TGain – Temp Channel 1 Tch2Coeff.TGain – Temp Channel 2 Tch3Coeff.TGain – Temp Channel 3	Default:	0x00200000 0x00200000 0x00200000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
23:0	TGain	0x200000	Gain coefficient for temperature *Gain_T*

Address:	0x63 0x67 0x6B	Register Name:	Tch1Coeff.TSot – Temp Channel 1 Tch2Coeff.TSot – Temp Channel 2 Tch3Coeff.TSot – Temp Channel 3	Default:	0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
23:0	TSot	0x0	Second-order term for temperature source *SOT_T*

Address:	0x64 0x68 0x6C	Register Name:	Tch1Coeff.TShift – Temp Channel 1 Tch2Coeff.TShift – Temp Channel 2 Tch3Coeff.TShift – Temp Channel 3	Default:	0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Default	Description
23:0	TShift	0x0	Shift for post-calibration/post-assembly offset compensation *T_Shift*

13.1.19. CCP Version

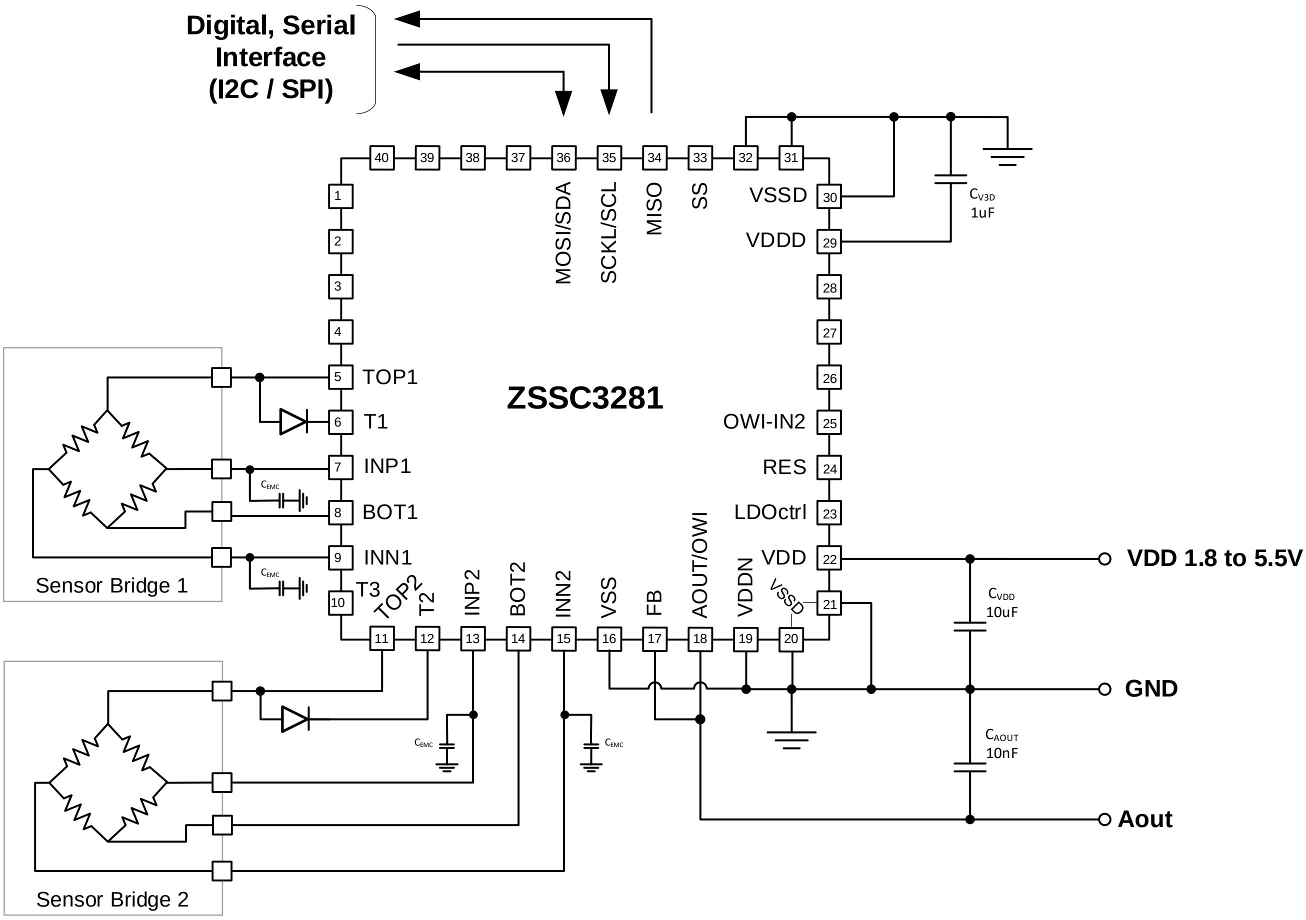
Address:	0xFF	Register Name:	CcpVersion	Default:	0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

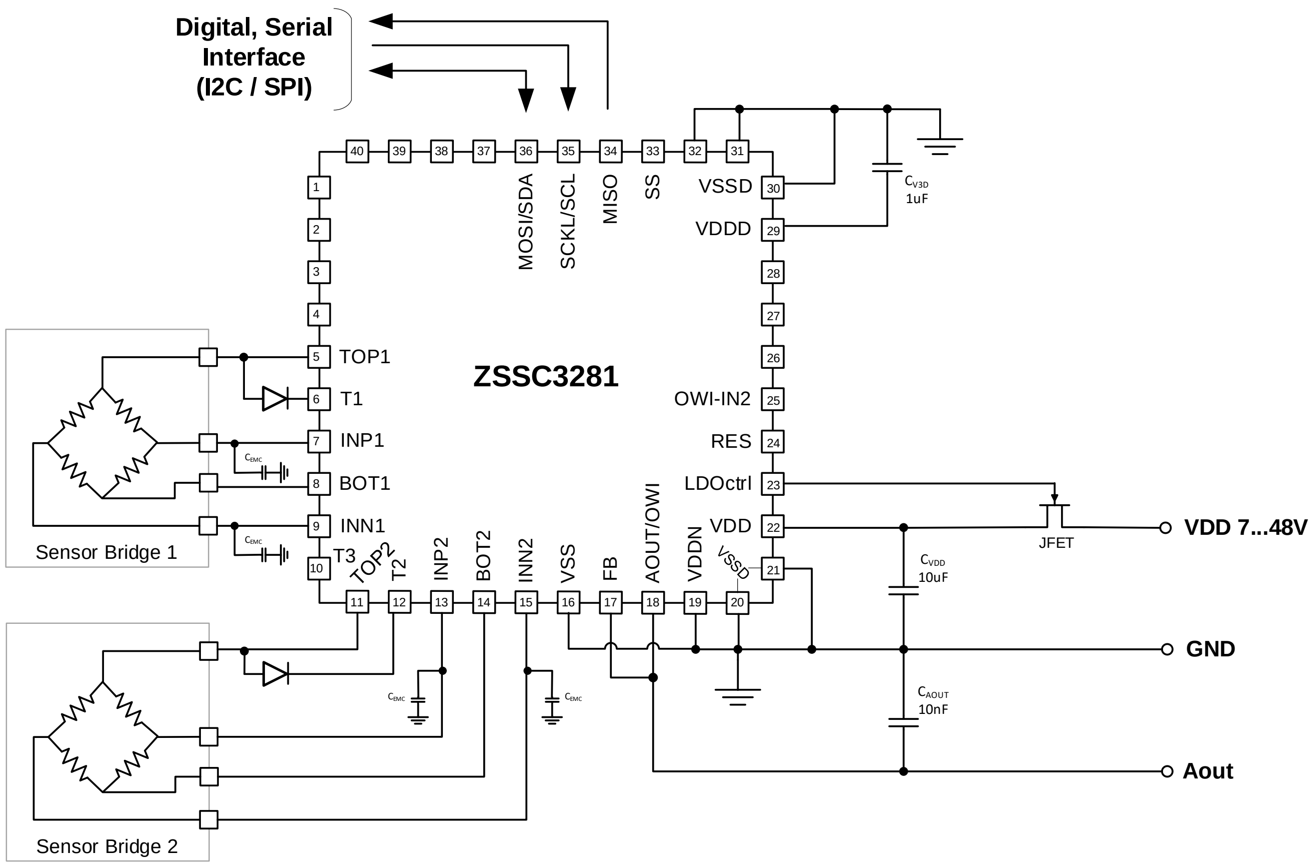
Bits	Field Name	Default	Description
7:0	MajorVer	0x0	CCP Major Version
15:8	MinorVer	0x0	CCP Minor Version
23:16	PatchVer	0x0	CCP Patch Version

14. Application Information

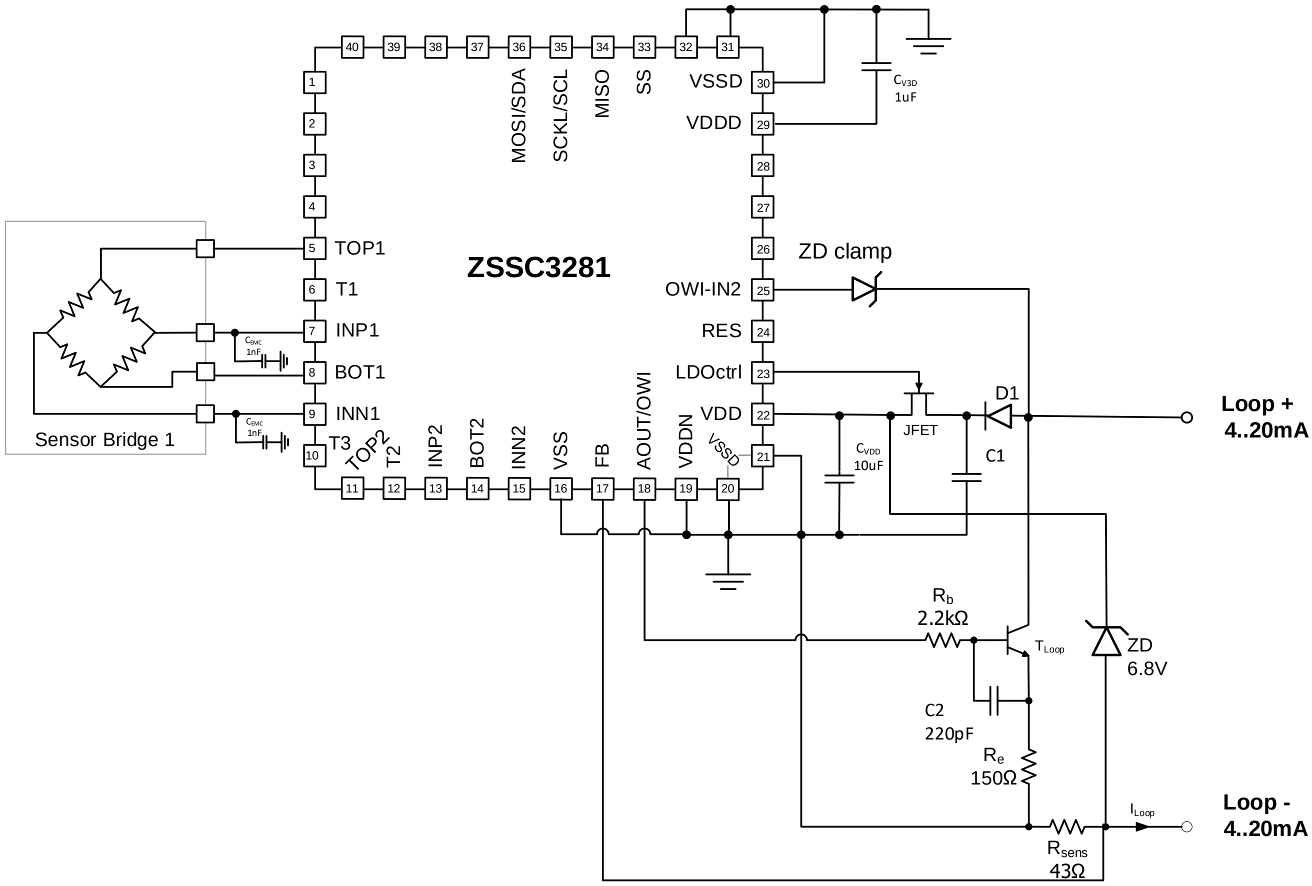
14.1 2-Bridge Application 1.8V to 5.5V Supply



14.2 2-Bridge Application 7V to 48V Supply



14.3 2-Wire Current Loop Application



15. Glossary

Term	Description
A2D	Analog to Digital
ADC	Analog to Digital Converter
AFE	Analog Front End
ARM	Provider of micro controller core
AUX	Auxiliary measurement, in addition to main sensor bridge measurement
AZ	Auto Zero
BOT	Bottom
CCP	Configuration and Calibration Page
CPU	Central Processing Unit
DAC	Digital to Analog Converter
DMA	Direct Memory Access
EMI	Electromagnetic Interference
EOC	End of Conversion signal
ESD	Electrostatic Discharge
FB	Feedback input for analog output buffer
FOUT	Frequency Output
I2C	Inter Integrated Circuit communication protocol
I3C	High speed communication protocol, extension of I2C standard
IFB	Interface Bridge – DMA Controller for serial interfaces
JFET	Junction Field Effect Transistor
LDR	Lower Diagnostic Range
LSB	Least Significant Bit
M3	Name of used micro controller core, full name is ARM Cortex M3
MCU	Micro Controller Unit
MIPI	Collaborative global organization serving industries that develop mobile and mobile-influenced devices.
MISO	Master-In Slave-Out
MOSI	Master-Out Slave-In
MSB	Most Significant Bit
NMOS	N-channel Metall Oxid Transistor
OWI	One Wire Interface
PGA	Programmable Gain Amplifier
PMW	Pulse Width Modulation
POR	Power On Reset
PTAT	Proportional to absolute temperature current source
RAM	Random Access Memory
RTD	Temperature dependent resistor
SDR	Single Data Rate
SM-	Main Sensor Measurement, inverted signal polarity
SM+	Main Sensor Measurement, standard (non-inverted) signal polarity
SOT	Second Order Term
SPI	Serial Peripheral Interface
SS	Slave Select
TLC	Third Logic Channel

UDR	Upper Diagnostic Range

16. Revision History

Revision	Date	Description
1.0	Jun.13.22	Initial release

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