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MDT0280A4IS-MULTI	240 x 320	Multi Interface	TFT Module

Specification

Version: 1	Date: 14/04/2019

Revision

1	11/04/2019	First issue

Display Features	
Display Size	2.8”
Resolution	240 x 320
Orientation	Portrait
Appearance	RGB
Logic Voltage	2.8V
Interface	Multi
Brightness	350 cd/m^2
Touchscreen	---
Module Size	50.20 x 69.20 x 2.75 mm
Operating Temperature	-20°C ~ +60°C
Pinout	50 way FFC
Pitch	0.50 mm

RoHS compliant

Box Quantity	Weight / Display
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* - For full design functionality, please use this specification in conjunction with the ILI9340X specification.(Provided Separately)

Display Accessories	
Part Number	**Description**

Optional Variants	
Appearances	**Voltage**

General Specifications

Feature		Spec
Characteristics	Size	2.8inch
	Resolution	240(horizontal)*320(Vertical)
	Interface	MCU-18/16/9/8 Bit RGB-18/16/6 Bit SPI 3-Line&4-Line
	Connect type	Connector
	Color Depth	262k
	Technology type	a-Si
	Display Spec. Pixel pitch (mm)	0.18 x 0.18
	Pixel Configuration	R.G.B. Vertical Stripe
	Display Mode	Normally Black
	Driver IC	ILI9340X
	Viewing Direction	Full view
Mechanical	LCM (W x H x D) (mm)	50.2*69.2*2.75
	Active Area(mm)	43.2*57.6
	Weight (g)	TBD
	LED Numbers	4 LEDs

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Note 1: RoHS
Note 2: LCM weight tolerance: +/- 5%

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Input/Output Terminals

<table>
<tr><th>No.</th><th>Symbol</th><th>Description</th></tr>
<tr><td>1</td><td>LEDK</td><td>LED Cathode K</td></tr>
<tr><td>2</td><td>LEDA1</td><td>LED Anode A1</td></tr>
<tr><td>3</td><td>LEDA2</td><td>LED Anode A2</td></tr>
<tr><td>4</td><td>LEDA3</td><td>LED Anode A3</td></tr>
<tr><td>5</td><td>LEDA4</td><td>LED Anode A4</td></tr>
<tr><td>6</td><td>IM0</td><td rowspan="4">
<table>
<tr><th rowspan="2">IM3</th><th rowspan="2">IM2</th><th rowspan="2">IM1</th><th rowspan="2">IM0</th><th rowspan="2">MCU-Interface Mode</th><th colspan="2">Pins in use</th></tr>
<tr><th>Register/Content</th><th>GRAM</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>8080 MCU 8-bit bus interface I</td><td>D[7:0]</td><td>D[7:0],WRX,RDX,CSX,D/CX</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>8080 MCU 16-bit bus interface I</td><td>D[7:0]</td><td>D[15:0],WRX,RDX,CSX,D/CX</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>8080 MCU 9-bit bus interface I</td><td>D[7:0]</td><td>D[8:0],WRX,RDX,CSX,D/CX</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>8080 MCU 18-bit bus interface I</td><td>D[7:0]</td><td>D[17:0],WRX,RDX,CSX,D/CX</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>3-wire 9-bit data serial interface I</td><td colspan="2">SCL,SDA,CSX</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>4-wire 8-bit data serial interface I</td><td colspan="2">SCL,SDA,D/CX,CSX</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>8080 MCU 16-bit bus interface II</td><td>D[8:1]</td><td>D[17:10],D[8:1],WRX,RDX,CSX,D/CX</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>8080 MCU 8-bit bus interface II</td><td>D[17:10]</td><td>D[17:10],WRX,RDX,CSX,D/CX</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>8080 MCU 18-bit bus interface II</td><td>D[8:1]</td><td>D[17:0],WRX,RDX,CSX,D/CX</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>8080 MCU 9-bit bus interface II</td><td>D[17:10]</td><td>D[17:9],WRX,RDX,CSX,D/CX</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>3-wire 9-bit data serial interface II</td><td colspan="2">SCL,SDI,SDO, CSX</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>4-wire 8-bit data serial interface II</td><td colspan="2">SCL,SDI,D/CX,SDO, CSX</td></tr>
</table>
</td></tr>
<tr><td>7</td><td>IM1</td></tr>
<tr><td>8</td><td>IM2</td></tr>
<tr><td>9</td><td>IM3</td></tr>
<tr><td>10</td><td>RESET</td><td>Reset signal pin</td></tr>
<tr><td>11</td><td>VSYNC</td><td>Frame Synchronous Signal</td></tr>
<tr><td>12</td><td>HSYNC</td><td>Line Synchronous Signal</td></tr>
<tr><td>13</td><td>DOTCLK</td><td>Dot-clock signal and oscillator source</td></tr>
<tr><td>14</td><td>DE</td><td>Display enable signal</td></tr>
<tr><td>15~32</td><td>DB17~ DB0</td><td>Data bus DB17~ DB0</td></tr>
<tr><td>33</td><td>SDO</td><td>Serial output signal</td></tr>
<tr><td>34</td><td>SDI</td><td>Serial input signal</td></tr>
<tr><td>35</td><td>RD</td><td>Read signal pin</td></tr>
<tr><td>36</td><td>WRX/DCX</td><td>8080-I system :Write signal
Serial interface: Data or command select.</td></tr>
<tr><td>37</td><td>DCX/SCL</td><td>8081-I system :Data or command select.
Serial interface:Serial clock signal.</td></tr>
<tr><td>38</td><td>CSX</td><td>Chip select pin</td></tr>
<tr><td>39</td><td>TE</td><td>FMARK</td></tr>
<tr><td>40</td><td>VDDI</td><td rowspan="2">Interface I/O Power supply (1.65~3.3V)</td></tr>
<tr><td>41</td><td>VDDI</td></tr>
<tr><td>42</td><td>VCI</td><td>Power supply of the System(2.8V)</td></tr>
<tr><td>43</td><td>GND</td><td>Power Ground</td></tr>
<tr><td>44</td><td>X+/XR(NC)</td><td>No connection</td></tr>
</table>

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45	Y+/YD(NC)	No connection
46	X-/XL(NC)	No connection
47	Y-/YU(NC)	No connection
48	GND	Power Ground
49	GND	Power Ground
50	GND	Power Ground

Absolute Maximum Ratings

Driving TFT LCD Panel

Item	Symbol	MIN	MAX	Unit	Remark
Supply Voltage	V_{CC}	-0.3	4.6	V	
Operating Temperature	T_{OPR}	-20	60	℃	
Storage Temperature	T_{STG}	-30	70	℃	

Electrical Characteristics

Driving TFT LCD Panel

Ta = 25 °C

Item		Symbol	MIN	TYP	MAX	Unit	Remark
Digital Supply Voltage		V_{CC}	2.5	2.8	3.3	V	
Operating Current		I_{VCC}	-	8.0	-	mA	
Sleeping Current		I_{ST}	-	200	-	uA	
Input Signal Voltage	Low Leve	V_{IL}	-0.3	-	0.2x IOVCC	V	
	High Level	V_{IH}	0.8x IOVCC	-	IOVCC	V	
TFT Common Electrode		V_{COMH}	3	5	5	V	
TFT Gata ON Voltage		V_{GH}	10	-	16	V	
TFT Gata ON Voltage		V_{GL}	-10	-	-5	V	

Driving Backlight

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Forward Current	I_F	-	80	-	mA	Constant current
Forward Voltage	V_F	3	3.2	3.4	V	
Backlight Power consumption	W_{BL}	-	0.256	-	W	

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LED Lifetime		-	25000	-	Hrs	

Note : Each LED : IF =20 mA, VF =3.2V.
Note 2: Optical performance should be evaluated at Ta=25℃ only.
Note 3: If LED is driven by high current, high ambient temperature & humidity condition. The life time of LED will be reduced.Operating life means brightness goes down to 50% initial brightness. Typical operating life time is estimated data.

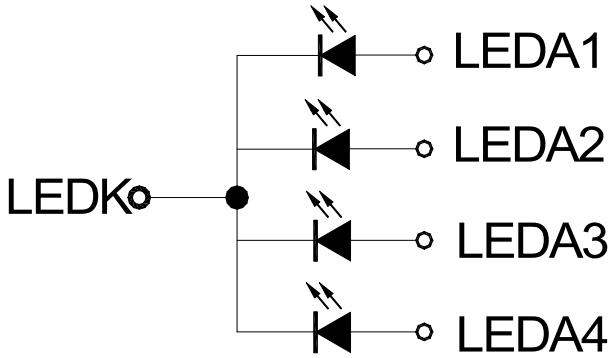
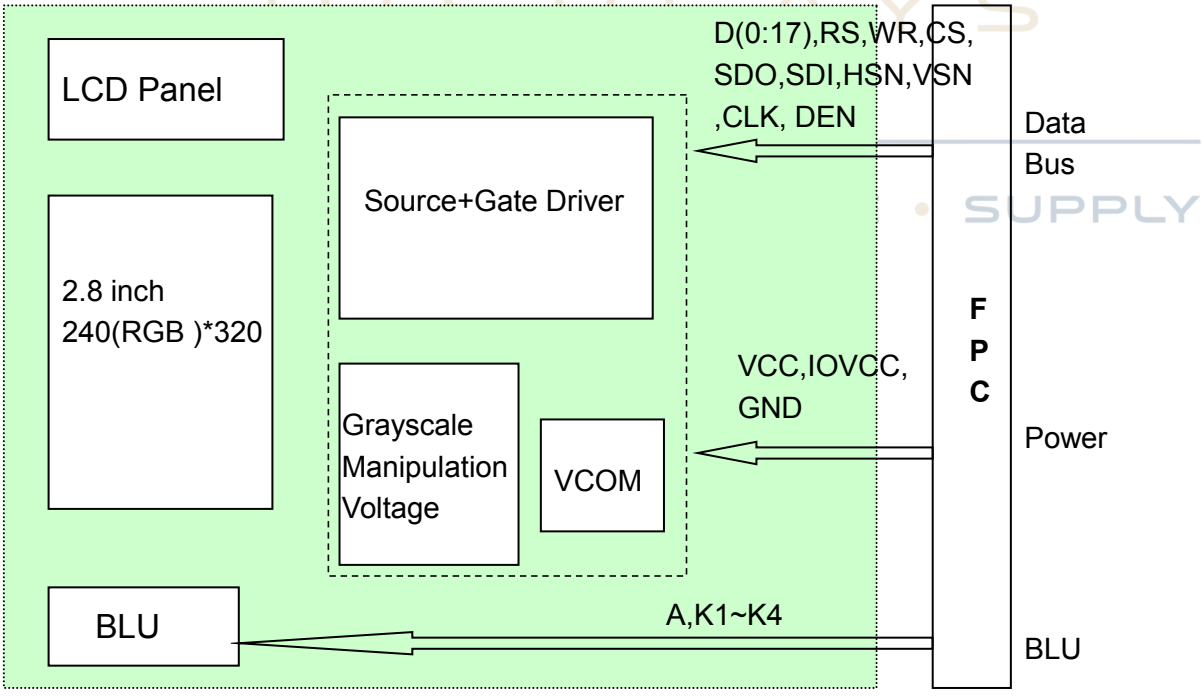


Figure : LED connection of backlight

Block Diagram

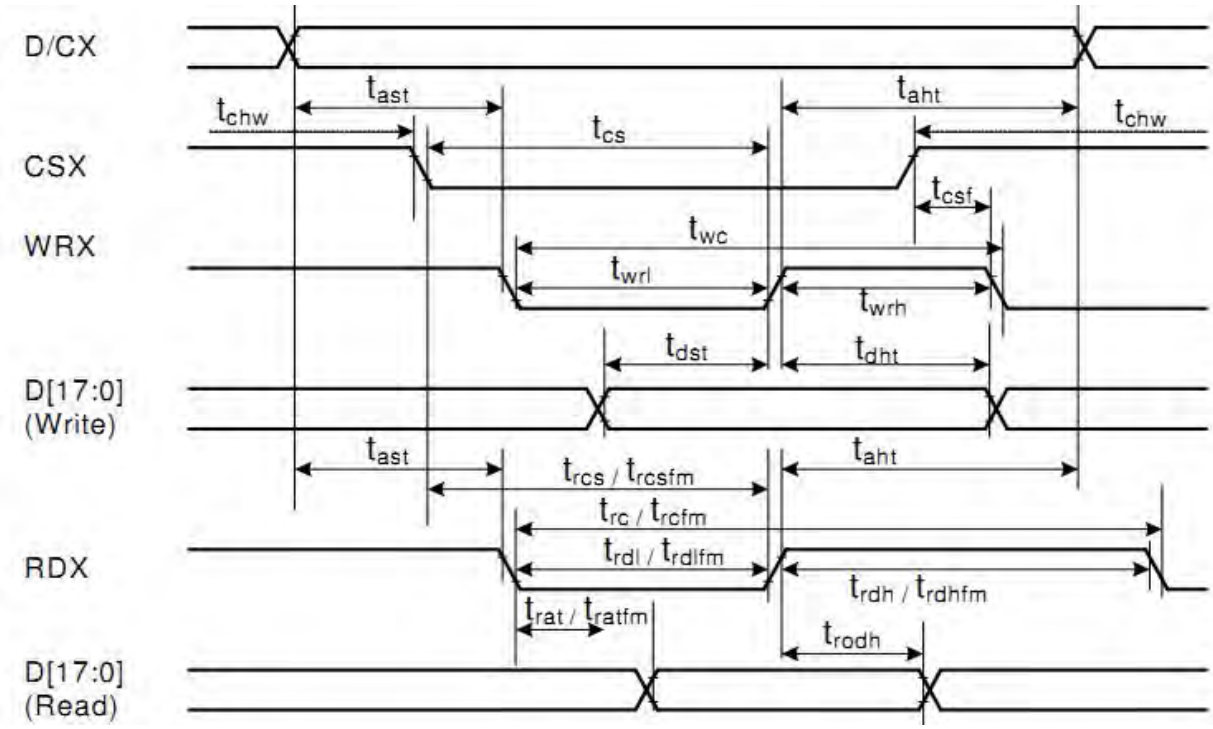


MIDAS DISPLAYS
SUPPLY

Interface Timing

Timing Parameter

Parallel 18/16/9/8 bit interface timing(8080-II system)



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Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time (Write/Read)	0	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
D[17:0], D[17:10]&D[8:1], D[17:10], D[17:9]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Note: Ta = -30 to 70 ℃, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, VSS=0V.

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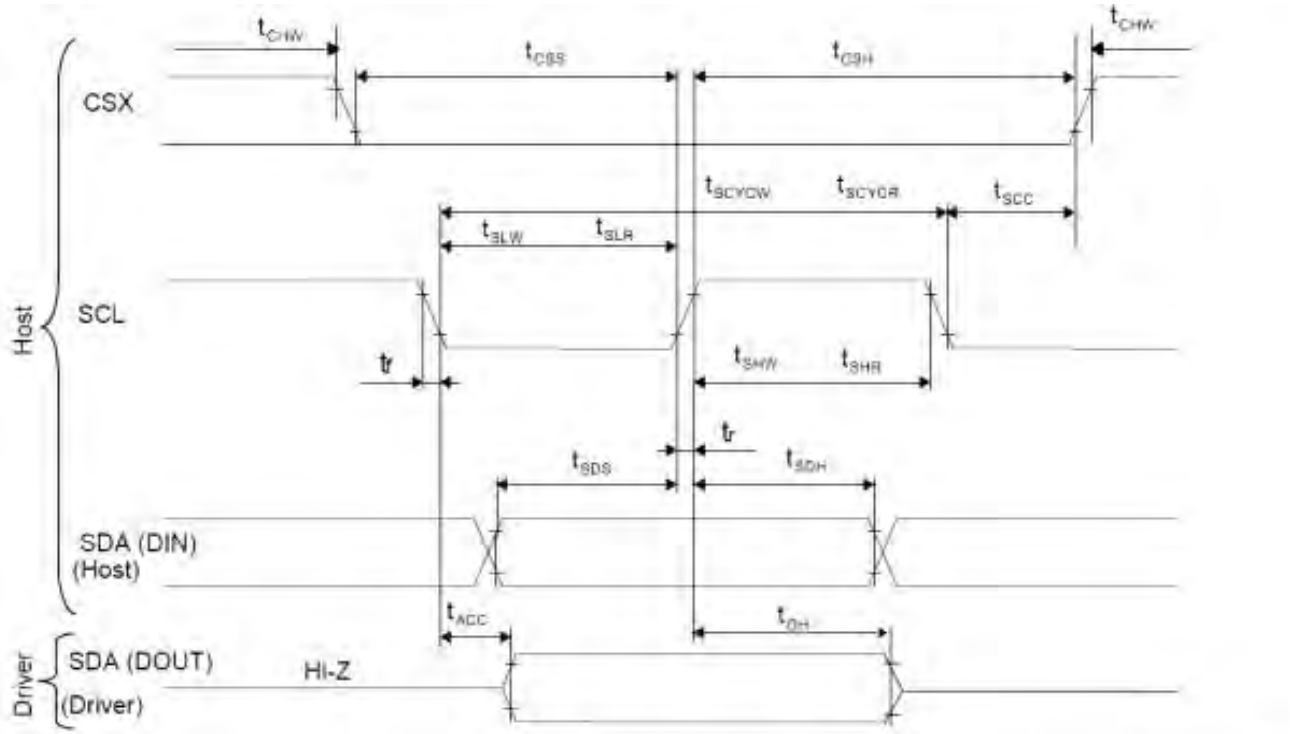
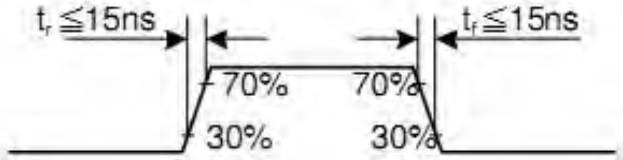
Serial interface timing characteristics (3-line SPI system)

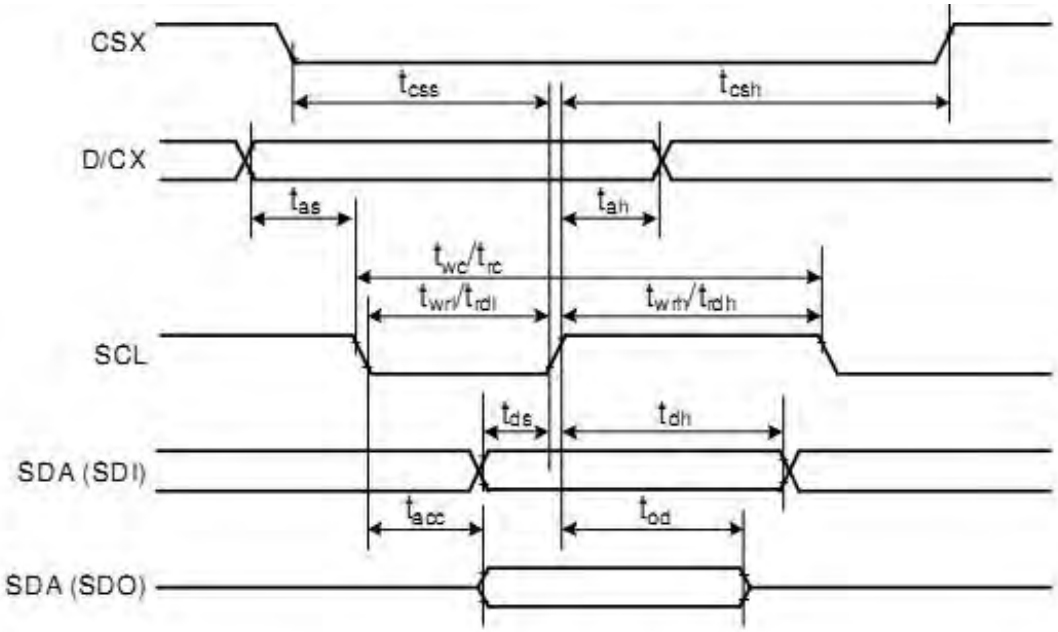


Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	100	-	ns	
	tshw	SCL "H" Pulse Width (Write)	40	-	ns	
	tslw	SCL "L" Pulse Width (Write)	40	-	ns	
	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL "H" Pulse Width (Read)	60	-	ns	
	tslr	SCL "L" Pulse Width (Read)	60	-	ns	
SDA / SDI (Input)	tsds	Data setup time (Write)	30	-	ns	
	tsdh	Data hold time (Write)	30	-	ns	
SDA / SDO (Output)	tacc	Access time (Read)	10	-	ns	
	toh	Output disable time (Read)	10	50	ns	
CSX	tscc	SCL-CSX	20	-	ns	
	tchw	CSX "H" Pulse Width	40	-	ns	
	tcss	CSX-SCL Time	60	-	ns	
	tcsh		65	-	ns	

Note: Ta = 25 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V

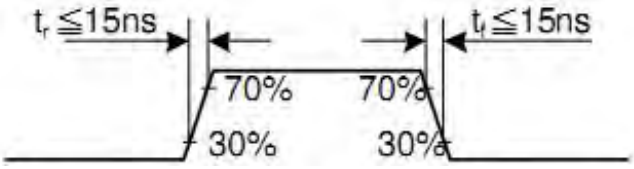


Serial interface timing characteristics (4-line SPI system)

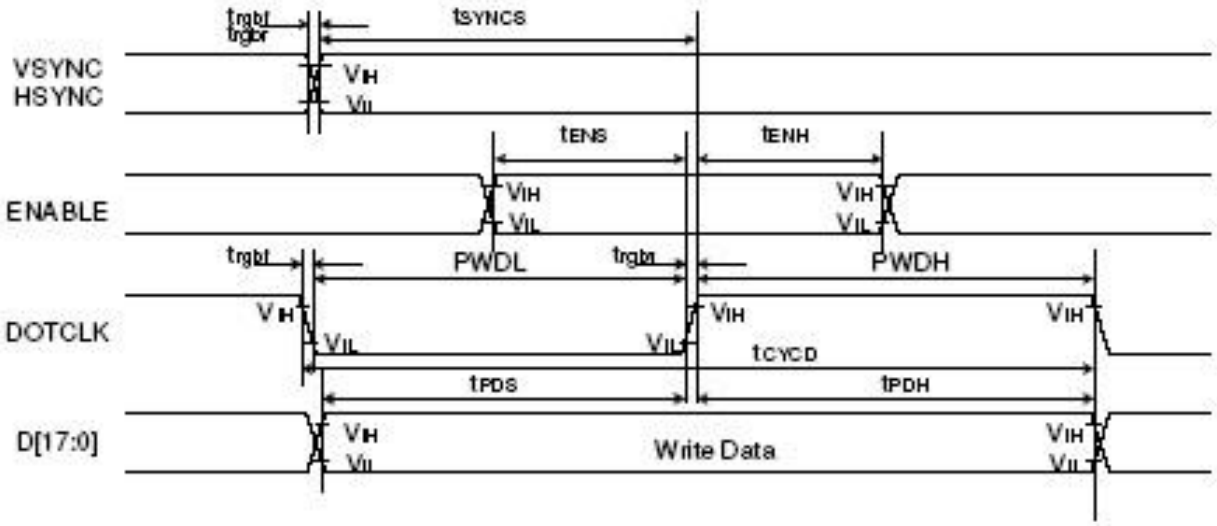


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	40	-	ns	
	tcsh	Chip select hold time (Read)	40	-	ns	
SCL	twc	Serial clock cycle (Write)	100	-	ns	
	twrh	SCL "H" pulse width (Write)	40	-	ns	
	twrl	SCL "L" pulse width (Write)	40	-	ns	
	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL "H" pulse width (Read)	60	-	ns	
	trdl	SCL "L" pulse width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	-		
	tah	D/CX hold time (Write / Read)	10	-		
SDA / SDI (Input)	tds	Data setup time (Write)	30	-	ns	
	tdh	Data hold time (Write)	30	-	ns	
SDA / SDO (Output)	tacc	Access time (Read)	10	-	ns	For maximum CL=30pF
	tod	Output disable time (Read)	10	50	ns	For minimum CL=8pF

Note: Ta = 25 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V

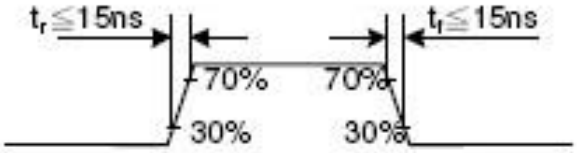


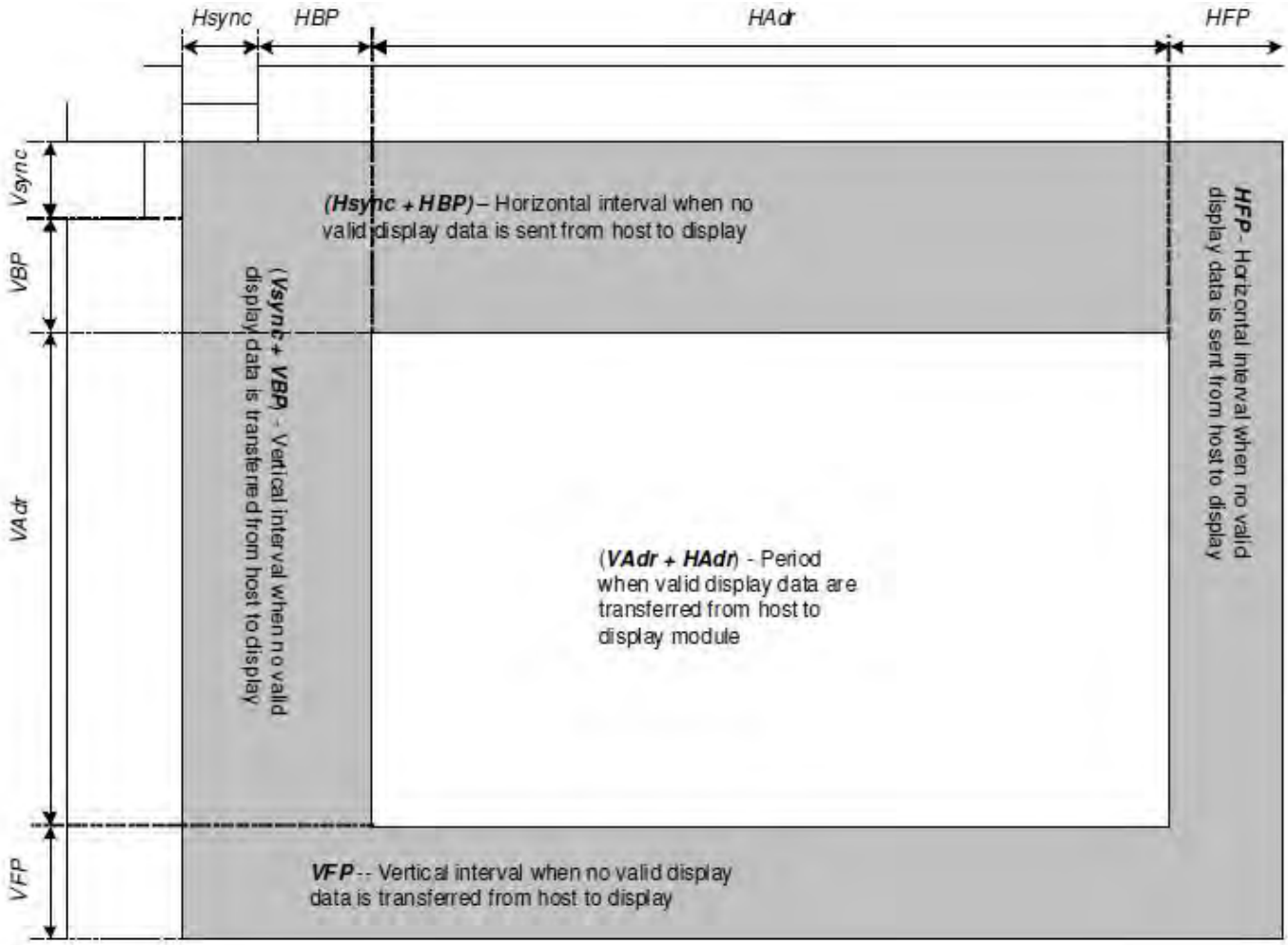
Parallel 18/16/9/8 bit RGB interface timing



Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
D[17:0]	t_{PDS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	15	-	ns	
	PWDL	DOTCLK low-level period	15	-	ns	
	t_{CYCD}	DOTCLK cycle time	100	-	ns	
	t_{rgbr}, t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	6-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
D[17:0]	t_{PDS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level pulse period	15	-	ns	
	PWDL	DOTCLK low-level pulse period	15	-	ns	
	t_{CYCD}	DOTCLK cycle time	100	-	ns	
	t_{rgbr}, t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V

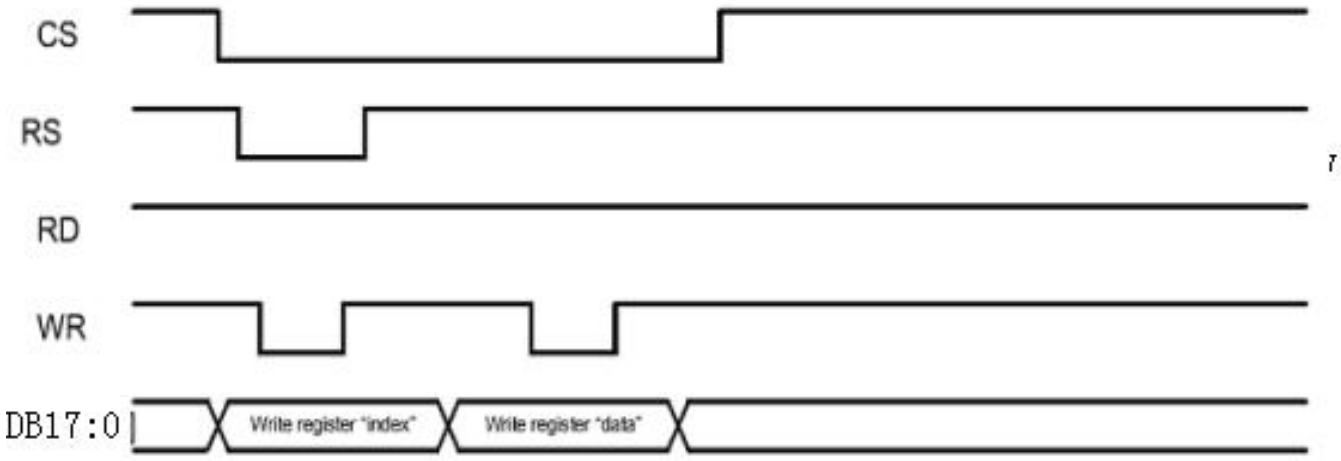




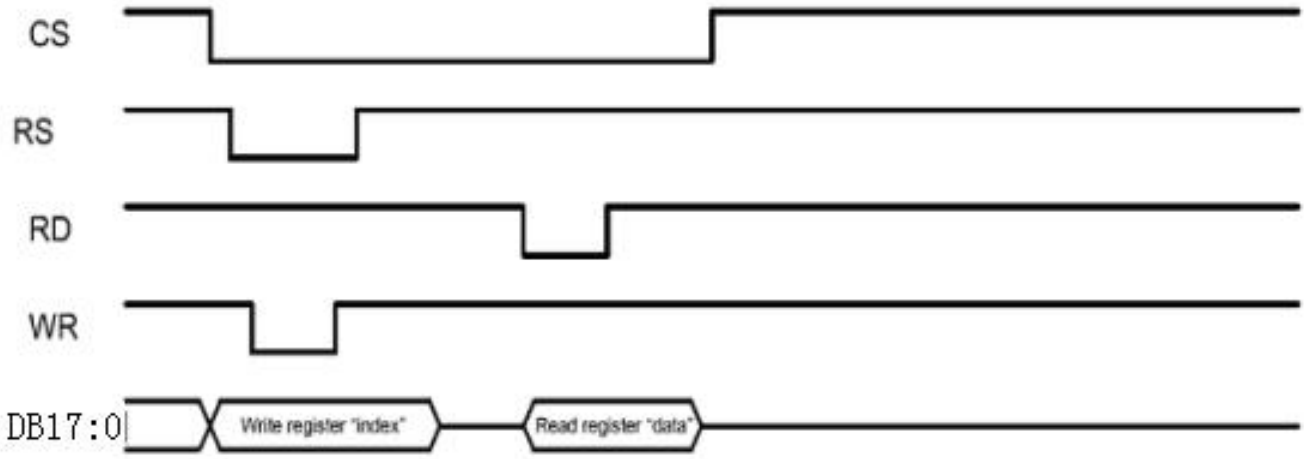
Parameters	Symbols	Condition	Min.	Typ.	Max.	Units
Horizontal Synchronization	Hsync		2	10	16	DOTCLK
Horizontal Back Porch	HBP		2	20	24	DOTCLK
Horizontal Address	HAdr		-	240	-	DOTCLK
Horizontal Front Porch	HFP		2	10	16	DOTCLK
Vertical Synchronization	Vsync		1	2	4	Line
Vertical Back Porch	VBP		1	2	-	Line
Vertical Address	VAdr		-	320	-	Line
Vertical Front Porch	VFP		3	4	-	Line

Register Wite/Read Timing

(a) Write to register

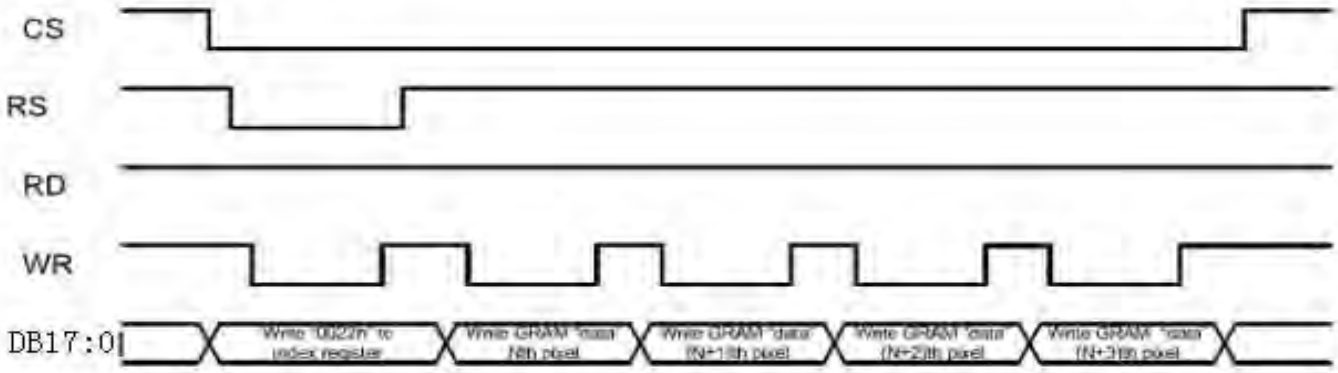


(b) Read from register

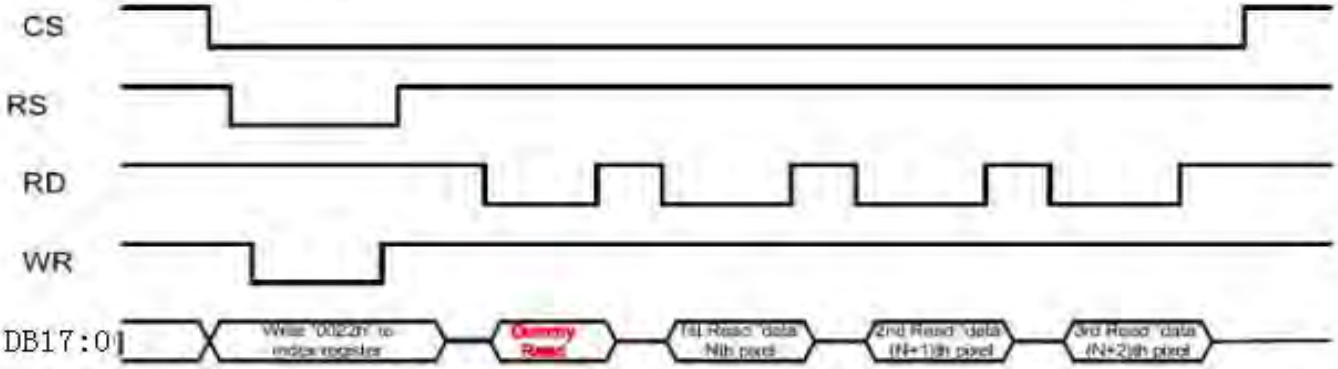


GRAM Wite/Read Timing

(a) Write to GRAM



(b) Read from GRAM



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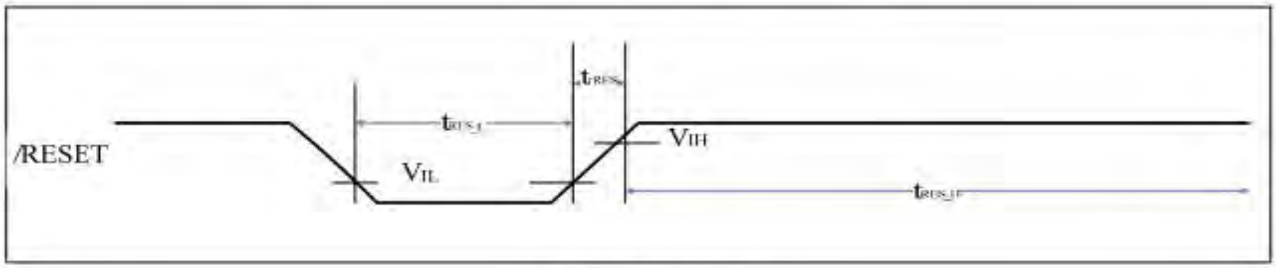
Reset Timing Characteristics

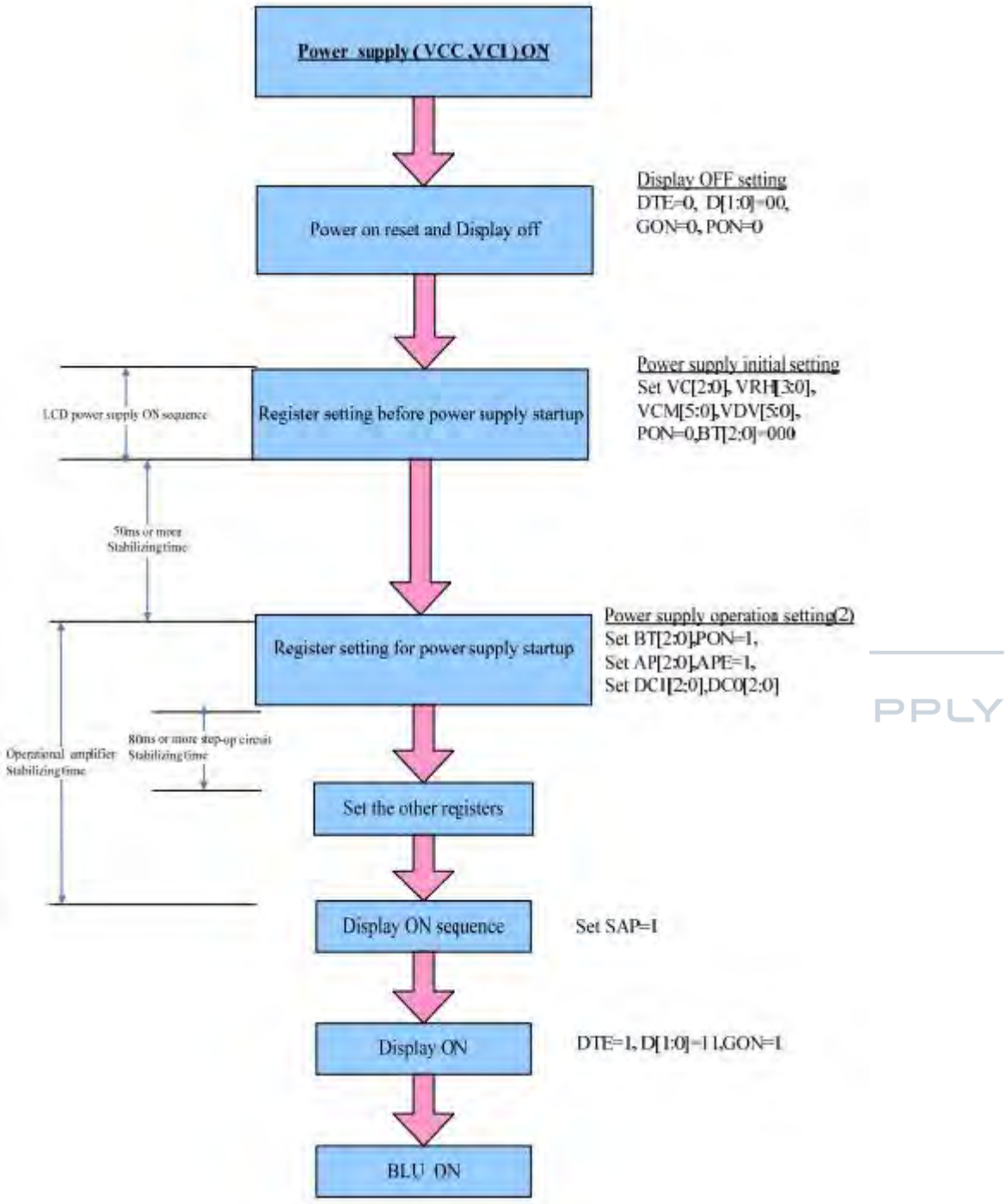
Item	Symbol	Unit	Min.	Typ.	Max.
Reset low-level width	$t_{RES\,L}$	ms	1	-	-
Reset rise time	t_{rRES}	µs	-	-	10
Reset high-level width	$t_{RES\,H}$	ms	50		



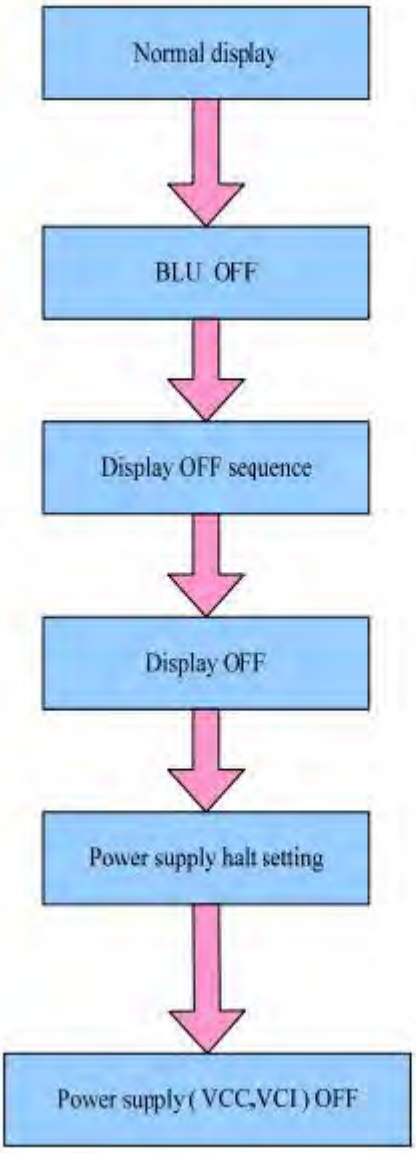
Reset timing

Power On/Off Sequence

Power On Sequence



Power Off Sequence



Display ON setting
DTE=1,
D[1:0]=11,GON=1

SAP[2:0]=000,
AP[2:0]=000, PON=0

Optical Characteristics

Items		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing angles		θ_T	Center CR≥10	-	80	-	Degree.	Note2
		θ_B		-	80	-		
		θ_L		-	80	-		
		θ_R		-	80	-		
Contrast Ratio		CR	Θ =0	400	500	-	-	Note1, Note3
Surface luminance		LV	θ =0°	300	350	-	cd/m2	**Note2**
Response Time		T_{ON}	25° C	-	30	40	ms	Note1, Note4
		T_{OFF}		-	30	40		
Chromaticity	White	X_W	Backlight is on	TBD	TBD	TBD	-	Note1, Note5
		Y_W		TBD	TBD	TBD	-	
	Red	X_R		TBD	TBD	TBD	-	
		Y_R		TBD	TBD	TBD	-	
	Green	X_G		TBD	TBD	TBD	-	
		Y_G		TBD	TBD	TBD	-	
	Blue	X_B		TBD	TBD	TBD	-	
		Y_B		TBD	TBD	TBD	-	
Uniformity		U		75	80	-	%	Note1, Note6
NTSC					65		%	Note5
Luminance		L		310	360	400		Note1, Note7

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Test Conditions:

1. IF= 20mA(one channel),the ambient temperature is 25
2. The test systems refer to Note 1 and Note 2.

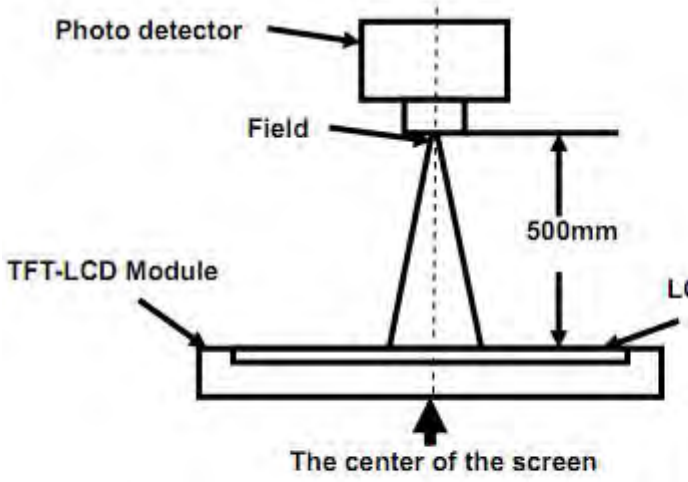
Note2. Definition of surface luminance.

Surface luminance is the luminance with all pixels displaying white. For more information see

Lv = Average Surface Luminance with all white pixels(P1,P2,P3, ...,Pn)

Note 1:Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 5 minutes operation, the optical properties are measured at the center point of the LCD screen. All input terminals LCD panel must be ground when measuring the center area of the panel.



Item	Photo detector	Field
Contrast Ratio	SR-3A	1°
Luminance		
Chromaticity		
Lum Uniformity		
Response Time	BM-7A	2°

DISPLAYS

Note 2: Definition of viewing angle range and measurement system.
viewing angle is measured at the center point of the LCD by CONOSCOPE(ergo-80).

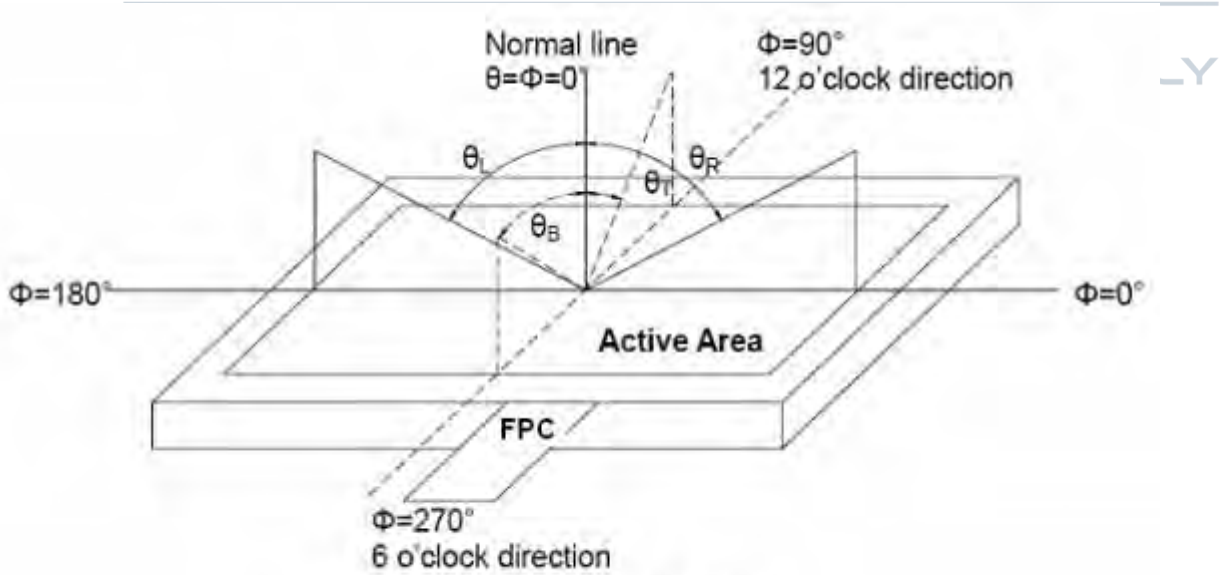


Fig. 1 Definition of viewing angle

Note 3: Definition of contrast ratio

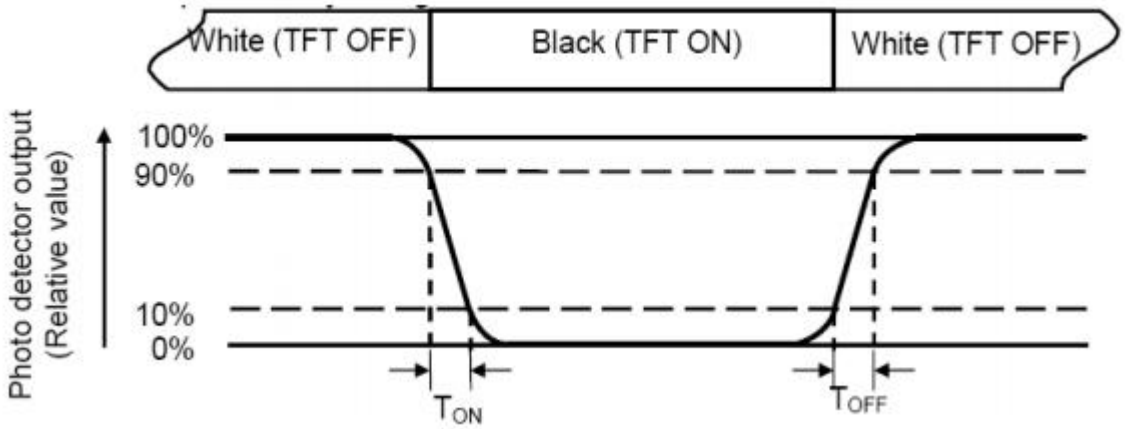
$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD is on the "White" state}}{\text{Luminance measured when LCD is on the "Black" state}}$$

“White state “:The state is that the LCD should driven by Vwhite.

“Black state”: The state is that the LCD should driven by Vblack.

Vwhite: To be determined Vblack: To be determined.

Note 4: Definition of Response time
The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time (TON) is the time between photo detector output intensity changed from 90% to 10%. And fall time (TOFF) is the time between photo detector output intensity changed from 10% to 90%.



Note 5: Definition of color chromaticity (CIE1931)
Color coordinates measured at center point of LCD.

Note 6: Definition of Luminance Uniformity
Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

Luminance Uniformity(U) = Lmin/ Lmax

L-------Active area length W----- Active area width

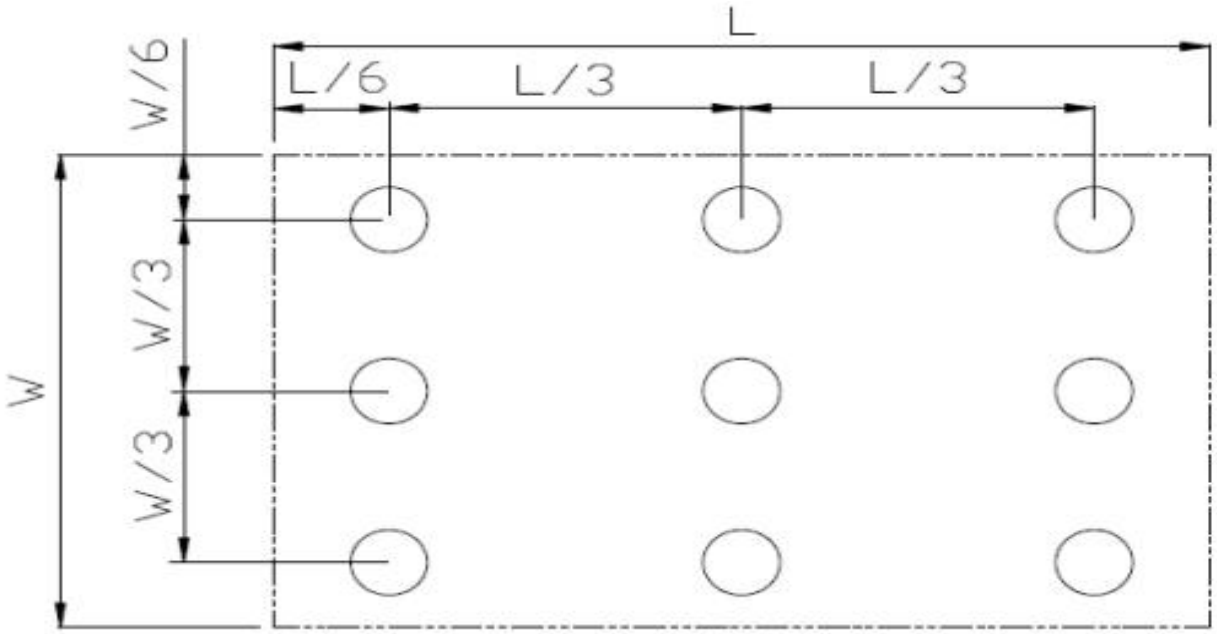


Fig. 2 Definition of uniformity

Lmax: The measured maximum luminance of all measurement position.
Lmin: The measured minimum luminance of all measurement position.

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Note 7: Definition of Luminance :
Measure the luminance of state at point.

Environmental / Reliability Tests

No	Test Item	Condition	Remarks
1	High Temperature Operation	Ts= +60℃, 120hrs	Note 1 IEC60068-2-2, GB2423. 2-89
2	Low Temperature Operation	Ta= -20℃, 120hrs	Note 2 IEC60068-2-1 GB2423.1-89
3	High Temperature Storage	Ta= +70℃, 240hrs	IEC60068-2-2 GB2423. 2-89
4	Low Temperature Storage	Ta= -30℃, 240hrs	IEC60068-2-1 GB/T2423.1-89
5	High Temperature & Humidity Storage	Ta= +60℃, 90% RH max, 160 hours	IEC60068-2-3 GB/T2423.3-2006
6	Thermal Shock (Non-operation)	-30℃ 30 min ~ +80℃ 30 min Change time: 5min, 30 Cycle	Start with cold temperature,end with high temperature IEC60068-2-14, GB2423.22-87
7	Electro Static Discharge (Opeartion)	C=150pF, R=330 Ω, 5 points/panel Air:±8KV, 5 times; Contact: ±4KV, 5 times; (Environment: 15℃ ~ 35℃, 30% ~ 60%, 86Kpa ~ 106Kpa)	IEC61000-4-2 GB/T17626.2-1998
8	Vibration (Non-operation)	Frequency range: 10~55Hz, Stroke: 1.mm Sweep: 10Hz~55Hz~10Hz 2 hours for each direction of X .Y. Z. (package condition)	IEC60068-2-6 GB/T2423.5-1995
9	Shock (Non-operation)	60G 6ms, ± X, ±Y, ± Z 3 times for each direction	IEC60068-2-27 GB/T2423.5-1995
10	Package Drop Test	Height: 80 cm, 1 corner, 3 edges, 6 surfaces	IEC60068-2-32 GB/T2423.8-1995

Note: 1. T_S is the temperature of panel's surface.
2. Ta is the ambient temperature of sample.

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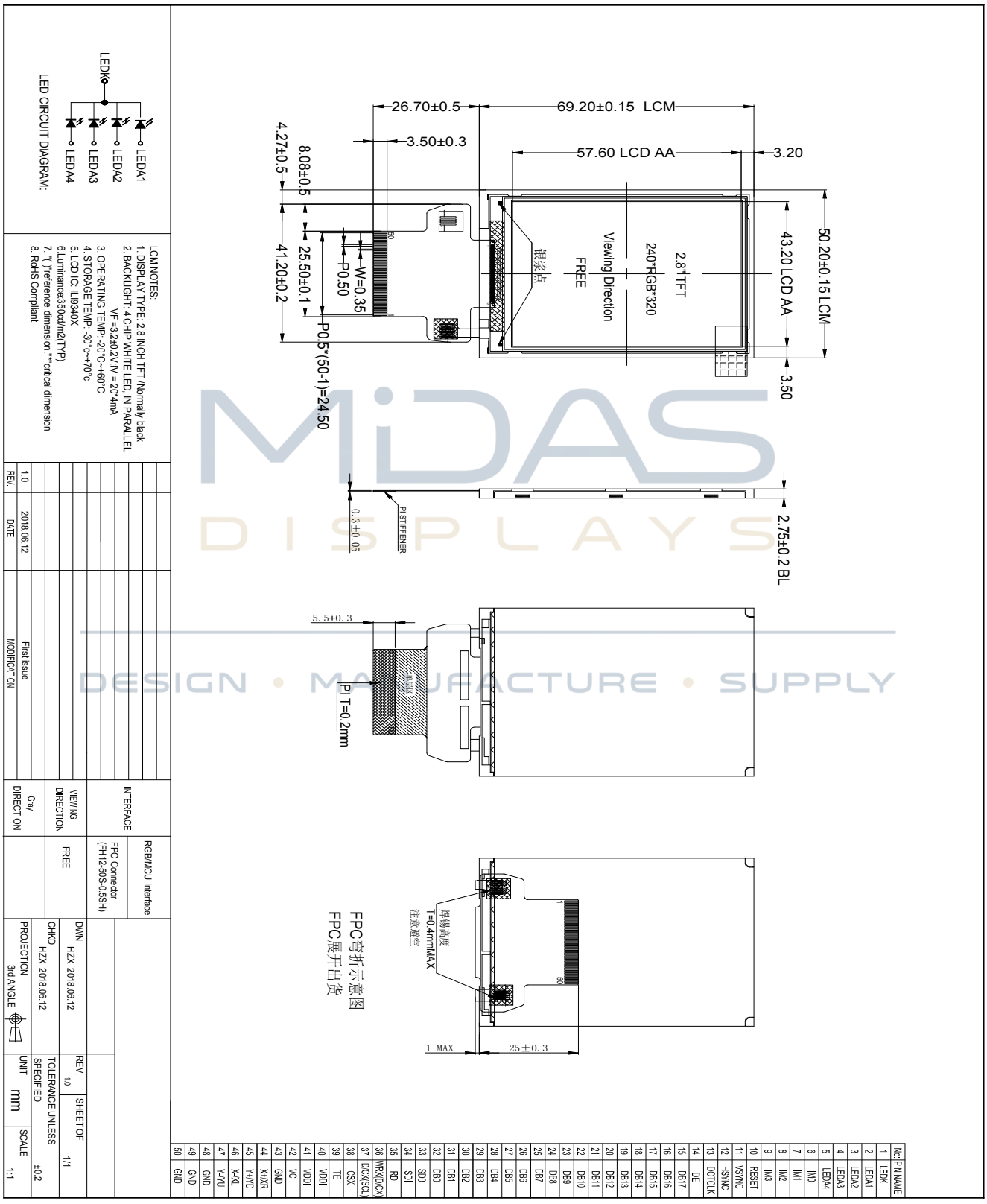
Mechanical Drawing



No.	PIN NAME
1	LEDK
2	LEDA1
3	LEDA2
4	LEDA3
5	LEDA4
6	IM0
7	IM1
8	IM2
9	IM3
10	RESET
11	VSYNC
12	HSYNC
13	DOTCLK
14	DE
15	DB17
16	DB16
17	DB15
18	DB14
19	DB13
20	DB12
21	DB11
22	DB10
23	DB9
24	DB8
25	DB7
26	DB6
27	DB5
28	DB4
29	DB3
30	DB2
31	DB1
32	DB0
33	SDO
34	SDI
35	RD
36	WRX/D/CX
37	DCX/SCL
38	CSX
39	TE
40	VDDI
41	VDDI
42	VCI
43	GND
44	X+/XR
45	Y+/YD
46	X-/XL
47	Y-/YU
48	GND
49	GND
50	GND

Precautions For Use of LCD modules

Handling Precautions

1.1. The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

1.2. If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

1.3. Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

1.4. The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

1.5. If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketone
- Aromatic solvents

1.6. Do not attempt to disassemble the LCD Module.

1.7. If the logic circuit power is off, do not apply the input signals.

1.8. To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

1.8.1. Be sure to ground the body when handling the LCD Modules.

1.8.2. Tools required for assembly, such as soldering irons, must be properly ground.

1.8.3. To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

1.8.4. The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

Storage Precautions

2.1. When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

2.2. The LCD modules should be stored under the storage temperature range If the LCD modules will be stored for a long time, the recommend condition is:

Temperature : 0℃ ～ 40℃ Relatively humidity: ≤80%

2.3. The LCD modules should be stored in the room without acid, alkali and harmful gas.

Inspection Sampling

3.1. Lot size : Quantity per shipment lot per model

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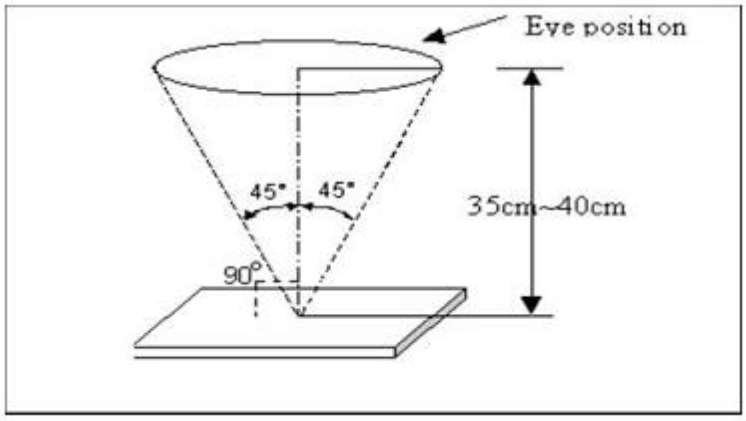
DESIGN • MANUFACTURE • SUPPLY

3.2. Sampling type: Normal inspection, Single sampling
3.3. Inspection level: II
3.4. Sampling table : MIL-STD-105D
3.5. Acceptable quality level （AQL ）
Major defect : AQL=0.65
Minor defect: AQL=1.00

Inspection Conditions

4.1 Ambient conditions:
a. Temperature: Room temperature 25±5℃
b. Humidity: (60±10) ％RH
c. Illumination: Single fluorescent lamp non-directive (300 to 700 Lux)
4.2 Viewing distance
The distance between the LCD and the inspector’ s eyes shall be at least 35±5 ㎝.
4.3 Viewing Angle
U/D: 45o/45o, L/R: 45o/45o



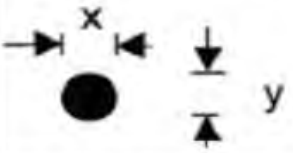
Inspection Criteria

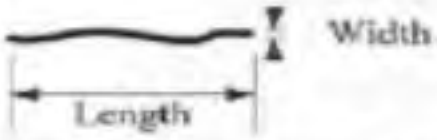
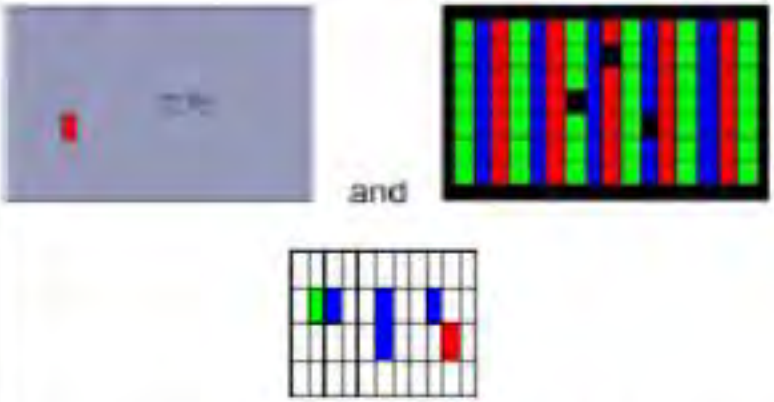
Defects are classified as major defects and minor defects according to the degree of defectiveness defined herein.

Major defect

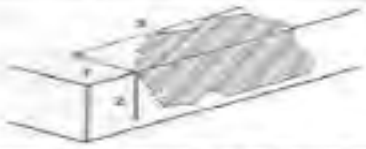
Item No	Items to be inspected	Inspection Standard
5.1.1	All functional defects	1) No display 2) Display abnormally 3) Short circuit 4) line defect
`5.1.2	Missing	Missing function component
5.1.3	Crack	Glass Crack

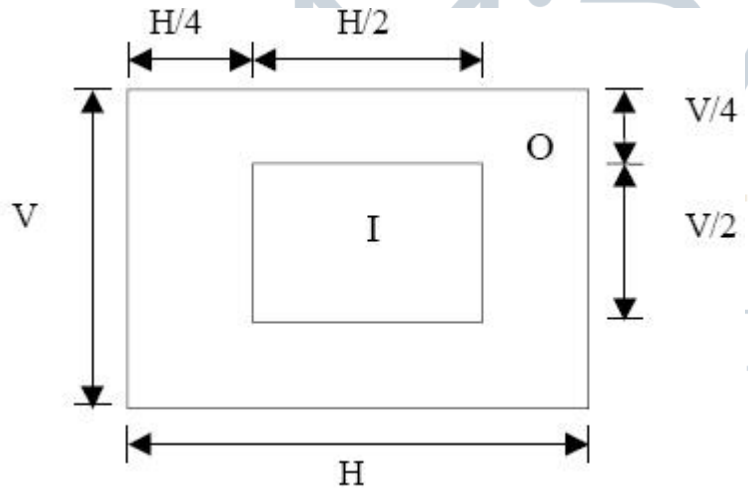
Minor defect

<table>
<tr><th>Item No</th><th>Items to be inspected</th><th colspan="2">Inspection standard</th></tr>
<tr><td rowspan="5">5.2.1</td><td rowspan="5">Spot Defect
Including
Black spot
White spot
Pinhole
Foreign particle</td><td colspan="2">For dark/white spot is defined
φ = (x+y) /2
  </td></tr>
<tr><td>Size φ(mm)</td><td>Acceptable Quantity</td></tr>
<tr><td>φ≤0.10</td><td>Ignore</td></tr>
<tr><td>0.10 < ϕ≤0.2</td><td>2</td></tr>
<tr><td>0.2 < ϕ</td><td>Not allowed</td></tr>
</table>

<table>
<tr><td>5.2.2</td><td>Polarizer dirt, particle</td><td>Size φ(mm)</td><td>Acceptable Quantity</td></tr>
<tr><td></td><td></td><td>φ≤0.15</td><td>1</td></tr>
<tr><td rowspan="5">5.2.3</td><td rowspan="5">Line Defect Including Black line White line Scratch</td><td colspan="2">Define:
 
</td></tr>
<tr><td>Width(mm)
Length(mm)</td><td>Acceptable Quantity</td></tr>
<tr><td>W≤0.05</td><td>Ignore</td></tr>
<tr><td>0.05 < W≤0.1
L≤1.5</td><td>2</td></tr>
<tr><td>0.1 < W, or L>1.5</td><td>Not allowed</td></tr>
<tr><td>5.2.4</td><td>Polarizer Dent/Bubble</td><td colspan="2">Not allowed</td></tr>
<tr><td rowspan="8">5.2.5</td><td rowspan="8">Electrical Dot Defect</td><td colspan="2">Bright and Black dot define:
 

Two Adjacent Dot</td></tr>
<tr><td colspan="2">Inspection pattern: Full white、Full black、Red、green and blue screens</td></tr>
<tr><td rowspan="2">Item</td><td colspan="3">Acceptable Quantity</td></tr>
<tr><td>I</td><td>O</td><td>Note</td></tr>
<tr><td>Black dot defect</td><td colspan="2">2</td><td rowspan="2">5mm≤Distance</td></tr>
<tr><td>Bright dot defect</td><td colspan="2">1</td></tr>
<tr><td>Two Adjacent Dot</td><td colspan="2">1</td><td></td></tr>
<tr><td>There or more Adjacent Dot</td><td colspan="3">Not allowed</td></tr>
<tr><td>Total Dot</td><td colspan="2">2</td><td></td></tr>
</table>

5.2.6	Glass defect	1.Corner Fragment: 	
		Size(mm)	Acceptable Quantity
		X≤2mm Y≤1mm Z≤T	Ignore T：Glass thickness X: Length Y: Width Z: thickness
		2. Side Fragment: 	
		Size(mm)	Acceptable Quantity
		X≤5.0mm Y ≤1mm Z≤T	T：Glass thickness X: Length Y: Width Z: thickness



Note: 1). Dot defect is defined as the defective area of the dot area is larger than 50% of the dot area.
2). The distance between two bright dot defects (red, green, blue, and white) should be larger than 15mm.
3). The distance between black dot defects or black and bright dot defects should be more than 5mm apart.
4). Polarizer bubble is defined as the bubble appears on active display area. The defect of polarizer bubble shall be ignored if the polarizer bubble appears on the outside of active display area.

Mechanics specification

As for the outside dimension of the modules, please refer to product specification for more details

Note: 1). Dot defect is defined as the defective area of the dot area is larger than 50% of the dot area.
2). The distance between two bright dot defects (red, green, blue, and white)

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