MOSFET - Power, Single N-Channel, SO8-FL

25 V, 0.68 mΩ, 365 A

NTMFS0D8N02P1E

Features

- Small Footprint (5x6mm) for Compact Design
- Low R_{DS(on)} to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- DC–DC Converters
- Power Load Switch
- Notebook Battery Management

MAXIMUM RATINGS (T_J = 25° C unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V _{DSS}	25	V
Gate-to-Source Voltage		V _{GS}	+16/ -12	V	
Continuous Drain		$T_{C} = 25^{\circ}C$	I _D	365	А
Current R _{θJC} (Note 1)	Steady	T _C =85°C		263	
Power Dissipation $R_{\theta JC}$ (Note 1)	State	T _C = 25°C	P _D	139	W
Continuous Drain		$T_A = 25^{\circ}C$	I _D	55	А
Current R _{θJA} (Notes 1, 3)	Steady	$T_A = 85^{\circ}C$		40	
Power Dissipation $R_{\theta JA}$ (Notes 1, 3)	State	$T_A = 25^{\circ}C$	PD	3.2	W
Continuous Drain		$T_A = 25^{\circ}C$	I _D	30	А
Current R _{θJA} (Notes 2, 3)	Steady	T _A = 85°C		21	
Power Dissipation $R_{\theta JA}$ (Notes 2, 3)	State	T _A = 25°C	PD	0.93	W
Pulsed Drain Current	$T_A = 25^{\circ}C, t_p = 10 \ \mu s$		I _{DM}	762	А
Single Pulse Drain-to-Source Avalanche Energy ($I_L = 115.4 A_{pk}, L = 0.1 mH$) (Note 4)			E _{AS}	666	mJ
Operating Junction and Storage Temperature Range		T _J , T _{STG}	–55 to +150	°C	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			ΤL	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted on FR4 board using 1 in² pad size, 2 oz Cu pad.

- 2. Surface-mounted on FR4 board using minimum pad size, 2 oz Cu pad.
- 3. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted. Actual continuous current will be limited by thermal & electro–mechanical application board design. $R_{\theta JC}$ is determined by the user's board design.

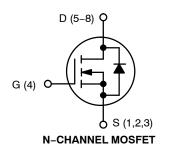
4. 100% UIS tested at L = 1 mH, I_{AS} = 30.7 A.

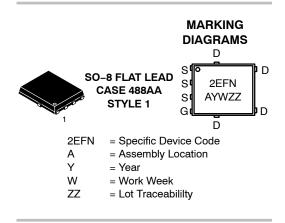


ON Semiconductor®

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V _{(BR)DSS}	R _{DS(ON)} MAX	I _D MAX
25 V	0.68 mΩ @ 10 V	365 A
25 V	$0.80~\mathrm{m}\Omega$ @ $4.5~\mathrm{V}$	303 A





ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 6 of this data sheet.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State (Note 1)	$R_{ ext{ heta}JC}$	0.9	°C/W
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	39	C/VV
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	135	°C/W

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

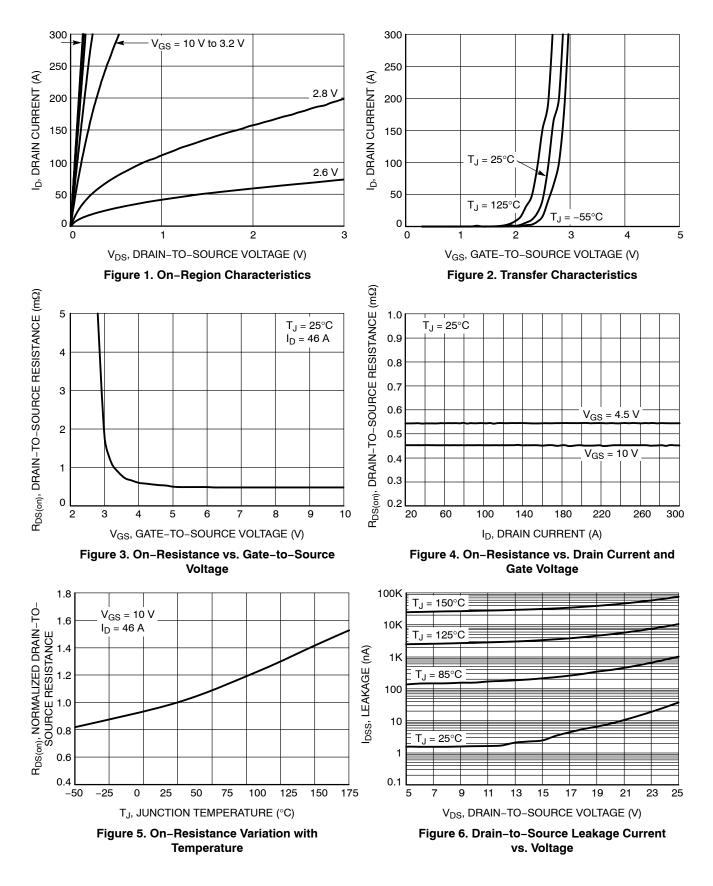
Parameter	Symbol	Test Condition		Min	Тур	Max	Unit	
OFF CHARACTERISTICS	•							
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 1 mA		25			V	
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} / T _J	$I_D = 1 \text{ mA. ref to } 25^{\circ}\text{C}$			16		mV/°C	
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V,	$T_J = 25^{\circ}C$			1		
		$V_{DS} = 20 \text{ V}$ $T_{J} = 125^{\circ}\text{C}$				250	μΑ	
Gate-to-Source Leakage Current	I _{GSS}	$V_{DS} = 0 V, V_{GS} = +$	-16 V/-12 V			±100	nA	
ON CHARACTERISTICS (Note 5)								
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}, I_D$	= 2 mA	1.2		2.0	V	
Threshold Temperature Coefficient	V _{GS(TH)} /T _J	I _D = 2 mA. ref	to 25°C		-4.4		mV/°C	
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 46 A			0.44	0.68	0	
		V _{GS} = 4.5 V, I _[₀ = 43 A		0.54	0.80	mΩ	
Forward Transconductance	9FS	$V_{DS} = 5 \text{ V}, \text{ I}_D$	= 46 A		307		S	
Gate Resistance	R _G	T _A = 25°C			0.48		Ω	
CHARGES AND CAPACITANCES					-	-		
Input Capacitance	C _{ISS}	V _{GS} = 0 V, V _{DS} = 13 V, f = 1 MHz			8600		pF	
Output Capacitance	C _{OSS}				2285			
Reverse Transfer Capacitance	C _{RSS}				129			
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 4.5 V, V _{DS} = 13 V; I _D = 46 A			52			
Threshold Gate Charge	Q _{G(TH)}				10			
Gate-to-Source Charge	Q _{GS}				21		nC	
Gate-to-Drain Charge	Q _{GD}				9			
Total Gate Charge	Q _{G(TOT)}	V_{GS} = 10 V, V_{DS} = 13 V; I_{D} = 46 A			116		nC	
SWITCHING CHARACTERISTICS, $V_{GS} = 4$	1.5 V (Note 6)							
Turn-On Delay Time	t _{d(ON)}				45			
Rise Time	tr	V _{GS} = 4.5 V, V _D	s = 13 V,		24]	
Turn-Off Delay Time	t _{d(OFF)}	V_{GS} = 4.5 V, V_{DS} = 13 V, I_D = 46 A, R_G = 6.0 Ω			68		- ns	
Fall Time	t _f				20			
SWITCHING CHARACTERISTICS, $V_{GS} = \frac{1}{2}$	10 V (Note 6)							
Turn-On Delay Time	t _{d(ON)}	V_{GS} = 10 V, V_{DS} = 13 V, I _D = 46 A, R _G = 6.0 Ω			23			
Rise Time	t _r				6.8		1	
Turn-Off Delay Time	t _{d(OFF)}				123		ns	
Fall Time	t _f				19		1	
DRAIN-SOURCE DIODE CHARACTERIS	rics							
Forward Diode Voltage	V _{SD}	V _{GS} = 0 V,	$T_J = 25^{\circ}C$		0.77	1.2	\ <i>\</i>	
		$V_{GS} = 0 V,$ $I_{S} = 46 A$ $T_{J} = 125^{\circ}C$			0.62		V	

ELECTRICAL CHARACTERISTICS (T_J = $25^{\circ}C$ unless otherwise specified)

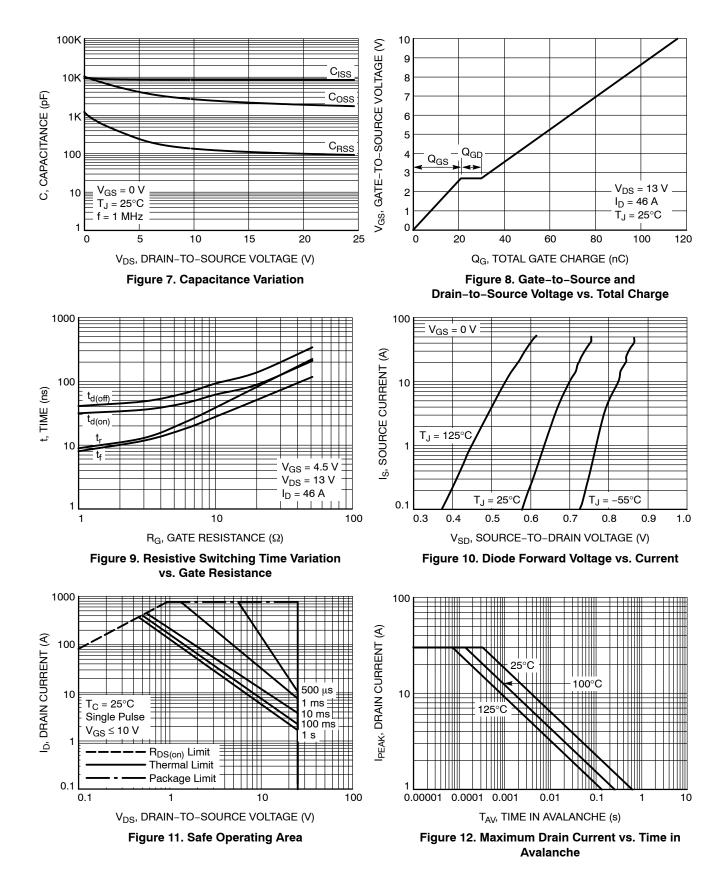
Parameter	Symbol Test Condition			Тур	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS						
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dIS/dt = 100 A/µs,		64		ns
Reverse Recovery Charge	Q _{RR}	I _S = 46 A		87		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions. 5. Pulse Test: pulse width $\leq 300 \ \mu$ s, duty cycle $\leq 2\%$. 6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS



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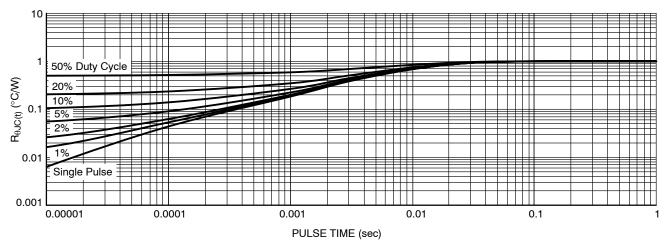


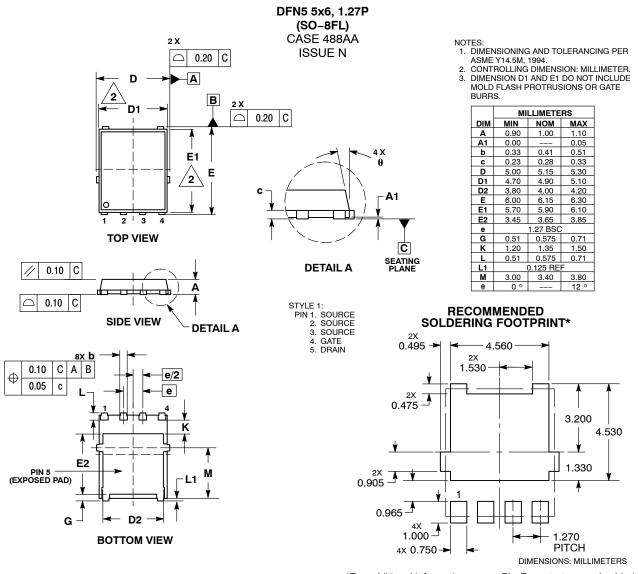
Figure 13. Thermal Response

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
NTMFS0D8N02P1ET1G	2EFN	DFN5 (Pb–Free)	1500 / Tape & Reel

+For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS



*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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