

MOSFET – Power, N-Channel, SUPERFET® III 800 V, 600 mΩ, 8 A

NTD600N80S3Z

Description

800 V SUPERFET III MOSFET is ON Semiconductor's high performance MOSFET family offering 800 V breakdown voltage.

New 800 V SUPERFET III MOSFET which is optimized for primary switch of flyback converter, enables lower switching losses and case temperature without sacrificing EMI performance thanks to its optimized design. In addition, internal Zener Diode significantly improves ESD capability.

This new family of 800 V SUPERFET III MOSFET enables to make more efficient, compact, cooler and more robust applications because of its remarkable performance in switching power applications such as Laptop adapter, Audio, Lighting, ATX power and industrial power supplies.

Features

- Typ. $R_{DS(on)}$ = 550 mΩ
- Ultra Low Gate Charge (Typ. Q_g = 15.5 nC)
- Low Stored Energy in Output Capacitance (E_{oss} = 1.74 μJ @ 400 V)
- 100% Avalanche Tested
- ESD Improved Capability with Zener Diode
- RoHS Compliant

Applications

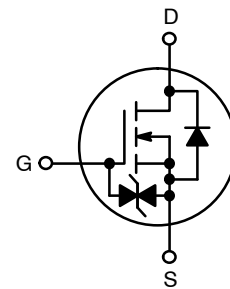
- Adapters / Chargers
- LED Lighting
- AUX Power
- Audio
- Industrial Power



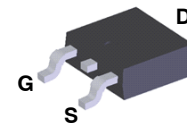
ON Semiconductor®

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$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
800 V	600 mΩ	8 A



POWER MOSFET



D-PAK
TO-252
CASE 369AS

MARKING DIAGRAM



T600N80S3Z	= Specific Device Code
A	= Assembly Location
Y	= Year
WW	= Work Week
ZZ	= Lot Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

NTD600N80S3Z

ABSOLUTE MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DSS}	Drain-to-Source Voltage	800	V
V_{GS}	Gate-to-Source Voltage	DC	± 20
		AC ($f > 1\text{ Hz}$)	± 30
I_D	Drain Current	Continuous ($T_C = 25^\circ\text{C}$)	8*
		Continuous ($T_C = 100^\circ\text{C}$)	5*
I_{DM}	Drain Current	Pulsed (Note 1)	21*
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	24	mJ
I_{AS}	Avalanche Current (Note 2)	1.2	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	0.6	mJ
dv/dt	MOSFET dv/dt	100	V/ns
	Peak Diode Recovery dv/dt (Note 3)	10	
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	60
		Derate Above 25°C	0.48
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from Case for 10 seconds)	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

*Drain current limited by maximum junction temperature.

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. $I_{AS} = 1.2\text{ A}$, $R_G = 25\ \Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 2\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} \leq 400\text{ V}$, starting $T_J = 25^\circ\text{C}$.

THERMAL RESISTANCE RATINGS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Junction-to-Case - Steady State	2.08	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient - Steady State	62.5	

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Reel Size	Tape Width	Quantity
NTD600N80S3Z	NTD600N80S3Z	TO-252	330 mm	16 mm	2500 Units

NTD600N80S3Z

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain-to-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 1 mA, T _J = 25°C	800			V
		V _{GS} = 0 V, I _D = 1 mA, T _J = 150°C	900			V
ΔBV _{DSS} / ΔT _J	Drain-to-Source Breakdown Voltage Temperature Coefficient	I _D = 1 mA, Referenced to 25°C		1.1		V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 800 V, V _{GS} = 0 V			1	μA
		V _{DS} = 640 V, T _C = 125°C		0.8		
I _{GSS}	Gate-to-Body Leakage Current	V _{GS} = ±20 V, V _{DS} = 0 V			1	μA

ON CHARACTERISTICS

V _{GS(th)}	Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 0.18 mA	2.2		3.8	V
R _{DS(on)}	Static Drain-to-Source On Resistance	V _{GS} = 10 V, I _D = 4 A		550	600	mΩ
g _{FS}	Forward Transconductance	V _{DS} = 20 V, I _D = 4 A		9.4		S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 400 V, V _{GS} = 0 V, f = 250 kHz		725		pF
C _{oss}	Output Capacitance			12		pF
C _{oss(eff.)}	Effective Output Capacitance	V _{DS} = 0 V to 400 V, V _{GS} = 0 V		139		pF
C _{oss(er.)}	Energy Related Output Capacitance	V _{DS} = 0 V to 400 V, V _{GS} = 0 V		21		pF
Q _{g(tot)}	Total Gate Charge at 10 V	V _{DD} = 400 V, I _D = 4 A, V _{GS} = 10 V (Note 4)		15.5		nC
Q _{gs}	Gate-to-Source Gate Charge			3.1		nC
Q _{gd}	Gate-to-Drain "Miller" Charge			5.1		nC
ESR	Equivalent Series Resistance	f = 1 MHz		3.5		Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = 400 V, I _D = 4 A, V _{GS} = 10 V, R _g = 4.7 Ω (Note 4)		12.3		ns
t _r	Turn-On Rise Time			5.9		ns
t _{d(off)}	Turn-Off Delay Time			39.5		ns
t _f	Turn-Off Fall Time			8.2		ns

SOURCE-TO-DRAIN DIODE CHARACTERISTICS

I _S	Maximum Continuous Source-to-Drain Diode Forward Current			8		A
I _{SM}	Maximum Pulsed Source-to-Drain Diode Forward Current			21		A
V _{SD}	Source-to-Drain Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 4 A			1.2	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 2 A, dI _F /dt = 100 A/μs		137		ns
Q _{rr}	Reverse Recovery Charge			0.91		μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

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TYPICAL CHARACTERISTICS

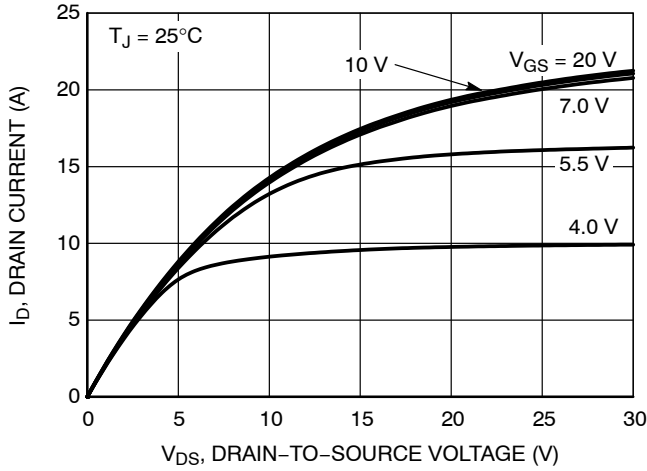


Figure 1. On-Region Characteristics

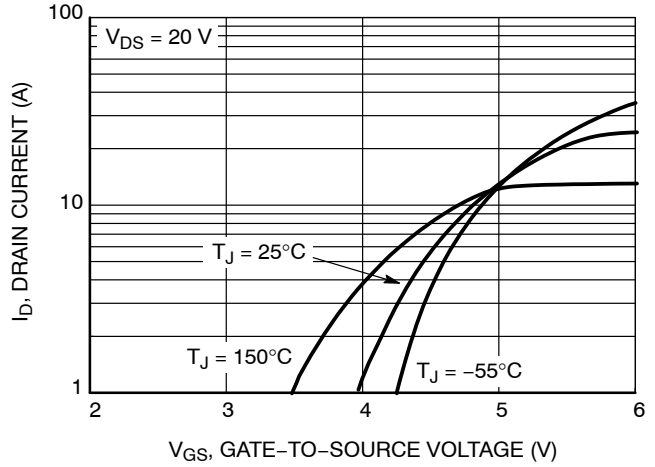


Figure 2. Transfer Characteristics

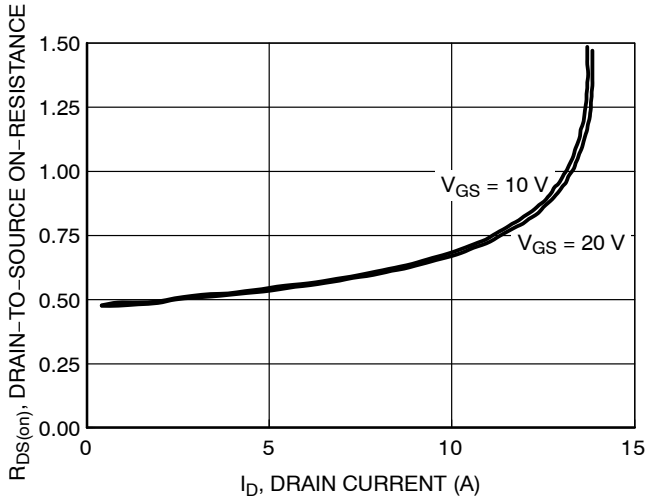


Figure 3. On Resistance vs. Drain Current

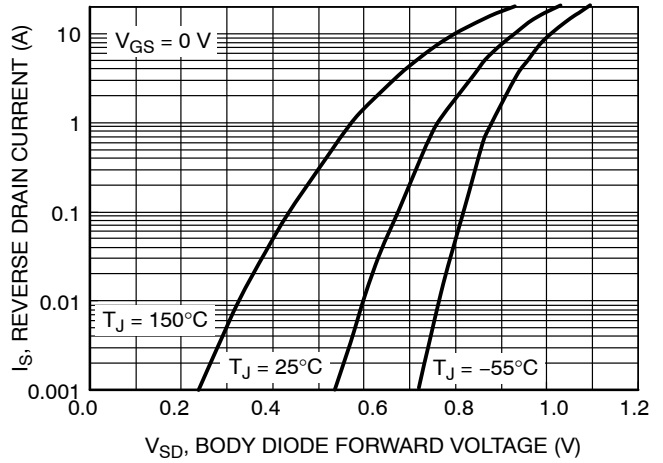


Figure 4. Diode Forward Voltage vs. Current

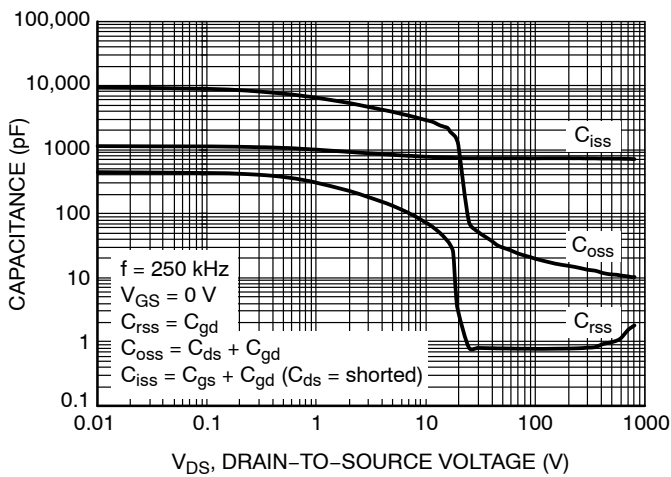


Figure 5. Capacitance Characteristics

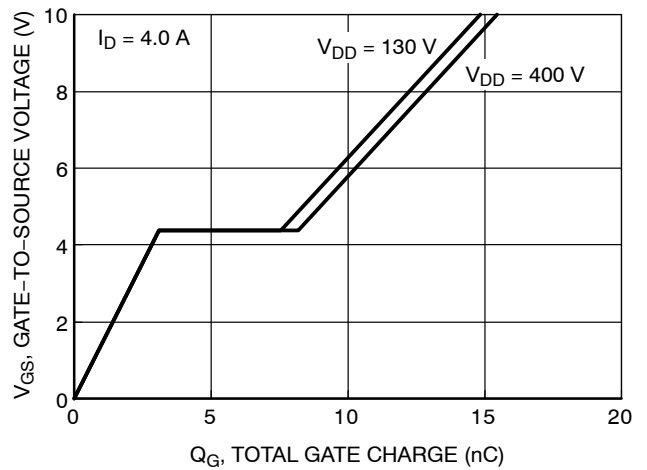


Figure 6. Gate Charge Characteristics

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TYPICAL CHARACTERISTICS

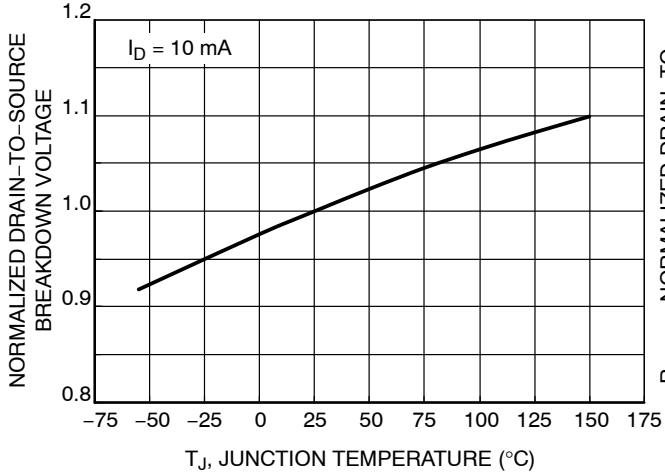


Figure 7. Normalized BV_{DSS} vs. Temperature

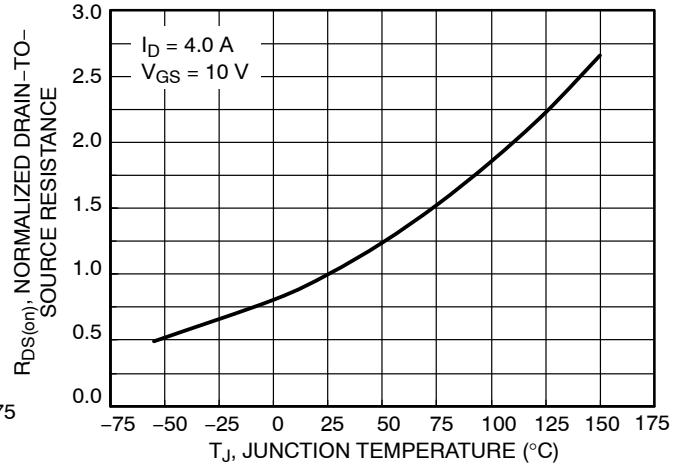


Figure 8. On-Resistance Variation vs. Temperature

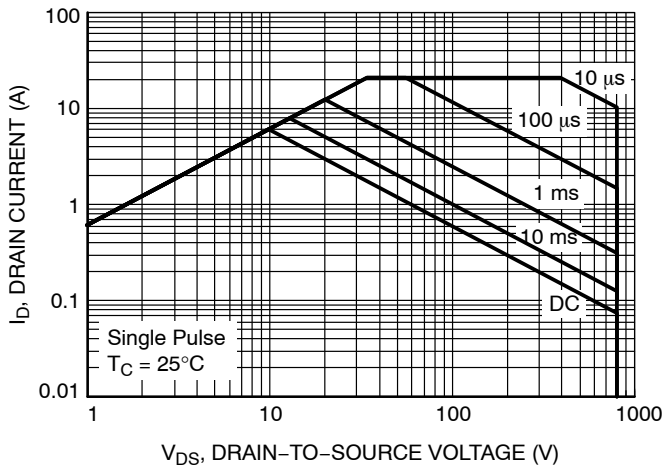


Figure 9. Safe Operating Area

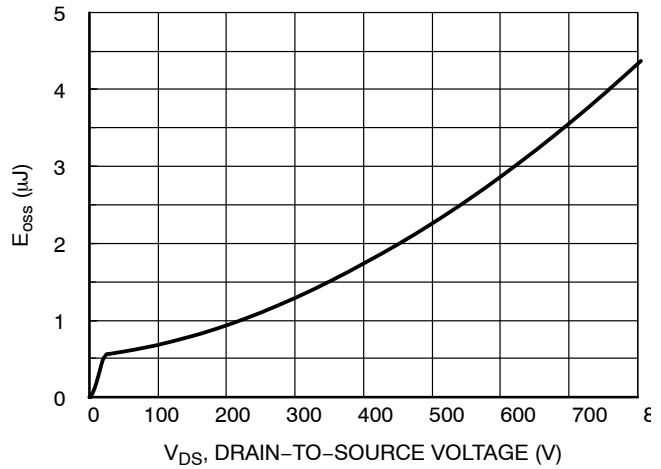


Figure 10. E_{OSS} vs. Drain-to-Source Voltage

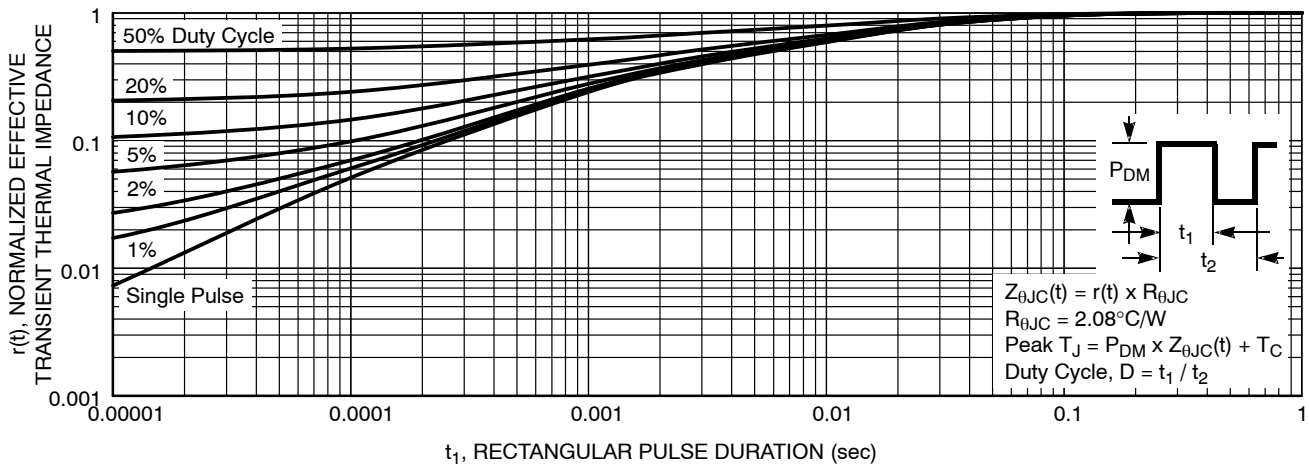


Figure 11. Transient Thermal Impedance

NTD600N80S3Z

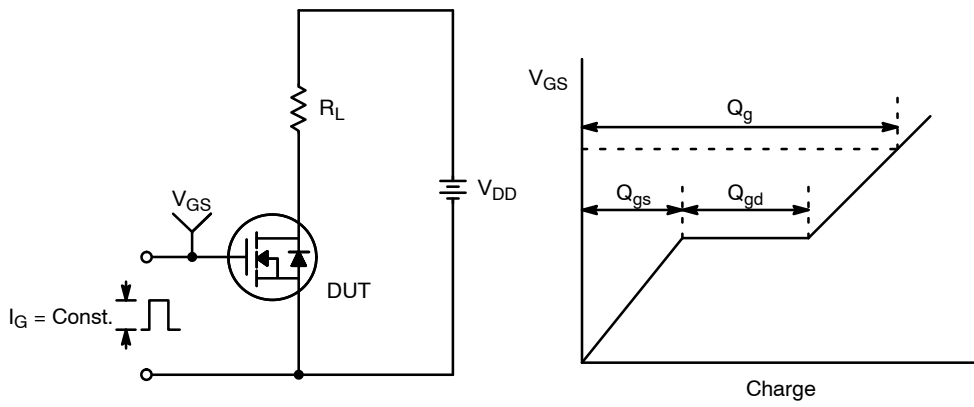


Figure 12. Gate Charge Test Circuit & Waveform

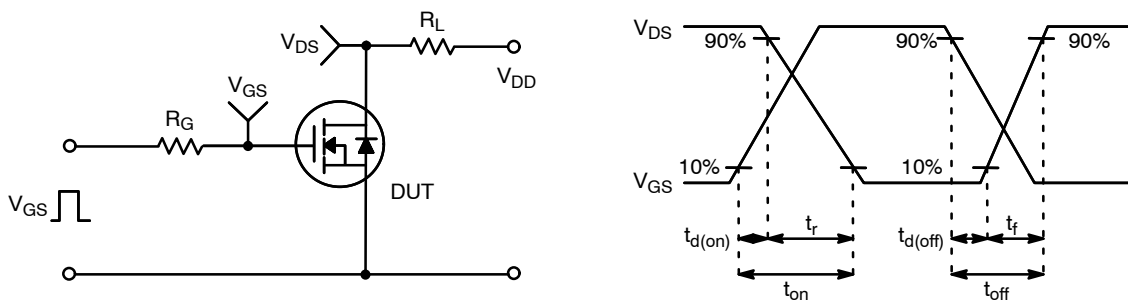


Figure 13. Resistive Switching Test Circuit & Waveforms

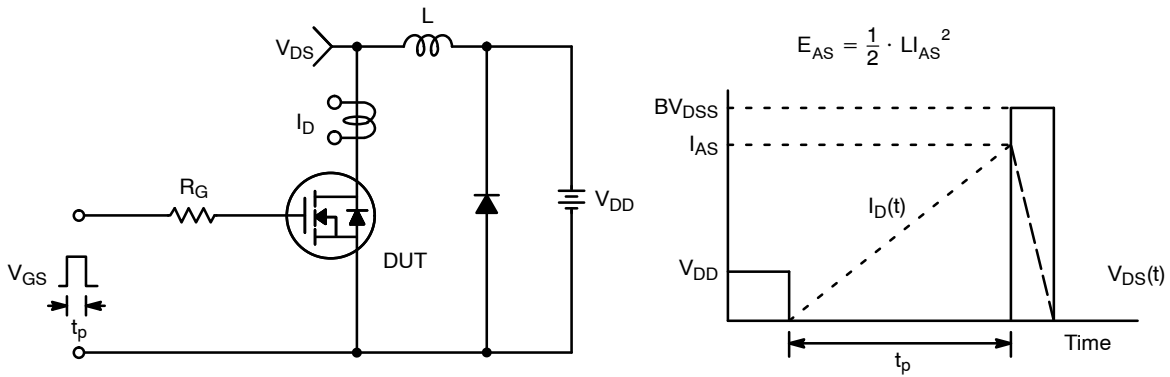


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

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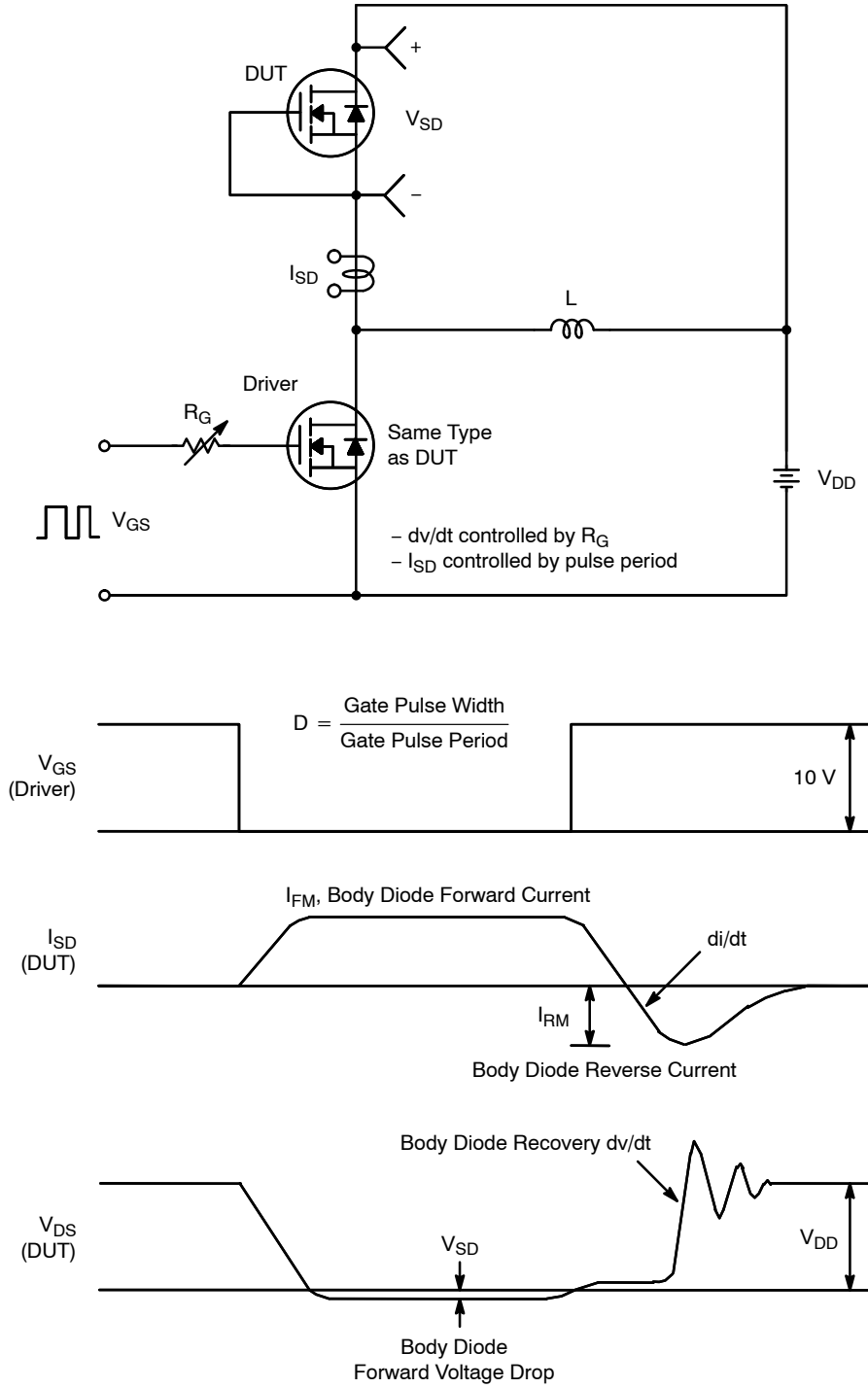


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®

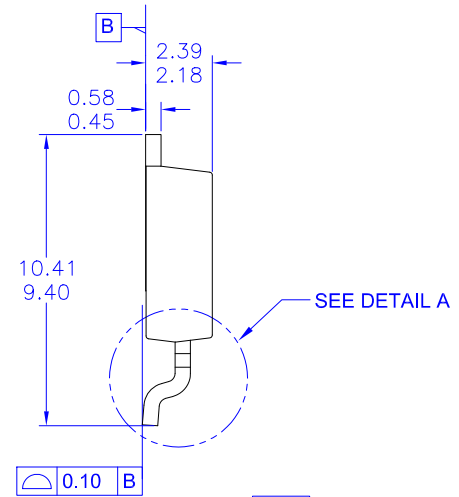
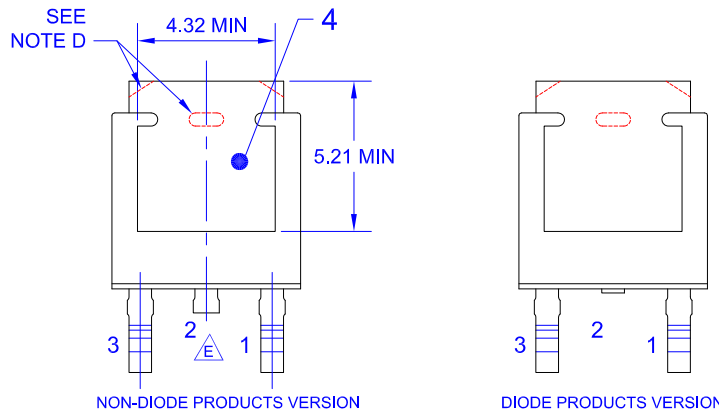
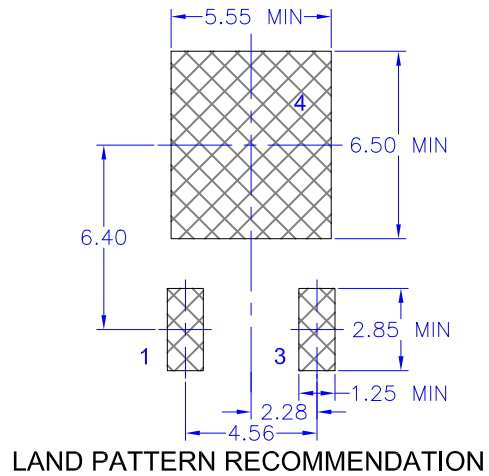
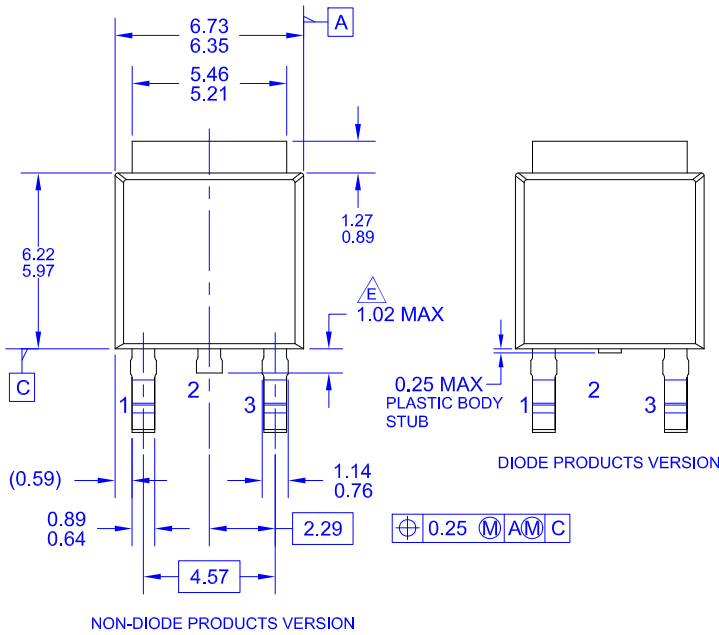


DPAK3 (TO-252 3 LD)

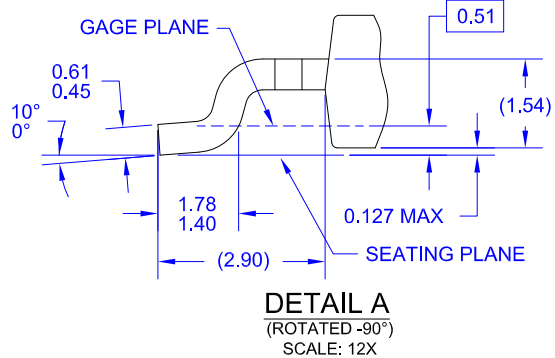
CASE 369AS

ISSUE O

DATE 30 SEP 2016



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
 - D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
 - E) TRIMMED CENTER LEAD IS PRESENT ONLY FOR DIODE PRODUCTS
 - F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
 - G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.



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DESCRIPTION:	DPAK3 (TO-252 3 LD)	PAGE 1 OF 1

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