# Product Change Notification - SYST-02LKZW876

**Date:**

03 May 2019

**Product Category:**

16-Bit - Microcontrollers and Digital Signal Controllers

**Affected CPNs:**

**Notification subject:**

ERRATA - dsPIC33CK64MP1xx Family Silicon Errata Errata Document Revision

**Notification text:**

SYST-02LKZW876

Microchip has released a new DeviceDoc for the dsPIC33CK64MP1xx Family Silicon Errata of devices. If you are using one of these read the document located at dsPIC33CK64MP1xx Family Silicon Errata

**Notification Status:** Final

**Description of Change:** Added silicon issue 16 (DMA).

**Impacts to Data Sheet:** None

**Reason for Change:** To Improve Productivity

**Change Implementation Status:** Complete

**Date Document Changes Effective:** 03 May 2019

**NOTE:** Please be advised that this is a change to the document only the product has not been changed.

**Markings to Distinguish Revised from Unrevised Devices:** N/A

**Attachment(s):**

dsPIC33CK64MP1xx Family Silicon Errata

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

DSPIC33CK64MP105-E/M4
DSPIC33CK64MP105-E/PT
DSPIC33CK64MP105-I/M4
DSPIC33CK64MP105-I/PT
DSPIC33CK64MP105T-I/M4
DSPIC33CK64MP105T-I/PT

# dsPIC33CK64MP105

# dsPIC33CK64MP105 Family
# Silicon Errata and Data Sheet Clarification

The dsPIC33CK64MP105 family devices that you have received conform functionally to the current Device Data Sheet (DS70005363**C**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the dsPIC33CK64MP105 silicon.

| | |
|---|---|
| **Note:** | This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A0**). |

Data Sheet clarifications and corrections start on page 6, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

| | |
|---|---|
| **Note:** | If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance. |

The DEVREV values for the various dsPIC33CK64MP105 silicon revisions are shown in Table 1.

**TABLE 1: SILICON DEVREV VALUES**

| Part Number | Device ID(1) | Revision ID for Silicon Revision |
|---|---|---|
| | | A0 |
| dsPIC33CK32MP102 | 0x8E00 | 0x0000 |
| dsPIC33CK32MP103 | 0x8E01 | |
| dsPIC33CK32MP105 | 0x8E02 | |
| dsPIC33CK64MP102 | 0x8E10 | |
| dsPIC33CK64MP103 | 0x8E11 | |
| dsPIC33CK64MP105 | 0x8E12 | |

**Note 1:** The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

**TABLE 2: SILICON ISSUE SUMMARY**

| Module | Feature | Item Number | Issue Summary | Affected Revisions |
|---|---|---|---|---|
| | | | | A0 |
| $I^2C$ | Interrupt | 1. | In Slave mode, an incorrect interrupt is generated when DHEN = 1. | X |
| $I^2C$ | Idle | 2. | Module SFR registers are reset in Idle mode. | X |
| $I^2C$ | SMBus 3.0 | 3. | When Configuration bit, SMB3EN (FDEVOPT[10]) = 1, the SMBus 3.0 VIH minimum specification may not be met. | X |
| Oscillator | XT, HS | 4. | The Primary Oscillator Start-up Timer (OST) may indicate the oscillator is ready for use too early. | X |
| PWM | Dead Time | 5. | When feed-forward PCI is used for dead-time compensation (DTCMPSEL = 1), the PWMx outputs are overridden. | X |
| UART | Frame Error | 6. | FERR bit will not get set if a Stop bit is received. | X |
| UART | Sleep | 7. | SLPEN needs to be set when waking from Sleep with a UART reception. | X |
| UART | Address Detect | 8. | When writing to UxP1 with UTXBRK = 1, the content of P1 will not get transmitted. | X |
| UART | IrDA® | 9. | When the UART is operating in IrDA mode, the received data may be corrupted. | X |
| I/O | POR | 10. | Spike on I/O at POR. | X |
| ICSP™ Flash Write Inhibit | Flash Write Inhibit | 11. | Flash memory cannot be protected against reprogramming. | X |
| CPU | FLIM Instruction | 12. | When the operands are of different signs, the FLIM instruction may not force the correct data limit. | X |
| CPU | DIV.SD Instruction | 13. | Overflow bit is not getting set when an overflow occurs. | X |
| CPU | MAXAB/MINAB/ MINZAB Instructions | 14. | MAXAB, MINAB and MINZAB do not work for different sign operands. | X |
| CPU | Byte Mode Instructions | 15. | Upper byte of the destination register may not be persistent. | X |
| DMA | ADC Triggers | 16. | DMA is triggered continuously from ADC. | X |

## Silicon Errata Issues

| | |
|---|---|
| **Note:** | This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A0**). |

### 1. Module: I²C

In Slave mode with DHEN = 1 (Data Hold Enable), if software sends a NACK, a Slave interrupt is asserted at the 9th falling edge of the clock.

**Work around**

Software should ignore the Slave interrupt that is asserted after sending a NACK.

**Affected Silicon Revisions**

| A0 | | | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

### 2. Module: I²C

In Slave mode, the SFRs are reset when the device is in Idle and the module is set for discontinue in Idle (I2CSIDL = 1).

**Work around**

None.

**Affected Silicon Revisions**

| A0 | | | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

### 3. Module: I²C

When selecting SMBus 3.0 operation using Configuration bit, SMB3EN (FDEVOPT[10]), the Voltage Input High ($V_{IH}$) of the SMBus 3.0 specification minimum may not be met.

**Work around**

None.

**Affected Silicon Revisions**

| A0 | | | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

### 4. Module: Oscillator

The Primary Oscillator Start-up Timer (OST) may indicate the oscillator is ready for use too early. Clocking the device before the oscillator is ready may result in incorrect execution and exceptions. This issue exists when the POSC is requested at power-on, during clock switching, when waking from Sleep or when a peripheral module requests the POSC directly. This issue affects XT and HS modes only.

**Work around**

Make sure that the Primary Oscillator clock is ready before using it by following these steps:

1. Running on a non-POSC source, request the POSC clock using a peripheral such as REFO.
2. Provide a delay to stabilize the POSC.
3. Then, switch to the POSC source.

**Affected Silicon Revisions**

| A0 | | | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

### 5. Module: PWM

When feed-forward PCI is used for dead-time compensation (DTCMPSEL = 1), the PWMx outputs are overridden.

**Work around**

Use Sync PCI (DTCMPSEL = 0) for dead-time compensation.

**Affected Silicon Revisions**

| A0 | | | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

### 6. Module: UART

When UART is operating with STSEL[1:0] = 2, (two Stop bits sent, two checked at receive) and STPMD = 0, the FERR bit will not get set if a Stop bit is received.

**Work around**

Use STPSEL = 3 instead of STSEL = 2. When operating with STSEL = 3 mode, the UART will be configured to send two Stop bits, but check one at receive.

**Affected Silicon Revisions**

| A0 | | | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

### 7. Module: UART

When waking from Sleep with a UART reception, SLPEN needs to be set in addition to WAKE = 1.

**Work around**

Set the SPLEN bit in addition to WAKE before entering Sleep.

**Affected Silicon Revisions**

| A0 | | | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

### 8. Module: UART

In UART Address Detect mode, writing to UxP1 with UTXBRK = 1 should cause a Break to be transmitted, followed by the content in P1, but the content of P1 will not get transmitted.

**Work around**

After writing to P1, wait for UTXBRK to get clear and then rewrite to P1.

**Affected Silicon Revisions**

| A0 | | | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

### 9. Module: UART

When the UART is operating in IrDA® mode, the received data may be corrupted.

**Work around**

None.

**Affected Silicon Revisions**

| A0 | | | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

### 10. Module: I/O

At device power-up, the I/O pins may drive a pulse up to 0.8V for a duration of up to 100 µSec.

**Work around**

It is recommended to ensure the circuitry that is connected to the pins can endure this pulse.

Example applications affected may include complementary power switches, where a transient current shoot-through might occur.

High-voltage applications with complementary switches should power the high-voltage 200 µSec later than powering the dsPIC® DSC to avoid the issue.

Behavior is specific to each part and not affected by aging.

**Affected Silicon Revisions**

| A0 | | | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

### 11. Module: ICSP™ Flash Write Inhibit

The ICSP Write Inhibit feature does not prevent ICSP Flash erase and program operations, even if the lock values are written.

**Work around**

None.

**Affected Silicon Revisions**

| A0 | | | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

### 12. Module: CPU

The FLIM instruction may incorrectly limit the data range when operating on signed operands of different sign values. If the operands are either all negative or all positive, the limit is correct.

**Work around**

None.

**Affected Silicon Revisions**

| A0 | | | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

### 13. Module: CPU

When using the Signed 32-by-16-bit Division instruction, `DIV.SD`, the Overflow bit may not always get set when an overflow occurs.

**Work around**

Test for and handle overflow conditions outside of the `div.sd` instruction.

**Affected Silicon Revisions**

| A0 | | | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

### 14. Module: CPU

When operating on signed operands of different sign values, the output for `MAXAB`, `MINAB` and `MINZAB` instructions may be incorrect. If the operands are either all negative or all positive, the output is correct.

**Work around**

None.

**Affected Silicon Revisions**

| A0 | | | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

### 15. Module: CPU

When using Byte mode instructions, the upper byte of the destination register may not be persistent.

**Work around**

None.

**Affected Silicon Revisions**

| A0 | | | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

### 16. Module: DMA

The DMA receives multiple continuous triggers from ADC until the trigger event from ADC is cleared. The OVRUNIF flag (DMAINTn[3]) will be set. When the OVRUNIF bit changes state, from '`0`' to '`1`', a DMA interrupt is generated.

**Work around**

Ignore the OVRUNIF bit and the first DMA interrupt. Clear the ADC trigger source, ANxRDY, with a DMA read of the ADC buffer, ADCBUFx, for the corresponding ADC channel.

**Affected Silicon Revisions**

| A0 | | | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

## Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS70005363**C**):

| **Note:** | Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity. |
|---|---|

None.

## APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (1/2019)

Initial version of this document; issued for revision A0.

Rev B Document (2/2019)

Updated device data sheet revision from B to C.

Rev C Document (3/2019)

Added silicon issue 16 (DMA).

**NOTES:**

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ISBN: 978-1-5224-4234-9

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