swissbit®

Product Data Sheet

Industrial CFast™ Card

F-66 Series

SATA Gen3 – 6.0 Gbit/s, pSLC

Commercial and Industrial Temperature Grade

Date: October 31, 2019
Revision: 1.04

everbit™

made in germany

Contents

F-66 Series – Industrial CFast™ Solid State Drive, pSLC 4 GBytes up to 120 GBytes

1. Product Summary

- **Capacities:** 4 GBytes, 8 GBytes, 16 GBytes, 30 GBytes, 60 GBytes, 120 GBytes
- **Form Factor:** CFast-Sized Solid State Drive (36.4 mm x 42.8 mm x 3.6 mm)
- **Compliance:** SATA Gen3 – 6 Gbit/s (Gen2 – 3 Gbit/s and Gen1 – 1.5 Gbit/s backward compatible)
- **CFast 2.0 Compatible**
- **Command Sets:** Supports ATA/ATAPI-8 and ACS-2
- **High Performance:**
  - Burst Transfer Rate: Up to 600 MBytes/s in SATA Gen3 – 6.0 Gbit/s
  - Read Performance: Sequential Read up to 520 MBytes/s, Random Read 4K up to 80,000 IOPS
  - Write Performance: Sequential Write up to 415 MBytes/s, Random Write 4K up to 75,000 IOPS
- **Operating Temperature Range[1]:**
  - Commercial: 0 °C to 70 °C
  - Industrial: -40 °C to 85 °C
- **Storage Temperature Range:** -40 °C to 85 °C
- **Operating Voltage:** 3.3V ± 5%
- **Power (Max Capacity):**
  - Read (Active): 1.4 W
  - Write (Active): 1.8 W
  - Idle: 380 mW
  - Slumber: 116 mW
- **Data Retention:** 10 Years @ Life Begin; 1 Year @ Life End
- **Endurance in TeraBytes Written (TBW) @ Max Capacity[2]:**
  - Client > 1805
  - Embedded > 495
  - Enterprise > 465
- **Shock/Vibration:** 1,500 *g* / 50 *g*
- **High-Performance 32-Bit Processor with Integrated, Parallel Flash Interface Engines:**
  - Pseudo Single-Level Cell (pSLC) NAND Flash
  - Hardware BCH Code ECC (up to 66 bit correction per 1 KByte page)
- **High Reliability:**
  - Mean Time Between Failure (MTBF): > 2,000,000 hours
  - Data Reliability: < 1 non-recoverable error per 10^{16} bits read

[1] Adequate airflow is required to ensure the temperature, as reported in the S.M.A.R.T. data, does not exceed 115°C (industrial temperature drive) and 100°C (commercial temperature drive) respectively.

[2] According to JEDEC (JESD47I), the time to write the full TBW is 18 months. Higher average daily data volume reduces the specified TBW. The values listed are estimates and are subject to change without notice.

2. Product Features

- Pseudo SLC Flash with 20,000 Program/Erase Cycles and everbit™ Reduced Write Amplification
- Dynamic and Static Wear Leveling
- Subpage Mode Flash Translation Layer (FTL)
- Data Care Management
  - Active: Adaptive Read Refresh
  - Passive: Background Media Scan
- Lifetime Enhancements
  - Dynamic Bad Block Remapping
  - Write Amplification Reduction
- On-Board Power Fail Protection
- AHCI, TRIM, and NCQ Support
- ATA Security Feature Set Support
- DEVSLP Compatible
- In-Field Firmware Update
- Enterprise-Grade Self-Monitoring, Analysis, and Reporting Technology (S.M.A.R.T.)
- Life Cycle Management
- Controlled "Locked" BOM
- RoHS-6 Compliant
- AES256 Encryption (on request)
- 30 µinch Gold-Plated Connector (on request)
- Swissbit Life Time Monitoring (SBLTM) Tool and SDK for SBLTM (on request)

3. Ordering Information

Table 1: Standard Product List

Capacity	Temperature	
	Commercial	Industrial
	Part Number	Part Number
4 GBytes	SFCA004GHxAA1T0-C-GS-2yP-STD	SFCA004GHxAA1T0-I-GS-2yP-STD
8 GBytes	SFCA008GHxAA2T0-C-GS-2yP-STD	SFCA008GHxAA2T0-I-GS-2yP-STD
16 GBytes	SFCA016GHxAA2T0-C-GS-2yP-STD	SFCA016GHxAA2T0-I-GS-2yP-STD
30 GBytes	SFCA030GHxAA2T0-C-LB-2yP-STD	SFCA030GHxAA2T0-I-LB-2yP-STD
60 GBytes	SFCA060GHxAA2T0-C-HC-2yP-STD	SFCA060GHxAA2T0-I-HC-2yP-STD
120 GBytes	SFCA120GHxAA2T0-C-OC-2yP-STD	SFCA120GHxAA2T0-I-OC-2yP-STD

x = product generation and y = firmware revision

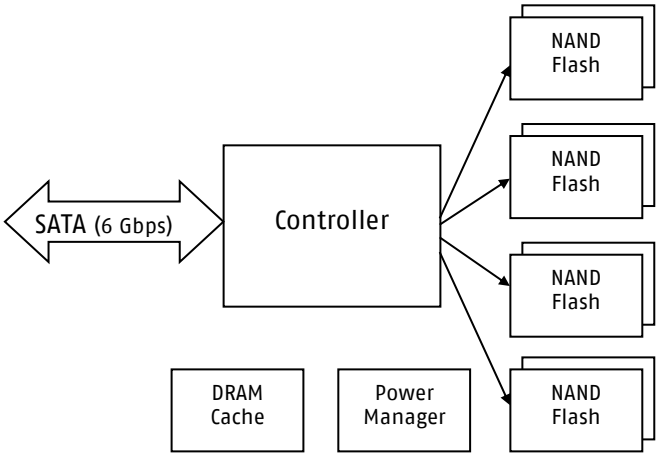
Table 2: Available Part Numbers

Capacity	Temperature	
	Commercial	Industrial
	Part Number	Part Number
4 GBytes	SFCA004GH3AA1T0-C-GS-22P-STD	SFCA004GH3AA1T0-I-GS-22P-STD
8 GBytes	SFCA008GH3AA2T0-C-GS-22P-STD	SFCA008GH3AA2T0-I-GS-22P-STD
16 GBytes	SFCA016GH3AA2T0-C-GS-22P-STD	SFCA016GH3AA2T0-I-GS-22P-STD
30 GBytes	SFCA030GH3AA2T0-C-LB-22P-STD	SFCA030GH3AA2T0-I-LB-22P-STD
60 GBytes	SFCA060GH3AA2T0-C-HC-22P-STD	SFCA060GH3AA2T0-I-HC-22P-STD
120 GBytes	SFCA120GH3AA2T0-C-OC-22P-STD	SFCA120GH3AA2T0-I-OC-22P-STD

4. Product Description

The Swissbit® F-66 Solid State Drive (SSD) leverages the CFast 2.0 compatible, industry-standard form factor and connectivity. Combined with a SATA Gen3 controller and pseudo Single-Level Cell (pSLC) NAND flash technology, the F-66 realizes a robust non-volatile storage solution for today's embedded storage applications. A functional block diagram of the F-66 SSD is provided below in Figure 1.

Figure 1: F-66 CFast Functional Block Diagram



The F-66 SSD incorporates two existing industry standards into a single product: the CompactFlash™ (CF) card form factor and the Serial ATA (SATA) interface commonly used with hard disk drives (HDDs) and SSDs. The interface consists of a female 7-pin SATA data connector and a female 17-pin power connector. Because standard SATA hard drives use male connectors, an adaptor is required to replace drives with CFast cards. CFast cards can be used to replace HDDs, SSDs, and Compact Flash™ cards in applications requiring smaller form factors, high endurance, and the ability to withstand shock, vibration, extreme temperatures (-40 °C to 85 °C), high altitude, and rough environmental conditions. The Swissbit CFast™ cards provide rugged storage for embedded and industrial systems where performance, data and system reliability, power fail protection, and flexibility are important design considerations.

The on-board SATA Gen3 controller manages the interface between the host and the non-volatile NAND flash memory array. The controller supports SATA Gen3 (6 Gbit/s) interface speeds and is fully backward compatible with SATA Gen2 (3 Gbit/s) and SATA Gen1 (1.5 Gbit/s) to enable the broadest possible range of platform compatibility. The controller utilizes an ARC 700 processing core, providing an optimum balance between read/write performance, Data Care Management, and power fail protection.

Swissbit's everbit™ F-66 CFast cards deliver an impressive IOPS rate and highest endurance by combining pSLC flash technology with a high-end controller architecture, firmware, and an optimized configuration. The everbit™ SSDs are designed for applications requiring high data transfer rates (see Table 3: Read/Write Performance). This performance is achieved through an on-board DRAM cache and the controller 4-channel NAND flash interface that supports ONFI and Toggle 2 (400 MT/s) interface speeds. The use of pSLC NAND increases the endurance of the drive, extending the rated program/erase (P/E) cycles to 20,000. In addition, the F-66 series feature Swissbit's proven power fail safety and support for the ATA security feature set, NCQ, TRIM, advanced wear leveling and bad block management, and in-field firmware updates.

An on-controller BCH Error Correction Code (ECC) engine provides the F-66 hardware ECC, which is capable of correcting up to 66 bits per 1 KByte page. This, combined with Swissbit's Data Care Management firmware, provides both passive and active data management strategies to ensure data integrity and extract the maximum possible endurance and reliability from the NAND flash array. These strategies include, but are not limited to, Global Wear Leveling, Adaptive Read Refresh, Background Media Scan, and Dynamic Block Remapping.

The risk of data loss as a result of an unexpected power fail event is mitigated using a robust sequence of voltage regulators and detectors designed to ensure a graceful shutdown of the controller and NAND flash array. A combination of both hardware and firmware power fail features prevent the possibility of resident data being corrupted during an unexpected power failure.

Related Documentation

- CFast Specification 2.0 (http://www.compactflash.org)
- Serial ATA International Organization Serial ATA Revision 3.0 (http://www.serialata.org)
- Serial Transport Protocols and Physical Interconnect (ATA/ATAPI-8) (http://www.t13.org)
- Electronic Industries Alliance (http://www.ecianow.org)

4.1 Performance Specifications

The F-66 read/write sequential and random CDM performance benchmarks are detailed in the following Table 3.

Table 3: Read/Write Performance[3]

Capacity	Sequential Read (MBPS)	Sequential Write (MBPS)	Random Read 4K (IOPS)	Random Write 4K (IOPS)
4 GBytes	150	70	17,000	15,000
8 GBytes	300	130	32,000	32,000
16 GBytes	300	110	32,000	27,000
30 GBytes	520	220	63,000	55,000
60 GBytes	520	410	80,000	72,000
120 GBytes	520	415	80,000	75,000

4.2 Current Consumption

The drive-level current consumption as a function of operating mode is shown in the following Table 4.

Table 4: Current Consumption[4]

Drive Capacity	Sequential Read	Sequential Write	Random Read 4K	Random Write 4K	Idle	Slumber	Unit
4 GBytes	225	235	225	235	105	35	mA
8 GBytes	270	295	265	290	105	35	
16 GBytes	275	295	265	290	105	35	
30 GBytes	350	385	340	380	105	35	
60 GBytes	425	550	415	530	110	35	
120 GBytes	435	560	425	555	115	35	

[3] The values are measured using Crystal Disk Mark (CDM) across the full drive density. Performance depends on flash type and number, file/cluster size, and burst speed.

[4] All values are the maximum recorded running IOMeter script for Read/Write operations with 1MB transfer size in 1 minute intervals at 25 °C, with nominal supply voltage and SATA transfer rate 6Gb/s.

4.3 Environmental Specifications

4.3.1 Recommended Operating Conditions

The recommended operating conditions for the F-66 SSD are provided in the following Table 5.

Table 5: Recommended Operating Conditions[5]

Parameter	Value
Commercial Operating Temperature	0 °C to 70 °C
Industrial Operating Temperature	-40 °C to 85 °C
Power Supply V_{CC} Voltage	3.3 V ± 5%

4.3.2 Recommended Storage Conditions

The recommended storage conditions are listed in the following Table 6.

Table 6: Recommended Storage Conditions

Parameter	Value
Commercial Storage Temperature	-40 °C to 85 °C
Industrial Storage Temperature	-40 °C to 85 °C

4.3.3 Shock, Vibration and Humidity

The maximum shock, vibration and humidity conditions are listed in the following Table 7.

Table 7: Shock, Vibration and Humidity

Parameter	Value
Non-Operating Shock	1,500 *g*, 0.5 ms pulse duration, half-sine wave (IEC 60068-2-27 and JESD22-B110 cond. B)
Non-Operating Vibration	50 *g*, 80-2,000 Hz, 3 axes, 12 cycles (IEC 60068-2-6, MIL-STD-883 H Method 2007.3)
Humidity (Non-Condensing)	85% RH 85 °C, 1000 hrs, max. supply voltage (JESD22-A101B)

[5] Adequate airflow is required to ensure the temperature, as reported in the S.M.A.R.T. data, does not exceed 115°C (industrial temperature drive) and 100°C (commercial temperature drive) respectively.

4.4 Regulatory Compliance

The F-66 devices comply with the standards listed in the following Table 8.

Table 8: Regulatory Compliance

Compliance	Country	Type	Standard(s)/Directive
CE	European Union	Certificate	2011/65/EU, 2012/19/EU, 2004/30/EU
CE/EMC	European Union	Compliance	2004/108/EC (AS/NZS CISPR22 :2009 +A1:2010, EN 61000-6-2:2005/AC:2005,EN 61000-6-4:2007/A1:2011 [EN55022:2010 Class B])
CE/RoHS	European Union	Compliance	2011/65/EU
CE/WEEE	European Union	Compliance	2012/19/EU
REACH	European Union	Certificate	1907/2006
FCC	United States	Certificate	47CFR Part 15, Class B
UL	United States	Compliance	UL/CSA 60950-1, Second Edition
VCCI	Japan	Compliance	ITE (Class A)
CCC	China	Compliance	Laws and Regulations of the People's Republic of China Governing Foreign-Related Matters (1991.7)
C-Tick	Australia	Compliance	AS/NZS CISPR22
TüV	Germany	Compliance	TüV IEC 60950-1; UL/CSA 60950-1, Second Edition
SATA-IO	International	Compliance	SATA Revision 1.4 Interoperability

4.5 Mechanical Specifications

The F-66 SSD consists of a flash controller and NAND flash memory devices. The controller interfaces with a host system allowing data to be written to and read from the flash memory array. The SSD has a female 7-pin SATA data connector and a female 17-pin power connector. Because standard SATA hard drives use male connectors, an adaptor is required to replace drives with CFast cards. Physical dimensions are detailed in the following Table 9. Figure 3 on page 12 illustrates the F-66 dimensions and connector location.

Table 9: Physical Dimensions

Physical Dimensions		Unit
Length	36.40±0.15	mm
Width	42.80±0.10	
Thickness (Max)	3.60	
Weight (Max Capacity)	10	g

4.6 Reliability and Endurance

The Mean Time Between Failure (MTBF) is specified to exceed the value listed in the following Table 10. Data reliability with effective error tolerance and data retention at the beginning and end of life is also provided.

Table 10: Reliability

Parameter	Value
MTBF (at 25 °C)	> 2,000,000 hours
Data Reliability	< 1 Non-Recoverable Error per 10^{16} Bits Read
Data Retention	10 Years at Start (JESD47), 1 Year at EOL

Endurance represented as both TeraBytes Written (TBW) and full Drive Writes Per Day (DWPD) for three different application scenarios is provided in the following Table 11.

Table 11: Endurance[6]

Drive Capacity	Client[7]		Enterprise		Embedded	
	TBW	DWPD[8]	TBW	DWPD[8]	TBW	DWPD[8]
4 GBytes	56.45	13.20	11.70	2.735	15.63	3.65
8 GBytes	112.90		25.53	2.984	31.25	
16 GBytes	225.83		58.13	3.40	62.50	
30 GBytes	451.65		116.26		125.00	
60 GBytes	903.31		232.53		250.00	
120 GBytes	1806.62		465.06		500.00	

4.7 Drive Geometry Specification

The F-66 drive geometry is set to report industry standard LBA settings per the IDEMA standard (LBA1-03). The values for each capacity are shown in the following Table 12.

Table 12: Drive Geometry

Raw Capacity	User Capacity[9]	Total LBA	User Addressable Bytes
		Decimal	(Unformatted)
4 GBytes	4 GBytes	7,732,368	3,958,972,416
8 GBytes	8 GBytes	15,465,744	7,918,460,928
16 GBytes	15 GBytes	29,323,728	15,013,748,736
32 GBytes	30 GBytes	58,626,288	30,016,659,456
64 GBytes	60 GBytes	117,231,408	60,022,480,896
128 GBytes	120 GBytes	234,441,648	120,034,123,776

[6] Client and Enterprise workloads follow the JEDEC JESD219 standard. the Embedded workload creates a 4 KByte file and appends it. Enterprise workload values are measured based on 168 hours of runtime. 1 TByte = 10^{12} bytes

[7] Because the JEDEC master trace file for the Client workload is designed for capacities ≥ 60 GBytes, the TBW and DWPD values for the capacities below 60 GBytes are estimates

[8] DWPD values are based on a service life of 3 years

[9] 1 GByte = 10^{9} bytes

5. Electrical Interface

The CFast card is connected with a standard 7-pin SATA connector and a standard 17-pin power connector. (Figure 2). The signal/pin assignments and descriptions are listed in the following Table 13.

Figure 2: F-66 CFast Connector

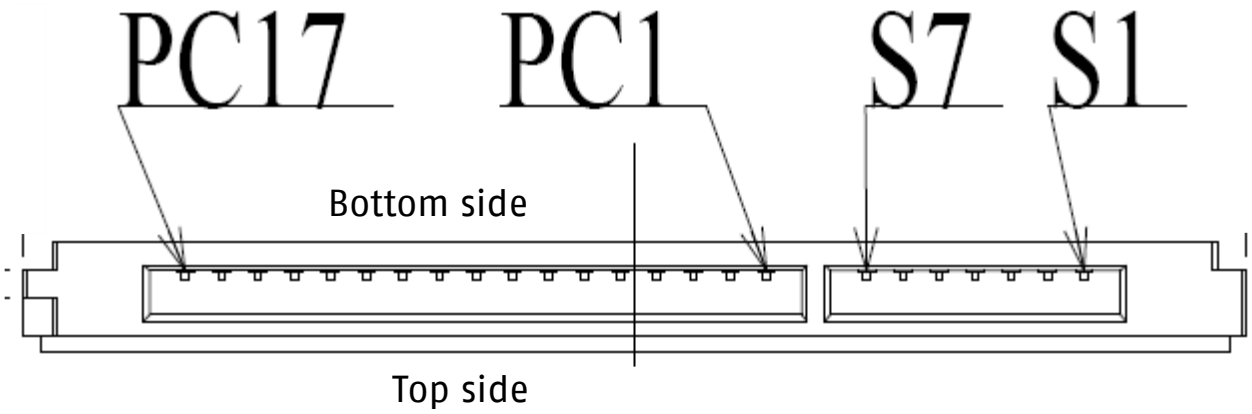


Table 13: Pin Assignment, Name and Description

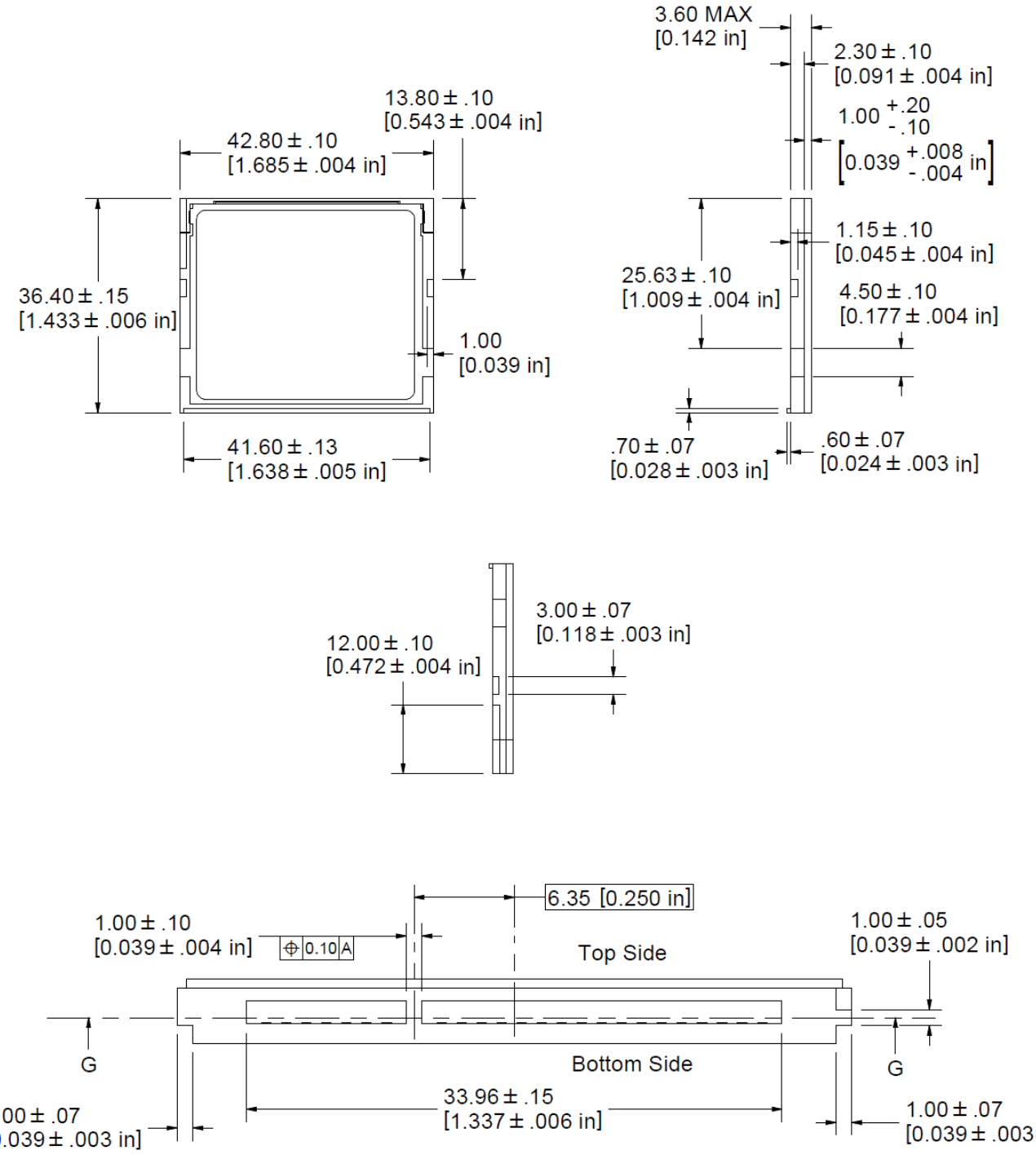
Pin	Signal Name	Description
S1	SGround	Signal Ground
S2	A+	+ Differential Device Transmit Signal
S3	A-	- Differential Device Transmit Signal
S4	SGround	Signal Ground
S5	B-	- Differential Device Receive Signal
S6	B+	+ Differential Device Receive Signal
S7	SGround	Signal Ground
PC1	CDI[10]	Card Detect In
PC2	PGround	Power Ground
PC3	DEVSLP	DEVSLP Input
PC4-PC6	NC	No Connect
PC7	PGround	Power Ground
PC8	LED1	Reserved
PC9	LED2	Reserved
PC10-PC11		Reserved
PC12	IFDet	Card Output, Connected to GND
PC13-PC14	3.3 V	Device Power 3.3 V
PC15-PC16	PGround	Power Ground
PC17	CDO[10]	Card Detect Out

[10] CDI and CDO are physically shorted together in the device. The CDO logic state shall follow the CDI logic state whether the device is powered up or not.

6. Package Mechanical

NOTE: The dimensions in the following Figure 3 are the maximum values based on the CFast specification. For the product dimensions, see the *Mechanical Specifications* section on page 9.

Figure 3: CFast SSD Dimensions in mm [in]



7. ATA Commands

This section provides information on the ATA commands supported by the SSD. The commands are issued to the ATA by loading the required registers in the command block with the supplied parameter and then writing the command code to the register. For backward compatibility, some commands are implemented as a "no operation". See the following Table 14 for a list of ATA commands the device supports. For details about setting up the command registers, see the latest ATA Specification.

Table 14: ATA Command Set

Command	Code	Protocol
General Feature Set		
Execute Device Diagnostic	90h	Execute Device Diagnostic
Flush Cache	E7h	Non-data
Identify Device	ECh	PIO data-in
Initialize Drive Parameters	91h	Non-data
Read DMA	C8h	DMA
Read Log Ext	2Fh	PIO data-in
Read Multiple	C4h	PIO data-in
Read Sector(s)	20h	PIO data-in
Read Verify Sector(s)	40h or 41h	Non-data
Set Feature	EFh	Non-data
Set Multiple Mode	C6h	Non-data
Write DMA	CAh	DMA
Write Multiple	C5h	PIO data-out
Write Sector(s)	30h	PIO data-out
NOP	00h	Non-data
Read Buffer	E4h	PIO data-in
Write Buffer	E8h	PIO data-out
Power Management Feature Set		
Check Power Mode	E5h or 98h	Non-data
Idle	E3h or 97h	Non-data
Idle Immediate	E1h or 95h	Non-data
Sleep	E6h or 99h	Non-data
Standby	E2h or 96h	Non-data
Standby Immediate	E0h or 94h	Non-data
Security Mode Feature Set		
Security Set Password	F1h	PIO data-out
Security Unlock	F2h	PIO data-out
Security Erase Prepare	F3h	Non-data
Security Erase Unit	F4h	PIO data-out
Security Freeze Lock	F5h	Non-data
Security Disable Password	F6h	PIO data-out
S.M.A.R.T. Feature Set		
S.M.A.R.T. Disable Operations	B0h	Non-data
S.M.A.R.T. Enable/Disable Autosave	B0h	Non-data
S.M.A.R.T. Enable Operations	B0h	Non-data
S.M.A.R.T. Execute OFF-LINE Immediate	B0h	Non-data
S.M.A.R.T. Read Data	B0h	PIO data-in
S.M.A.R.T. Read Log	B0h	PIO data-in
S.M.A.R.T. Read Threshold	B0h	PIO data-in
S.M.A.R.T. Return Status	B0h	Non-data
S.M.A.R.T. Save Attribute Values	B0h	Non-data
S.M.A.R.T. Write Attribute Values	B0h	Non-data
S.M.A.R.T. Write Log	B0h	PIO data-out

Command	Code	Protocol
Host Protected Area Feature Set		
Read Native Max Address	F8h	Non-data
Set Max Address	F9h	Non-data
Set Max Set Password	F9h	PIO data-out
Set Max Lock	F9h	Non-data
Set Max Freeze Lock	F9h	Non-data
Set Max Unlock	F9h	PIO data-out
48-Bit Address Feature Set		
Flush Cache Ext	EAh	Non-data
Read Sector(s) Ext	24h	PIO data-in
Read DMA Ext	25h	DMA
Read Multiple Ext	29h	PIO data-in
Read Native Max Address Ext	27h	Non-data
Read Verify Sector(s) Ext	42h	Non-data
Set Max Address Ext	37h	Non-data
Write DMA Ext	35h	DMA
Write DMA FUA Ext	3Dh	DMA
Write Multiple Ext	39h	PIO data-out
Write Multiple FUA Ext	CEh	PIO data-out
Write Sector(s) Ext	34h	PIO data-out
NCQ Feature Set		
Read FPDMA Queued	60h	DMA Queued
Write FPDMA Queued	61h	DMA Queued
Others		
Data Set Management	06h	DMA
Seek	70h	Non-data

8. Identify Device Information

The following Table 15 describes the 512 bytes of data the drive returns for the Identify Device command (ECh).

Table 15: Identify Device Information

Word(s)	Default Value	Total Bytes	Data Field Type Information
0	0040h*	2	Standard Configuration Fixed (optional 848Ah for removable)
1	XXXXh	2	Default number of cylinders
2	0000h	2	Reserved
3	00XXh	2	Default number of heads
4-5	0000h	4	Obsolete
6	XXXXh	2	Default number of sectors per track
7-8	XXXXh	4	Number of sectors per drive (Word 7 = MSW, Word 8 = LSW)
9	0000h	2	Obsolete
10-19	aaaa	20	Serial number in ASCII (right-justified)
20-22	0000h	6	Obsolete
23-26	XXXX*	8	Firmware revision in ASCII (big-endian byte order in Word)
27-46	XXXX*	40	Model number in ASCII (right-justified)
47	8002h	2	Maximum number of sectors on Read/Write Multiple command
48	4000h	2	Trusted Computing feature set not supported
49	2F00h*	2	Standby Timer, DMA, LBA, IORDY supported
50	4000h	2	Capabilities
51	0000h	2	PIO data transfer cycle timing mode 0
52	0000h	2	Obsolete
53	0007h*	2	Words 88 and 64-70 valid
54	XXXXh	2	Current numbers of cylinders
55	XXXXh	2	Current numbers of heads
56	XXXXh	2	Current sectors per track
57-58	XXXXh	4	Current capacity in LBAs (Word 57 = LSW, Word 58 = MSW)
59	910Xh*	2	Multiple sector setting (host changeable)
60-61	XXXXh	4	Total number of sectors addressable in LBA mode
62	0000h	2	Obsolete
63	0007h* 0000h*	2	Multiword DMA transfer support modes 2, 1, and 0 Multiword DMA not supported
64	0003h	2	Advanced PIO modes supported
65	0078h*	2	Minimum Multiword DMA transfer cycle time per Word
66	0078h*	2	Recommended Multiword DMA transfer cycle time
67	0078h*	2	Minimum PIO transfer cycle time without flow control
68	0078h*	2	Minimum PIO transfer cycle time with IORDY flow control
69	4D20h	2	Trimmed range returning zeros, 28-bit commands supported, download microcode DMA, write/read Buffer DMA, deterministic read after TRIM
70-74	0000h	10	Reserved
75	001Fh	1	Queue Depth
76	830Eh	2	SATA Capabilities
77	0086h	2	Additional SATA Capabilities
78	014Ch	2	SATA feature support
79	0040h*	2	SATA features enabled (host changeable)
80	03F0h	2	Major revision
81	0000h	2	Minor revision
82 -84	746Bh* 7701h* 4063h*	6	Features/command sets supported
85-87	7469h* 7469h* 4063h*	6	Features/command sets enabled (may change in operation)
88	407Fh*	2	UDMA mode supported
89	0002h*	2	Time for security erase unit completion
90	0002h*	4	Time for enhanced security erase completion
91	0000h	2	Power Management
92	FFFEh*	2	Master password revision code

Word(s)	Default Value	Total Bytes	Data Field Type Information
93-99	0000h*	14	Reserved
100-103	XXXXh	8	Max user LBA48 address feature set
104-105	0000h	4	Reserved
106	4000h	2	Sector size
107-118	0000h	24	Reserved
119-120	4018h 4018h	4	Command set supported settings Command set features enabled
121-127	0000h	14	Reserved
128	0021h*	2	Security status (may change in operation)
129-159	XXXXh	62	"Swissbit SSD"
160	0000h*	2	Power requirement
161	0000h	2	Reserved
162	0000h	2	Management schemes
163	0000h	2	IDE Timing
164	0000h	2	IO Timing
165-168	0000h	8	Reserved
169	0001h	2	Data Set Management supported
170-208	XXXXh	78	Reserved
209	4000h	2	Logical block alignment
210-216	0000h	14	Reserved
217	0001h*	2	Nominal media rotation rate: Solid State Device
218-221	0000h	8	Reserved
222	107Fh	2	Transport major revision
223-233	0000h	22	Reserved
234	0001h	2	Minimum number of 512-byte units per segmented download
235	0200h	2	Maximum number of 512-byte units per segmented download
236-254	0000h	38	Reserved
255	XXXXh	2	Integrity Word

* Standard values for full functionality are listed. Values depend on device configuration.

9. S.M.A.R.T. Functionality

The F-66 SSD fully supports the ATA Specification for Self-Monitoring, Analysis and Reporting Technology (S.M.A.R.T.).

9.1 S.M.A.R.T. Subcommands

The following Table 16 lists the supported S.M.A.R.T. subcommands and the Features register values.

Table 16: S.M.A.R.T. Features Supported

Features	Operation
D0h	S.M.A.R.T. Read Data
D1h	S.M.A.R.T. Read Attribute Thresholds
D2h	S.M.A.R.T. Enable/Disable Autosave
D3h	S.M.A.R.T. Save Attribute Values
D4h	S.M.A.R.T. Execute Off-Line Immediate
D5h	S.M.A.R.T. Read Log
D6h	S.M.A.R.T. Write Log
D7h	S.M.A.R.T. Write Attribute Thresholds
D8h	S.M.A.R.T. Enable Operations
D9h	S.M.A.R.T. Disable Operations
DAh	S.M.A.R.T. Return Status

The device aborts any S.M.A.R.T. subcommands with Features register values not listed in the above table.

9.2 S.M.A.R.T. Read Data

When the drive receives the S.M.A.R.T. Read Data subcommand, it returns one sector (512 bytes) of data. See the following Table 17 for the data structure of this sector.

Table 17: S.M.A.R.T. Data Structure

Byte(s)	Value	Description
0-1	0100h	S.M.A.R.T. structure version
2-361	XXh	Attribute entries 1 to 30 (see Table 19)
362	00h	Off-line data collection status (no off-line data collection started)
363	00h	Self-test execution status byte (self-test completed)
364-365	0000h	Total time, in seconds, to complete off-line data collection
366	00h	Vendor specific
367	00h	Off-line data collection capability (no off-line data collection)
368-369	0002h	S.M.A.R.T. capabilities
370	01h	Error logging capability
371	00h	Vendor specific
372	01h	Short self-test routine recommended polling time, in minutes
373	01h	Extended self-test routine recommended polling time, in minutes
374	01h	Conveyance self-test routine recommended polling time, in minutes
375-385	00h	Reserved
386-395	XXh	Firmware version in ASCII
396-399	00h	Reserved
400-405	XXh	Controller model in ASCII ("SM2246")
406-510	00h	Reserved
511	XXh	Data structure checksum

9.3 S.M.A.R.T. Attributes

The F-66 drives support the S.M.A.R.T. attributes listed in the following Table 18.

Table 18: S.M.A.R.T. Attributes

ID	Worst	Threshold	Attribute	Description
01h	100	0	Raw Read Error Rate	Total number of Cyclic Redundancy Check (CRC) errors that occurred over the SATA interface
05h	100	0	Reallocated Sector Count	Total number of runtime identified (field marked) bad blocks
09h	100	0	Power-On Hours	Total hours that the device has been powered on and operational (not in Sleep mode)
0Ch	100	0	Power Cycle Count	Total number of power cycles that have occurred during the life of the drive
A0h	100	0	Uncorrectable Sector Count	Total number of sectors read (active or passive) with UECC errors
A1h	100	25*	Spare Blocks	Total number of spare blocks currently available
A3h	100	0	Number of Initial Invalid Blocks	Total number of initially identified (factory marked and pretest) bad blocks
A4h	100	0	Total Erase Count	Total number of erase operations that have ever been performed on all currently valid blocks (excluding the system, bad and reserved blocks)
A5h	100	0	Maximum Erase Count	The maximum number of erase operations that have ever been performed on a single block (excluding the system, bad and reserved blocks)
A6h	100	0	Minimum Erase Count	The minimum number of erase operations that have ever been performed on a single block (excluding the system, bad and reserved blocks)
A7h	100	1*	Average Erase Count	The average number of erase operations that have ever been performed on a single block (excluding the system, bad and reserved blocks)
A8h	100	0	Maximum Specified Erase Count	The specified maximum erase count; equivalent to number of program/erase (P/E) cycles rated for the device
A9h	100	0	Power on UECC Count	The number of uncorrectable errors encountered during a power up event
C0h	100	0	Initial Spare Block Count	Total number of original spare blocks
C1h	100	0	Dynamic Remaps	Total number of dynamic remap operations
C2h	100	0	Temperature	Temperature (minimum, maximum, and current) of the device
C3h	100	0	Flash ECC Recovered	Total number of times the read-retry process was required to recover data
C4h	0	0	Reallocation Event Count	Total count of remapping operations
C6h	100	0	Uncorrectable Sector Count Offline	Total number of sectors read (active only) with UECC errors
C7h	100	0	SATA PHY CRC Error Count	Total count of PHY errors (including CRC) that occurred over the interface cable
D7h	100	0	TRIM Count	Total number of TRIM commands issued by the host
EBh	100	0	Total Flash LBAs Written	The lower 7 bytes of the total number of LBAs (in 32 KByte increments) written to the flash; the higher 5 bytes are located in attribute EDh
EDh	100	0	Total Flash LBAs Written Expanded	The upper 5 bytes of the total number of LBAs (in 32 KByte increments) written to the flash; the lower 7 bytes are located in attribute EBh
F1h	100	0	Total Host LBAs Written	The lower 7 bytes of the total number of LBAs written to the device by the host; the higher 5 bytes are located in attribute F3h
F2h	100	0	Total Host LBAs Read	The lower 7 bytes of the total number of LBAs read from the device by the host; the higher 5 bytes are located in attribute F4h
F3h	100	0	Total Host LBAs Written Expanded	The upper 5 bytes of the total number of LBAs written to the device by the host; the lower 7 bytes are located in attribute F1h

ID	Worst	Threshold	Attribute	Description
F4h	100	0	Total Host LBAs Read Expanded	The upper 5 bytes of the total number of LBAs read from the device by the host; the lower 7 bytes are located in attribute F2h
F8h	100	0	SSD Remaining Life	Percent of SSD life remaining on the SSD (a value from 0 to 64h), normalized to 100; based upon Average Erase Count (A7h) scaled by the Maximum Specified Erase Count (A8h)
F9h	100	0	Spare Block Remaining Life	Percent of spare blocks remaining

* These threshold values are changeable using the Write Attribute Thresholds command.

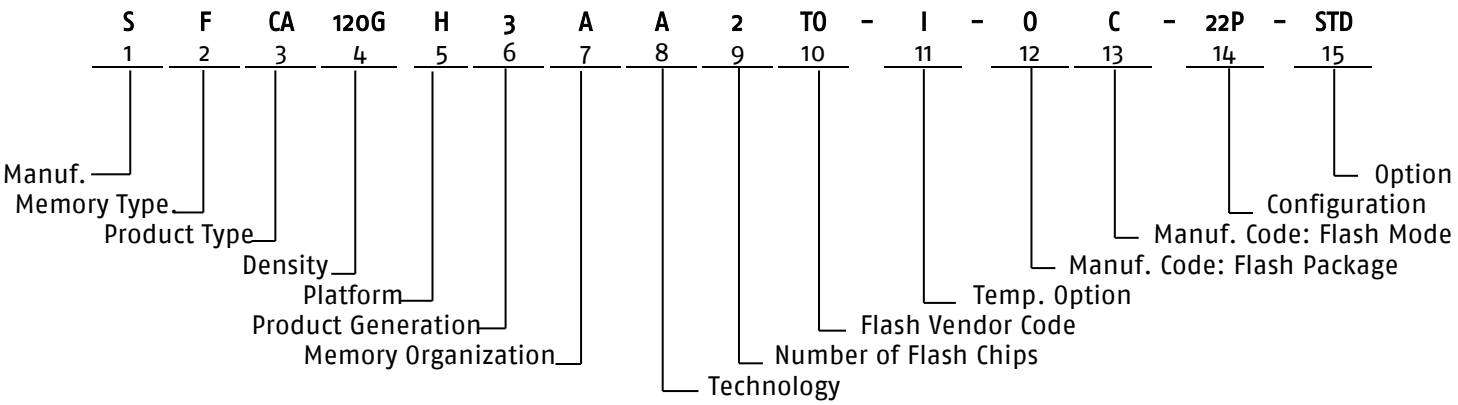
9.4 S.M.A.R.T. Attribute Entry Structure

Each attribute entry consists of 12 bytes. See the following Table 19 for the data structure of each entry.

Table 19: Attribute Entry

Byte(s)	Value	Description
0	XXh	Attribute ID (see Table 18)
1–2	XXXXh	Flags (little-endian)
3	XXh	Attribute value as a percentage
4	XXh	Worst value as a percentage
5–8	XXXXh	Raw value (little-endian)
9–11	00h	Reserved

10. Part Number Decoder



10.1 Manufacturer

Swissbit code	S

10.2 Memory Type

Flash	F

10.3 Product Type

CFast Interface	CA

10.4 Density

4 GBytes	004G
8 GBytes	008G
16 GBytes	016G
30 GBytes	030G
60 GBytes	060G
120 GBytes	120G

10.5 Platform

CFast SSD	H

10.6 Product Generation

10.7 Memory Organization

x8	A

10.8 Technology

F-66 Series	A

10.9 Number of Flash Chips

1 Flash	1
2 Flash	2

10.10 Flash Code

Toshiba	T0

10.11 Temperature Option

Commercial Temperature Range: 0 °C to 70 °C	C
Industrial Temperature Range: -40 °C to 85 °C	I

10.12 Die Classification

MLC MONO (single die package)	G
MLC DDP (dual die package)	L
MLC QDP (quad die package)	H
MLC ODP (octal die package)	O

10.13 Pin Mode

	TSOP	BGA
Single nCE and Single R/nB	S	A
Dual nCE and Dual R/nB	T	B
Quad nCE and Quad R/nB	U	C
Octal nCE and Octal R/nB	*	V
Sexdec nCE & Sexdec R/nB	*	W

*Not Available

10.14 Drive configuration XYZ

X = Type

Drive Mode	PIO	DMA Support	X
Fix	Yes	Yes	2

Y = Firmware Revision

FW Revision	Y
SBR13037	2

Z = Feature

Feature	Z
pSLC	P

10.15 Option

Standard	STD

11. Marking Specification

11.1 Top View

Figure 4: F-66 top view

11.2 Bottom View

Figure 5: F-66 top view

11.3 Label Content

- Swissbit Logo
- CFast Logo
- Part Number
- Lot Code information with Bar Code
- CE Logo
- RoHS Logo
- WEEE Logo
- Manufacturing Date
- Country of Origin

12. Revision History

Table 20: Document Revision History

Date	Revision	Description	Revision Details
9-Jun-2017	01	Initial draft.	
30-Aug-2017	1.00	Initial release.	Doc. req. no. 1837
26-Oct-2018	1.01	Updated endurance values for 4GB and 8GB, Current Consumption data, part number decoder sections and feature icons.	Doc. req. no. 2639
16-Apr-2019	1.02	Part number of 4GB density corrected, updated sections to meet standard data sheet review criteria.	Doc. req. no. 2882
22-Oct-2019	1.03	Minor information and formatting changes	Doc. req. no. 3230
31-Oct-2019	1.04	Fixed typo	Doc. req. no. 3248