User Guide

EVAL-ADAU1850

Evaluating the ADAU1850 Three ADCs, One DAC, Low Power Codec with Audio/ Fast DSP

EVALUATION KIT CONTENTS

- EVAL-ADAU1850EBZ evaluation board
- USB cable with mini USB plug

DOCUMENTS NEEDED

- ADAU1850 data sheet
- EVAL-ADAU1850EBZ user guide

GENERAL DESCRIPTION

This user guide explains the design and setup of the EVAL-ADAU1850EBZ evaluation board.

This evaluation board provides access to all analog and digital inputs/outputs on the ADAU1850. The ADAU1850 core is controlled by Analog Devices, Inc., Lark Studio™ software, which interfaces to the EVAL-ADAU1850EBZ via a USB connection. The software development kit (SDK) is also provided by Analog Devices for code development.

The EVAL-ADAU1850EBZ can be powered by the USB bus or by a single 3.8 V to 5 V supply. These supply options are regulated to the voltages required on the EVAL-ADAU1850EBZ. The printed circuit board (PCB) is a 4-layer design, with a ground plane and a power plane on the inner layers. The EVAL-ADAU1850EBZ contains connectors for external microphones and speakers. The master clock can be generated through the internal RC oscillator in the absence of an external clock source. It also can be provided externally or by the on-board 24.576 MHz oscillator.

EVAL-ADAU1850EBZ BOARD PHOTOGRAPH

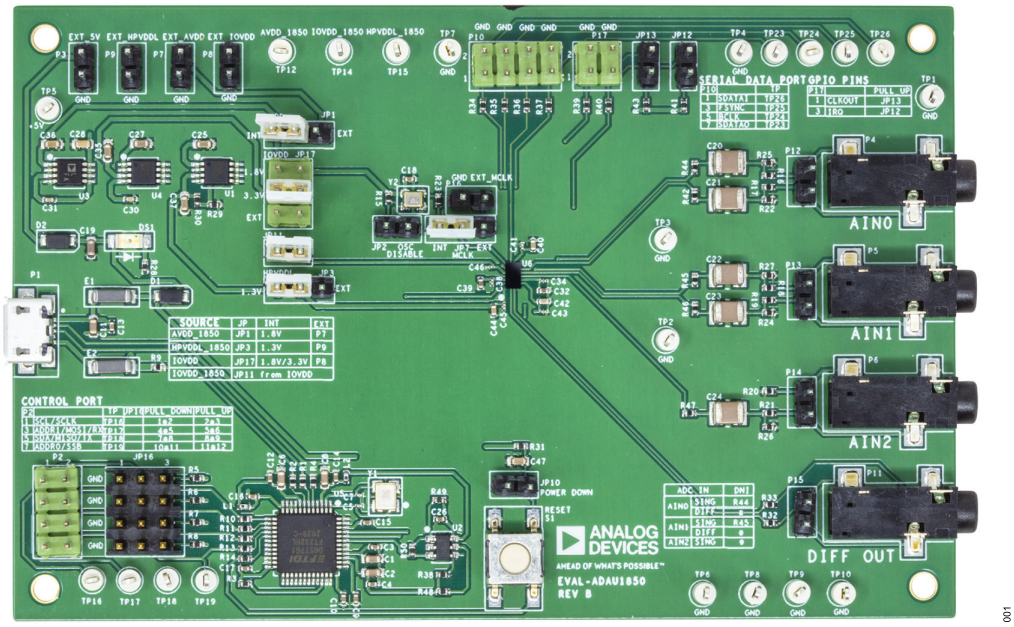

Figure 1.

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REVISION HISTORY

10/2022—Rev. 0 to Rev. A

Changes to General Description Section 1
Changes to Master Clock Options Section 4
Changes to Creating a Basic Flown Section 5
Changes to Clock Option Section 8

7/2021—Revision 0: Initial Version

EVALUATION BOARD BLOCK DIAGRAM

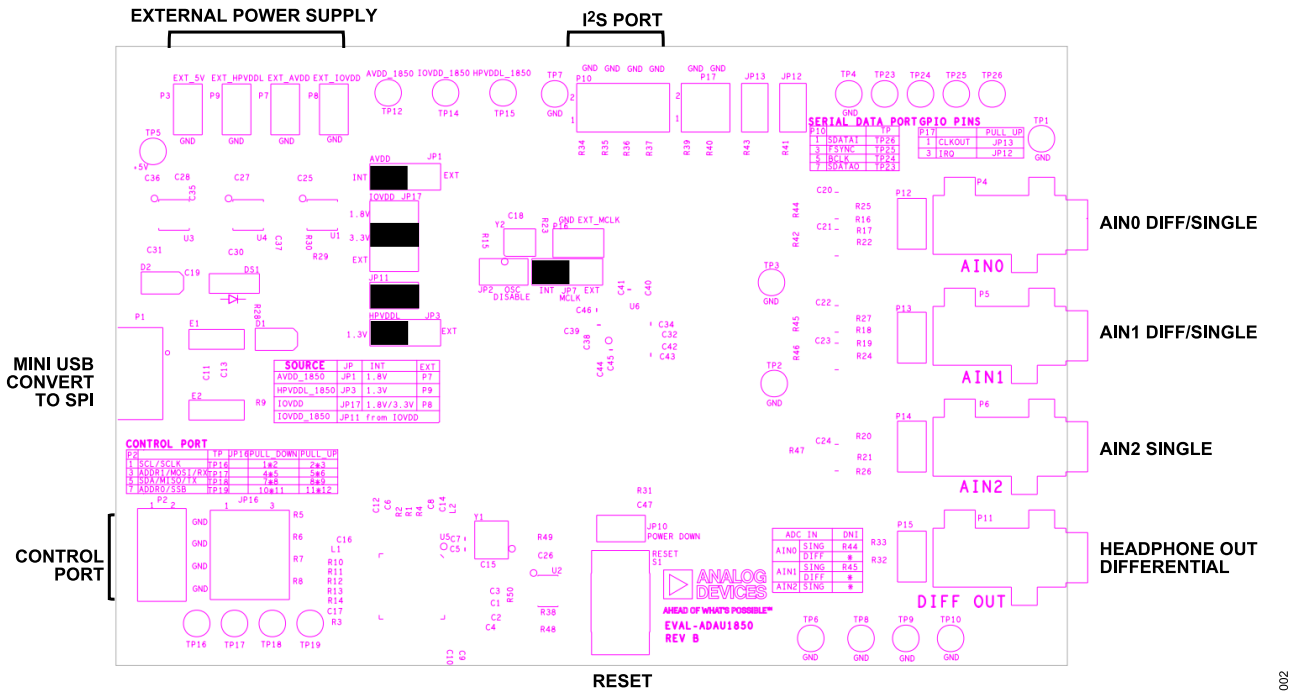

Figure 2. EVAL-ADAU1850EBZ Board Block Diagram

SETTING UP THE EVALUATION BOARD

INSTALLING THE LARK STUDIO SOFTWARE

Download and install the latest version of Lark Studio by completing the following steps:

1. Download the installer, and run the executable file.
2. Follow the prompts, including accepting the license agreement, to install the software.

INSTALLING THE USB DRIVERS

If the USB interface is not recognized by the Lark Studio software and PC, go to the Future Technology Devices International (FTDI) Chip official web page and download the relevant drivers.

DEFAULT SWITCH AND JUMPER SETTINGS

The JP3, JP1, JP11, and JP17 jumpers are used to set the HPVDD_L, AVDD, and IOVDD supplies to the ADAU1850. The external supply must be connected to P3, P7, P8, or P9.

MASTER CLOCK OPTIONS

The EVAL-ADAU1850EBZ has three options for providing a master clock to the ADAU1850. The first option is to provide an external master clock (MCLK) signal directly to the CLKIN pin of the codec. The second option is to use the on-board 24.576 MHz oscillator. The third option is to use the internal RC oscillator to generate a master clock without an external clock source.

SETTING UP COMMUNICATION IN SOFTWARE

POWERING UP THE BOARD

To power up the evaluation board, connect the ribbon cable to P1 of the EVAL-ADAU1850EBZ.

CONNECTING THE AUDIO CABLES

Two channels of the microphone inputs are differential, and one is single-ended. The headphone output is differential and is dc-coupled. Digital audio signal can be I^2S or TDM mode through the serial audio interface.

CREATING A BASIC SIGNAL FLOW

To create a basic signal flow in LARK Studio, follow these steps:

1. Download Lark Studio from www.analog.com/ADAU1850 to the desktop.
2. Start Lark Studio by double clicking the shortcut on the desktop.
3. Click **New Project** from the **Project** menu, or click **Create a New Project** in the **Welcome** section to create a new project, as shown in Figure 3. The **New Project** window shows the **Project Type** options.
4. Click the **Lark-Lite** option for the ADAU1850 and then **OK**.
5. Edit the file name, and save the file to a user specified location.
6. Click **Target Connection** in the left navigation panel, and configure the **Connection settings** pane that opens on the right to set up the connection. If the USB connects, **Target Connected** displays (see Figure 4).

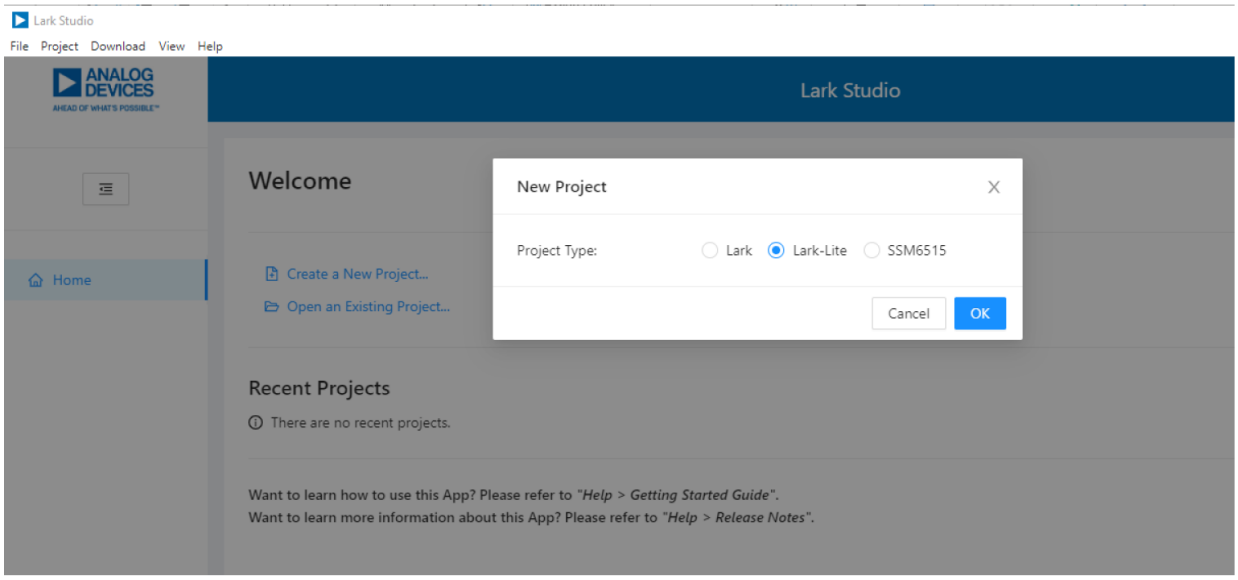

Figure 3. Create a New Project

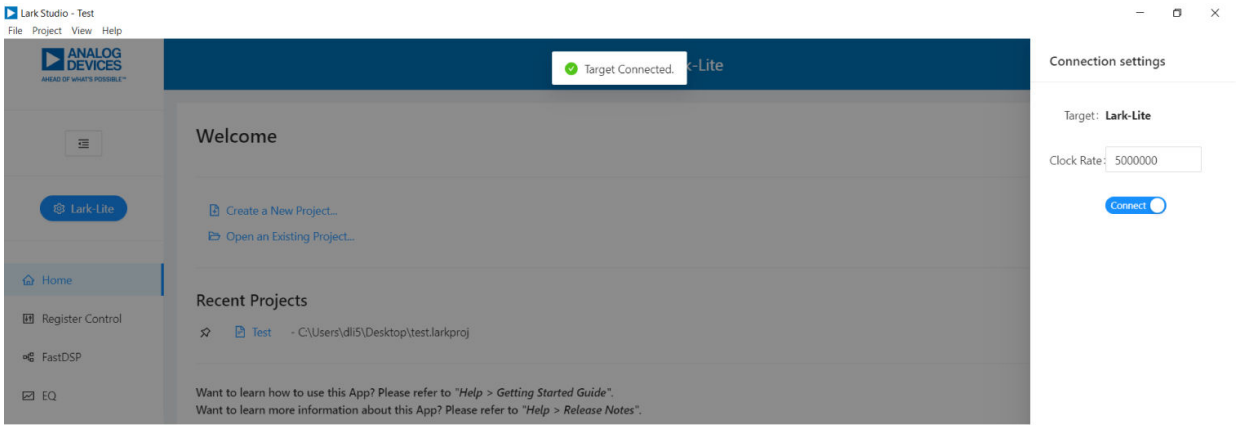

Figure 4. Connect with EVAL-ADAU1850EBZ

SETTING UP COMMUNICATION IN SOFTWARE

Configure the **Register Control**, **FastDSP**, and **EQ** settings on the left navigation panel. **Lark-Lite Register Control** has multiple tabs that control different sections of the ADAU1850. Figure 5 shows the **Power** tab, which allows the user to power up or power down various blocks within the ADAU1850. When a block is powered up, that block can be configured.

The **Clock** tab allows the PLL to be used or bypassed. By register default, the PLL is enabled but bypassed to save power. To generate a 24.576 MHz master clock, enable or disable the PLL according to the provided clock source. On the evaluation board, a 24.576 MHz oscillator is supplied.

To configure an application, follow these steps:

1. Enable **POWER_EN**, **MASTER_BLOCK_EN**, and **CM_START-UP_OVER** in the **CHIP_PWR** block in the **Power** tab by clicking the **OFF** button to switch to **ON** (see Figure 5). When an on-board 24.576 MHz oscillator is used, ensure MCLKIN_EN is enabled in the **Clock** tab.
2. With the default 24.576 MHz oscillator on board, set **PLL_FM_BYPASS** to **PLL_FM_BP** in the **Clock** tab.
3. Configure the other blocks.

When a register value is changed, click the related **Write** button in a block to update a single register, or the **Write this Page** button below the tabs to update multiple registers. Click **Write All** after all register changes to avoid a configuration error.

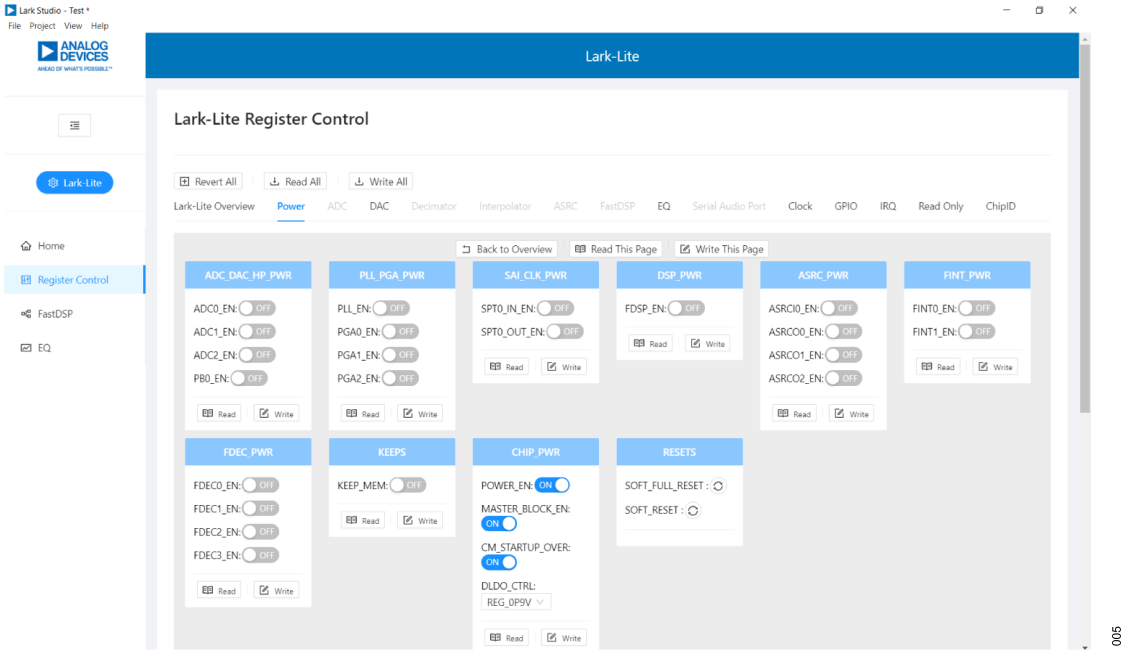

Figure 5. Register Configuration

SETTING UP COMMUNICATION IN SOFTWARE

If FastDSP is needed in the project, a schematic must be created with the desired path for the ADAU1850.

1. Click **FastDSP** in the left navigation panel.
2. In the left pane of the **Lark-Lite FastDSP Schematic** window, click an arrow to expand a folder.
3. Select and drag an icon into the schematic window, for example, the **ADC** icon within the **IO** folder (see Figure 6). In this example, AIN1 and ASRCI are being routed to FastDSP **Output 0** and **Output 1**.
4. To download the correct parameter generated from the schematic, set **fs** to be the same as the FastDSP source, **FDSP_RATE_SOURCE**, which is set in the **FastDSP** tab in the **Lark-Lite Register Control** window.
5. Click **Download to Target** to write the parameter and command to FastDSP memory. After the download finishes, FastDSP is enabled and runs automatically.

If the equalizer is needed in the project, a configuration of the filters must be set for the ADAU1850.

1. Click **EQ** in the navigation panel.
2. Select the filter numbers and relative filter parameters.
3. Set **fs** to be same as the equalizer source, **EQ_ROUTE**, which is set in the **EQ** tab in the **Lark-Lite Register Control** window.
4. Click **Download to Target** to write the parameter and command to equalizer memory. After the download finishes, the equalizer is enabled and runs automatically.

For full details on the operation of **Lark-Lite**, click **Getting Start Guide** from the **Help** menu of the Lark Studio GUI.

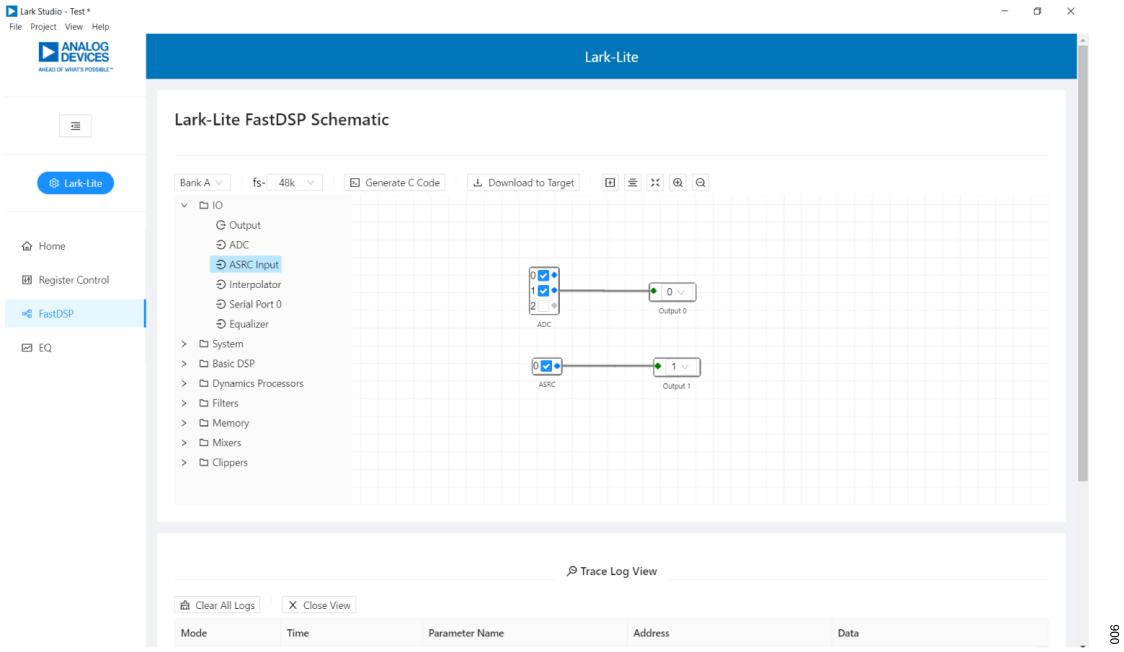

Figure 6. FastDSP Schematic Configuration

USING THE EVALUATION BOARD

POWER SUPPLY

Power can be supplied to the EVAL-ADAU1850EBZ in one of three ways:

- Connecting the USB cable to P1 (see Figure 2)
- Connecting a 3.8 V to 5 V dc power to P3
- Connecting an isolated external power supply to P7 for AVDD, P8 for IOVDD, and P9 for HPVDD_L

If using a 5 V power supply, the on-board regulator generates the 1.8 V, 3.3 V, and 1.3 V dc supplies. The 1.3 V dc supply from U1 can be adjusted by changing the values of R29 and R30. For detailed power supply and jumpers, refer to Table 1. When using the default SPI communication on board, the IOVDD supply can only be jumped to 3.3 V.

Table 1. Power Supply Jumper Settings

Source	Jumpers	Internal	External
AVDD_1850	JP1	1.8 V	P7
HPVDDL_1850	JP3	1.3 V	P9
IOVDD	JP17	1.8 V or 3.3 V	P8
IOVDD_1850	JP11 from IOVDD	JP11 from IOVDD	JP11 from IOVDD

CONTROL PORT

The EVAL-ADAU1850EBZ is configured to SPI mode by default. To operate the codec in I^2C or universal asynchronous receiver/transmitter (UART) mode, R10 to R14 are recommended to be uninstalled. By default, these resistors are connected. For detailed connection and jumpers on P2 and JP16, refer to Table 2.

Table 2. Control Port Settings

P2	Pin Name	Test Point	JP16 Pull-Up	JP16 Pull- Down
1	SCL/SCLK	TP16	Pin 1 and Pin 2	Pin 2 and Pin 3
3	ADDR1/MOSI/RX	TP17	Pin 4 and Pin 5	Pin 5 and Pin 6
5	SDA/MISO/TX	TP18	Pin 7 and Pin 8	Pin 8 and Pin 9
7	ADDR0/$\overline{SS}$	TP19	Pin 10 and Pin 11	Pin 11 and Pin 12

CODEC SYSTEM

Clock Option

The EVAL-ADAU1850EBZ has three options for providing a master clock to the ADAU1850. The first option is to provide an external MCLK signal directly to the CLKIN pin of the codec from P16 and disable the on-board oscillator by placing a jumper on Header JP2. The second option is to use the on-board 24.576 MHz oscillator. These two options can be chosen through JP7. The third option is to use the internal RC oscillator to generate a master clock where JP2 needs to be jumped to disable the on-board oscillator.

Power-Down

The EVAL-ADAU1850EBZ can power down all analog and digital circuits of the codec in two ways: pressing the S1 button or placing a jumper on the JP10 header.

Inputs and Outputs

The EVAL-ADAU1850EBZ has multiple audio input and output options, including digital and analog. Three analog inputs are configurable as microphone or line inputs. Two of these analog inputs are differential or single-ended, and one is only single-ended. One differential output can also be used in headphone or line output mode.

For microphone signals, the two differential (ADC0 and ADC1) ADAU1850 analog inputs can be configured as single-ended inputs with an optional programmable gain amplifier (PGA) mode. But the ADC2 can only be single-ended with an optional PGA mode. The headphone output can be set as a line output driver or as a headphone driver. In line output mode, the typical load is 10 kΩ. In headphone output mode, the typical load is 16 Ω to 32 Ω.

Serial Audio Interface

Serial audio signals in I^2S, left justified, right justified, or time division multiplexed (TDM) format are available via the P10 serial audio interface header to connect an external I^2S- or TDM-compatible device. The IOVDD logic level is 1.8 V or 3.3 V.

HARDWARE DESCRIPTION

JUMPERS

Table 3. Connector and Jack Descriptions

Reference Designator	Function	Description
P1	USB interface	USB 5 V power and communication with Lark Studio
P2	Control port	Allow three ways of communication: SPI, I^2C, and UART
P3	External 5 V	External 5 V source
P4	Analog Input 0	Default differential input 3.5 mm jack
P5	Analog Input 1	Default differential input 3.5 mm jack
P6	Analog Input 2	Single-ended input 3.5 mm jack
P7	External AVDD	AVDD power from external source
P8	External IOVDD	IOVDD power from external source
P9	External HPVDDL	HPVDD_L power from external source
P10	Serial data port	Input and output header for serial audio signals
P11	Analog Output	Differential output
P12	Analog Input 0	Default differential input pins connection
P13	Analog Input 1	Default differential input pins connection
P14	Analog Input 2	Single ended input pins connection
P15	Analog output	Differential output pins connection
P16	External clock	Master clock from external source
P17	IRQ/MCLKO pull-up	Select IRQ or master clock output pull-up
JP1	Internal/external AVDD select	Used to select the external AVDD source or on-board regulator for AVDD
JP2	Disable oscillator	Used to disable on-board oscillator
JP3	Internal/external HPVDD_L select	Used to select the external HPVDD_L source or on-board regulator for HPVDD_L.
JP7	Internal/external MCLK select	Used to select the external source or oscillator
JP10	Power-down	Used to enter power-down mode
JP11	IOVDD_1850	Used to provide IOVDD source to the ADAU1850
JP12	IRQ pull-up	Used to pull up IRQ pin
JP13	MCLKO pull-up	Used to pull up CLKOUT/IRQ pin
JP16	Control port pull-up/down select	Used to pull up or pull down control pins (SCL/SCLK, SDA/MISO/TX, ADDR1/MOSI/RX, and ADDR0/$\overline{SS}$)
JP17	Internal/external IOVDD select	Used to select the external IOVDD source or on-board regulator for IOVDD

EVALUATION BOARD SCHEMATIC

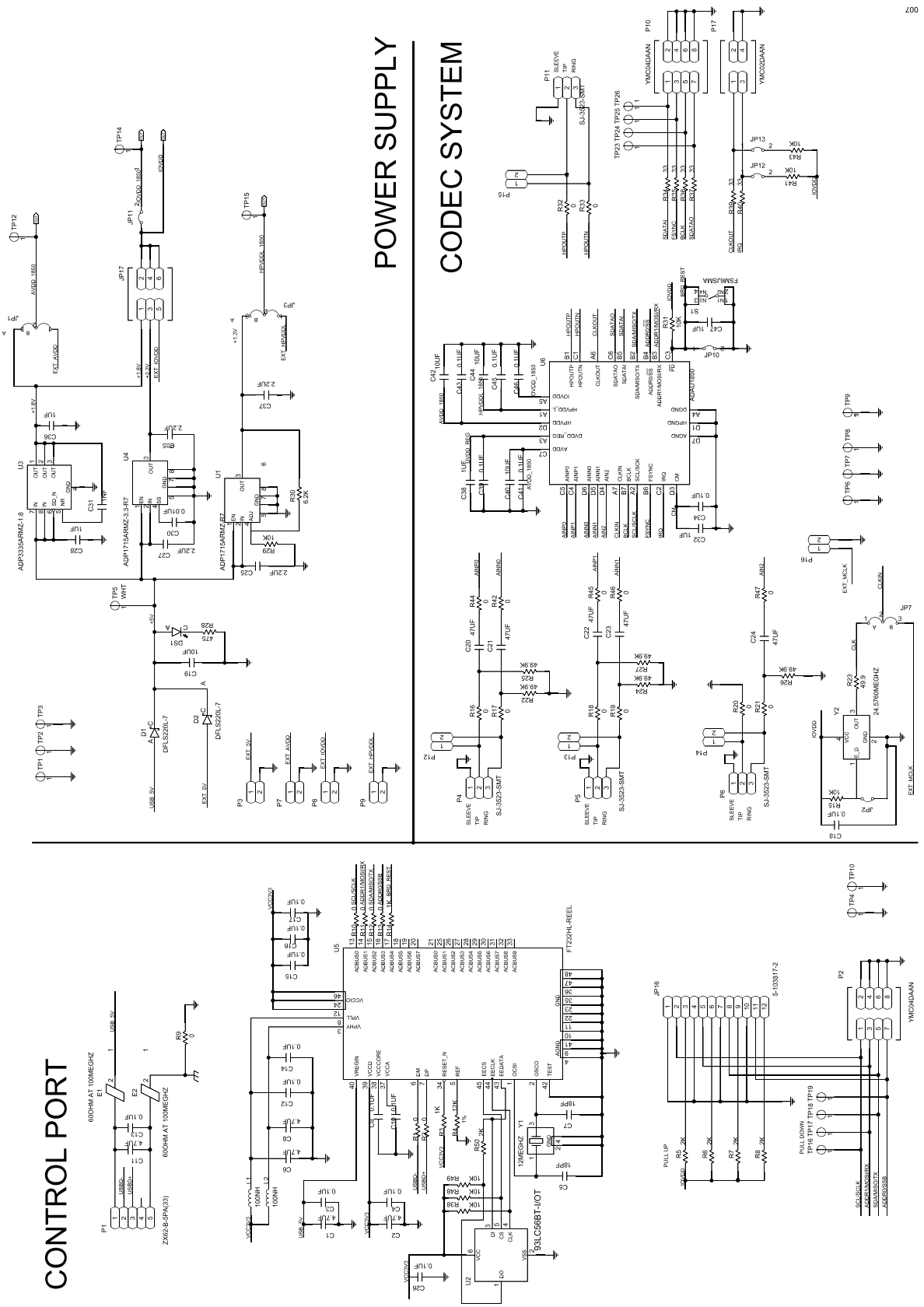

Figure 7. Evaluation Board Schematic

ORDERING INFORMATION

BILL OF MATERIALS

Table 4.

Qty	Reference Designator	Description	Value	Vendor Order Number
5	C1, C2, C6, C8, C11	4.7 µF, 25 V, 10%, X5R, 0603 ceramic capacitors	4.7 µF	GRT188R61E475KE13D
12	C3, C4, C9, C10, C12, C13, C14, C15, C16, C17, C18, C26	0.1 µF, 25 V, 10%, X7R, 0402, ceramic capacitors	0.1 µF	GRM155R71E104KE14D
1	C19	10 µF, 25 V, 10%, X5R, 0603, ceramic capacitor	10 µF	GRM188R61E106KA73D
5	C20, C21, C22, C23, C24	47 µF, 6.3 V, 10%, X7R, 1210, ceramic capacitors	47 µF	GCJ32ER70J476KE19L
4	C25, C27, C35, C37	2.2 µF, 25 V, 10%, X5R, 0603, ceramic capacitors	2.2 µF	GRM188R61E225KA12D
3	C28, C36, C47	1 µF, 25 V, 10%, X7R, 0603, ceramic capacitors	1 µF	GCM188R71E105KA64D
1	C30	0.01 µF, 25 V, 10%, X7R, 0402, ceramic capacitors	0.01 µF	C1005X7R1E103K050BB
1	C31	1 nF, 25 V, 10%, X7R, 0402, ceramic capacitors	1 nF	04023C102KAT2A
2	C32, C38	1 µF, 6.3 V, 10%, X7R, 0402, ceramic capacitors	1 µF	GRM155R70J105KA12D
5	C34, C39, C41, C43, C45	0.1 µF, 6.3 V, 10%, X5R, 0201, ceramic capacitors	0.1 µF	GRM033R60J104KE19D
1	C46	Surface-mount device (SMD)/surface-mount technology (SMT), 0201, 0.1 µF, 10 V, X5R, 10% multilayer ceramic capacitor	0.1 µF	GRM033R61A104KE15D
3	C40, C42, C44	10 µF, 6.3 V, 20%, X5R, 0402, ceramic capacitors	10 µF	GRM155R60J106ME15J
2	C5, C7	18 pF, 25 V, 5%, C0G, 0201, ceramic capacitors	18 pF	GRM0335C1E180JA01D
2	D1, D2	Schottky diode barrier rectifier	DFLS220L-7	DFLS220L-7
2	E1, E2	Inductor, ferrite bead	80 Ω at 100 MHz	BLM41PF800SN1L
2	L1, L2	Inductor, RF ceramic chip	100 nH	L-07CR10JV6T
1	P1	Connector PCB, micro USB 2.0, right angle, 0.65 mm pitch	ZX62-B-5PA(33)	ZX62-B-5PA(33)
4	P4, P5, P6, P11	Connector PCB, 3.5 mm, surface-mount audio jack stereo	SJ-3523-SMT	SJ-3523-SMT
20	R1, R2, R9, R10, R11, R12, R13, R16, R17, R18, R19, R20, R21, R32, R33, R42, R44, R45, R46, R47	0 Ω jumper, 1/16 W, 0402	0 Ω	RC0402JR-070RL
2	R3, R14	SMD, 1 kΩ, 1%, 1/10 W, 0402 resistors	1 kΩ	ERJ-2RKF1001X
8	R15, R29, R31, R38, R41, R43, R48, R49	SMD, 10 kΩ, 5%, 1/10 W, 0402 resistors	10 kΩ	ERJ-2GEJ103X
5	R22, R24, R25, R26, R27	SMD 49.9 kΩ, 1%, 1/10 W, 0402 resistors	49.9 kΩ	ERJ-2RKF4992X
1	R23	SMD 49.9 Ω, 1%, 1/10 W, 0402 resistor	49.9 Ω	ERJ-2RKF49R9X
1	R28	SMD 475 Ω, 1%, 1/10 W, 0402 resistor	475 Ω	ERJ-2RKF4750X
1	R30	SMD 6.2 kΩ, 5%, 1/10 W, 0402 resistor	6.2 kΩ	ERJ-2GEJ622X
6	R34, R35, R36, R37, R39, R40	SMD 33 Ω, 1%, 1/10 W, 0402 resistors	33 Ω	ERJ-2RKF33R0X
1	R4	SMD 12 kΩ 1%, 1/16 W, 0402 resistor	12 kΩ	RC0402FR-0712KL
5	R5, R6, R7, R8, R50	SMD 2 kΩ, 1%, 1/10 W, 0402 resistors	2 kΩ	ERJ-2RKF2001X
1	U1	500 mA low dropout (LDO) CMOS linear regulator	ADP1715ARMZ-R7	ADP1715ARMZ-R7
1	U2	Electrically erasable programmable read only memory (EEPROM)	93LC56BT-I/OT	93LC56BT-I/OT
1	U3	High accuracy, ultralow LDO regulator	ADP3335ARMZ-1.8	ADP3335ARMZ-1.8
1	U4	500 mA, low dropout CMOS linear regulator	ADP1715ARMZ-3.3-R7	ADP1715ARMZ-3.3-R7
1	U5	USB to multipurpose UART/first in, first out (FIFO)	FT232HL-REEL	FT232HL-REEL
1	U6	ADAU1850 Lark-Lite	ADAU1850	ADAU1850
1	Y1	12 MHz, 10 ppm, 18 pF, 3.2 mm × 2.5 mm × 0.8 mm	12 MHz	ABM8AIG-12.000MHZ-1Z-T
1	Y2	IC crystal clock oscillator	24.5760 MHz	KC2520K24.5760C10E00

ORDERING INFORMATION

NOTES

I^2C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).