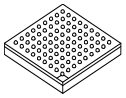
NXP Semiconductors
Data Sheet: Technical Data

Document Number: IMX8MNCEC
Rev. 0, 10/2019

MIMX8MN6DVTJZAA **MIMX8MN6DVTJZCA**
MIMX8MN6DVTJZDA **MIMX8MN5DVTJZAA**
MIMX8MN4DVTJZAA **MIMX8MN3DVTJZAA**
MIMX8MN2DVTJZAA **MIMX8MN1DVTJZAA**

i.MX 8M Nano Applications Processor Datasheet for Consumer Products



Package Information
Plastic Package
FCBGA 14 x 14 mm, 0.5 mm pitch

Ordering Information
See Table 2 on page 6

1 i.MX 8M Nano introduction

The i.MX 8M Nano application processor represents NXP's latest graphics and audio experience combining state-of-the-art media-specific features with high-performance processing while optimized for lowest power consumption.

The i.MX 8M Nano family of processors features advanced implementation of a quad Arm® Cortex®-A53 core, which operates at speeds of up to 1.5 GHz. A general purpose Cortex®-M7 running up to 750 MHz core processor is for real-time and low-power processing.

The i.MX 8M Nano family of processors provides additional computing resources and peripherals:

- Advanced security modules for secure boot, cipher acceleration and DRM support
- A wide range of audio interfaces, including I2S, AC 97, TDM, and S/PDIF
- Large set of peripherals that are commonly used in consumer/industrial market, including USB and Ethernet

Table 1. Features

Subsystem	Feature
Cortex®-A53 MPCore platform	Quad symmetric Cortex® -A53 processors • 32 KB L1 Instruction Cache • 32 KB L1 Data Cache • Media Processing Engine (MPE) with Arm® NEON™ technology supporting the Advanced Single Instruction Multiple Data architecture: • Floating Point Unit (FPU) with support of the Arm® VFPv4-D16 architecture
	Support of 64-bit Arm®v8-A architecture
	512 KB unified L2 cache
Cortex®-M7 core platform	Low power microcontroller available for customer application: • low power standby mode • IoT features including Weave • Manage IR or wireless remote • ML inference applications (enhanced for i.MX 8M Nano)
	Cortex® M7 CPU: • 256 KB tightly coupled memory (TCM)
Connectivity	One USB 2.0 OTG controllers with integrated PHY interfaces: • Spread spectrum clock support
	Three Ultra Secure Digital Host Controller (uSDHC) interfaces: • MMC 5.1 compliance with HS400 DDR signaling to support up to 400 MB/sec • SD/SDIO 3.0 compliance with 200 MHz SDR signaling to support up to 100 MB/sec • Support for SDXC (extended capacity)
	One Gigabit Ethernet controller with support for Energy Efficient Ethernet (EEE), Ethernet AVB, and IEEE 1588
	Four Universal Asynchronous Receiver/Transmitter (UART) modules
	Four I^2C modules
	Three SPI modules
On-chip memory	Boot ROM (256 KB)
	On-chip RAM (512 KB + 32 KB)
GPIO and pin multiplexing	General-purpose input/output (GPIO) modules with interrupt capability
	Input/output multiplexing controller (IOMUXC) to provide centralized pad control
Power management	Temperature sensor with programmable trip points
	Flexible power domain partitioning with internal power switches to support efficient power management

Table 1. Features (continued)

Subsystem	Feature
External memory interface	16-bit DRAM interfaces: • LPDDR4-3200 • DDR4-2400 • DDR3L-1600
	8-bit NAND-Flash, including support for Raw MLC/SLC devices, BCH ECC up to 62-bit, and ONFi3.2 compliance (clock rates up to 100 MHz and data rates up to 200 MB/sec)
	eMMC 5.1 Flash (3 interfaces)
	SPI NOR Flash (3 interfaces)
	QuadSPI Flash with support for XIP (for Cortex®-M7 in low-power mode) and parallel read mode of two identical FLASH devices
Multimedia	Graphic Processing Unit: • GC7000UL with OpenCL and Vulkan support • 2 shader • 99.8 million triangles/sec • 0.6 giga pixel/sec • 9.6 GFLOPs 32-bit/19.2 GFLOPs 16-bit • Supports OpenGL ES 1.1, 2.0, 3.0, OpenCL • Core clock frequency of 600 MHz • Shader clock frequency of 600 MHz
	LCDIF Display Controller: • Support up to 1080p60 display through MIPI DSI
	MIPI Interfaces: • 4-lane MIPI DSI interface • 4-lane MIPI CSI interface
	Audio: • S/PDIF input and output, including a raw capture input mode • Five external synchronous audio interface (SAI) modules supporting I2S, AC97, TDM, codec/DSP, and DSD interfaces, comprising one SAI with 4 Tx and 4 Rx lanes, two SAI with 2 Tx and 2 Rx lanes, and two SAI with 1 Tx and 1Rx lane. All ports support 49.152 MHz BCLK. • ASRC supports processing 32 audio channels, 4 context groups, 8 kHz to 384 kHz sample rate and 1/16 to 8x sample rate conversion ratio. • Pulse Density Modulation (PDM) input

Table 1. Features (continued)

Subsystem	Feature
Security	Resource Domain Controller (RDC): • supports 4 domains and up to 8 regions of DDR
	Arm® TrustZone® (TZ) architecture: • Arm® Cortex-A53 MPCore TrustZone support
	On-chip RAM (OCRAM) secure region protection using OCRAM controller
	High Assurance Boot (HAB)
	Cryptographic acceleration and assurance module (CAAM): • Support Widevine and PlayReady content protection • Public Key Cryptography (PKHA) with RSA and Elliptic Curve (ECC) algorithms • Real-time integrity checker (RTIC) • DRM support for RSA, AES, 3DES, DES • Side channel attack resistance • True random number generation (RNG) • Manufacturing protection support
	Secure non-volatile storage (SNVS): • Secure real-time clock (RTC)
	Secure JTAG controller (SJC)
System debug	Arm® CoreSight™ debug and trace technology
	Trace Port Interface Unit (TPIU) to support off-chip real-time trace
	Embedded Trace FIFO (ETF) with 4 KB internal storage to provide trace buffering
	Unified trace capability for Quad Cortex®-A53 and Cortex®-M7 CPUs
	Cross Triggering Interface (CTI)
	Support for 4-pin (JTAG) debug interface

NOTE

The actual feature set depends on the part numbers as described in Table 2. Functions such as display and camera interfaces, and connectivity interfaces, may not be enabled for specific part numbers.

1.1 Block diagram

Figure 1 shows the functional modules in the i.MX 8M Nano applications processor system.

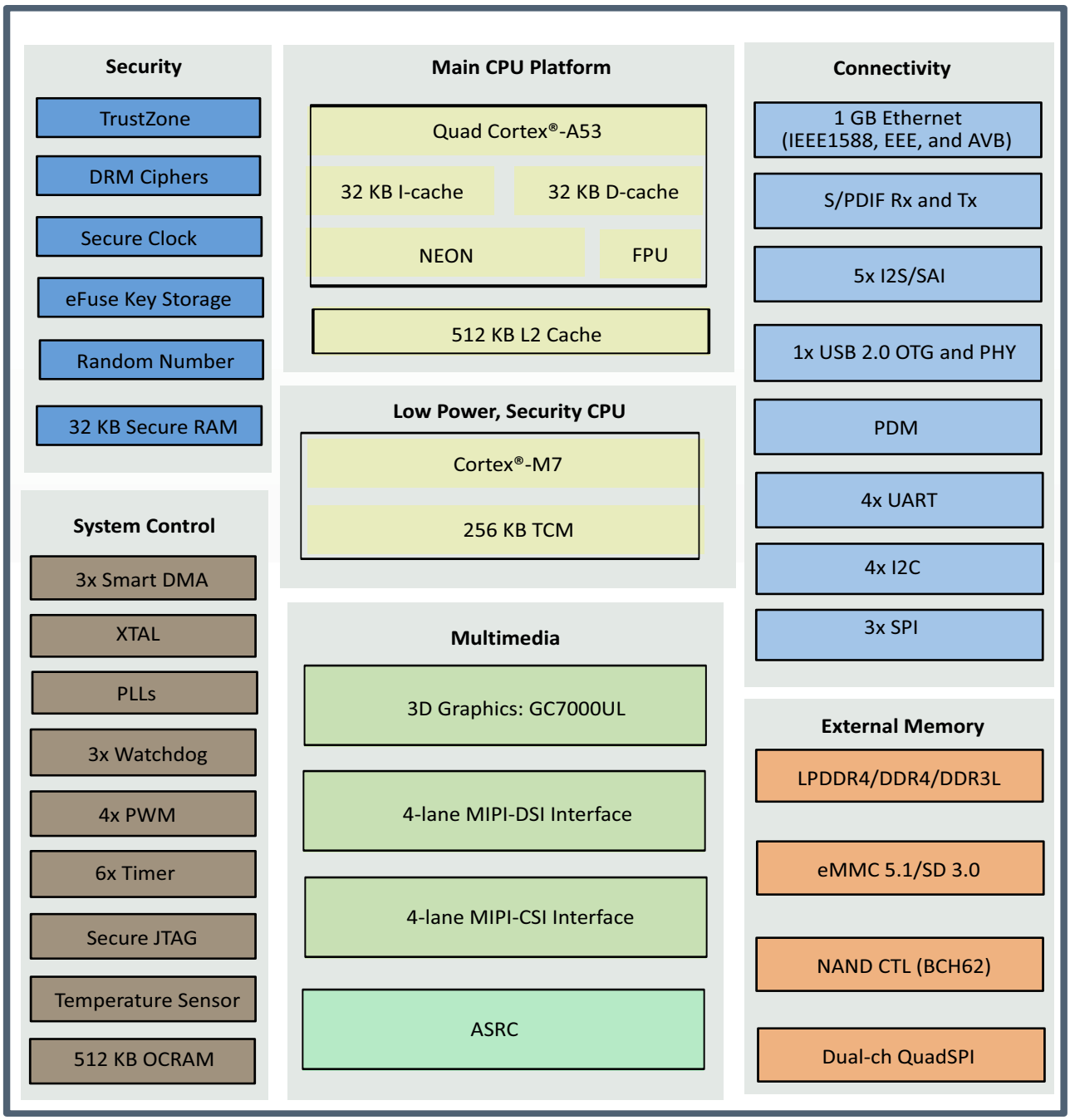


Figure 1. i.MX 8M Nano system block diagram

1.2 Ordering information

Table 2 shows examples of orderable sample part numbers covered by this data sheet. This table does not include all possible orderable part numbers. If your desired part number is not listed in the table, or you have questions about available parts, contact your NXP representative.

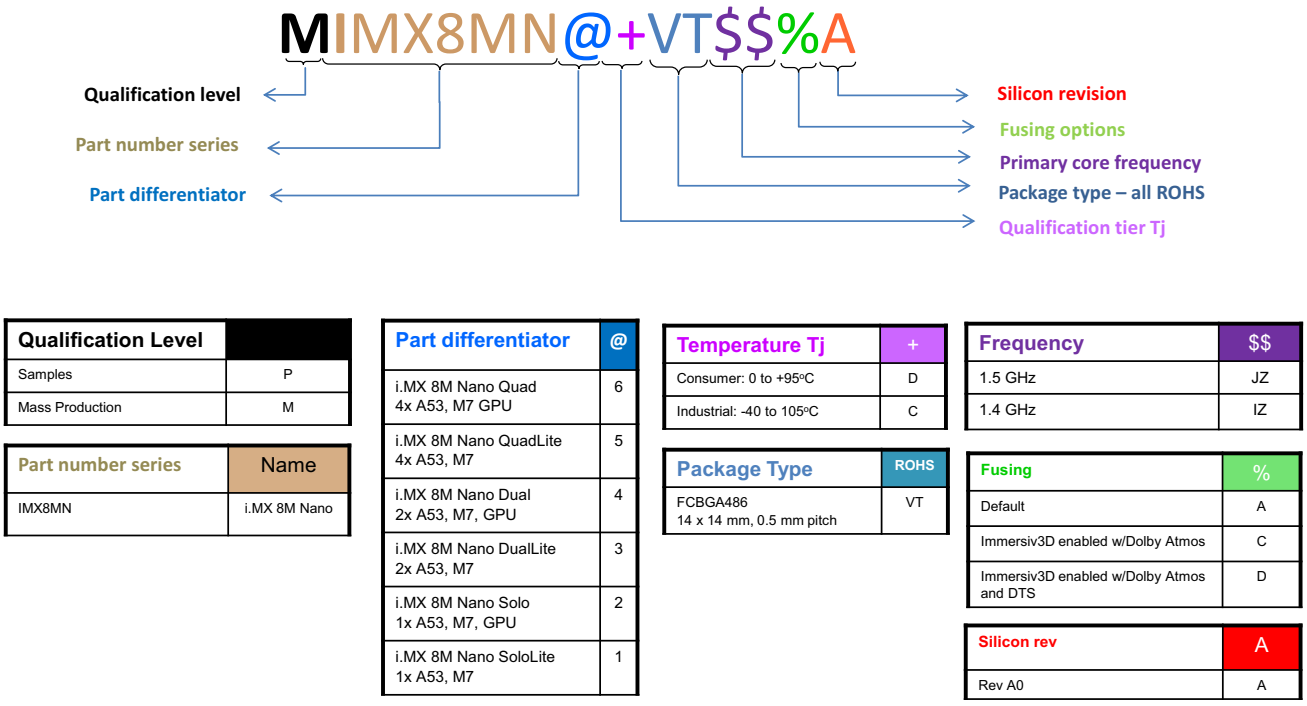
Table 2. Orderable part numbers

Part number	Sub-Family	Options	Cortex-A53 CPU speed grade	Qualification tier	Temperature T_j (°C)	Package
MIMX8MN6DVTJZAA	i.MX 8M Nano Quad	4x A53, M7, GPU	1.5 GHz	Consumer	0 to 95	14 x 14 mm, 0.5 mm pitch
MIMX8MN6DVTJZCA	i.MX 8M Nano Quad	4x A53, M7, GPU, Immersiv3D with Dolby ATMOS support[1]	1.5 GHz	Consumer	0 to 95	14 x 14 mm, 0.5 mm pitch
MIMX8MN6DVTJZDA	i.MX 8M Nano Quad	4x A53, M7, GPU, Immersiv3D with Dolby ATMOS and DTS support[1]	1.5 GHz	Consumer	0 to 95	14 x 14 mm, 0.5 mm pitch
MIMX8MN5DVTJZAA	i.MX 8M Nano QuadLite	4x A53, M7	1.5 GHz	Consumer	0 to 95	14 x 14 mm, 0.5 mm pitch
MIMX8MN4DVTJZAA	i.MX 8M Nano Dual	2x A53, M7, GPU	1.5 GHz	Consumer	0 to 95	14 x 14 mm, 0.5 mm pitch
MIMX8MN3DVTJZAA	i.MX 8M Nano DualLite	2x A53, M7	1.5 GHz	Consumer	0 to 95	14 x 14 mm, 0.5 mm pitch
MIMX8MN2DVTJZAA	i.MX 8M Nano Solo	1x A53, M7, GPU	1.5 GHz	Consumer	0 to 95	14 x 14 mm, 0.5 mm pitch
MIMX8MN1DVTJZAA	i.MX 8M Nano SoloLite	1x A53, M7	1.5 GHz	Consumer	0 to 95	14 x 14 mm, 0.5 mm pitch

[1] Supply of this Implementation of Dolby technology does not convey a license nor imply a right under any patent, or any other industrial or intellectual property right of Dolby Laboratories, to use this Implementation in any finished end-user or ready-to-use final product. It is hereby notified that a license for such use is required from Dolby Laboratories.

Figure 2 describes the part number nomenclature so that the users can identify the characteristics of the specific part number.

Contact an NXP representative for additional details.



Qualification Level	
Samples	P
Mass Production	M

Part number series	Name
IMX8MN	i.MX 8M Nano

Part differentiator	@
i.MX 8M Nano Quad 4x A53, M7 GPU	6
i.MX 8M Nano QuadLite 4x A53, M7	5
i.MX 8M Nano Dual 2x A53, M7, GPU	4
i.MX 8M Nano DualLite 2x A53, M7	3
i.MX 8M Nano Solo 1x A53, M7, GPU	2
i.MX 8M Nano SoloLite 1x A53, M7	1

Temperature Tj	+
Consumer: 0 to +95°C	D
Industrial: -40 to 105°C	C

Package Type	ROHS
FCBGA486 14 x 14 mm, 0.5 mm pitch	VT

Frequency	$$
1.5 GHz	JZ
1.4 GHz	IZ

Fusing	%
Default	A
Immersiv3D enabled w/Dolby Atmos	C
Immersiv3D enabled w/Dolby Atmos and DTS	D

Silicon rev	A
Rev A0	A

Figure 2. Part number nomenclature—i.MX 8M Nano family of processors

2 Modules list

The i.MX 8M Nano family of processors contains a variety of digital and analog modules. Table 3 describes these modules in alphabetical order.

Table 3. i.MX 8M Nano modules list

Block mnemonic	Block name	Brief description
APBH-DMA	NAND Flash and BCH ECC DMA Controller	DMA controller used for GPMI2 operation.
Arm	Arm Platform	The Arm Core Platform includes a quad Cortex-A53 core and a Cortex-M7 core. The Cortex-A53 core includes associated sub-blocks, such as the Level 2 Cache Controller, Snoop Control Unit (SCU), General Interrupt Controller (GIC), private timers, watchdog, and CoreSight debug modules. The Cortex-M7 core is used as a customer microcontroller.
BCH	Binary-BCH ECC Processor	The BCH module provides up to 62-bit ECC encryption/decryption for NAND Flash controller (GPMI)
CAAM	Cryptographic accelerator and assurance module	CAAM is a cryptographic accelerator and assurance module. CAAM implements several encryption and hashing functions, a run-time integrity checker, entropy source generator, and a Pseudo Random Number Generator (PRNG). The PRNG is certifiable by the Cryptographic Algorithm Validation Program (CAVP) of the National Institute of Standards and Technology (NIST). CAAM also implements a Secure Memory mechanism. In i.MX 8M Nano processors, the secure memory provided is 32 KB.
CCM GPC SRC	Clock Control Module, General Power Controller, System Reset Controller	These modules are responsible for clock and reset distribution in the system, and also for the system power management.
CSU	Central Security Unit	The Central Security Unit (CSU) is responsible for setting comprehensive security policy within the i.MX 8M Nano platform.
CTI-0 CTI-1 CTI-2 CTI-3 CTI-4	Cross Trigger Interface	Cross Trigger Interface (CTI) allows cross-triggering based on inputs from masters attached to CTIs. The CTI module is internal to the Cortex-A53 core platform.
DAP	Debug Access Port	The DAP provides real-time access for the debugger without halting the core to access: • System memory and peripheral registers • All debug configuration registers The DAP also provides debugger access to JTAG scan chains.
DDRC	Double Data Rate Controller	The DDR Controller has the following features: • Supports 16-bit LPDDR4-3200, DDR4-2400, and DDR3L-1600 • Supports up to 8 Gbyte DDR memory space
eCSPI1 eCSPI2 eCSPI3	Configurable SPI	Full-duplex enhanced Synchronous Serial Interface, with data rate up to 52 Mbit/s. Configurable to support Master/Slave modes, four chip selects to support multiple peripherals.

Table 3. i.MX 8M Nano modules list (continued)

Block mnemonic	Block name	Brief description
ENET1	Ethernet Controller	The Ethernet Media Access Controller (MAC) is designed to support 10/100/1000 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The module has dedicated hardware to support the IEEE 1588 standard. See the ENET chapter of the *i.MX 8M Nano Applications Processor Reference Manual* (IMX8MNRM) for details.
FlexSPI	FlexSPI	The FlexSPI module acts as an interface to external serial flash devices. This module contains the following features: • Flexible sequence engine to support various flash vendor devices • Single pad/Dual pad/Quad pad mode of operation • Single Data Rate/Double Data Rate mode of operation • Parallel Flash mode • DMA support • Memory mapped read access to connected flash devices • Multi master access with priority and flexible and configurable buffer for each master
GIC	Generic Interrupt Controller	The GIC handles all interrupts from the various subsystems and is ready for virtualization.
GPC	General Power Control Module	The GPC independently control reset and gated clock to each switched power domain when powering on/off the domain.
GPIO1 GPIO2 GPIO3 GPIO4 GPIO5	General Purpose I/O Modules	Used for general purpose input/output to external ICs. Each GPIO module supports up to 32 bits of I/O.
GPMI	General Purpose Memory Interface	The GPMI module supports up to 8x NAND devices and 62-bit ECC encryption/decryption for NAND Flash Controller (GPMI2). GPMI supports separate DMA channels for each NAND device.
GPT1 GPT2 GPT3 GPT4 GPT5 GPT6	General Purpose Timer	Each GPT is a 32-bit “free-running” or “set-and-forget” mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set-and-forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.
GPU3D	Graphics Processing Unit-3D	The GPU3D provides hardware acceleration for 3D graphics algorithms with sufficient processor power to run desktop quality interactive graphics applications on displays.
I2C1 I2C2 I2C3 I2C4	I^2C Interface	I^2C provides serial interface for external devices. Data rates of up to 320 kbps are supported.

Table 3. i.MX 8M Nano modules list (continued)

Block mnemonic	Block name	Brief description
IOMUXC	IOMUX Control	This module enables flexible I/O multiplexing. Each IO pad has a default as well as several alternate functions. The alternate functions are software configurable.
LCDIF	LCD interface	The LCDIF is a general purpose display controller used to drive a wide range of display devices varying in size and capability, the key feature of the display controller includes: • Support 8-bit/16-bit/24-bit/32-bit pixel depth • Support DOTCLK mode for MIPI-DPI interface • Support resolution up to 1920x1080p60 and 1800x1200p60
MIPI CSI (four-lane)	MIPI Camera Serial Interface	This module provides one four-lane MIPI camera serial interfaces, which operates up to a maximum bit rate of 1.5 Gbps.
MIPI DSI (four-lane)	MIPI Display Serial Interface	This module provides a four-lane MIPI display serial interface operating up to a maximum bit rate of 1.5 Gbps.
OCOTP_CTRL	OTP Controller	The On-Chip OTP controller (OCOTP_CTRL) provides an interface for reading, programming, and/or overriding identification and control information stored in on-chip fuse elements. The module supports electrically programmable poly fuses (eFUSEs). The OCOTP_CTRL also provides a set of volatile software-accessible signals that can be used for software control of hardware elements, not requiring non volatility. The OCOTP_CTRL provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, JTAG secure mode, boot characteristics, and various control signals requiring permanent non volatility.
OCRAM	On-Chip Memory controller	The On-Chip Memory controller (OCRAM) module is designed as an interface between the system's AXI bus and the internal (on-chip) SRAM memory module. In i.MX 8M Nano processors, the OCRAM is used for controlling the 512 KB multimedia RAM through a 64-bit AXI bus.
PDM	Pulse Density Modulation	The PDM supports up to 8-channels (4 lanes).
PWM1 PWM2 PWM3 PWM4	Pulse Width Modulation	The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images. It can also generate tones. It uses 16-bit resolution and a 4x16 data FIFO to generate sound.
SAI2 SAI3 SAI5 SAI6 SAI7	Synchronous Audio Interface	The SAI module provides a synchronous audio interface (SAI) that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces.

Table 3. i.MX 8M Nano modules list (continued)

Block mnemonic	Block name	Brief description
SDMA	Smart Direct Memory Access	The SDMA is a multichannel flexible DMA engine. It helps in maximizing system performance by offloading the various cores in dynamic data routing. It has the following features: • Powered by a 16-bit Instruction-Set micro-RISC engine • Multi channel DMA supporting up to 32 time-division multiplexed DMA channels • 48 events with total flexibility to trigger any combination of channels • Memory accesses including linear, FIFO, and 2D addressing • Shared peripherals between Arm and SDMA • Very fast Context-Switching with 2-level priority based preemptive multi tasking • DMA units with auto-flush and prefetch capability • Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address) • DMA ports can handle unidirectional and bidirectional flows (Copy mode) • Up to 8-word buffer for configurable burst transfers for EMIv2.5 • Support of byte-swapping and CRC calculations • Library of Scripts and API is available
SJC	Secure JTAG Controller	The SJC provides JTAG interface (designed to be compatible with JTAG TAP standards) to internal logic. The i.MX 8M Nano family of processors uses JTAG port for system debugging. The JTAG port must be accessible during platform initial laboratory bring-up, for troubleshooting, as well as for software debugging by authorized entities. The i.MX 8M Nano SJC incorporates three security modes for protecting against unauthorized accesses. Modes are selected through eFUSE configuration.
SNVS	Secure Non-Volatile Storage	Secure Non-Volatile Storage, including Secure Real Time Clock, Security State Machine, Master Key Control, and Violation/Tamper Detection and reporting.
SPDIF1	Sony Philips Digital Interconnect Format	A standard audio file transfer format, developed jointly by the Sony and Phillips corporations. It supports Transmitter and Receiver functionality.
TEMPSENSOR	Temperature Sensor	Temperature sensor
TZASC	Trust-Zone Address Space Controller	The TZASC (TZC-380 by Arm) provides security address region control functions required for intended application. It is used on the path to the DRAM controller.
UART1 UART2 UART3 UART4	UART Interface	Each of the UARTv2 modules supports the following serial data transmit/receive protocols and configurations: • 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd, or none) • Programmable baud rates up to 4 Mbps. This is a higher max baud rate relative to the 1.875 MHz, which is stated by the TIA/EIA-232-F standard. • 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud

Table 3. i.MX 8M Nano modules list (continued)

Block mnemonic	Block name	Brief description
uSDHC1 uSDHC2 uSDHC3	SD/MMC and SDXC Enhanced Multi-Media Card / Secure Digital Host Controller	i.MX 8M Nano SoC characteristics: All the MMC/SD/SDIO controller IPs are based on the uSDHC IP. They are designed to support: • SD/SDIO standard, up to version 3.0. • MMC standard, up to version 5.1. • 1.8 V and 3.3 V operation, but do not support 1.2 V operation. • 1-bit/4-bit SD and SDIO modes, 1-bit/4-bit/8-bit MMC mode. One uSDHC controller (SD1) can support up to an 8-bit interface, the other controller (SD2) can only support up to a 4-bit interface.
USB 2.0	1x USB 2.0 controller and PHY	One USB controller and PHY that support USB 2.0.
WDOG1 WDOG2 WDOG3	Watchdog	The watchdog (WDOG) timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the Arm core, and a second point evokes an external event on the WDOG line.

2.1 Recommended connections for unused input/output

If a function of the i.MX 8M Nano is not in use, the I/Os and power rails of that function can be terminated to reduce overall board power.

Table 4 shows the recommended connections for unused power supply rails.

Table 4. Recommended connections for unused power supply rails

Function	Ball Name	Recommendations if Unused
MIP-CSI and MIPI-DSI	VDD_MIPI_0P8, VDD_MIPI_1P2, VDD_MIPI_1P8	Leave unconnected
USB1	VDD_USB_0P8, VDD_USB_1P8, VDD_USB_3P3	Leave unconnected
GPU	VDD_GPU	Leave unconnected
Digital I/O supplies	NVCC_CLK, NVCC_ECSPI, NVDD_ENET, NVCC_GPIO1, NVCC_I2C, NVCC_JTAG, NVCC_NAND, NVCC_SAI2, NVCC_SAI3, NVCC_SAI5, NVCC_SD1, NVCC_SD2, NVCC_UART, NVCC_SNVS_1P8, PVCC0_1P8, PVCC1_1P8, PVCC2_1P8	All digital I/O supplies listed in this table must be powered under normal conditions whether the associated I/O pins are in use or not, and associated I/O pins need to enable pull in pad control register to limit any floating gate current.

Table 5 shows recommended connections for unused signal contacts/interfaces.

Table 5. Recommended connections for unused signal contacts/interfaces

Function	Ball Name	Recommendations if Unused
MIPI-CSI	MIPI_CSI_CLK_P, MIPI_CSI_CLK_N, MIPI_CSI_Dx_P, MIPI_CSI_Dx_N	Tie all signals to ground
MIPI-DSI	MIPI_VREG_CAP, MIPI_DSI_CLK_P, MIPI_DSI_CLK_N, MIPI_DSI_Dx_P, MIPI_DSI_Dx_N	Leave unconnected
USB1	USB1_VBUS, USB1_DN, USB1_DP, USB1_ID, USB1_TXRTUNE	Leave unconnected

3 Electrical characteristics

This section provides the device and module-level electrical characteristics for the i.MX 8M Nano family of processors.

3.1 Chip-level conditions

This section provides the device-level electrical characteristics for the IC. See Table 6 for a quick reference to the individual tables and sections.

Table 6. i.MX 8M Nano chip-level conditions

For these characteristics, …	Topic appears …
Absolute maximum ratings	on page 14
FCBGA package thermal resistance	on page 16
Operating ranges	on page 17
External clock sources	on page 18
Maximum supply currents	on page 19
Power modes	on page 20
Power supplies requirements and restrictions	on page 22

3.1.1 Absolute maximum ratings

CAUTION

Stresses beyond those listed under Table 7 may affect reliability or cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operating ranges or parameters tables is not implied.

Table 7. Absolute maximum ratings

Parameter description	Symbol	Min	Max	Unit	Notes
Core supply voltages	VDD_ARM VDD_SOC	-0.3	1.15	V	—
Power supply for GPU	VDD_GPU	-0.3	1.15	V	—
DDR PHY supply voltage	VDD_DRAM	-0.3	1.15	V	—
DDR I/O supply voltage	NVCC_DRAM	-0.3	1.575	V	—
DRAM PLL supply voltage	VDD_DRAM_PLL_0P8	-0.3	1.15	V	—
	VDD_DRAM_PLL_1P8	-0.3	2.15	V	—
SNVS IO supply voltage	NVCC_SNVS_1P8	-0.3	2.15	V	—
VDD_SNVS supply voltage	VDD_SNVS_0V8	-0.3	0.95	V	—

Table 7. Absolute maximum ratings (continued)

Parameter description	Symbol	Min	Max	Unit	Notes
GPIO supply voltage	NVCC_JTAG, NVCC_GPIO1, NVCC_ENET, NVCC_SD1, NVCC_SD2, NVCC_NAND, NVCC_SAI2, NVCC_SAI3, NVCC_SAI5, NVCC_ECSPI, NVCC_I2C, NVCC_UART, NVCC_CLK	-0.3	3.8	V	—
GPIO pre-driver supply voltage	PVCC0_1P8, PVCC1_1P8, PVCC2_1P8	-0.3	2.15	V	—
Isolated core supply voltage	VDD_ANA_0P8	-0.3	1.15	V	—
Analog core supply voltage	VDD_ANA0_1P8	-0.3	2.15	V	—
	VDD_ANA1_1P8	-0.3	2.15	V	—
Arm PLL supply voltage	VDD_ARM_PLL_0P8	-0.3	0.95	V	—
	VDD_ARM_PLL_1P8	-0.3	2.15	V	—
MIPI PHY supply voltage	VDD_MIPI_0P8	-0.3	1.15	V	—
	VDD_MIPI_1P2	-0.3	1.45	V	—
	VDD_MIPI_1P8	-0.3	2.15	V	—
USB PHY supply voltage	VDD_USB_0P8	-0.3	0.95	V	—
	VDD_USB_1P8	-0.3	2.15	V	—
	VDD_USB_3P3	-0.3	3.95	V	—
USB_VBUS input detected	USB1_VBUS	-0.3	3.95	V	—
XTAL supply voltage	VDD_24M_XTAL_1P8	-0.3	2.15	V	—
Storage temperature range	$T_{STORAGE}$	-40	150	°C	—

Table 8. Electrostatic discharge and latch up ratings

Parameter description		Rating	Reference	Comment
Electrostatic Discharge (ESD)	Human Body Model (HBM)	±1000 V	JS-001-2017	—
	Charged Device Model (CDM)	±250 V	JS-002-2018	—
Latch UP (LU)	Immunity level: • Class I@ 25 °C ambient temperature • Class II @ 105 °C ambient temperature	 A A	JESD78E	Mandatory requirement: JTAG_TMS pin must be connected with a 50 ohm series resistor near the component.

3.1.2 Thermal resistance

3.1.2.1 FCBGA package thermal resistance

Table 9 displays the FCBGA package thermal resistance data.

Table 9. Thermal resistance data

Rating	Test conditions	Symbol	Value	Unit	Notes
Junction to Ambient Natural Convection	Single layer board (1s) Four layer board (2s2p)	$R_{\theta JA}$	30	°C/W	1, 2
Junction to Ambient Natural Convection	Four layer board (2s2p) Four layer board (2s2p)	$R_{\theta JA}$	22.9	°C/W	1, 2, 3
Junction to Ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	24	°C/W	1, 3
Junction to Ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	18.5	°C/W	1, 3
Junction to Board	—	$R_{\theta JB}$	7.8	°C/W	4
Junction to Case	—	$R_{\theta JC}$	4	°C/W	5
Junction to Package Top	Natural Convection	Ψ_{JT}	0.2	°C/W	6

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per SEMI G38-87 and JESD51-2 with the single layer board horizontal.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

3.1.3 Operating ranges

Table 10 provides the operating ranges of the i.MX 8M Nano applications processor. For details on the chip's power structure, see the "Power Management Unit (PMU)" chapter of the *i.MX 8M Nano Applications Processor Reference Manual* (IMX8MNRM).

Table 10. Operating ranges

Symbol	Min	Typ	Max[1]	Unit	Comment
VDD_ARM	0.805	0.850	0.950	V	Power supply for Cortex® A53, 1.2 GHz
	0.900	0.950	1.000	V	Power supply for Cortex® A53, 1.4 GHz
	0.950	1.000	1.050	V	Power supply for Cortex® A53, 1.5 GHz
VDD_SOC	0.805	0.850	0.900	V	Power supply for SoC logic[2], Cortex® M7 600 MHz
	0.900	0.950	1.000	V	Power supply for SoC logic, overdrive mode, Cortex® M7 750 MHz
VDD_GPU	0.805	0.850	0.900	V	Power supply for 3D GPU, nominal mode, 400 MHz
	0.900	0.950	1.000	V	Power supply for 3D GPU, overdrive mode, 600 MHz
VDD_DRAM	0.805	0.850	0.900	V	Power supply for DDRC, 0.85 V supports up to 1.2 GHz (DDR clock)
	0.900	0.950	1.000	V	Power supply for DDRC, 0.95 V supports up to 1.6 GHz (DDR clock)
VDD_SNVS_0P8	0.760	0.800	0.900	V	Power supply for SNVS core logic
NVCC_SNVS_1P8	1.620	1.800	1.980	V	Power supply for GPIO pre-driver in SNVS bank
NVCC_JTAG, NVCC_GPIO1, NVCC_ENET, NVCC_SD1, NVCC_SD2, NVCC_NAND, NVCC_SAI2, NVCC_SAI3, NVCC_SAI5, NVCC_ECSPI, NVCC_I2C, NVCC_UART, NVCC_CLK	1.650	1.800	1.950	V	Power supply for GPIO when it is in 1.8 V mode
	3.000	3.300	3.600	V	Power supply for GPIO when it is in 3.3 V mode
NVCC_ENET	2.250	2.500	2.750	V	Power supply for GPIO when it is in 2.5 V mode
PVCC0_1P8, PVCC1_1P8, PVCC2_1P8	1.650	1.800	1.950	V	Power supply for GPIO pre-driver
VSS	—	—	—	V	Ground for all core logic and I/O
NVCC_DRAM	1.283	1.35	1.425	V	DDR3L
	1.14	1.2	1.26	V	DDR4
	1.06	1.1	1.14	V	LPDDR4

Table 10. Operating ranges (continued)

Symbol	Min	Typ	Max[1]	Unit	Comment
DRAM_VREF	0.49 x NVCC_DRAM	0.5 x NVCC_DRAM	0.51 x NVCC_DRAM	V	Internal output, no connection is needed.
VDD_DRAM_PLL_0P8	0.805	0.850	1.000	V	0.8 V logic power supply for DSM. It should be connected to the separate logic power.
VDD_ANA0_1P8 VDD_ANA1_1P8	1.71	1.8	1.89	V	Analog 1.8 V core power
VDD_ANA_0P8	0.805	0.850	1.000	V	Isolated 0.8 V core power
VDD_ARM_PLL_0P8	0.805	0.850	1.000	V	Arm PLL 0.8 V power
VDD_ARM_PLL_1P8	1.71	1.8	1.89	V	Arm PLL 1.8 V power
VDD_24M_XTAL_1P8	1.71	1.8	1.89	V	XTAL 1.8 V power
VDD_DRAM_PLL_1P8	1.71	1.8	1.89	V	Analog 1.8 V core power
VDD_MIPI_0P8	0.805	0.850	1.000	V	0.9 V power for PLL and internal logic
VDD_MIPI_1P2	1.14	1.2	1.26	V	1.2 V power for analog
VDD_MIPI_1P8	1.71	1.8	1.89	V	1.8 V power for PLL and analog
VDD_USB_0P8	0.805	0.850	1.000	V	Digital power supply from PHY's I/O power pads
VDD_USB_1P8	1.71	1.80	1.89	V	1.8 V analog power supply
VDD_USB_3P3	3.069	3.30	3.6	V	3.3 V analog power supply
USB1_VBUS	0.800	1.40	3.60	V	USB_VBUS input detect signal
Temperature Sensor Accuracy[3]	—	±3	±5	°C	Sensing temperature range 10°C to 105°C
T_J	0	—	+95	°C	See Table 2 for complete list of junction temperature capabilities.

1 Applying the maximum voltage results in maximum power consumption and heat generation. A voltage set point = (Vmin + the supply tolerance) is recommended. This results in an optimized power/speed ratio.

2 Booting VDD_SOC at 0.800 V ±5% is acceptable (Vmin = 0.760 V). Software is expected to program the VDD_SOC voltage to the typical value in this table prior to first DRAM memory access.

3 "EN" of TMU Enable Register (TMU_TER) is required to be always enabled for the part to operate correctly.

3.1.4 External clock sources

Each i.MX 8M Nano processor has two external input system clocks: a low frequency (RTC_XTALI) and a high frequency (XTALI).

The RTC_XTALI is used for low-frequency functions. It supplies the clock for wake-up circuit, power-down real time clock operation, and slow system and watch-dog counters. The clock input can only be connected to an external oscillator. RTC_XTALO should be directly connected to VDD_SNVS_0P8.

The system clock input XTALI is used to generate the main system clock. It supplies the PLLs and other peripherals. The system clock input can be connected to either an external oscillator or a crystal using internal oscillator amplifier.

Table 11 shows the interface frequency requirements.

Table 11. External input clock frequency

Parameter Description	Symbol	Min	Typ	Max	Unit
RTC_XTALI Oscillator[1]	f_{ckil}	—	32.768[2]	—	kHz
XTALI Oscillator[1,3]	f_{xtal}		24		MHz

1 The required frequency stability of this clock source is application dependent.

2 Recommended nominal frequency 32.768 kHz.

3 External oscillator or a fundamental frequency crystal appropriately coupled to the internal oscillator amplifier.

The typical values shown in Table 11 are required for use with NXP software to ensure precise time keeping and USB operation. For RTC_XTALI operation, an external oscillator is necessary. RTC_XTALO should be directly connected to VDD_SNVS_0P8 when using an external 32.768 kHz oscillator.

NOTE

There is no internal RC oscillator.

Table 12 shows the external input clock for OSC32K.

Table 12. External input clock for OSC32K

	Symbol	Min	Typ	Max	Unit
Frequency	f	—	32.768	—	kHz
RTC_XTALI	VIH	0.7 x NVCC_SNVS_1P8	—	NVCC_SNVS_1P8	V
	VIL	0	—	0.3 x NVCC_SNVS_1P8	V

3.1.5 Maximum supply currents

Power consumption is highly dependent on the application. Estimating the maximum supply currents required for power supply design is difficult because the use cases that requires maximum supply current is not a realistic use cases.

To help illustrate the effect of the application on power consumption, data was collected while running consumer standard benchmarks that are designed to be compute and graphic intensive. The results provided are intended to be used as guidelines for power supply design.

Table 13. Maximum supply currents

Power rail	Max current	Unit
VDD_ARM	2200	mA
VDD_SOC	1000	mA
VDD_GPU	800	mA

Table 13. Maximum supply currents (continued)

Power rail	Max current	Unit
VDD_DRAM	800	mA
VDD_ANA_0P8	50	mA
VDD_ANA0_1P8 VDD_ANA1_1P8	250	mA
NVCC_SNVS_1P8	3	mA
NVCC_<XXX>	I_{max} = N x C x V x (0.5 x F) Where: N—Number of IO pins supplied by the power line C—Equivalent external capacitive load V—IO voltage (0.5 x F)—Data change rate. Up to 0.5 of the clock rate (F). In this equation, I_{max} is in Amps, C in Farads, V in Volts, and F in Hertz.	
NVCC_DRAM		
DRAM_VFEF	10	mA

3.1.6 Power modes

The i.MX 8M Nano supports the following power modes:

- RUN Mode: All external power rails are on, CPU is active and running; other internal modules can be on/off based on application.
- IDLE Mode: When there is no thread running and all high-speed devices are not active, the CPU can automatically enter this mode. The CPU can be in the power-gated state but with L2 data retained, DRAM and the bus clock are reduced. Most of the internal logic is clock gated but still remains powered. The M7 core can remain running. Compared with RUN mode, all the external power rails from the PMIC remain the same, and most of the modules still remain in their state.
- SUSPEND Mode: The most efficient power saving mode where all the clocks are off and all the unnecessary power supplies are off.
- SNVS Mode: This mode is also called RTC mode. Only the power for the SNVS domain remains on to keep RTC and SNVS logic alive.
- OFF Mode: All power rails are off.

Table 14. Chip power in different LP mode

Mode	Supply	Typ.[1]	Unit
SNVS	VDD_SNVS_0P8	0.10	mW
	NVCC_SNVS_1P8	1.20	
	Total[2]	1.30	

Table 14. Chip power in different LP mode (continued)

Mode	Supply	Typ.[1]	Unit
SUSPEND	NVCC	0.80	mW
	NVCC_DRAM	2.40	
	NVCC_ENET	0.10	
	NVCC_SNVS_1P8	0.20	
	PVCC	0.60	
	VDD_DRAM	9.40	
	VDD_MIPI_0P8	0.10	
	VDD_SNVS_0P8	0.10	
	VDD_SOC	4.50	
	VDD_ARM_PLL_0P8	0.10	
	VDD_USB_0P8	2.50	
	Total[2]	20.80	

1 All the power numbers defined in the table are for information only. These numbers are based on typical silicon at 25°C, under non-OS environment and use case dependent. For power numbers with OS and real use cases, see *Power consumption measurement application note* for more details.

2 Sum of the listed supply rails.

Table 15 summarizes the power supply states in all the power modes.

Table 15. The power supply states

Power rail	OFF	SNVS	SUSPEND	IDLE	RUN
VDD_ARM	OFF	OFF	OFF	ON	ON
VDD_SOC	OFF	OFF	ON	ON	ON
VDD_GPU	OFF	OFF	OFF	OFF	ON/OFF
VDD_DRAM	OFF	OFF	ON	ON	ON
Misc_1P8[1]	OFF	OFF	ON	ON	ON
Misc_0P8[1]	OFF	OFF	ON	ON	ON
VDD_MIPI_1P2	OFF	OFF	ON	ON	ON
VDD_MIPI_0P8	OFF	OFF	ON	ON	ON
VDD_DRAM_PLL_0P8	OFF	OFF	ON	ON	ON
VDD_SNVS_0P8	OFF	ON	ON	ON	ON
NVCC_SNVS_1P8	OFF	ON	ON	ON	ON
NVCC_<XXX>	OFF	OFF	ON	ON	ON

Table 15. The power supply states (continued)

Power rail	OFF	SNVS	SUSPEND	IDLE	RUN
PVCCx_1P8	OFF	OFF	ON	ON	ON
NVCC_DRAM	OFF	OFF	ON	ON	ON

[1] See Table 16

Table 16. Group name

Misc_1P8	VDD_24M_XTAL_1P8 VDD_ANA0_1P8 VDD_ANA1_1P8 VDD_ARM_PLL_1P8 VDD_DRAM_PLL_1P8 VDD_MIPI_1P8 VDD_USB_1P8
Misc_0P8	VDD_ANA_0P8 VDD_ARM_PLL_0P8 VDD_USB_0P8

3.2 Power supplies requirements and restrictions

The system design must comply with power-up sequence, power-down sequence, and steady state guidelines as described in this section to guarantee the reliable operation of the device. Any deviation from these sequences may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the processor (worst-case scenario)

3.2.1 Power-up sequence

Figure 3 illustrates the power-up sequence of i.MX 8M Nano applications processor.

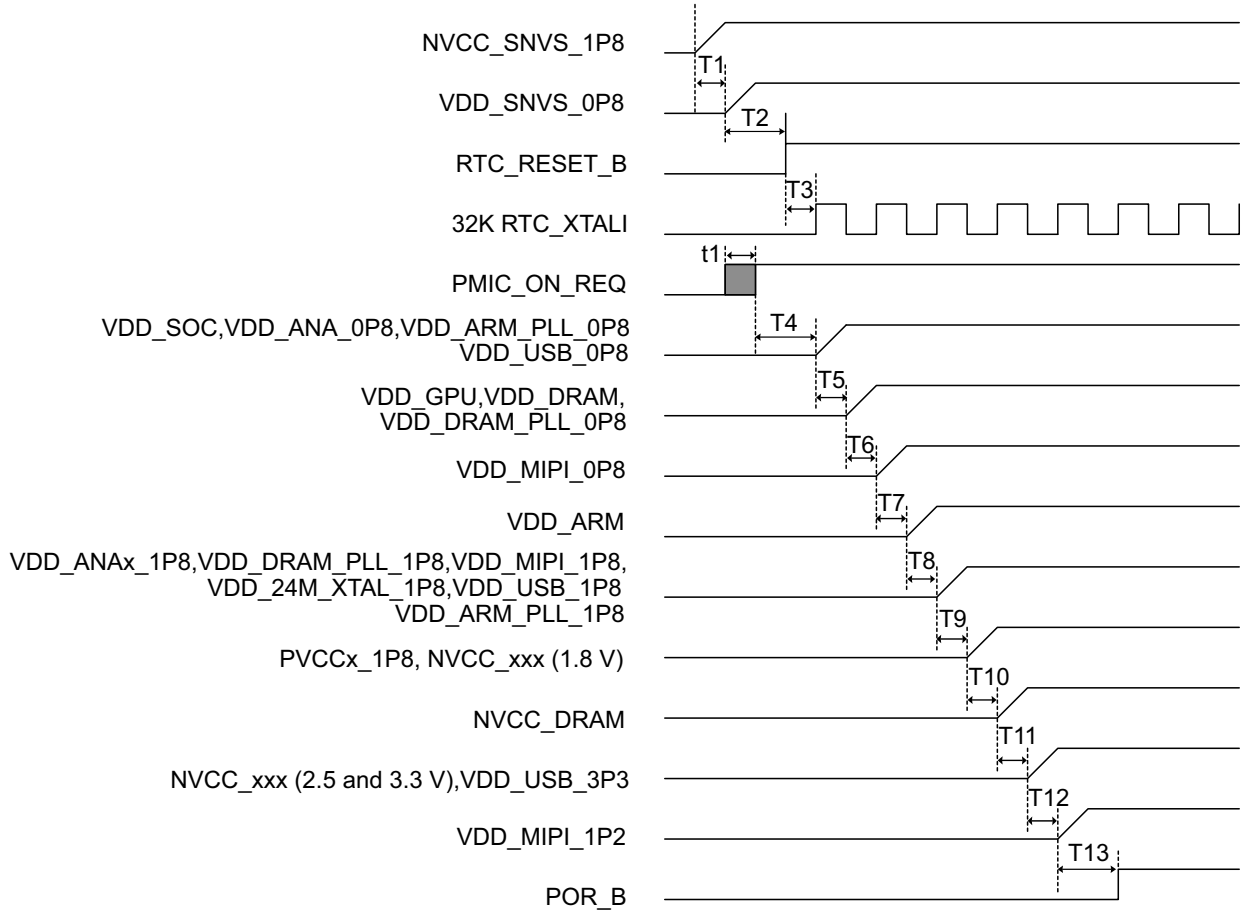


Figure 3. The power-up sequence

Table 17 represents the timing parameters of the power-up sequence.

Table 17. Power-up sequence

	Description	Min	Typ	Max	Unit
T1	Delay from NVCC_SNVS_1P8 to VDD_SNVS_0P8	0	2	—	ms
T2	Delay from VDD_SNVS_0P8 high or RTC_SET_B de-assert	0	10	—	ms
T3	Delay from RTC_RESET_B de-assert to stable 32 k existed	—	40	100	µs
T4	Delay from PMIC_ON_REQ assert to analog 0.8 V on	0	0.2	—	ms
T5	Delay from analog 0.8 V on to analog 0.8/0/9 V on	0	2	—	ms
T6	Delay from analog 0.8/0.9 V on to PHY 0.9 V on	0	15	—	µs
T7	Delay from PHY 0.9 V on to VDD_ARM on	0	2	—	ms
T8	Delay from VDD_ARM on to analog 1.8 V on	0	15	—	µs
T9	Delay from analog 1.8 V on to digital 1.8 V on	0	2	—	ms
T10	Delay from digital 1.8 V on to NVCC_DRAM on	0	2	—	ms
T11	Delay from NVCC_DRAM on to digital 2.5 V and 3.3 V on	0	2	—	ms
T12	Delay from digital 2.5 V and 3.3 V on to PHY 1.2 V on	0	2	—	ms
T13[1]	Delay from PHY 1.2 V on to POR_B de-assert	0	20	—	ms
t1	Uncertain period before PMIC_ON_REQ assert during VDD_SNVS_0P8 ramp up.				
	For ramp up requirement, only VDD_ANA0_1P8 has 5 µs minimum requirement, others do not have such requirement. During power-up, make sure NVCC_xxx - PVCCx_1P8 < 2 V.				

[1] The values of T13 depend on T2. RTC_RESET_B must be de-assert before POR_B de-asserts.

3.2.2 Power-down sequence

Figure 4 illustrates the power-down sequence of i.MX 8M Nano applications processor.

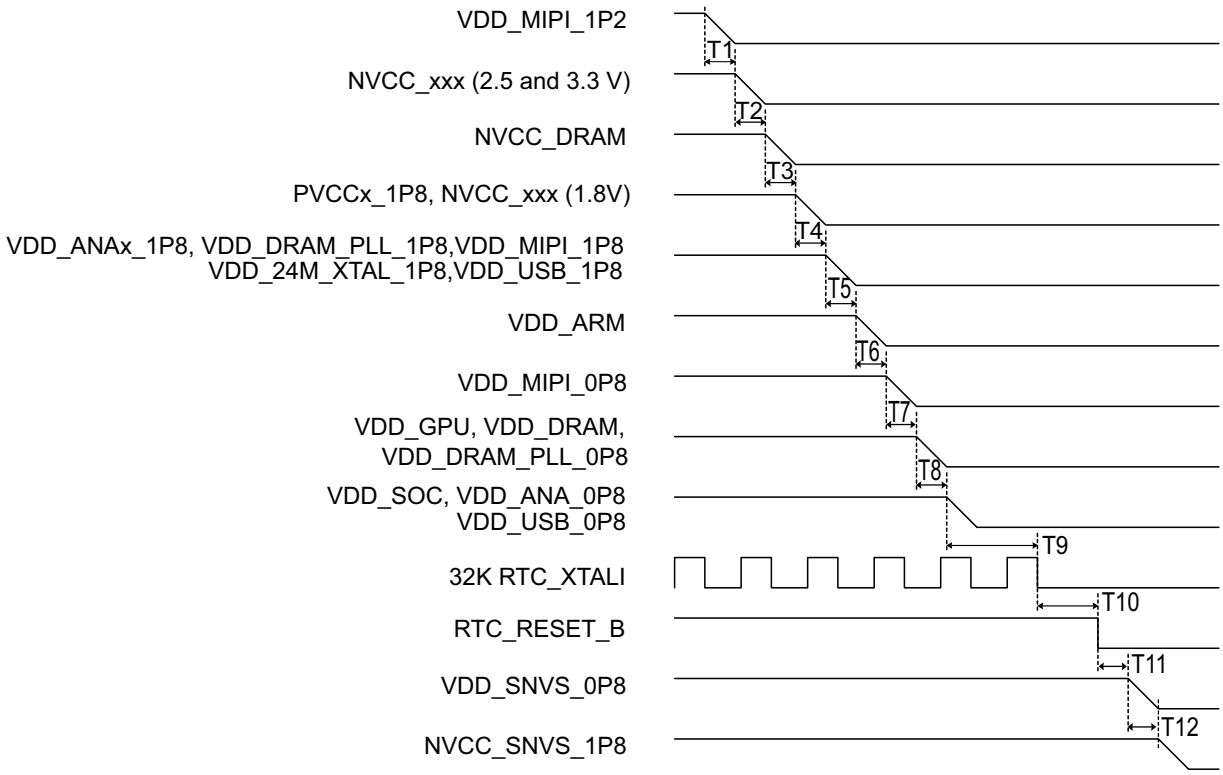


Figure 4. The power-down sequence

Table 18 represents the timing parameters of the power-down sequence.

Table 18. Power-down sequence

	Description	Min	Typ	Max	Unit
T1	Delay from PHY 1.2 V off to digital 2.5 V and 3.3 V off	0	10	—	ms
T2	Delay from digital 2.5 V and 3.3 V off to NVCC_DRAM off	0	10	—	ms
T3	Delay from NVCC_DRAM off to digital 1.8 V off	0	10	—	ms
T4	Delay from digital 1.8 V off to analog 1.8 V off	0	10	—	ms
T5	Delay from analog 1.8 V off to VDD_ARM off	0	10	—	ms
T6	Delay from VDD_ARM off to PHY 0.9 V off	0	10	—	ms
T7	Delay from PHY 0.9 V off to analog 0.8/0.9 V off	0	10	—	ms
T8	Delay from analog 0.8/0.9 V off to analog 0.8 V off	0	10	—	ms
T9	Delay from analog 0.8 V off to 32k off	0	10	—	ms
T10	Delay from 32k off to RTC_RESET_B assert	0	10	—	ms
T11	Delay from RTC_RESET_B assert to VDD_SNVS_0P8 off	0	10	—	ms
T12	Delay from VDD_SNVS_0P8 off to NVCC_SNVS_1P8 off	0	10	—	ms
	During power-down, make sure NVCC_xxx - PVCCx_1P8 < 2 V.				

3.2.3 Power supplies constraints

Table 19 shows constraints for some power supplies:

Table 19. Power supplies constraints

Profile	VDD_ARM	VDD_SOC	VDD_GPU	VDD_DRAM	Unit
Consumer	0.85 or 0	0.85	0.85 or 0	0.85 or 0	V
Consumer	0.95 or 0	0.95	0.95 or 0	0.95 or 0	V
Consumer	1.0 or 0	0.95	0.95 or 0	0.95 or 0	V

- The VDD_SOC, VDD_DRAM, and VDD_GPU must be the same or grounded.
- If VDD_ARM ≥ 0.95 V, VDD_SOC/GPU/DDR must be 0.95 V.
- If VDD_SOC/GPU/DDR = 0.95 V, then VDD_ARM must be ≥ 0.95 V.

3.3 PLL electrical characteristics

Table 20 shows PLL electrical characteristics.

Table 20. PLL electrical parameters

PLL type	Parameter	Value
AUDIO_PLL1	Clock output range	Maximum 650 MHz
	Reference clock	24 MHz
	Lock time	375 μs
AUDIO_PLL2	Clock output range	Maximum 650 MHz
	Reference clock	24 MHz
	Lock time	375 μs
VIDEO_PLL1	Clock output range	Maximum 650 MHz
	Reference clock	24 MHz
	Lock time	375 μs
SYS_PLL1	Clock output range	800 MHz
	Reference clock	24 MHz
	Lock time	25 μs
SYS_PLL2	Clock output range	1 GHz
	Reference clock	24 MHz
	Lock time	25 μs
SYS_PLL3	Clock output range	600 MHz — 1 GHz
	Reference clock	24 MHz
	Lock time	25 μs
ARM_PLL	Clock output range	800 MHz — 2 GHz
	Reference clock	24 MHz
	Lock time	25 μs
DRAM_PLL	Clock output range	400 MHz — 800 MHz
	Reference clock	24 MHz
	Lock time	375 μs
GPU_PLL	Clock output range	Normal drive 400 MHz / Overdrive 600 MHz
	Reference clock	24 MHz
	Lock time	25 μs

3.4 On-chip oscillators

3.4.1 OSC24M

A 24 MHz oscillator is used as the primary clock source for the PLLs to generate the clock for the CPU, BUS, and high-speed interfaces. For fractional PLLs, the 24 MHz clock from the oscillator can be used as the PLL reference clock directly.

Table 21. Crystal specifications[1]

Parameter Description	Min	Typ	Max	Unit
Frequency	—	24	—	MHz
Cload	—	12	—	pF
Drive level	100	—	—	μW
ESR	—	—	80	Ω

1 Actual working drive level is depend on real design. Please contact crystal vendor for selecting drive level of crystal.

3.4.2 OSC32K

An external 32.768 kHz oscillator is necessary.

3.5 General purpose I/O (GPIO) DC parameters

Table 22 shows DC parameters for GPIO pads. The parameters in Table 22 are guaranteed per the operating ranges in Table 10, unless otherwise noted.

Table 22. GPIO DC parameters

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
High-level output voltage	$V_{OH\ (1.8\ V)}$	I_{OH} = 1.6/3.2/6.4/9.6 mA (1.8 V) I_{OH} = 2/4/8/12 mA (3.3 V)	0.8 x V_{DD}	—	V_{DD}	V
	$V_{OH\ (3.3\ V)}$		0.8 x V_{DD}	—	V_{DD}	V
Low-level output voltage	$V_{OL\ (1.8\ V)}$	I_{OL} = 1.6/3.2/6.4/9.6 mA (1.8 V) I_{OL} = 2/4/8/12 mA (3.3 V)	0	—	0.2 x V_{DD}	V
	$V_{OL\ (3.3\ V)}$		0	—	0.2 x V_{DD}	V
High-level input voltage	V_{IH}	—	0.7 x V_{DD}	—	V_{DD} + 0.3	V
Low-level input voltage	V_{IL}	—	-0.3	—	0.3 x V_{DD}	V
Pull-up resistor	—	V_{DD} = 1.65 - 1.95V Temp = 0 - 95 °C	12	22	49	KΩ
Pull-down resistor	—		13	23	48	KΩ
Pull-up resistor	—	V_{DD} = 2.25 - 2.75V Temp = 0 - 95 °C	13	24	69	KΩ
Pull-down resistor	—		9.1	33	69	KΩ

Table 22. GPIO DC parameters (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Pull-up resistor	—	V_{DD} = 3.0 - 3.6V Temp = 0 - 95 °C	18	37	72	KΩ
Pull-down resistor	—		24	43	87	KΩ
High level input current	IIH	—	-4	—	4	μA
Low level input current	IIL	—	-0.7	—	0.7	μA

Table 23. Additional leakage parameters

Parameter	Symbol	Pins	Min	Max	Unit
High level input current	IIH	USB1_Dx	-30	30	μA
		MIPI_CSI	-4	4	
		USB1_ID, ONOFF, POR_B	-1	1	
Low level input current	IIL	USB1_ID	-200	200	μA
		USB1_Dx	-6	6	
		MIPI_CSI, ONOFF, POR_B	-0.7	0.7	

3.5.1 DDR I/O DC electrical characteristics

The DDR I/O pads support LPDDR 4, DDR4, and DDR3L operational modes. The DDR Memory Controller (DDRMC) is designed to be compatible with JEDEC-compliant SDRAMs.

DDRMC operation is contingent upon the board's DDR design adherence to the DDR design and layout requirements stated in the hardware development guide for the i.MX 8M Nano applications processor.

3.6 I/O AC parameters

This section includes the AC parameters of the following I/O types:

- General Purpose I/O (GPIO)

The GPIO load circuit and output transition time waveforms are shown in Figure 5 and Figure 6.

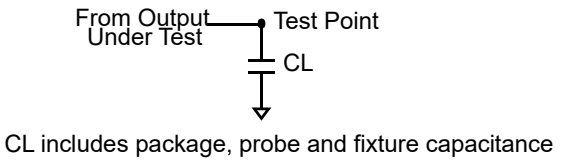


Figure 5. Load circuit for output

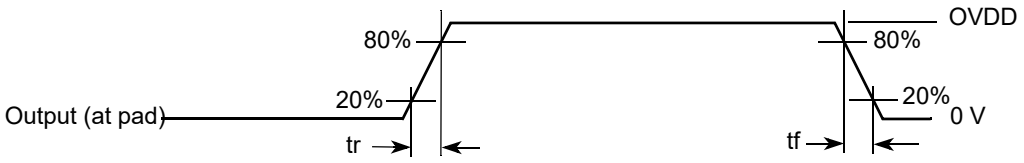


Figure 6. Output transition time waveform

3.6.1 General purpose I/O AC parameters

This section presents the I/O AC parameters for GPIO in different modes. Note that the fast or slow I/O behavior is determined by the appropriate control bits in the IOMUXC control registers.

Table 24. Maximum frequency of operation for input

Maximum frequency (MHz)	
VDD = 1.8 V, CL = 50 pF	**VDD = 3.3 V, CL = 50 pF**
450	440

Table 25. Maximum frequency of operation for output

Parameter			Maximum Frequency (MHz)			
			VDD = 1.8 V		VDD = 3.3 V	
dse[2:0]	**sre[1:0]**	**Driver type**	**CL = 10 pF**	**CL = 20 pF**	**CL = 10 pF**	**CL = 20 pF**
00X	0X	1x Slow Slew	150	80	120	65
00X	1X	1x Fast Slew	150	80	120	65
10X	0X	2x Slow Slew	160	90	150	80
10X	1X	2x Fast Slew	160	90	150	80
01X	0X	4x Slow Slew	200	100	180	90
01X	1X	4x Fast Slew	200	100	180	90
11X	0X	6x Slow Slew	250	130	200	100
11X	1X	6x Fast Slew	250	130	200	100

3.7 Output buffer impedance parameters

This section defines the I/O impedance parameters of the i.MX 8M Nano family of processors for the following I/O types:

NOTE

DDR I/O output driver impedance is measured with “long” transmission line of impedance Ztl attached to I/O pad and incident wave launched into transmission line. Rpu/Rpd and Ztl form a voltage divider that defines specific voltage of incident wave relative to OVDD. Output driver impedance is calculated from this voltage divider (see Figure 7).

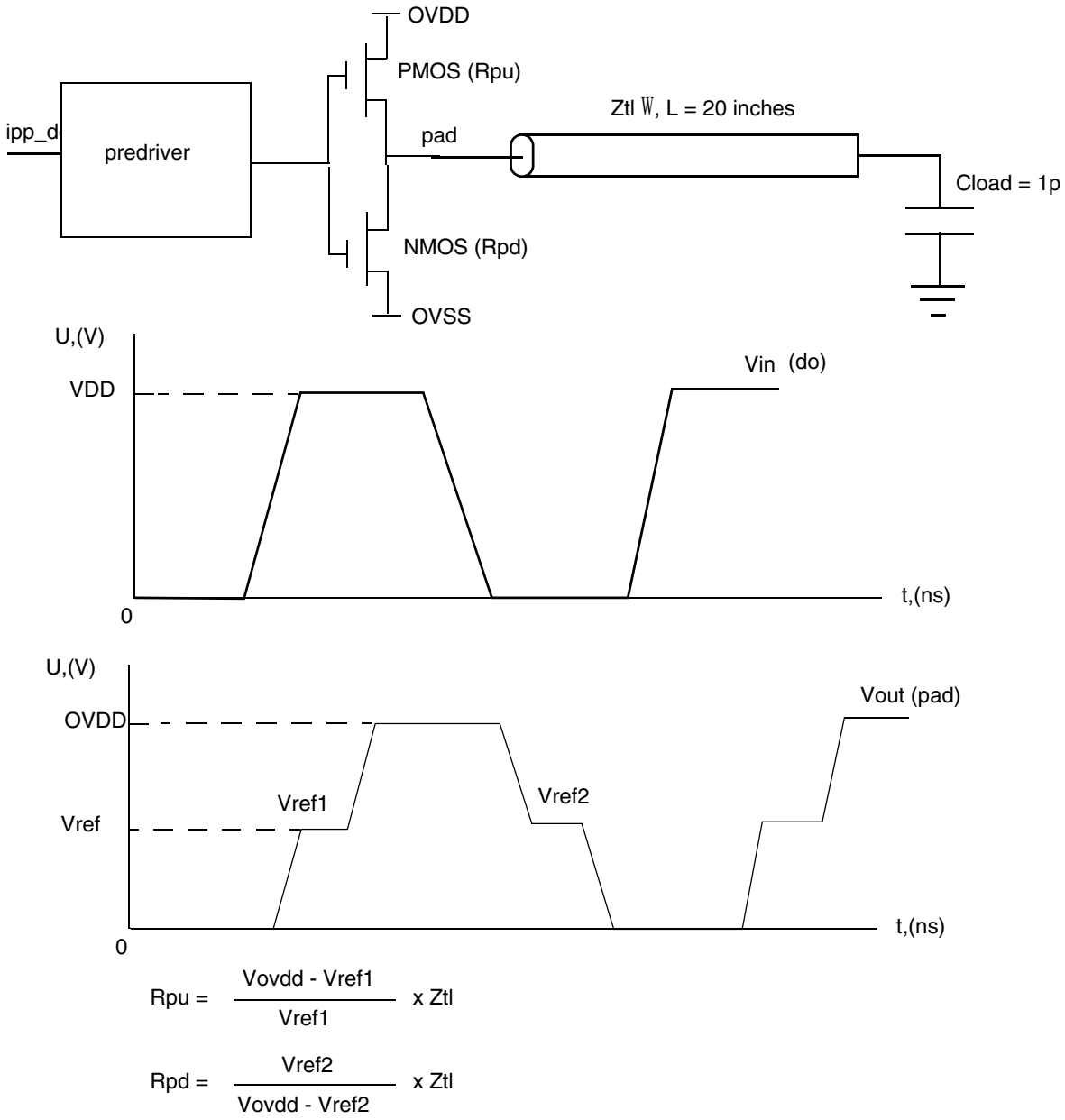


Figure 7. Impedance matching load for measurement

3.7.1 DDR I/O output buffer impedance

Table 26 shows DDR I/O output buffer impedance of i.MX 8M Nano family of processors.

Table 26. DDR I/O output buffer impedance

Parameter	Symbol	Test Conditions DSE (Drive Strength)	Typical			Unit
			NVCC_DRAM = 1.35 V (DDR3L)	NVCC_DRAM = 1.2 V (DDR4)	NVCC_DRAM = 1.1 V (LPDDR4)	
Output Driver Impedance	Rdrv	000000	Hi-Z	Hi-Z	Hi-Z	Ω
		000010	240	240	240	
		001000	120	120	120	
		001010	80	80	80	
		011000	60	60	60	
		011010	48	48	48	
		111000	40	40	40	
		111010	34	34	34	

Note:

1. Output driver impedance is controlled across PVTs using ZQ calibration procedure.
2. Calibration is done against 240 Ω external reference resistor.
3. Output driver impedance deviation (calibration accuracy) is ±5% (max/min impedance) across PVTs.

3.8 System modules timing

This section contains the timing and electrical parameters for the modules in each i.MX 8M Nano processor.

3.8.1 Reset timings parameters

Figure 8 shows the reset timing and Table 27 lists the timing parameters.

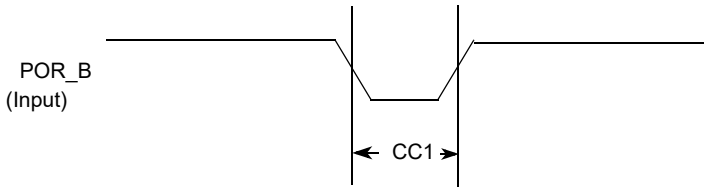


Figure 8. Reset timing diagram

Table 27. Reset timing parameters

ID	Parameter	Min	Max	Unit
CC1	Duration of POR_B to be qualified as valid.	1	—	RTC_XTALI cycle

3.8.2 WDOG Reset timing parameters

Figure 9 shows the WDOG reset timing and Table 28 lists the timing parameters.

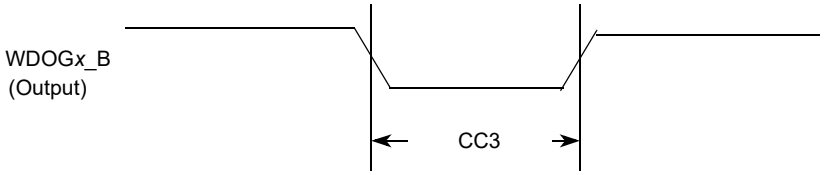


Figure 9. WDOG*x*_B timing diagram

Table 28. WDOG*x*_B timing parameters

ID	Parameter	Min	Max	Unit
CC3	Duration of WDOG1_B Assertion	1	—	RTC_XTALI cycle

NOTE

RTC_XTALI is approximately 32 kHz. RTC_XTALI cycle is one period or approximately 30 µs.

NOTE

WDOG*x*_B output signals (for each one of the Watchdog modules) do not have dedicated pins, but are muxed out through the IOMUX. See the IOMUXC chapter of the *i.MX 8M Nano Applications Processor Reference Manual* (IMX8MNRM) for detailed information.

3.9 External peripheral interface parameters

The following subsections provide information on external peripheral interfaces.

3.9.1 ECSPI timing parameters

This section describes the timing parameters of the ECSPI blocks. The ECSPI have separate timing parameters for master and slave modes.

3.9.1.1 ECSPI Master mode timing

Figure 10 depicts the timing of ECSPI in master mode. Table 29 lists the ECSPI master mode timing characteristics.

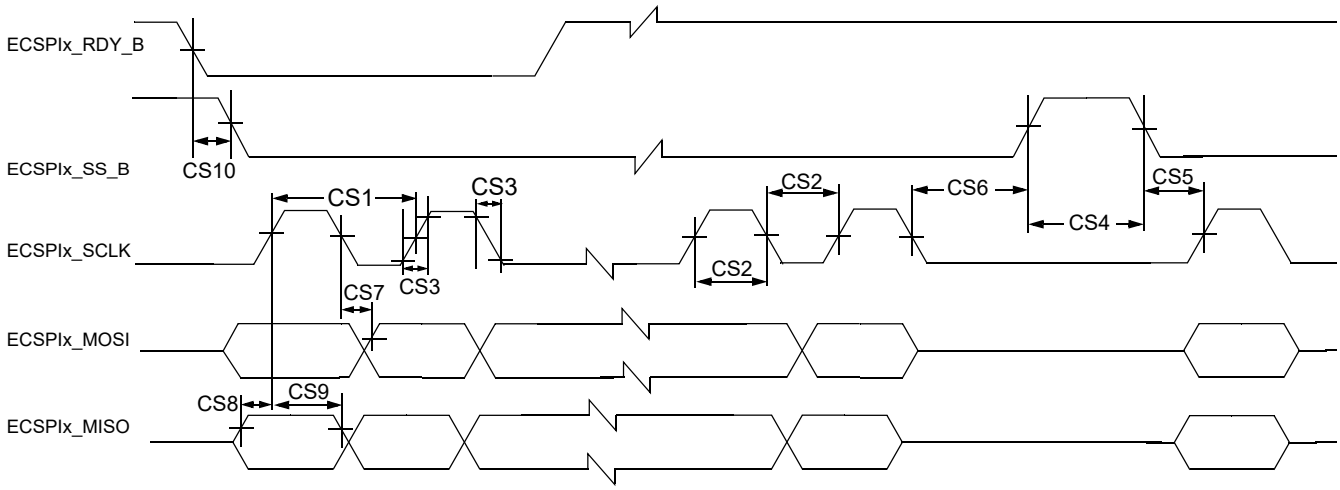


Figure 10. ECSPI Master mode timing diagram

Table 29. ECSPI Master mode timing parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	ECSPIx_SCLK Cycle Time–Read ECSPIx_SCLK Cycle Time–Write	t_{clk}	43 15	—	ns
CS2	ECSPIx_SCLK High or Low Time–Read ECSPIx_SCLK High or Low Time–Write	t_{SW}	21.5 7	—	ns
CS3	ECSPIx_SCLK Rise or Fall[1]	$t_{RISE/FALL}$	—	—	ns
CS4	ECSPIx_SS_B pulse width	t_{CSLH}	Half ECSPIx_SCLK period	—	ns
CS5	ECSPIx_SS_B Lead Time (CS setup time)	t_{SCS}	Half ECSPIx_SCLK period - 4	—	ns
CS6	ECSPIx_SS_B Lag Time (CS hold time)	t_{HCS}	Half ECSPIx_SCLK period - 2	—	ns
CS7	ECSPIx_MOSI Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmosi}	-1	1	ns
CS8	ECSPIx_MISO Setup Time	t_{Smiso}	18	—	ns
CS9	ECSPIx_MISO Hold Time	t_{Hmiso}	0	—	ns
CS10	RDY to ECSPIx_SS_B Time[2]	t_{SDRY}	5	—	ns

1 See specific I/O AC parameters Section 3.6, I/O AC parameters".

2 SPI_RDY is sampled internally by ipg_clk and is asynchronous to all other CSPI signals.

3.9.1.2 ECSPI Slave mode timing

Figure 11 depicts the timing of ECSPI in Slave mode. Table 30 lists the ECSPI Slave mode timing characteristics.

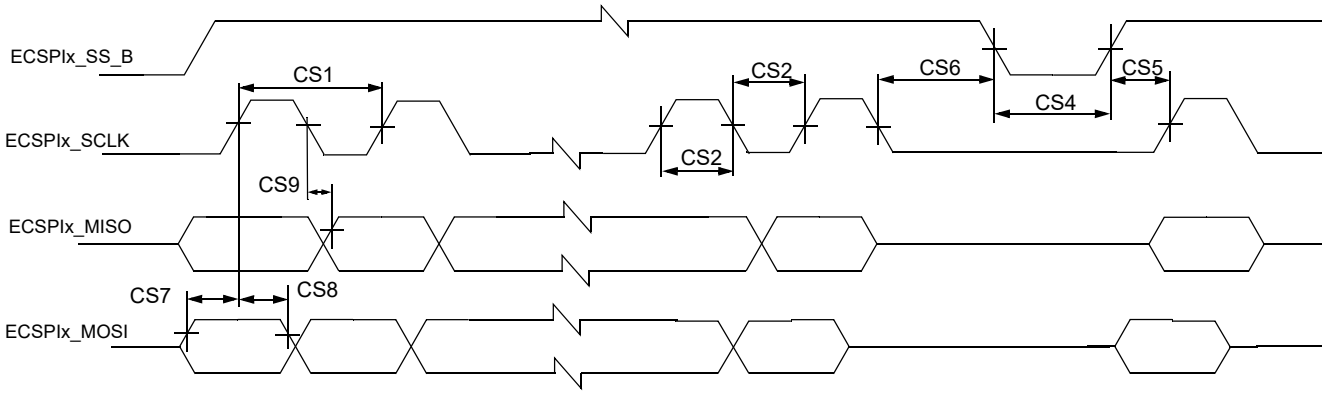


Figure 11. ECSPI Slave mode timing diagram

Table 30. ECSPI Slave mode timing parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	ECSPIx_SCLK Cycle Time–Read ECSPI_SCLK Cycle Time–Write	t_{clk}	15 43	—	ns
CS2	ECSPIx_SCLK High or Low Time–Read ECSPIx_SCLK High or Low Time–Write	t_{SW}	7 21.5	—	ns
CS4	ECSPIx_SS_B pulse width	t_{CSLH}	Half ECSPIx_SCLK period	—	ns
CS5	ECSPIx_SS_B Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	ECSPIx_SS_B Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	ECSPIx_MOSI Setup Time	t_{Smosi}	4	—	ns
CS8	ECSPIx_MOSI Hold Time	t_{Hmosi}	4	—	ns
CS9	ECSPIx_MISO Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmiso}	4	19	ns

3.9.2 Ultra-high-speed SD/SDIO/MMC host interface (uSDHC) AC timing

This section describes the electrical information of the uSDHC, which includes SD/eMMC 5.1 (single data rate) timing, eMMC 5.1/SD3.0 (dual data rate) AC timing, and SDR50/SDR104 AC timing.

3.9.2.1 SD/eMMC5.1 (single data rate) AC timing

Figure 12 depicts the timing of SD3.0/eMMC5.1 (SDR), and Table 31 lists the SD3.0/eMMC5.1 (SDR) timing characteristics.

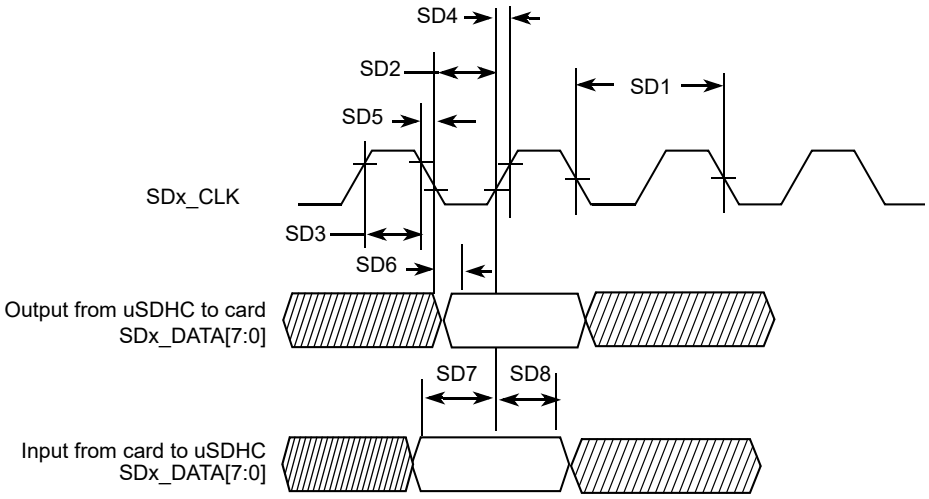


Figure 12. SD3.0/eMMC5.1 (SDR) timing

Table 31. SD3.0/eMMC5.1 (SDR) interface timing specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}[3]	0	20/52	MHz
	Clock Frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
SD4	Clock Rise Time	t_{TLH}	—	3	ns
SD5	Clock Fall Time	t_{THL}	—	3	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD6	uSDHC Output Delay	t_{OD}	6.6	3.6	ns

Table 31. SD3.0/eMMC5.1 (SDR) interface timing specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD7	uSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD8	uSDHC Input Hold Time[4]	t_{IH}	1.5	—	ns

1 In Low-Speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

2 In Normal (Full) -Speed mode for SD/SDIO card, clock frequency can be any value between 0 — 25 MHz. In High-speed mode, clock frequency can be any value between 0 — 50 MHz.

3 In Normal (Full) -Speed mode for MMC card, clock frequency can be any value between 0 — 20 MHz. In High-speed mode, clock frequency can be any value between 0 — 52 MHz.

4 To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

3.9.2.2 eMMC5.1/SD3.0 (dual data rate) AC timing

Figure 13 depicts the timing of eMMC5.1/SD3.0 (DDR). Table 32 lists the eMMC5.1/SD3.0 (DDR) timing characteristics. Be aware that only DATA is sampled on both edges of the clock (not applicable to CMD).

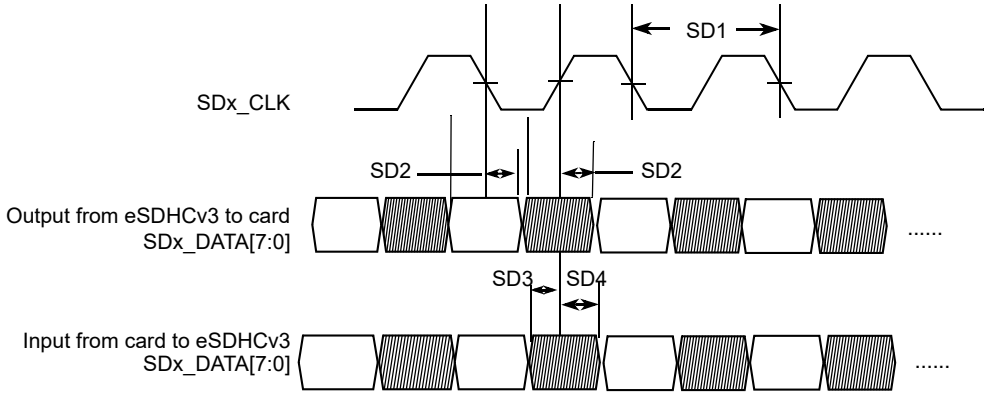


Figure 13. eMMC5.1/SD3.0 (DDR) timing

Table 32. eMMC5.1/SD3.0 (DDR) interface timing specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (eMMC5.1 DDR)	f_{PP}	0	52	MHz
SD1	Clock Frequency (SD3.0 DDR)	f_{PP}	0	50	MHz
uSDHC Output / Card Inputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD2	uSDHC Output Delay	t_{OD}	2.7	6.9	ns
uSDHC Input / Card Outputs SD_CMD, SDx_DATAx (Reference to CLK)					

Table 32. eMMC5.1/SD3.0 (DDR) interface timing specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
SD3	uSDHC Input Setup Time	t_{ISU}	2.4	—	ns
SD4	uSDHC Input Hold Time	t_{IH}	1.3	—	ns

3.9.2.3 HS400 DDR AC timing

Figure 14 depicts the timing of HS400 mode, and Table 33 lists the HS400 timing characteristics. Be aware that only data is sampled on both edges of the clock (not applicable to CMD). The CMD input/output timing for HS400 mode is the same as CMD input/output timing for SDR104 mode. Check SD5, SD6, and SD7 parameters in Table 35 SDR50/SDR104 Interface Timing Specification for CMD input/output timing for HS400 mode.

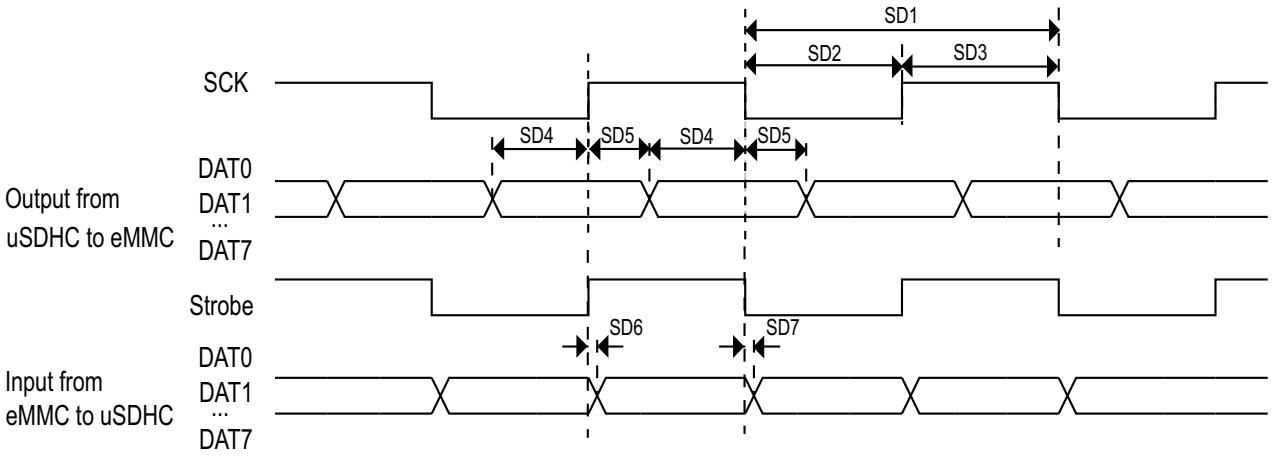


Figure 14. HS400 Mode timing

Table 33. HS400 interface timing specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock frequency	f_{PP}	0	200	MHz
SD2	Clock low time	t_{CL}	0.46 x t_{CLK}	0.54 x t_{CLK}	ns
SD3	Clock high time	t_{CH}	0.46 x t_{CLK}	0.54 x t_{CLK}	ns
uSDHC Output/Card Inputs DAT (Reference to SCK)					
SD4	Output skew from data of edge of SCK	t_{OSkew1}	0.45	—	ns
SD5	Output skew from edge of SCk to data	t_{OSkew2}	0.45	—	ns
uSDHC Input/Card Outputs DAT (Reference to Strobe)					

Table 33. HS400 interface timing specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
SD6	uSDHC input skew	t_{RQ}	—	0.45	ns
SD7	uSDHC hold skew	t_{RQH}	—	0.45	ns

3.9.2.4 HS200 Mode AC timing

Figure 15 depicts the timing of HS200 mode, and Table 34 lists the HS200 timing characteristics.

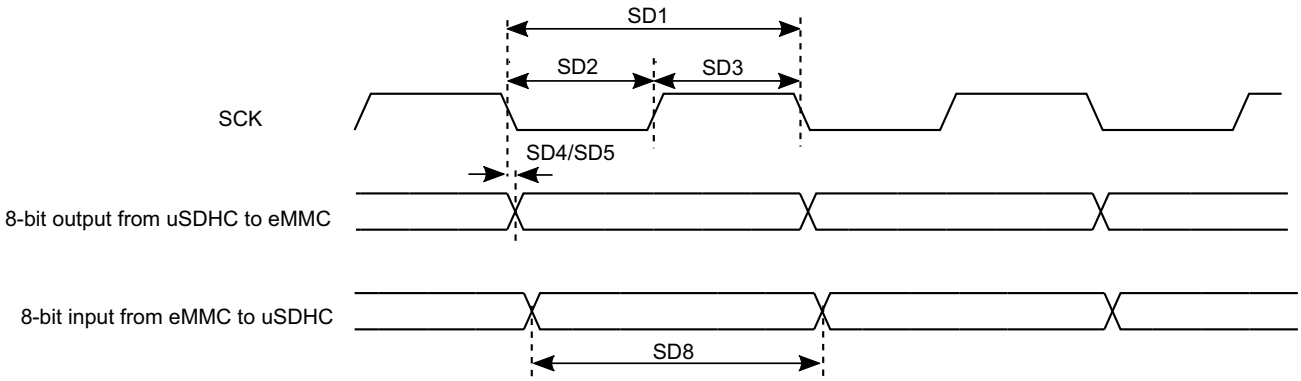


Figure 15. HS200 timing

Table 34. HS200 interface timing specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	5.0	—	ns
SD2	Clock Low Time	t_{CL}	0.3 x t_{CLK}	0.7 x t_{CLK}	ns
SD3	Clock High Time	t_{CH}	0.3 x t_{CLK}	0.7 x t_{CLK}	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in HS200 (Reference to CLK)					
SD5	uSDHC Output Delay	t_{OD}	-1.6	1	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in HS200 (Reference to CLK)[1]					
SD8	uSDHC Output Data Window	t_{ODW}	0.5 x t_{CLK}	—	ns

1 HS200 is for 8 bits while SDR104 is for 4 bits.

3.9.2.5 SDR50/SDR104 AC timing

Figure 16 depicts the timing of SDR50/SDR104, and Table 35 lists the SDR50/SDR104 timing characteristics.

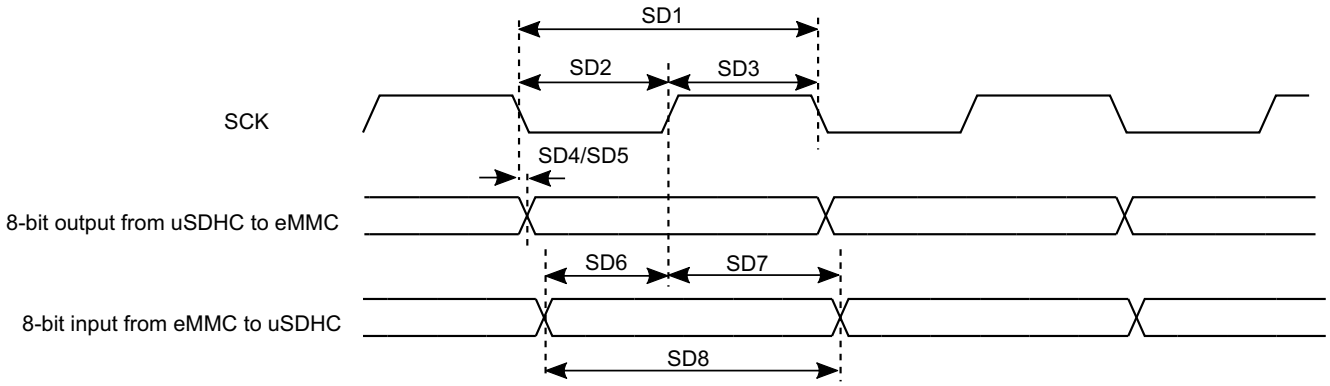


Figure 16. SDR50/SDR104 timing

Table 35. SDR50/SDR104 interface timing specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	5	—	ns
SD2	Clock Low Time	t_{CL}	0.46 x t_{CLK}	0.54 x t_{CLK}	ns
SD3	Clock High Time	t_{CH}	0.46 x t_{CLK}	0.54 x t_{CLK}	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR50 (Reference to CLK)					
SD4	uSDHC Output Delay	t_{OD}	-3	1	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR104 (Reference to CLK)					
SD5	uSDHC Output Delay	t_{OD}	-1.6	1	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR50 (Reference to CLK)					
SD6	uSDHC Input Setup Time	t_{ISU}	2.4	—	ns
SD7	uSDHC Input Hold Time	t_{IH}	1.4	—	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR104 (Reference to CLK)[1]					
SD8	uSDHC Output Data Window	t_{ODW}	0.5 x t_{CLK}	—	ns

[1] Data window in SDR100 mode is variable.

3.9.2.6 Bus operation condition for 3.3 V and 1.8 V signaling

Signaling level of SD/eMMC4.5/5.0/5.1 can be 1.8 V or 3.3 V depending on the working mode. The DC parameters for the NVCC_SD1, NVCC_SD2 and NVCC_SD3 supplies are identical to those shown in Table 22, "GPIO DC parameters," on page 28.

3.9.3 Ethernet controller (ENET) AC electrical specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

Table 36. ENET signal mapping

Pad name	RGMII/RMII signal	Mode	Alt mode	Direction	Comments
ENET_MDC	MDC	RMII/RGMII	ALT0	O	—
ENET_MDIO	MDIO	RMII/RGMII	ALT0	I/O	—
ENET_TD3	TX_D3	RGMII	ALT0	O	Only used for RGMII
ENET_TD2	REF_CLK	RMII	ALT1	I/O	Used as RMII clock and RGMII data, there are two RMII clock schemes. • MAC generate output 50M reference clock for PHY, and MAC also use this 50M clock. • MAC use external 50M clock. For RMII—ENET_TD2 functions as RMII REF_CLK when configured in the ALT1 mode.
	TX_D2	RGMII	ALT0		
ENET_TD1	TX_D1	RMII/RGMII	ALT0	O	—
ENET_TD0	TX_D0	RMII/RGMII	ALT0	O	—
ENET_TX_CTL	TX_EN	RMII	ALT0	O	—
	TX_CTL	RGMII	ALT0		
ENET_TXC	TX_ER	RMII	ALT1	O	For RMII—ENET_TXC functions as RMII TX_ER when configured in the ALT1 mode. For RGMII—ENET_TXC functions as RGMII TXC when configured in the ALT0 mode.
	TXC	RGMII	ALT0		
ENET_RX_CTL	RX_EN (CRS_DV)	RMII	ALT0	I	—
	RX_CTL	RGMII	ALT0		
ENET_RXC	RX_ER	RMII	ALT1	I	For RMII—ENET_RXC functions as RMII RX_ER when configured in the ALT1 mode. For RGMII—ENET_RXC functions as RGMII RXC when configured in the ALT0 mode.
	RXC	RGMII	ALT0		
ENET_RD0	RX_D0	RMII/RGMII	ALT0	I	—
ENET_RD1	RX_D1	RMII/RGMII	ALT0	I	—
ENET_RD2	RX_D2	RGMII	ALT0	I	—
ENET_RD3	RX_D3	RGMII	ALT0	I	—
GPIO1_IO06	MDC	RMII/RGMII	ALT1	O	—
GPIO1_IO07	MDIO	RMII/RGMII	ALT1	I/O	—
I2C1_SCL	MDC	RMII/RGMII	ALT1	O	—
I2C1_SDA	MDIO	RMII/RGMII	ALT1	I/O	—

Table 36. ENET signal mapping (continued)

Pad name	RGMII/RMII signal	Mode	Alt mode	Direction	Comments
GPIO1_IO08	1588_EVENT0_IN	RMII/RGMII	ALT1	I	Capture/compare block input/output event bus signal. When configured for capture and a rising edge is detected, the current timer value is latched and transferred into the corresponding ENET_TCCRn register for inspection by software. When configured for compare, the corresponding signal 1588_EVENT is asserted for one cycle when the timer reaches the compare value programmed in register ENET_TCCRn. An interrupt or DMA request can be triggered if the corresponding bit in ENET_TCSRn[TIE] or ENET_TSCRn[TDRE] is set.
GPIO1_IO09	1588_EVENT0_OUT	RMII/RGMII	ALT1	O	—
I2C2_SCL	1588_EVENT1_IN	RMII/RGMII	ALT1	I	—
I2C2_SDA	1588_EVENT1_OUT	RMII/RGMII	ALT1	O	—
GPIO1_IO00	ENET_PHY_REF_CLK_ROOT	RGMII	ALT1	O	Reference clock for PHY.
SD1_CLK	MDC	RMII	ALT1	O	—
SD1_CMD	MDIO	RMII	ALT1	I/O	—
SD1_DATA0	TX_D1	RMII	ALT1	O	—
SD1_DATA1	TX_D0	RMII	ALT1	O	—
SD1_DATA2	RX_D0	RMII	ALT1	I	—
SD1_DATA3	RX_D1	RMII	ALT1	I	—
SD1_DATA4	TX_EN	RMII	ALT1	O	—
SD1_DATA5	TX_ER	RMII	ALT1	O	For RMII—SD1_DATA5 functions as RMII TX_ER when configured in the ALT1 mode.
SD1_DATA6	RX_EN (CRS_DV)	RMII	ALT1	I	—
SD1_DATA7	RX_ER	RMII	ALT1	I	For RMII—SD1_DATA7 functions as RMII RX_ER when configured in the ALT1 mode.
SD1_RESET_B	REF_CLK	RMII	ALT1	O	For RMII—SD1_RESET_B functions as RMII REF_CLK when configured in the ALT1 mode.

3.9.3.1 RMII mode timing

Figure 17 shows RMII mode timings. Table 37 describes the timing parameters (M16–M21) shown in the figure.

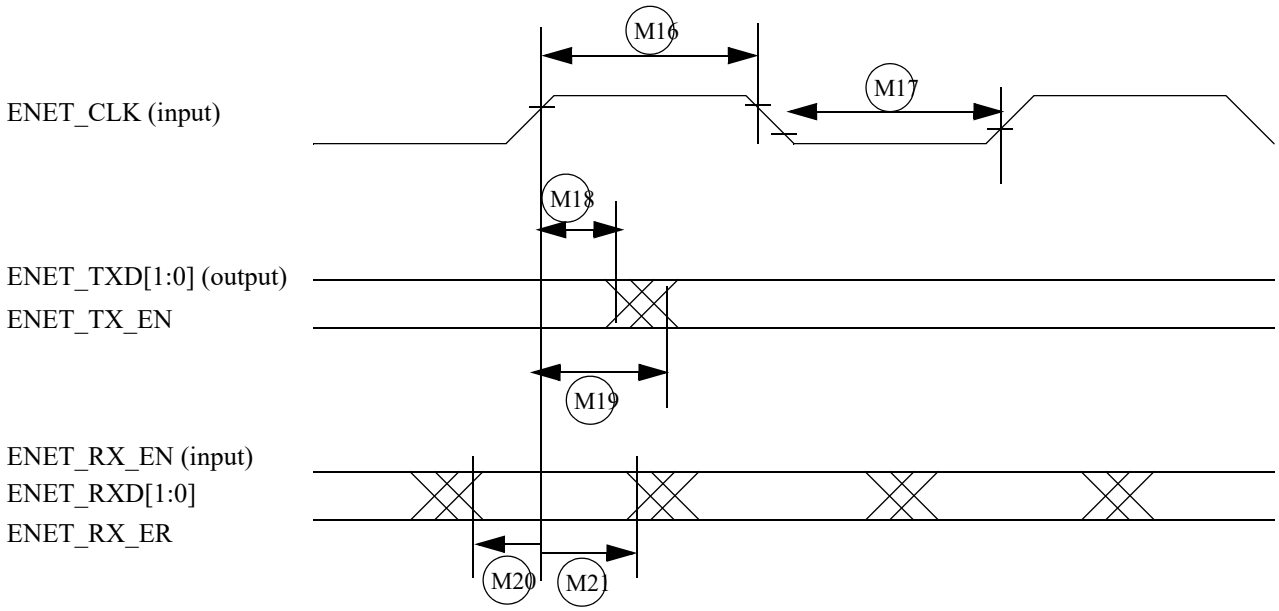


Figure 17. RMII mode signal timing diagram

Table 37. RMII signal timing

ID	Characteristic	Min.	Max.	Unit
M16	ENET_CLK pulse width high	35%	65%	ENET_CLK period
M17	ENET_CLK pulse width low	35%	65%	ENET_CLK period
M18	ENET_CLK to ENET_TXD[1:0], ENET_TXD invalid	4	—	ns
M19	ENET_CLK to ENET_TXD[1:0], ENET_TXD valid	—	15	ns
M20	ENET_RXD[1:0], ENET_RX_EN, ENET_RX_ER to ENET_CLK setup	4	—	ns
M21	ENET_CLK to ENET_RXD[1:0], ENET_RX_EN, ENET_RX_ER hold	2	—	ns

3.9.3.2 RGMII signal switching specifications

The following timing specifications meet the requirements for RGMII interfaces for a range of transceiver devices.

Table 38. RGMII signal switching specifications[1]

Symbol	Description	Min.	Max.	Unit
T_{cyc}[2]	Clock cycle duration	7.2	8.8	ns
T_{skewT}[3]	Data to clock output skew at transmitter	-500	500	ps
T_{skewR}[3]	Data to clock input skew at receiver	1	2.6	ns
Duty_G[4]	Duty cycle for Gigabit	45	55	%
Duty_T[4]	Duty cycle for 10/100T	40	60	%
Tr/Tf	Rise/fall time (20–80%)	—	0.75	ns

1 The timings assume the following configuration:
DDR_SEL = (11)b
DSE (drive-strength) = (111)b

2 For 10 Mbps and 100 Mbps, T_{cyc} will scale to 400 ns ±40 ns and 40 ns ±4 ns respectively.

3 For all versions of RGMII prior to 2.0; this implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns and less than 2.0 ns will be added to the associated clock signal. For 10/100, the Max value is unspecified.

4 Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.

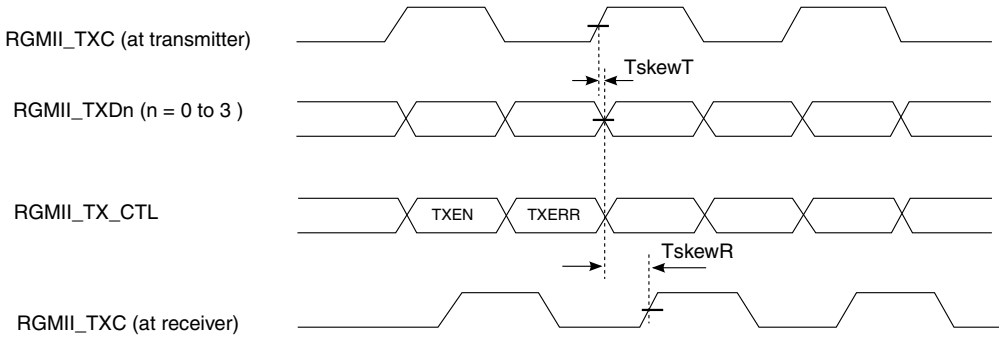


Figure 18. RGMII transmit signal timing diagram original

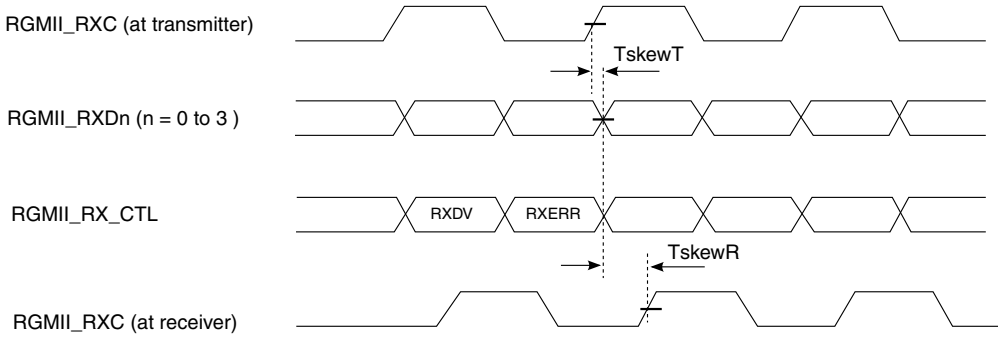


Figure 19. RGMII receive signal timing diagram original

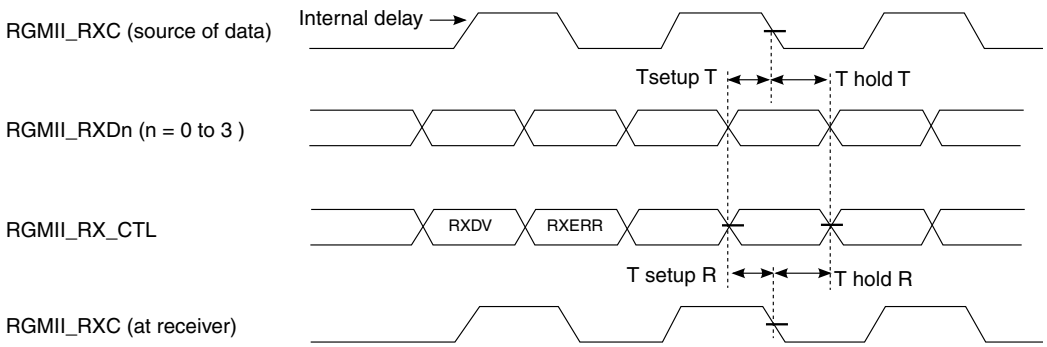


Figure 20. RGMII receive signal timing diagram with internal delay

3.9.4 General-purpose media interface (GPMI) timing

The i.MX 8M Nano GPMI controller is a flexible interface NAND Flash controller with 8-bit data width, up to 200 MB/s I/O speed and individual chip select.

It supports Asynchronous Timing mode, Source Synchronous Timing mode and Toggle Timing mode separately, as described in the following subsections.

3.9.4.1 Asynchronous mode AC timing (ONFI 1.0 compatible)

Asynchronous mode AC timings are provided as multiplications of the clock cycle and fixed delay. The maximum I/O speed of GPMI in Asynchronous mode is about 50 MB/s. Figure 21 through Figure 24 depicts the relative timing between GPMI signals at the module level for different operations under Asynchronous mode. Table 39 describes the timing parameters (NF1–NF17) that are shown in the figures.

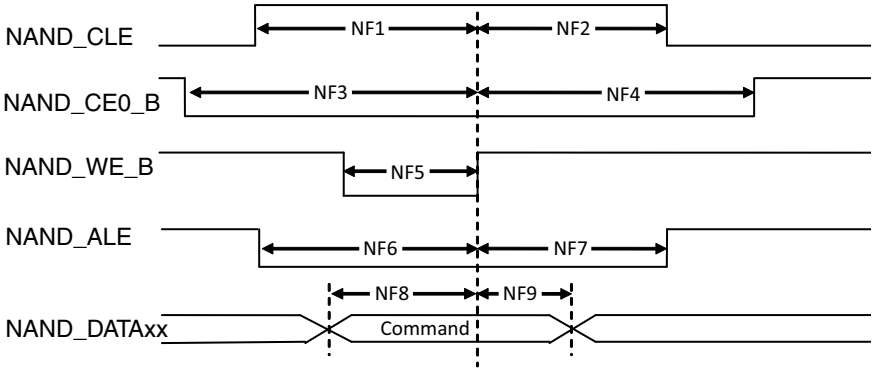


Figure 21. Command Latch cycle timing diagram

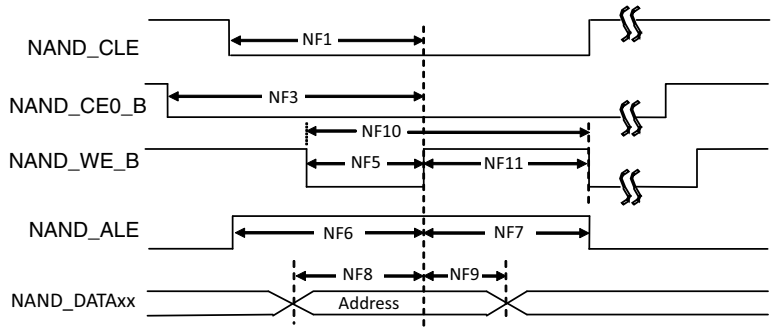


Figure 22. Address Latch cycle timing diagram

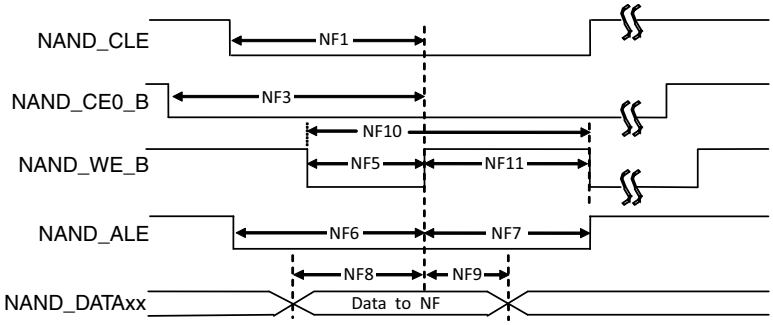


Figure 23. Write Data Latch cycle timing diagram

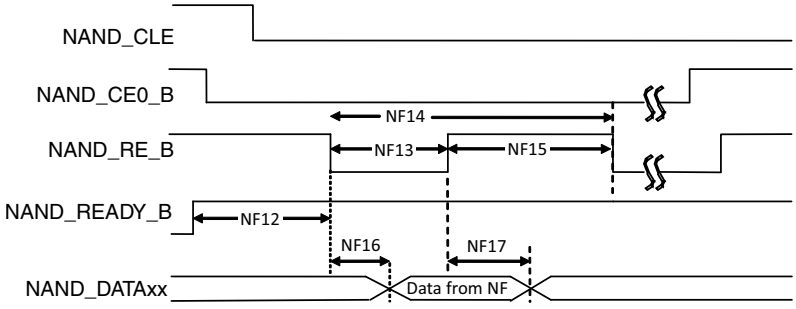


Figure 24. Read Data Latch cycle timing diagram (Non-EDO Mode)

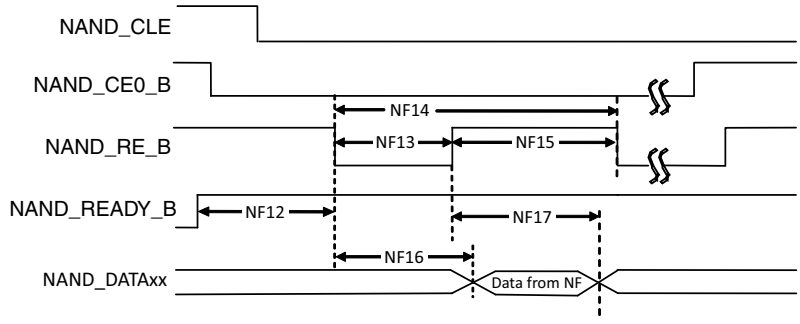


Figure 25. Read Data Latch cycle timing diagram (EDO mode)

Table 39. Asynchronous mode timing parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF1	NAND_CLE setup time	tCLS	(AS + DS) × T - 0.12 [see notes[2,3]]		ns
NF2	NAND_CLE hold time	tCLH	DH × T - 0.72 [see note[2]]		ns
NF3	NAND_CE0_B setup time	tCS	(AS + DS + 1) × T [see notes[3,2]]		ns
NF4	NAND_CE0_B hold time	tCH	(DH+1) × T - 1 [see note[2]]		ns
NF5	NAND_WE_B pulse width	tWP	DS × T [see note[2]]		ns
NF6	NAND_ALE setup time	tALS	(AS + DS) × T - 0.49 [see notes[3,2]]		ns
NF7	NAND_ALE hold time	tALH	DH × T - 0.42 [see note[2]]		ns
NF8	Data setup time	tDS	DH × T - 0.26 [see note[2]]		ns
NF9	Data hold time	tDH	DH × T - 1.37 [see note[2]]		ns
NF10	Write cycle time	tWC	(DS + DH) × T [see note[2]]		ns
NF11	NAND_WE_B hold time	tWH	DH × T [see note[2]]		ns
NF12	Ready to NAND_RE_B low	tRR[4]	(AS + 2) × T [see [3,2]]	—	ns
NF13	NAND_RE_B pulse width	tRP	DS × T [see note[2]]		ns
NF14	READ cycle time	tRC	(DS + DH) × T [see note[2]]		ns
NF15	NAND_RE_B high hold time	tREH	DS × T [see note[2]]		ns
NF16	Data setup on read	tDSR	—	(DS × T -0.67)/18.38 [see notes[5,6]]	ns
NF17	Data hold on read	tDHR	0.82/11.83 [see notes[5,6]]	—	ns

1 GPMI's Asynchronous mode output timing can be controlled by the module's internal registers HW_GPMI_TIMING0_ADDRESS_SETUP, HW_GPMI_TIMING0_DATA_SETUP, and HW_GPMI_TIMING0_DATA_HOLD. This AC timing depends on these registers settings. In the table, AS/DS/DH represents each of these settings.

2 AS minimum value can be 0, while DS/DH minimum value is 1.

3 T = GPMI clock period -0.075 ns (half of maximum p-p jitter).

4 NF12 is guaranteed by the design.

5 Non-EDO mode.

6 EDO mode, GPMI clock ≈ 100 MHz
(AS=DS=DH=1, GPMI_CTL1 [RDN_DELAY] = 8, GPMI_CTL1 [HALF_PERIOD] = 0).

In EDO mode (Figure 24), NF16/NF17 are different from the definition in non-EDO mode (Figure 23). They are called tREA/tRHOH (RE# access time/RE# HIGH to output hold). The typical values for them are 16 ns (max for tREA)/15 ns (min for tRHOH) at 50 MB/s EDO mode. In EDO mode, GPMI samples NAND_DATAxx at the rising edge of delayed NAND_RE_B provided by an internal DPLL. The delay value can be controlled by GPMI_CTRL1.RDN_DELAY (see the GPMI chapter of the *i.MX 8M Nano Applications Processor Reference Manual* [IMX8MNRM]). The typical value of this control register is 0x8 at 50 MT/s EDO mode. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

3.9.4.2 Source synchronous mode AC timing (ONFI 2.x compatible)

Figure 26 to Figure 28 show the write and read timing of Source Synchronous mode.

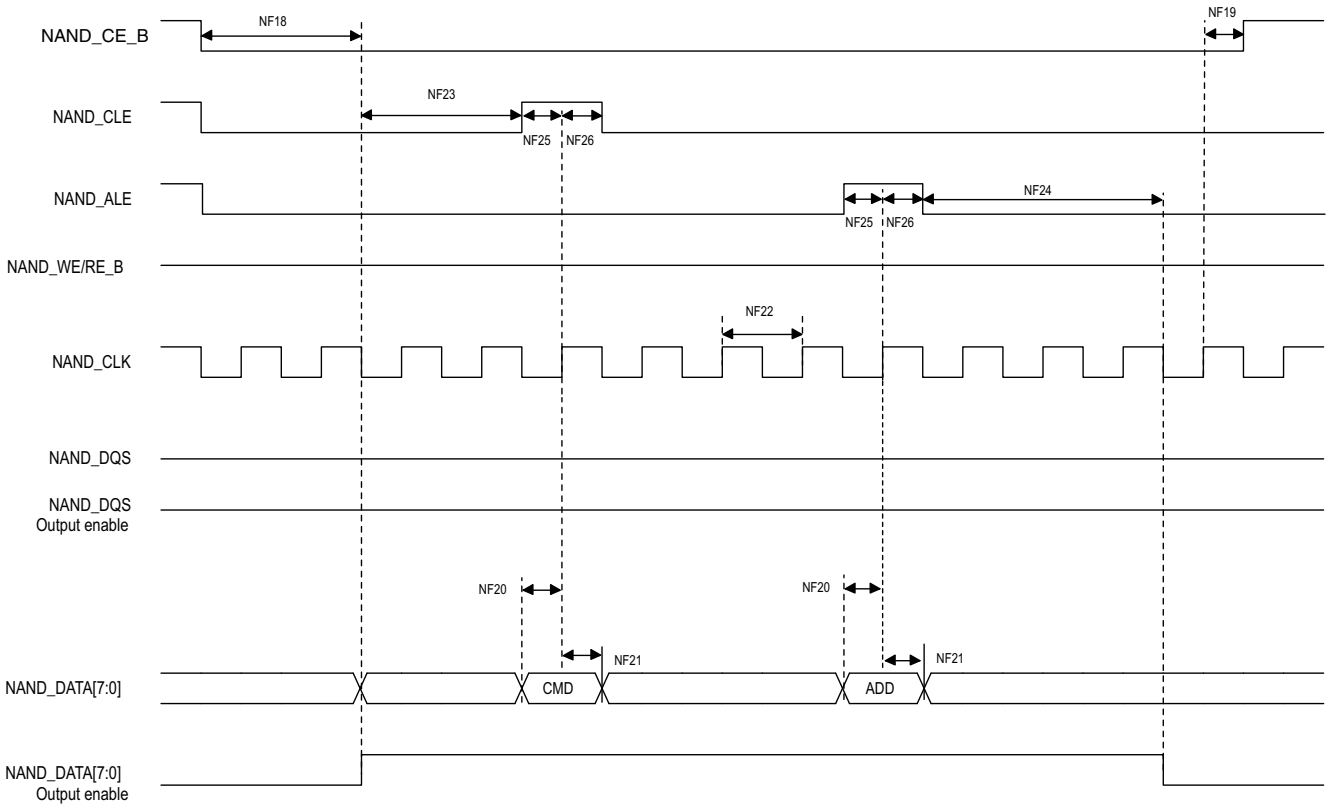


Figure 26. Source Synchronous mode command and address timing diagram

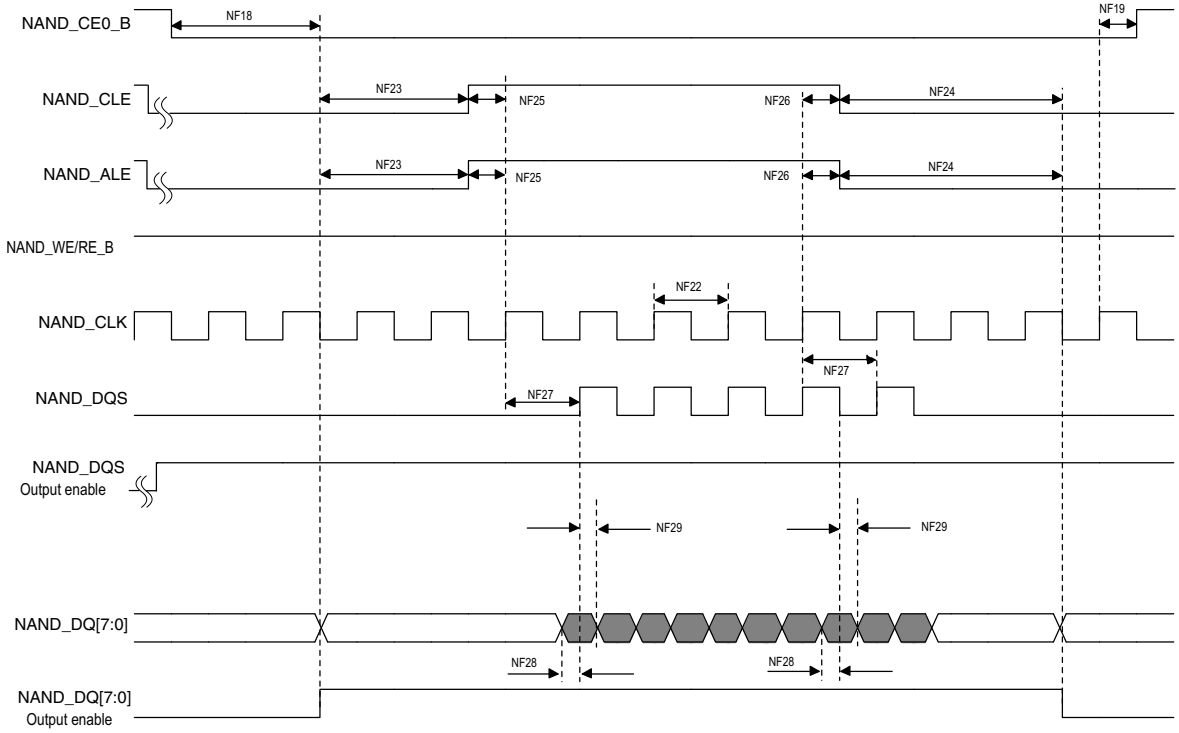


Figure 27. Source Synchronous mode data write timing diagram

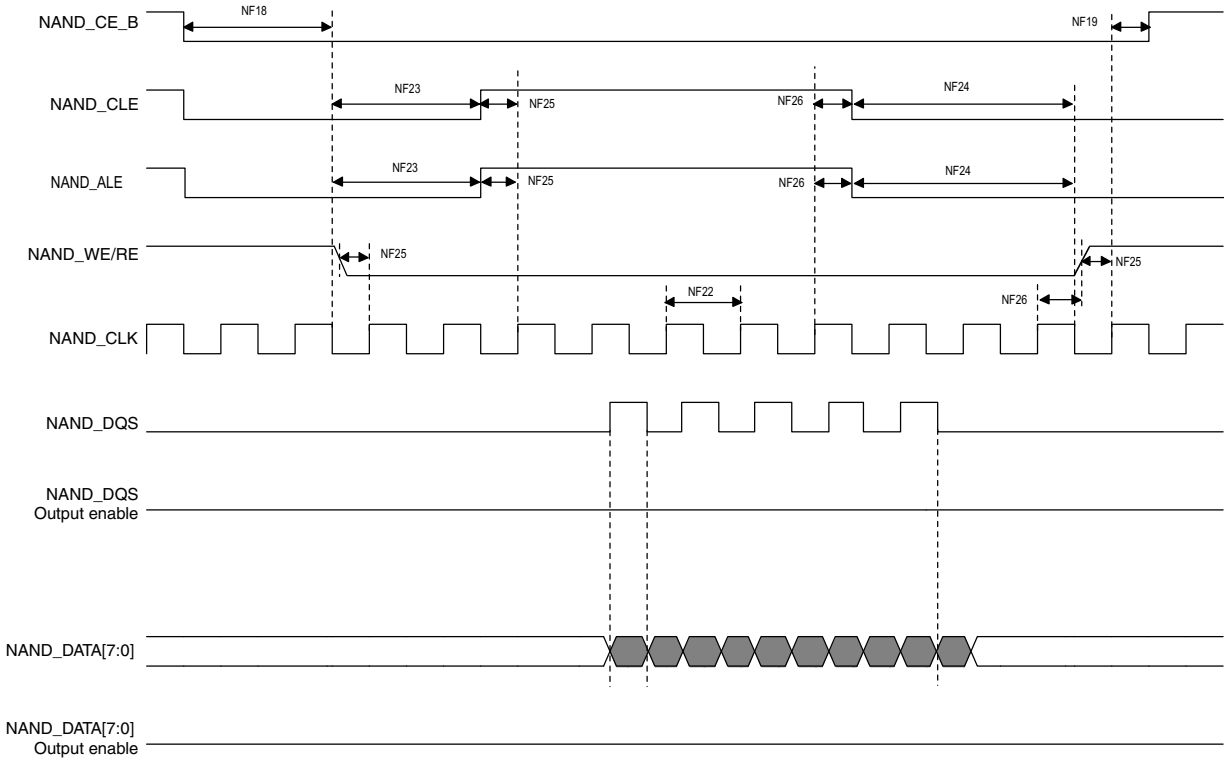


Figure 28. Source Synchronous mode data read timing diagram

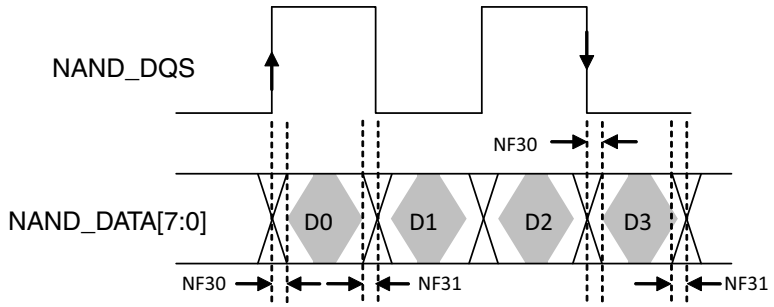


Figure 29. NAND_DQS/NAND_DQ read valid window

Table 40. Source Synchronous mode timing parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF18	NAND_CE0_B access time	tCE	CE_DELAY × T - 0.79 [see note[2]]		ns
NF19	NAND_CE0_B hold time	tCH	0.5 × tCK - 0.63 [see note[2]]		ns
NF20	Command/address NAND_DATAxx setup time	tCAS	0.5 × tCK - 0.05		ns
NF21	Command/address NAND_DATAxx hold time	tCAH	0.5 × tCK - 1.23		ns
NF22	clock period	tCK	—		ns
NF23	preamble delay	tPRE	PRE_DELAY × T - 0.29 [see note[2]]		ns
NF24	postamble delay	tPOST	POST_DELAY × T - 0.78 [see note[2]]		ns
NF25	NAND_CLE and NAND_ALE setup time	tCALS	0.5 × tCK - 0.86		ns
NF26	NAND_CLE and NAND_ALE hold time	tCALH	0.5 × tCK - 0.37		ns
NF27	NAND_CLK to first NAND_DQS latching transition	tDQSS	T - 0.41 [see note[2]]		ns
NF28	Data write setup	—	0.25 × tCK - 0.35		
NF29	Data write hold	—	0.25 × tCK - 0.85		
NF30	NAND_DQS/NAND_DQ read setup skew	—	—	2.06	
NF31	NAND_DQS/NAND_DQ read hold skew	—	—	1.95	

1 GPMI's Source Synchronous mode output timing can be controlled by the module's internal registers GPMI_TIMING2_CE_DELAY, GPMI_TIMING_PREAMBLE_DELAY, GPMI_TIMING2_POST_DELAY. This AC timing depends on these registers settings. In the table, CE_DELAY/PRE_DELAY/POST_DELAY represents each of these settings.

2 T = tCK(GPMI clock period) –0.075 ns (half of maximum p-p jitter).

For DDR Source Synchronous mode, Figure 29 shows the timing diagram of NAND_DQS/NAND_DATAxx read valid window. The typical value of tDQSQ is 0.85 ns (max) and 1 ns (max) for tQHS at 200 MB/s. GPMI will sample NAND_DATA[7:0] at both rising and falling edge of an delayed NAND_DQS signal, which can be provided by an internal DPLL. The delay value can be controlled by GPMI register GPMI_READ_DDR_DLL_CTRL.SLV_DLY_TARGET (see the GPMI chapter of the *i.MX 8M Nano Applications Processor Reference Manual* [IMX8MNRM]). Generally, the typical delay value of this register is equal to 0x7 which means 1/4 clock cycle delay expected. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

3.9.4.3 ONFI NV-DDR2 mode (ONFI 3.2 compatible)

3.9.4.3.1 Command and address timing

ONFI 3.2 mode command and address timing is the same as ONFI 1.0 compatible Async mode AC timing. See Section 3.9.4.1, Asynchronous mode AC timing (ONFI 1.0 compatible), for details.

3.9.4.3.2 Read and write timing

ONFI 3.2 mode read and write timing is the same as Toggle mode AC timing. See Section 3.9.4.4, Toggle mode AC Timing, for details.

3.9.4.4 Toggle mode AC Timing

3.9.4.4.1 Command and address timing

NOTE

Toggle mode command and address timing is the same as ONFI 1.0 compatible Asynchronous mode AC timing. See Section 3.9.4.1, Asynchronous mode AC timing (ONFI 1.0 compatible), for details.

3.9.4.4.2 Read and write timing

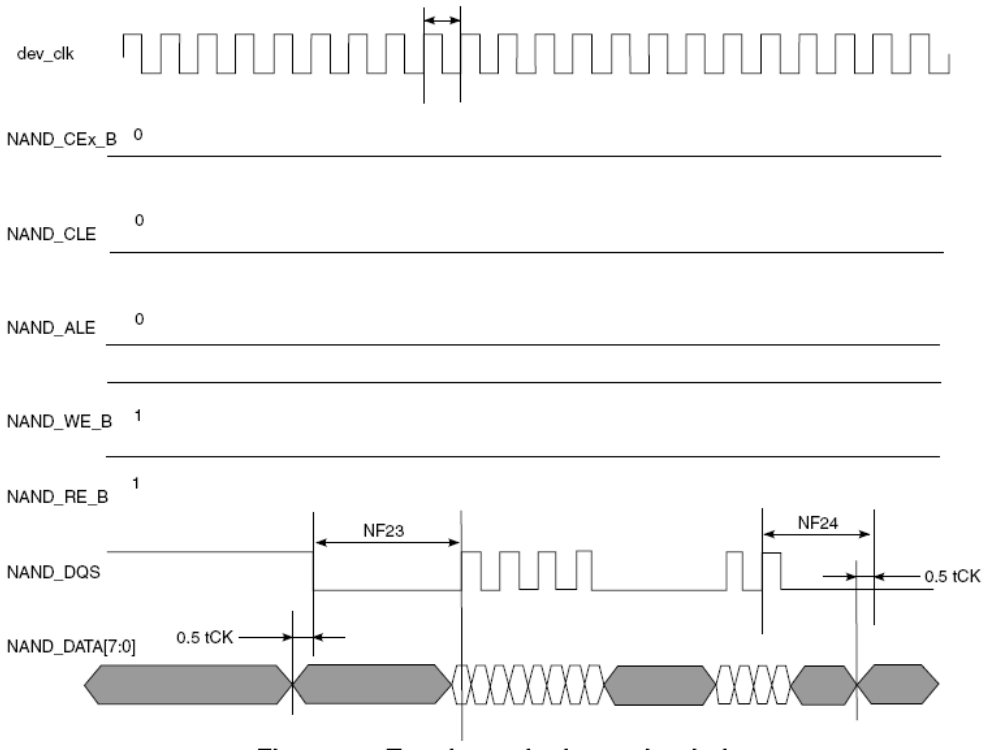


Figure 30. Toggle mode data write timing

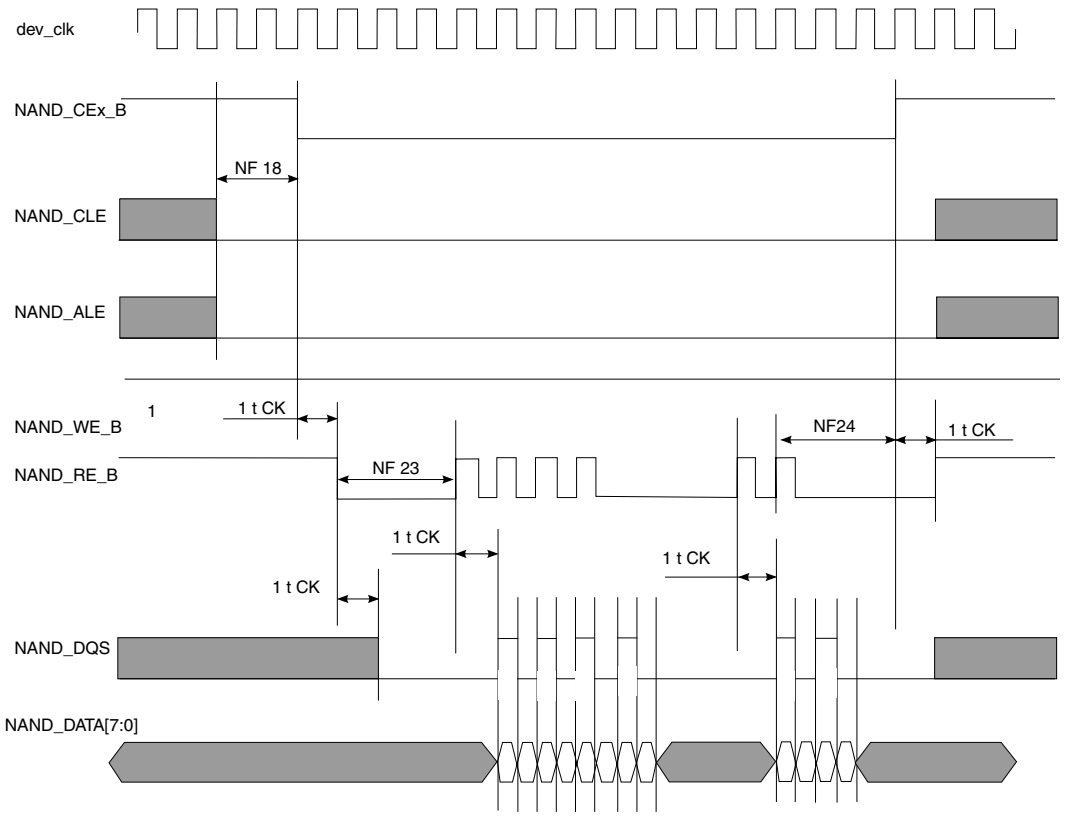


Figure 31. Toggle mode data read timing

Table 41. Toggle mode timing parameters

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF1	NAND_CLE setup time	tCLS	(AS + DS) × T - 0.12 [see note[1]s,[2]]		
NF2	NAND_CLE hold time	tCLH	DH × T - 0.72 [see note[2]]		
NF3	NAND_CE0_B setup time	tCS	(AS + DS) × T - 0.58 [see notes,[2]]		
NF4	NAND_CE0_B hold time	tCH	DH × T - 1 [see note[2]]		
NF5	NAND_WE_B pulse width	tWP	DS × T [see note[2]]		
NF6	NAND_ALE setup time	tALS	(AS + DS) × T - 0.49 [see notes,[2]]		
NF7	NAND_ALE hold time	tALH	DH × T - 0.42 [see note[2]]		
NF8	Command/address NAND_DATAxx setup time	tCAS	DS × T - 0.26 [see note[2]]		
NF9	Command/address NAND_DATAxx hold time	tCAH	DH × T - 1.37 [see note[2]]		
NF18	NAND_CEx_B access time	tCE	CE_DELAY × T [see notes[3,2]]	—	ns
NF22	clock period	tCK	—	—	ns
NF23	preamble delay	tPRE	PRE_DELAY × T [see notes[4,2]]	—	ns

Table 41. Toggle mode timing parameters (continued)

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF24	postamble delay	tPOST	POST_DELAY × T + 0.43 [see note[2]]	—	ns
NF28	Data write setup	tDS[5]	0.25 × tCK - 0.32	—	ns
NF29	Data write hold	tDH[5]	0.25 × tCK - 0.79	—	ns
NF30	NAND_DQS/NAND_DQ read setup skew	tDQSQ[6]	—	3.18	ns
NF31	NAND_DQS/NAND_DQ read hold skew	tQHS[6]	—	3.27	ns

1 AS minimum value can be 0, while DS/DH minimum value is 1.

2 T = tCK (GPMI clock period) - 0.075 ns (half of maximum p-p jitter).

3 CE_DELAY represents HW_GPMI_TIMING2[CE_DELAY]. NF18 is guaranteed by the design. Read/Write operation is started with enough time of ALE/CLE assertion to low level.

4 PRE_DELAY + 1 ≥ (AS + DS)

5 Shown in Figure 30.

6 Shown in Figure 31.

For DDR Toggle mode, Figure 29 shows the timing diagram of NAND_DQS/NAND_DATAxx read valid window. The typical value of tDQSQ is 1.4 ns (max) and 1.4 ns (max) for tQHS at 133 MB/s. GPMI samples NAND_DATA[7:0] at both the rising and falling edges of a delayed NAND_DQS signal, which is provided by an internal DPLL. The delay value of this register can be controlled by the GPMI register GPMI_READ_DDR_DLL_CTRL.SLV_DLY_TARGET (see the GPMI chapter of the *i.MX 8M Nano Applications Processor Reference Manual* [IMX8MNRM]). Generally, the typical delay value is equal to 0x7, which means a 1/4 clock cycle delay is expected. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

3.9.5 I²C bus characteristics

The Inter-Integrated Circuit (I2C) provides functionality of a standard I2C master and slave. The I2C is designed to be compatible with the I2C Bus Specification, version 2.1, by Philips Semiconductor (now NXP Semiconductors).

3.9.6 MIPI D-PHY timing parameters

MIPI D-PHY electrical specifications are compliance.

Table 42. MIPI PHY worst power dissipation[1]

MODE		Power consume on VDD_MIPI_0P8 (mW)	Power consume on VDD_MIPI_1P2 (mW)	Power consume on VDD_MIPI_1P8 (mW)	Total power consume (mW)
2.1 Gbps	M4 on S4 on	226.1	4.1	35.6	265.8
	M4 on S4 off	164.7	4.03	28.6	197.33
	M4 off S4 on	63.02	0	15.8	78.82
ULPS		4.26	0.0367	0.0584	4.36

1 M4 indicates MIPI DSI have 4 data lane enable (at least 1 clock lane enable). S4 indicates MIPI CSI have 4 data lane enable (at least 1 clock lane enable).

3.9.7 PDM timing parameters

Figure 32 illustrates the input timing of the PDM.

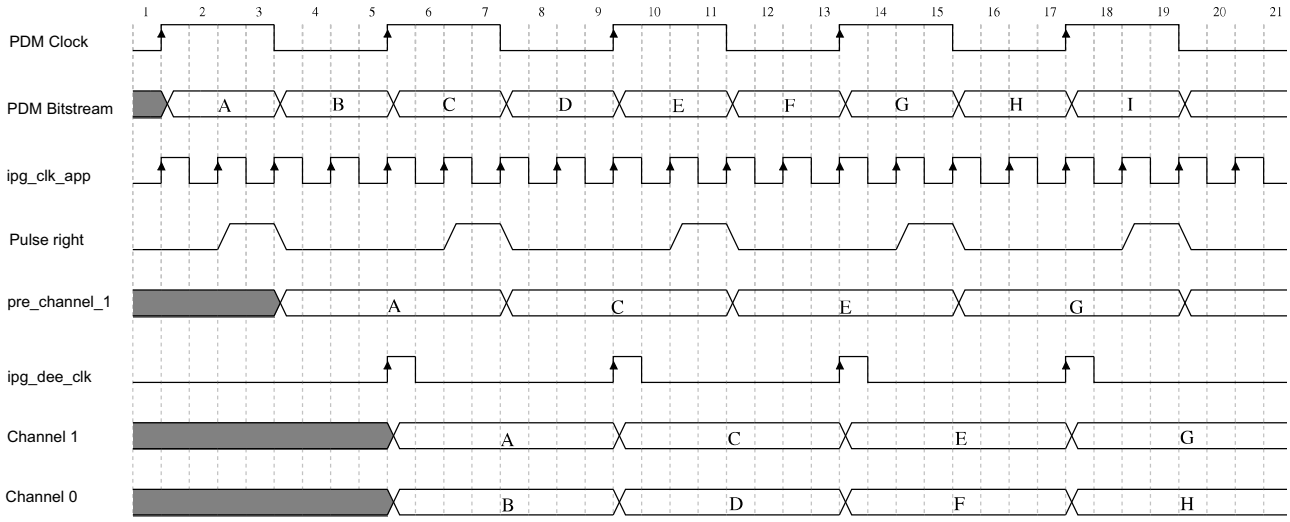


Figure 32. PDM input timing

PDM clock operative range is from 500 kHz to 6 MHz. Within range, only need to configure ipg_clk_app rate and CLKDIV without I/O timing concerns.

3.9.8 Pulse width modulator (PWM) timing parameters

This section describes the electrical information of the PWM. The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before

being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin.

Figure 33 depicts the timing of the PWM, and Table 43 lists the PWM timing parameters.

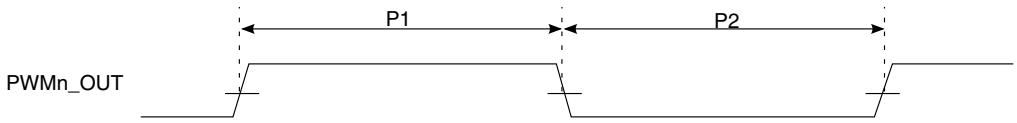


Figure 33. PWM timing

Table 43. PWM output timing parameters

ID	Parameter	Min	Max	Unit
	PWM Module Clock Frequency	0	66 (ipg_clk)	MHz
P1	PWM output pulse width high	12	—	ns
P2	PWM output pulse width low	12	—	ns

3.9.9 FlexSPI timing parameters

Measurements are with a load of 15 pF and an input slew rate of 1 V/ns.

3.9.9.1 FlexSPI input/read timing

There are three sources for the internal sample clock for FlexSPI read data:

- Dummy read strobe generated by FlexSPI controller and looped back internally (FlexSPI*n*_MCR0[RXCLKSRC] = 0x0)
- Dummy read strobe generated by FlexSPI controller and looped back through the DQS pad (FlexSPI*n*_MCR0[RXCLKSRC] = 0x1)
- Read strobe provided by memory device and input from DQS pad (FlexSPI*n*_MCR0[RXCLKSRC] = 0x3)

The following sections describe input signal timing for each of these four internal sample clock sources.

3.9.9.1.1 SDR mode with FlexSPI*n*_MCR0[RXCLKSRC] = 0x0, 0x1, 0x2

Table 44. FlexSPI input timing in SDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x0

Symbol	Parameter	Min.	Max.	Unit	Notes
—	[D:] Frequency of operation	—	66	MHz	—
F1	[D:] Setup time for incoming data	8.67	—	ns	[1]
F2	[D:] Hold time for incoming data	0	—	ns	—

[1] The setup specification here assumes the data learning feature is not used. If data learning is enabled, then TIS can be decreased by up to 2ns.

Table 45. FlexSPI input timing in SDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x1, 0x2

Symbol	Parameter	Min.	Max.	Unit	Notes
—	[D:] Frequency of operation	—	133	MHz	—
F1	[D:] Setup time for incoming data	1.5	—	ns	[1]
F2	[D:] Hold time for incoming data	1	—	ns	—

[1] The setup specification here assumes the data learning feature is not used. If data learning is enabled, then TIS can be decreased by up to 2ns.

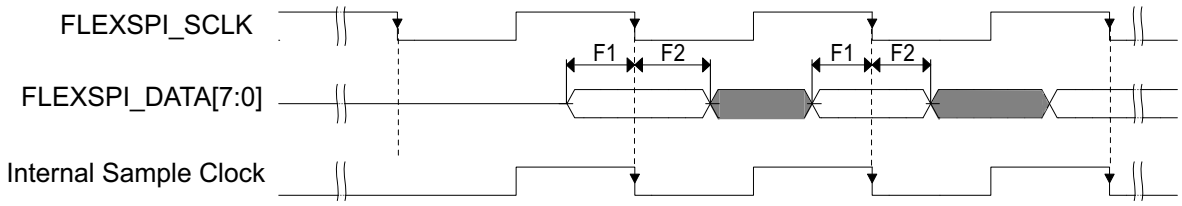


Figure 34. FlexSPI input timing in SDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x0, 0x1, 0x2

NOTE

Timing shown is based on the memory generating read data on the SCK falling edge, and FlexSPI controller sampling read data on the falling edge.

3.9.9.1.2 SDR mode with FlexSPI*n*_MCR0[RXCLKSRC] = 0x3

There are two cases when the memory provides both read data and the read strobe in SDR mode:

- A1—Memory generates both read data and read strobe on SCK rising edge (or falling edge)
- A2—Memory generates read data on SCK falling edge and generates read strobe on SCK rising edge

Table 46. FlexSPI input timing in SDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x3 (Case A1)

Symbol	Parameter	Min.	Max.	Unit
—	[D:] Frequency of operation	—	166	MHz
F3	[D:] Time from SCK to data valid	—	—	ns
F4	[D:] Time from SCK to DQS	—	—	ns
—	[D:] Time delta between TSCKD and TSCKDQS	-2	2	ns

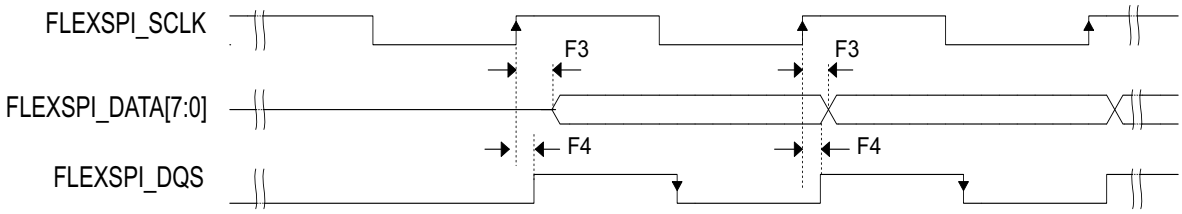


Figure 35. FlexSPI input timing in SDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x3 (Case A1)

NOTE

Timing shown is based on the memory generating read data and read strobe on the SCK rising edge. The FlexSPI controller samples read data on the DQS falling edge.

Table 47. FlexSPI input timing in SDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x3 (Case A2)

Symbol	Parameter	Min.	Max.	Unit
—	[D:] Frequency of operation	—	166	MHz
F5	[D:] Time from SCK to data valid	—	—	ns
F6	[D:] Time from SCK to DQS	—	—	ns
—	[D:] Time delta between TSCKD and TSCKDQS	-2	2	ns

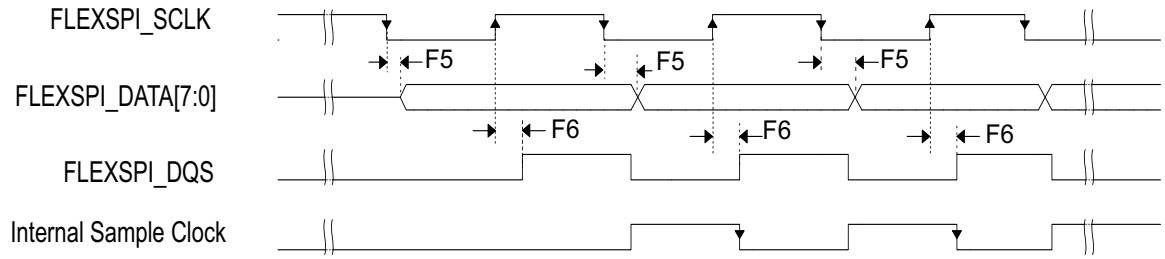


Figure 36. FlexSPI input timing in SDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x3 (Case A2)

NOTE

Timing shown is based on the memory generating read data on the SCK falling edge and read strobe on the SCK rising edge. The FlexSPI controller samples read data on a half-cycle delayed DQS falling edge.

3.9.9.1.3 DDR mode with FlexSPI*n*_MCR0[RXCLKSRC] = 0x0, 0x1, 0x2

Table 48. FlexSPI input timing in DDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x0

Symbol	Parameter	Min.	Max.	Unit	Notes
—	[D:] Frequency of operation	—	33	MHz	—
F1	[D:] Setup time for incoming data	8.67	—	ns	[1]
F2	[D:] Hold time for incoming data	0	—	ns	—

[1] The setup specification here assumes the data learning feature is not used. If data learning is enabled, then TIS can be decreased by up to 2ns.

Table 49. FlexSPI input timing in DDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x1, 0x2

Symbol	Parameter	Min.	Max.	Unit	Notes
—	[D:] Frequency of operation	—	66	MHz	—
F1	[D:] Setup time for incoming data	1.5	—	ns	[1]
F2	[D:] Hold time for incoming data	1	—	ns	—

[1] The setup specification here assumes the data learning feature is not used. If data learning is enabled, then TIS can be decreased by up to 2ns.

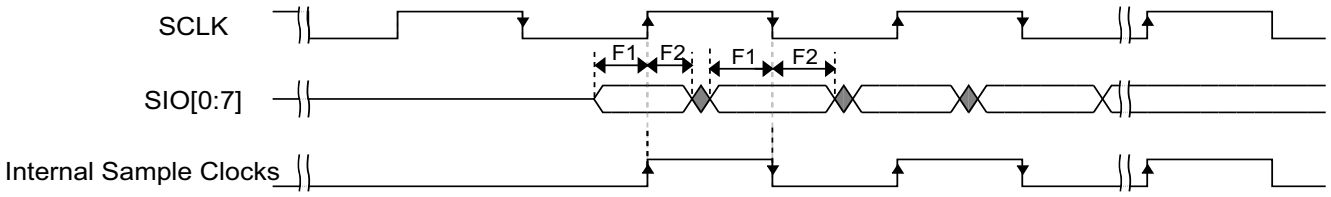


Figure 37. FlexSPI input timing in DDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x0, 0x1, 0x2

3.9.9.1.4 DDR mode with FlexSPI*n*_MCR0[RXCLKSRC] = 0x3

Table 50. FlexSPI input timing in DDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x3 (Case 1)

Symbol	Parameter	Min.	Max.	Unit
—	[D:] Frequency of operation	—	166	MHz
T_{SCKD}	[D:] Time from SCK to data valid	—	—	ns
T_{SCKDQS}	[D:] Time from SCK to DQS	—	—	ns
$T_{SCKD} - T_{SCKDQS}$	[D:] Time delta between TSCKD and TSCKDQS	-0.6	0.6	ns

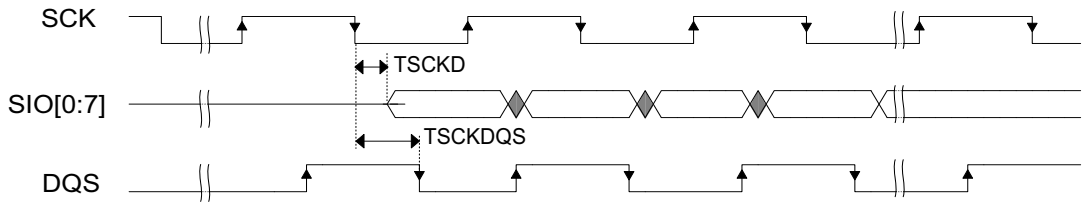


Figure 38. FlexSPI input timing in DDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x3

3.9.9.2 FlexSPI output/write timing

The following sections describe output signal timing for the FlexSPI controller including control signals and data outputs.

3.9.9.2.1 SDR mode

Table 51. FlexSPI output timing in SDR mode

Symbol	Parameter	Min.	Max.	Unit
—	[D:] Frequency of operation[1]	—	166	MHz
T_{CK}	[D:] SCK clock period	6.02	—	ns
T_{DSO}	[D:] Output data setup time	2	—	ns
T_{DHO}	[D:] Output data hold time	2	—	ns
T_{CSS}	[D:] Chip select output setup time	3 x T_{CK} - 1	—	ns
T_{CSH}	[D:] Chip select output hold time	3 x T_{CK} - 1	—	ns

1 The actual maximum frequency supported is limited by the FlexSPI*n*_MCR0[RXCLKSRC] configuration used. See the FlexSPI SDR input timing specifications.

NOTE

T_{CSS} and T_{CSH} are configured by the FlexSPI*n*_FLSHAxCR1 register, the default values are shown above. See the *i.MX 8M Nano Applications Processor Reference Manual* (IMX8MNRM) for more details.

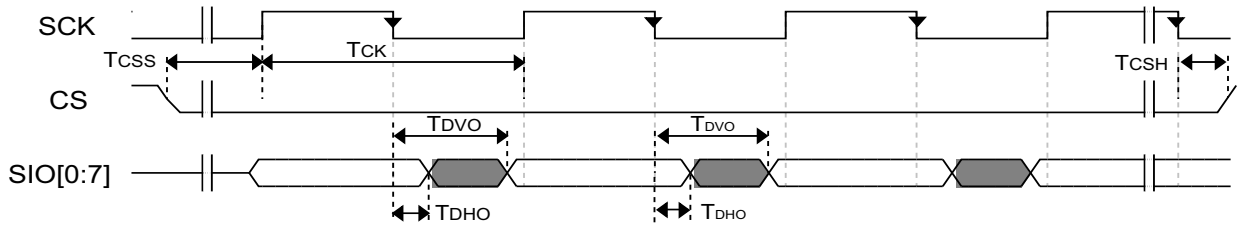


Figure 39. FlexSPI output timing in SDR mode

3.9.9.2.2 DDR mode

Table 52. FlexSPI output timing in DDR mode

Symbol	Parameter	Min.	Max.	Unit
—	[D:] Frequency of operation[1]	—	166	MHz
T_{CK}	[D:] SCK clock period	6.02	—	ns
T_{DSO}	[D:] Output data setup time	—	0.6	ns
T_{DHO}	[D:] Output data hold time	0.6	—	ns
T_{CSS}	[D:] Chip select output setup time	3 x T_{CK} - 1.075	—	ns
T_{CSH}	[D:] Chip select output hold time	3 x T_{CK} - 1.075	—	ns

[1] The actual maximum frequency supported is limited by the FlexSPI*n*_MCR0[RXCLKSRC] configuration used. See the FlexSPI SDR input timing specifications.

NOTE

T_{CSS} and T_{CSH} are configured by the FlexSPI*n*_FLSHAxCR1 register, the default values are shown above. See the *i.MX 8M Nano Applications Processor Reference Manual* (IMX8MNRM) for more details.

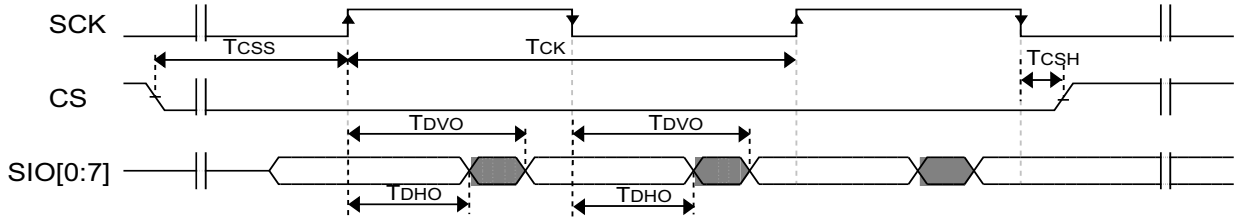


Figure 40. FlexSPI output timing in DDR mode

3.9.10 SAI/I2S switching specifications

This section provides the AC timings for the SAI in Master (clocks driven) and Slave (clocks input) modes. All timings are given for non inverted serial clock polarity (SAI_TCR[TSCKP] = 0, SAI_RCR[RSCKP] = 0) and non inverted frame sync (SAI_TCR[TFSI] = 0, SAI_RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (SAI_BCLK) and/or the frame sync (SAI_FS) shown in the figures below.

Table 53. Master mode SAI timing (50 MHz)[1]

Num	Characteristic	Min	Max	Unit
S1	SAI_MCLK cycle time	20	—	ns
S2	SAI_MCLK pulse width high/low	40%	60%	MCLK period
S3	SAI_BCLK cycle time	20	—	ns

Table 53. Master mode SAI timing (50 MHz)[1] (continued)

Num	Characteristic	Min	Max	Unit
S4	SAI_BCLK pulse width high/low	40%	60%	BCLK period
S5	SAI_BCLK to SAI_FS output valid	—	2	ns
S6	SAI_BCLK to SAI_FS output invalid	0	—	ns
S7	SAI_BCLK to SAI_TXD valid	—	2	ns
S8	SAI_BCLK to SAI_TXD invalid	0	—	ns
S9	SAI_RXD/SAI_FS input setup before SAI_BCLK	2	—	ns
S10	SAI_RXD/SAI_FS input hold after SAI_BCLK	0	—	ns

[1] To achieve 50 MHz for BCLK operation, clock must be set in feedback mode.

Table 54. Master mode SAI timing (25 MHz)

Num	Characteristic	Min	Max	Unit
S1	SAI_MCLK cycle time	40	—	ns
S2	SAI_MCLK pulse width high/low	40%	60%	MCLK period
S3	SAI_BCLK cycle time	40	—	ns
S4	SAI_BCLK pulse width high/low	40%	60%	BCLK period
S5	SAI_BCLK to SAI_FS output valid	—	2	ns
S6	SAI_BCLK to SAI_FS output invalid	0	—	ns
S7	SAI_BCLK to SAI_TXD valid	—	2	ns
S8	SAI_BCLK to SAI_TXD invalid	0	—	ns
S9	SAI_RXD/SAI_FS input setup before SAI_BCLK	12	—	ns
S10	SAI_RXD/SAI_FS input hold after SAI_BCLK	0	—	ns

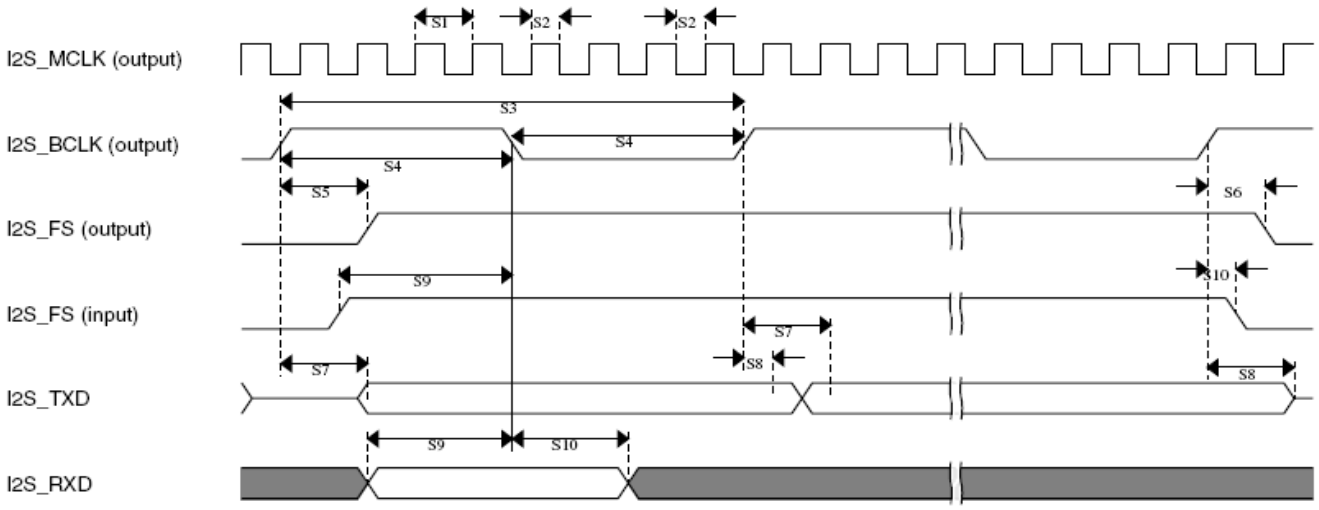


Figure 41. SAI timing—Master modes

Table 55. Slave mode SAI timing (50 MHz)[1]

Num	Characteristic	Min	Max	Unit
S11	SAI_BCLK cycle time (input)	20	—	ns
S12	SAI_BCLK pulse width high/low (input)	40%	60%	BCLK period
S13	SAI_FS input setup before SAI_BCLK	2	—	ns
S14	SAI_FA input hold after SAI_BCLK	2	—	ns
S17	SAI_RXD setup before SAI_BCLK	2	—	ns
S18	SAI_RXD hold after SAI_BCLK	2	—	ns

1 TX does not support 50 MHz operation in Slave mode.

Table 56. Slave mode SAI timing (25 MHz)

Num	Characteristic	Min	Max	Unit
S11	SAI_BCLK cycle time (input)	40	—	ns
S12	SAI_BCLK pulse width high/low (input)	40%	60%	BCLK period
S13	SAI_FS input setup before SAI_BCLK	12	—	ns
S14	SAI_FA input hold after SAI_BCLK	2	—	ns
S15	SAI_BCLK to SAI_TXD/SAI_FS output valid	—	7	ns
S16	SAI_BCLK to SAI_TXD/SAI_FS output invalid	0	—	ns
S17	SAI_RXD setup before SAI_BCLK	12	—	ns
S18	SAI_RXD hold after SAI_BCLK	2	—	ns

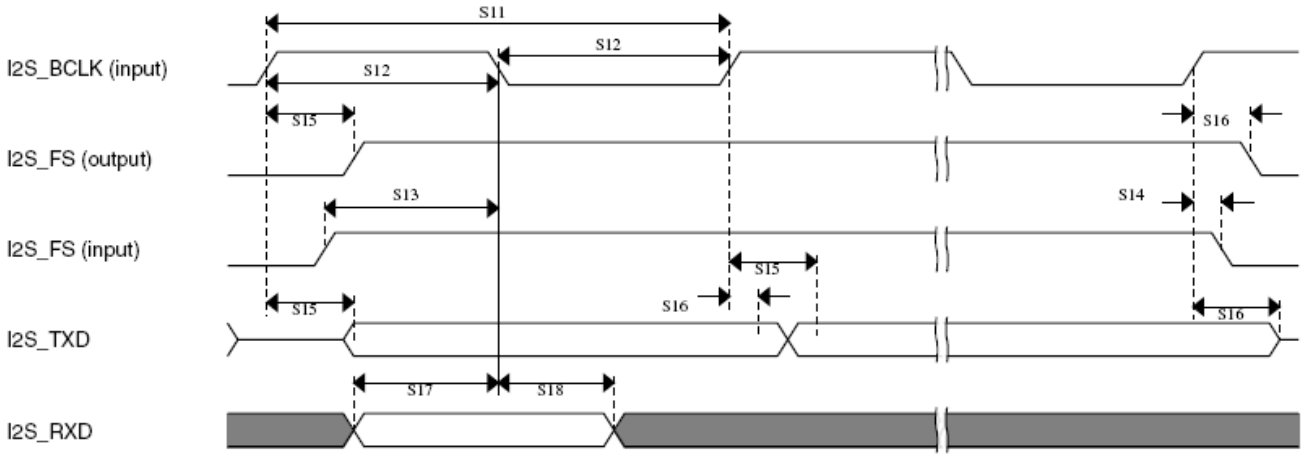


Figure 42. SAI Timing — Slave Modes

3.9.11 SPDIF timing parameters

The Sony/Philips Digital Interconnect Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

Table 57 and Figure 43 and Figure 44 show SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SPDIF_SR_CLK) for SPDIF in Rx mode and the timing of the modulating Tx clock (SPDIF_ST_CLK) for SPDIF in Tx mode.

Table 57. SPDIF timing parameters

Parameter	Symbol	Timing Parameter Range		Unit
		Min	Max	
SPDIF_IN Skew: asynchronous inputs, no specs apply	—	—	0.7	ns
SPDIF_OUT output (Load = 50 pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 24.2 31.3	ns
SPDIF_OUT output (Load = 30 pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	1.5 13.6 18.0	ns
Modulating Rx clock (SPDIF_SR_CLK) period	srckp	40.0	—	ns
SPDIF_SR_CLK high period	srckph	16.0	—	ns
SPDIF_SR_CLK low period	srckpl	16.0	—	ns
Modulating Tx clock (SPDIF_ST_CLK) period	stclkp	40.0	—	ns
SPDIF_ST_CLK high period	stclkph	16.0	—	ns
SPDIF_ST_CLK low period	stclkpl	16.0	—	ns

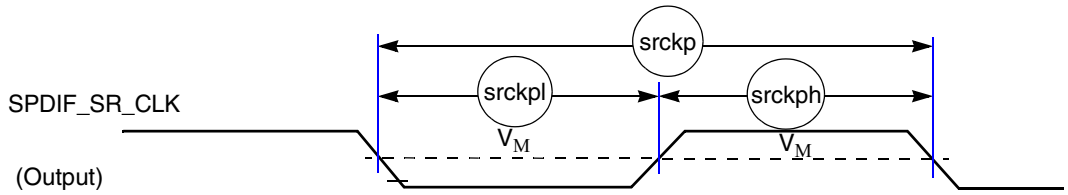


Figure 43. SPDIF_SR_CLK timing diagram

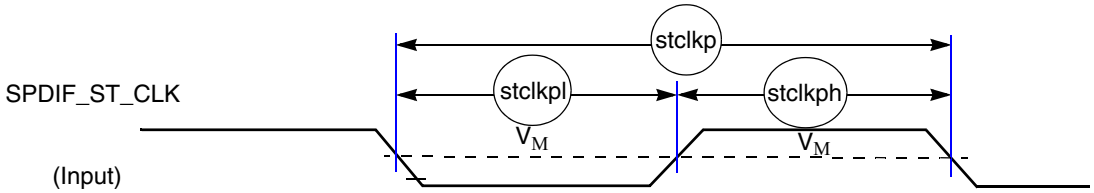


Figure 44. SPDIF_ST_CLK timing diagram

3.9.12 UART I/O configuration and timing parameters

3.9.12.1 UART RS-232 I/O configuration in different modes

The i.MX 8M Nano UART interfaces can serve both as DTE or DCE device. This can be configured by the DCEDTE control bit (default 0—DCE mode). Table 58 shows the UART I/O configuration based on the enabled mode.

Table 58. UART I/O configuration vs. mode

Port	DTE Mode		DCE Mode	
	Direction	Description	Direction	Description
UARTx_RTS_B	Output	UARTx_RTS_B from DTE to DCE	Input	UARTx_RTS_B from DTE to DCE
UARTx_CTS_B	Input	UARTx_CTS_B from DCE to DTE	Output	UARTx_CTS_B from DCE to DTE
UARTx_TX_DATA	Input	Serial data from DCE to DTE	Output	Serial data from DCE to DTE
UARTx_RX_DATA	Output	Serial data from DTE to DCE	Input	Serial data from DTE to DCE

3.9.12.2 UART RS-232 Serial mode timing

This section describes the electrical information of the UART module in the RS-232 mode.

3.9.12.2.1 UART transmitter

Figure 45 depicts the transmit timing of UART in the RS-232 Serial mode, with 8 data bit/1 stop bit format. Table 59 lists the UART RS-232 Serial mode transmit timing characteristics.

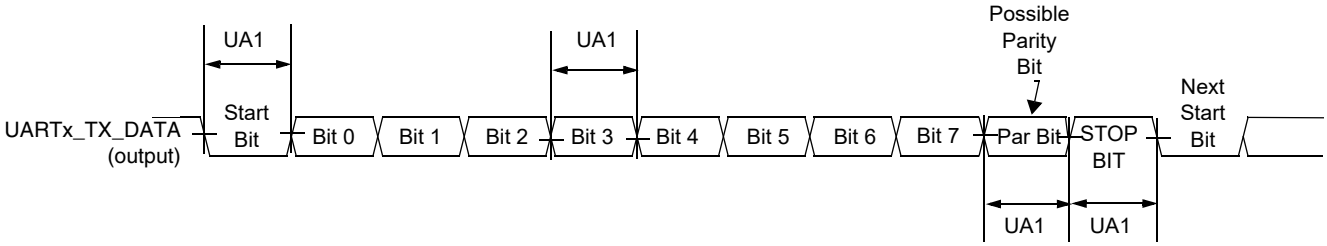


Figure 45. UART RS-232 Serial mode transmit timing diagram

Table 59. RS-232 Serial mode transmit timing parameters

ID	Parameter	Symbol	Min	Max	Unit
UA1	Transmit Bit Time	t_{Tbit}	$1/F_{baud\_rate}$[1] - T_{ref_clk}[2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—

[1] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

[2] T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

3.9.12.2.2 UART receiver

Figure 46 depicts the RS-232 Serial mode receive timing with 8 data bit/1 stop bit format. Table 60 lists Serial mode receive timing characteristics.

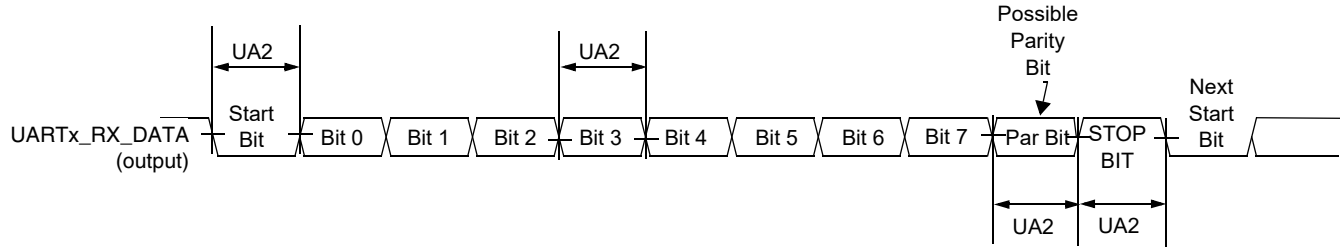


Figure 46. UART RS-232 Serial mode receive timing diagram

Table 60. RS-232 Serial mode receive timing parameters

ID	Parameter	Symbol	Min	Max	Unit
UA2	Receive Bit Time[1]	t_{Rbit}	$1/F_{baud\_rate}$[2] - 1/(16 x F_{baud_rate})	$1/F_{baud\_rate}$ + 1/(16 x F_{baud_rate})	—

[1] The UART receiver can tolerate 1/(16 x F_{baud_rate}) tolerance in each bit. But accumulation tolerance in one frame must not exceed 3/(16 x F_{baud_rate}).

[2] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

3.9.13 USB PHY parameters

This section describes the USB-OTG PHY parameters.

3.9.13.1 Pad/Package/Board connections

The USB1_VBUS pin cannot directly connect to the 5 V VBUS voltage on the USB2.0 link.

The USB1_VBUS pin must be isolated by an external 30 KΩ 1% precision resistor.

The USB 2.0 PHY uses USB1_TXRTUNE and an external resistor to calibrate the USB1_DP/DN 45 Ω source impedance. The external resistor value is 200 Ω 1% precision on USB1_TXRTUNE pad to ground.

3.9.13.2 USB PHY worst power consumption

Table 61 shows the USB 2.0 PHY worst power dissipation.

Table 61. USB 2.0 PHY worst power dissipation

Mode	VDD_USB_0P8		VDD_USB_3P3		VDD_USB_1P8		Total Power	
HS TX	8.286	mA	4.63	mA	23.409	mA	70.448	mW
FS TX	6.767		12.52		5.968		63.22	
LS TX	7.001		13.58		6.224		67.779	
Suspend	0.752		0.164		0.106		1.465	
Sleep	0.761		0.163		0.106		1.472	

4 Boot mode configuration

This section provides information on Boot mode configuration pins allocation and boot devices interfaces allocation.

4.1 Boot mode configuration pins

Table 62 provides boot options, functionality, fuse values, and associated pins. Several input pins are also sampled at reset and can be used to override fuse values, depending on the value of BT_FUSE_SEL fuse. The boot option pins are in effect when BT_FUSE_SEL fuse is '0' (cleared, which is the case for an unblown fuse). For detailed Boot mode options configured by the Boot mode pins, see the "System Boot, Fusemap, and eFuse" chapter in the *i.MX 8M Nano Applications Processor Reference Manual* (IMX8MNRM).

Table 62. Fuses and associated pins used for boot

Interface	IP instance	Allocated pads during boot	Comment
BOOT_MODE0	Input	ccmsrcgpcmix.BOOT_MODE[0]	Boot mode selection
BOOT_MODE1	Input	ccmsrcgpcmix.BOOT_MODE[1]	
BOOT_MODE2	Input	ccmsrcgpcmix.BOOT_MODE[2]	
BOOT_MODE3	Input	ccmsrcgpcmix.BOOT_MODE[3]	

4.2 Boot device interface allocation

Table 63 lists the interfaces that can be used by the boot process in accordance with the specific Boot mode configuration. The table also describes the interface's specific modes and IOMUXC allocation, which are configured during boot when appropriate.

Table 63. Interface allocation during boot

Interface	IP Instance	Allocated Pads During Boot	Comment
SPI	ECSPI-1	ECSPI1_SCLK, ECSPI1_MOSI, ECSPI1_MISO, ECSPI1_SS0	The chip-select pin used depends on the fuse "CS select (SPI only)".
SPI	ECSPI-2	ECSPI2_SCLK, ECSPI2_MOSI, ECSPI2_MISO, ECSPI2_SS0	The chip-select pin used depends on the fuse "CS select (SPI only)".
SPI	ECSPI-3	UART1_RXD, UART1_TXD, UART2_RXD, UART2_TXD	The chip-select pin used depends on the fuse "CS select (SPI only)".
NAND Flash	GPMI	NAND_ALE, NAND_CE0_B, NAND_CLE, NAND_DATA00,NAND_DATA01,NAND_DATA02, NAND_DATA03,NAND_DATA04,NAND_DATA05, NAND_DATA06, NAND_DATA07, NAND_DQS, NAND_RE_B, NAND_READY_B, NAND_WE_B, NAND_WP_B	8-bit, only CS0 is supported.

Table 63. Interface allocation during boot (continued)

Interface	IP Instance	Allocated Pads During Boot	Comment
SD/MMC	USDHC-1	GPIO1_IO03, GPIO1_IO06, GPIO1_IO07, SD1_RESET_B, SD1_CLK, SD1_CMD, SD1_STROBE, SD1_DATA0, SD1_DATA1, SD1_DATA2, SD1_DATA3, SD1_DATA4, SD1_DATA5, SD1_DATA6, SD1_DATA7	1, 4, or 8-bit
SD/MMC	USDHC-2	GPIO1_IO04, GPIO1_IO08, GPIO1_IO07, SD2_RESET_B, SD2_WP, SD2_CLK, SD2_CMD, SD2_DATA0, SD2_DATA1, SD2_DATA2, SD2_DATA3	1 or 4-bit
SD/MMC	USDHC-3	NAND_CE1_B, NAND_CE2_B, NAND_CE3_B, NAND_CLE, NAND_DATA02, NAND_DATA03, NAND_DATA04,NAND_DATA05,NAND_DATA06, NAND_DATA07,NAND_RE_B,NAND_READY_B, NAND_WE_B, NAND_WP_B	1, 4, or 8-bit
FlexSPI	FlexSPI	NAND_ALE, NAND_CE0_B, NAND_CE1_B, NAND_CE2_B, NAND_CE3_B, NAND_CLE, NAND_DATA00,NAND_DATA01,NAND_DATA02, NAND_DATA03,NAND_DATA04,NAND_DATA05, NAND_DATA06, NAND_DATA07, NAND_DQS, NAND_RE_B	For FlexSPI flash
USB	USB_OTG PHY	Dedicated USB pins	—

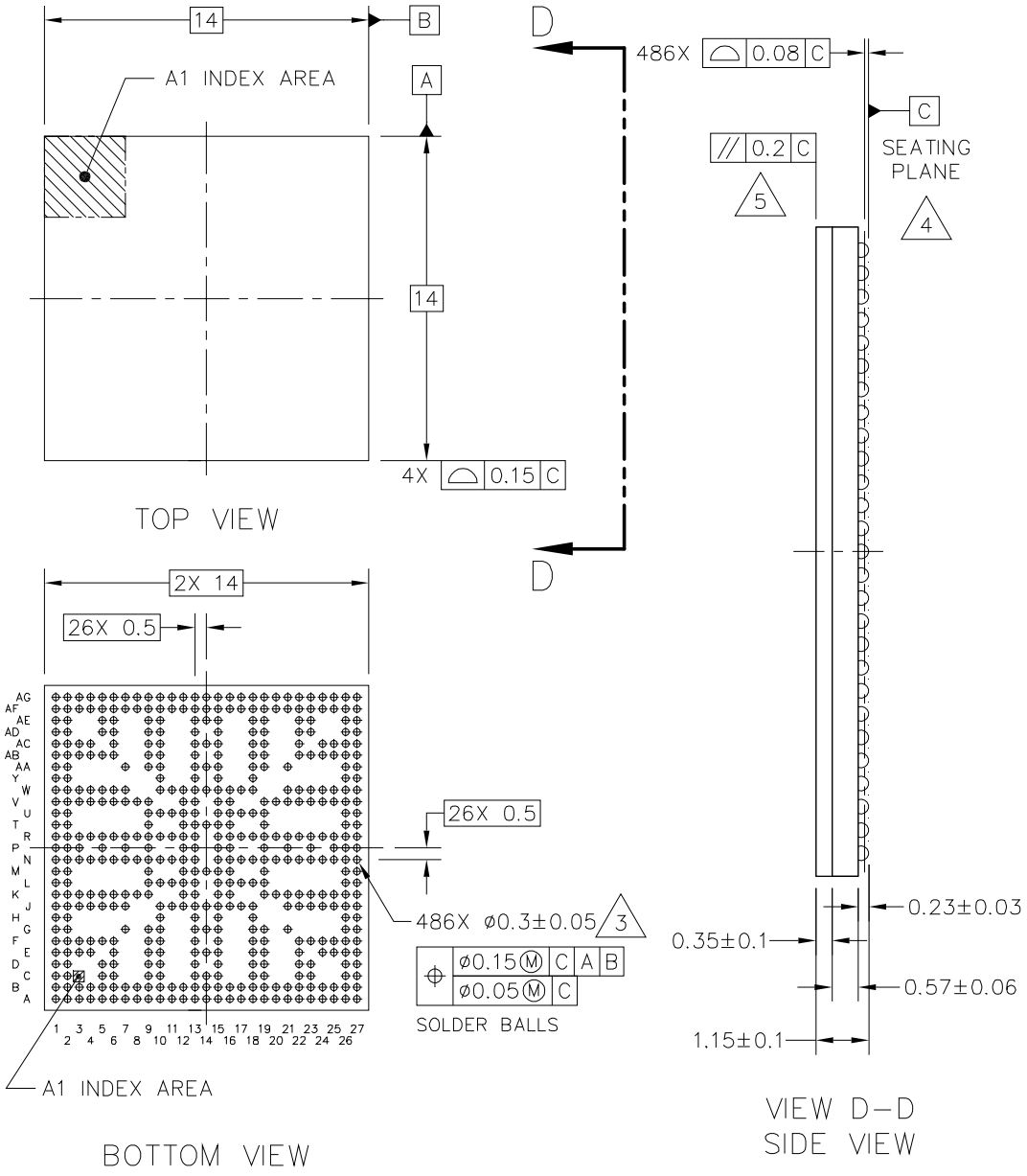
5 Package information and contact assignments

This section includes the contact assignment information and mechanical package drawing.

5.1 14 x 14 mm package information

5.1.1 14 x 14 mm, 0.5 mm pitch, ball matrix

Figure 47 shows the top, bottom, and side views of the 14 × 14 mm FCBGA package.



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TITLE: FCPBGA, MOLDED ARRAY, 14 X 14 X 1.15 PKG, 0.5 MM PITCH, 486 I/O	DOCUMENT NO: 98ASA01200D	REV: B
	STANDARD: NON–JEDEC	
	SOT1967–1	02 AUG 2018

Figure 47. 14 X 14 MM BGA, case x package top, bottom, and side views

5.1.2 14 x 14 mm supplies contact assignments and functional contact assignments

Table 64 shows supplies contact assignments for the 14 x 14 mm package.

Table 64. i.MX 8M Nano 14 x 14 mm supplies contact assignments

Supply Rail Name	Ball(s) Position(s)	Remark
NVCC_CLK	M19	Supply for CLK interface
NVCC_DRAM	P7, K8, N8, R8, V8, K9, L9, M9, N9, R9, T9, U9, V9	Supply for DRAM interface
NVCC_ECSPI	H10	Supply for ESCPI interface
NVCC_ENET	W22	Supply for ENET interface
NVCC_GPIO1	W12	Supply for GPIO1 interface
NVCC_I2C	J11	Supply for I2C interface
NVCC_JTAG	L19	Supply for JTAG interface
NVCC_NAND	U19	Supply for NAND interface
NVCC_SAI2	V19	Supply for SAI interface
NVCC_SAI3	Y10	Supply for SAI interface
NVCC_SAI5	W17	Supply for SAI interface
NVCC_SD1	V20	Supply for SD interface
NVCC_SD2	V22	Supply for SD interface
NVCC_SNVS_1P8	J22	Supply for SNVS interface
NVCC_UART	J12	Supply for UART interface
PVCC0_1P8	AB13	Digital IO pre-drive
PVCC1_1P8	T19	Digital IO pre-drive
PVCC2_1P8	J13	Digital IO pre-drive
VDD_24M_XTAL_1P8	N19	Supply for XTAL
VDD_ANA_0P8	L17, N17	Supply for Analog logic
VDD_ANA0_1P8	AA14, Y15	Supply for Analog logic
VDD_ANA1_1P8	P19, N20	Supply for Analog logic
VDD_ARM	R13, T13, U13, V13, W13, T14, W14, R15, T15, U15, V15, W15, V16, W16	Supply for ARM
VDD_ARM_PLL_0P8	P16	Supply for ARM PLL
VDD_ARM_PLL_1P8	R19	Supply for ARM PLL
VDD_DRAM	J10, L10, N10, R10, U10, W10	Supply for DRAM module
VDD_DRAM_PLL_0P8	P9	Supply for DRAM PLL
VDD_DRAM_PLL_1P8	P5	Supply for DRAM PLL

Table 64. i.MX 8M Nano 14 x 14 mm supplies contact assignments (continued)

VDD_GPU	R11, U11, W11, P12, V12	Supply for GPU
VDD_MIPI_0P8	J14	Supply for MIPI PHY
VDD_MIPI_1P2	J15	Supply for MIPI PHY
VDD_MIPI_1P8	H13	Supply for MIPI PHY
VDD_SNVS_0P8	K22	Supply for SNVS logic
VDD_SOC	N13, K15, L15, M15, N15, K16, R17, U17, L18, N18, R18, U18	Supply for SOC logic
VDD_USB_0P8	J17	Supply for USB PHY
VDD_USB_1P8	H15	Supply for USB PHY
VDD_USB_3P3	K19	Supply for USB PHY
VSS	A1, AG1, C2, H2, Y2, AE2, B3, E3, F3, J3, K3, N3, P3, R3, V3, W3, AB3, AC3, AF3, C5, AE5, C6, AE6, G7, J7, K7, N7, R7, V7, W7, AA7, C9, G9, AA9, AE9, C10, G10, AA10, AE10, L12, M12, N12, R12, T12, U12, C13, G13, P13, Y13, AA13, AE13, C14, AE14, C15, G15, P15, AA15, AE15, L16, M16, N16, R16, T16, U16, C18, G18, H18, Y18, AA18, AE18, C19, G19, AA19, AE19, K20, R20, G21, J21, K21, N21, P21, R21, V21, W21, AA21, C22, AE22, C23, AE23, E25, F25, J25, K25, N25, P25, R25, V25, W25, AB25, AC25, B26, A27, AG27	—

Table 65 shows an alpha-sorted list of functional contact assignments for the 14 x 14 mm package.

Table 65. i.MX 8M Nano 14 x 14 mm functional contact assignments

Ball name	Ball	Power group	Ball type	Reset condition		
				Default mode	Default function	Input/ Output status
24M_XTALI	B27	NVCC_CLK	ANALOG	—	—	Input
24M_XTALO	C26	NVCC_CLK	ANALOG	—	—	Output
BOOT_MODE0	G26	NVCC_JTAG	GPIO	ALT0	ccmsrcgpcmix.BOOT_MODE[0]	Input with PD
BOOT_MODE1	G27	NVCC_JTAG	GPIO	ALT0	ccmsrcgpcmix.BOOT_MODE[1]	Input with PD
BOOT_MODE2	C27	NVCC_JTAG	GPIO	ALT0	ccmsrcgpcmix.BOOT_MODE[2]	Input with PD
BOOT_MODE3	D26	NVCC_JTAG	GPIO	ALT0	ccmsrcgpcmix.BOOT_MODE[3]	Input with PD
CLKIN1	H27	NVCC_CLK	GPIO	—	—	Input without PU/PD
CLKIN2	J27	NVCC_CLK	GPIO	—	—	Input without PU/PD
CLKOUT1	H26	NVCC_CLK	GPIO	—	—	Output low without PU/PD

Table 65. i.MX 8M Nano 14 x 14 mm functional contact assignments (continued)

Ball name	Ball	Power group	Ball type	Reset condition		
				Default mode	Default function	Input/ Output status
CLKOUT2	J26	NVCC_CLK	GPIO	—	—	Output low without PU/PD
DRAM_AC00	F4	NVCC_DRAM	DDR	—	—	Output low
DRAM_AC01	F5	NVCC_DRAM	DDR	—	—	Output low
DRAM_AC02	K4	NVCC_DRAM	DDR	—	—	Input
DRAM_AC03	J4	NVCC_DRAM	DDR	—	—	Input
DRAM_AC04	L2	NVCC_DRAM	DDR	—	—	Input
DRAM_AC05	L1	NVCC_DRAM	DDR	—	—	Input
DRAM_AC06	F6	NVCC_DRAM	DDR	—	—	Input
DRAM_AC07	J5	NVCC_DRAM	DDR	—	—	Input
DRAM_AC08	J6	NVCC_DRAM	DDR	—	—	Input
DRAM_AC09	K6	NVCC_DRAM	DDR	—	—	Input
DRAM_AC10	E4	NVCC_DRAM	DDR	—	—	Input
DRAM_AC11	D5	NVCC_DRAM	DDR	—	—	Input
DRAM_AC12	N4	NVCC_DRAM	DDR	—	—	Input
DRAM_AC13	N5	NVCC_DRAM	DDR	—	—	Input
DRAM_AC14	K5	NVCC_DRAM	DDR	—	—	Input
DRAM_AC15	N6	NVCC_DRAM	DDR	—	—	Input
DRAM_AC16	M1	NVCC_DRAM	DDR	—	—	Input
DRAM_AC17	M2	NVCC_DRAM	DDR	—	—	Input
DRAM_AC19	N2	NVCC_DRAM	DDR	—	—	Input
DRAM_AC20	AB4	NVCC_DRAM	DDR	—	—	Output low
DRAM_AC21	AB5	NVCC_DRAM	DDR	—	—	Output low
DRAM_AC22	W4	NVCC_DRAM	DDR	—	—	Input
DRAM_AC23	V4	NVCC_DRAM	DDR	—	—	Input
DRAM_AC24	U2	NVCC_DRAM	DDR	—	—	Input
DRAM_AC25	U1	NVCC_DRAM	DDR	—	—	Input
DRAM_AC26	N1	NVCC_DRAM	DDR	—	—	Input
DRAM_AC27	R6	NVCC_DRAM	DDR	—	—	Input
DRAM_AC28	W6	NVCC_DRAM	DDR	—	—	Input

Table 65. i.MX 8M Nano 14 x 14 mm functional contact assignments (continued)

Ball name	Ball	Power group	Ball type	Reset condition		
				Default mode	Default function	Input/ Output status
DRAM_AC29	V6	NVCC_DRAM	DDR	—	—	Input
DRAM_AC30	AC4	NVCC_DRAM	DDR	—	—	Input
DRAM_AC31	AD5	NVCC_DRAM	DDR	—	—	Input
DRAM_AC32	R4	NVCC_DRAM	DDR	—	—	Input
DRAM_AC33	R5	NVCC_DRAM	DDR	—	—	Input
DRAM_AC34	T1	NVCC_DRAM	DDR	—	—	Input
DRAM_AC35	T2	NVCC_DRAM	DDR	—	—	Input
DRAM_AC36	V5	NVCC_DRAM	DDR	—	—	Input
DRAM_AC37	W5	NVCC_DRAM	DDR	—	—	Input
DRAM_AC38	AB6	NVCC_DRAM	DDR	—	—	Input
DRAM_ALERT_N	R2	NVCC_DRAM	DDR	—	—	Input
DRAM_DM0	A4	NVCC_DRAM	DDR	—	—	Input
DRAM_DM1	F1	NVCC_DRAM	DDR	—	—	Input
DRAM_DQ00	A5	NVCC_DRAM	DDR	—	—	Input
DRAM_DQ01	B5	NVCC_DRAM	DDR	—	—	Input
DRAM_DQ02	D2	NVCC_DRAM	DDR	—	—	Input
DRAM_DQ03	D1	NVCC_DRAM	DDR	—	—	Input
DRAM_DQ04	C1	NVCC_DRAM	DDR	—	—	Input
DRAM_DQ05	B1	NVCC_DRAM	DDR	—	—	Input
DRAM_DQ06	A3	NVCC_DRAM	DDR	—	—	Input
DRAM_DQ07	B4	NVCC_DRAM	DDR	—	—	Input
DRAM_DQ08	F2	NVCC_DRAM	DDR	—	—	Input
DRAM_DQ09	G2	NVCC_DRAM	DDR	—	—	Input
DRAM_DQ10	J1	NVCC_DRAM	DDR	—	—	Input
DRAM_DQ11	J2	NVCC_DRAM	DDR	—	—	Input
DRAM_DQ12	K2	NVCC_DRAM	DDR	—	—	Input
DRAM_DQ13	K1	NVCC_DRAM	DDR	—	—	Input
DRAM_DQ14	E1	NVCC_DRAM	DDR	—	—	Input
DRAM_DQ15	E2	NVCC_DRAM	DDR	—	—	Input
DRAM_DQS0_N	B2	NVCC_DRAM	—	—	—	Input

Table 65. i.MX 8M Nano 14 x 14 mm functional contact assignments (continued)

Ball name	Ball	Power group	Ball type	Reset condition		
				Default mode	Default function	Input/ Output status
DRAM_DQS0_P	A2	NVCC_DRAM	DDRCLK	—	—	Input
DRAM_DQS1_N	H1	NVCC_DRAM	—	—	—	Input
DRAM_DQS1_P	G1	NVCC_DRAM	DDRCLK	—	—	Input
DRAM_RESET_N	R1	NVCC_DRAM	DDR	—	—	Output low
DRAM_VREF	P1	NVCC_DRAM	DDR	—	—	—
DRAM_ZN	P2	NVCC_DRAM	DDR	—	—	—
ECSPI1_MISO	A7	NVCC_ECSPI	GPIO	ALT5	GPIO5.IO[8]	Input with PD
ECSPI1_MOSI	B7	NVCC_ECSPI	GPIO	ALT5	GPIO5.IO[7]	Input with PD
ECSPI1_SCLK	D6	NVCC_ECSPI	GPIO	ALT5	GPIO5.IO[6]	Input with PD
ECSPI1_SS0	B6	NVCC_ECSPI	GPIO	ALT5	GPIO5.IO[9]	Input with PD
ECSPI2_MISO	A8	NVCC_ECSPI	GPIO	ALT5	GPIO5.IO[12]	Input with PD
ECSPI2_MOSI	B8	NVCC_ECSPI	GPIO	ALT5	GPIO5.IO[11]	Input with PD
ECSPI2_SCLK	E6	NVCC_ECSPI	GPIO	ALT5	GPIO5.IO[10]	Input with PD
ECSPI2_SS0	A6	NVCC_ECSPI	GPIO	ALT5	GPIO5.IO[13]	Input with PD
ENET_MDC	AC27	NVCC_ENET	GPIO	ALT5	GPIO1.IO[16]	Input with PD
ENET_MDIO	AB27	NVCC_ENET	GPIO	ALT5	GPIO1.IO[17]	Input with PD
ENET_RD0	AE27	NVCC_ENET	GPIO	ALT5	GPIO1.IO[26]	Input with PD
ENET_RD1	AD27	NVCC_ENET	GPIO	ALT5	GPIO1.IO[27]	Input with PD
ENET_RD2	AD26	NVCC_ENET	GPIO	ALT5	GPIO1.IO[28]	Input with PD
ENET_RD3	AC26	NVCC_ENET	GPIO	ALT5	GPIO1.IO[29]	Input with PD
ENET_RXC	AE26	NVCC_ENET	GPIO	ALT5	GPIO1.IO[25]	Input with PD
ENET_RX_CTL	AF27	NVCC_ENET	GPIO	ALT5	GPIO1.IO[24]	Input with PD
ENET_TD0	AG26	NVCC_ENET	GPIO	ALT5	GPIO1.IO[21]	Input with PD
ENET_TD1	AF26	NVCC_ENET	GPIO	ALT5	GPIO1.IO[20]	Input with PD
ENET_TD2	AG25	NVCC_ENET	GPIO	ALT5	GPIO1.IO[19]	Input with PD
ENET_TD3	AF25	NVCC_ENET	GPIO	ALT5	GPIO1.IO[18]	Input with PD
ENET_TXC	AG24	NVCC_ENET	GPIO	ALT5	GPIO1.IO[23]	Input with PD
ENET_TX_CTL	AF24	NVCC_ENET	GPIO	ALT5	GPIO1.IO[22]	Input with PD
GPIO1_IO00	AG14	NVCC_GPIO1	GPIO	ALT6	GPIO1.IO[0]	Input with PD
GPIO1_IO01	AF14	NVCC_GPIO1	GPIO	ALT6	GPIO1.IO[1]	[1]

Table 65. i.MX 8M Nano 14 x 14 mm functional contact assignments (continued)

Ball name	Ball	Power group	Ball type	Reset condition		
				Default mode	Default function	Input/ Output status
GPIO1_IO02	AG13	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[2]	Input with PU
GPIO1_IO03	AF13	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[3]	Input with PD
GPIO1_IO04	AG12	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[4]	Input with PD
GPIO1_IO05	AF12	NVCC_GPIO1	GPIO	ALT6	GPIO1.IO[5]	[1]
GPIO1_IO06	AG11	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[6]	Input with PD
GPIO1_IO07	AF11	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[7]	Input with PU
GPIO1_IO08	AG10	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[8]	Input with PD
GPIO1_IO09	AF10	NVCC_GPIO1	GPIO	ALT1	GPIO1.IO[9]	Input with PD
GPIO1_IO10	AD10	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[10]	Input with PD
GPIO1_IO11	AC10	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[11]	Input with PD
GPIO1_IO12	AB10	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[12]	Input with PD
GPIO1_IO13	AD9	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[13]	Input with PD
GPIO1_IO14	AC9	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[14]	Input with PD
GPIO1_IO15	AB9	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[15]	Input with PD
I2C1_SCL	E9	NVCC_I2C	GPIO	ALT5	GPIO5.IO[14]	Input with PD
I2C1_SDA	F9	NVCC_I2C	GPIO	ALT5	GPIO5.IO[15]	Input with PD
I2C2_SCL	D10	NVCC_I2C	GPIO	ALT5	GPIO5.IO[16]	Input with PD
I2C2_SDA	D9	NVCC_I2C	GPIO	ALT5	GPIO5.IO[17]	Input with PD
I2C3_SCL	E10	NVCC_I2C	GPIO	ALT5	GPIO5.IO[18]	Input with PD
I2C3_SDA	F10	NVCC_I2C	GPIO	ALT5	GPIO5.IO[19]	Input with PD
I2C4_SCL	D13	NVCC_I2C	GPIO	ALT5	GPIO5.IO[20]	Input with PD
I2C4_SDA	E13	NVCC_I2C	GPIO	ALT5	GPIO5.IO[21]	Input with PD
JTAG_MOD	D27	NVCC_JTAG	GPIO	ALT0	cjtag_wrapper.MOD	Input with PD
JTAG_TCK	F26	NVCC_JTAG	GPIO	ALT0	cjtag_wrapper.TCK	Input with PU
JTAG_TDI	E27	NVCC_JTAG	GPIO	ALT0	cjtag_wrapper.TDI	Input with PU
JTAG_TDO	E26	NVCC_JTAG	GPIO	ALT0	cjtag_wrapper.TDO	Input with PU
JTAG_TMS[2]	F27	NVCC_JTAG	GPIO	ALT0	cjtag_wrapper.TMS	Input with PU
MIPI_CSI_CLK_N	A16	VDD_MIPI_1P8	PHY	—	—	Input
MIPI_CSI_CLK_P	B16	VDD_MIPI_1P8	PHY	—	—	Input
MIPI_CSI_D0_N	A14	VDD_MIPI_1P8	PHY	—	—	Input

Table 65. i.MX 8M Nano 14 x 14 mm functional contact assignments (continued)

Ball name	Ball	Power group	Ball type	Reset condition		
				Default mode	Default function	Input/ Output status
MIPI_CSI_D0_P	B14	VDD_MIPI_1P8	PHY	—	—	Input
MIPI_CSI_D1_N	A15	VDD_MIPI_1P8	PHY	—	—	Input
MIPI_CSI_D1_P	B15	VDD_MIPI_1P8	PHY	—	—	Input
MIPI_CSI_D2_N	A17	VDD_MIPI_1P8	PHY	—	—	Input
MIPI_CSI_D2_P	B17	VDD_MIPI_1P8	PHY	—	—	Input
MIPI_CSI_D3_N	A18	VDD_MIPI_1P8	PHY	—	—	Input
MIPI_CSI_D3_P	B18	VDD_MIPI_1P8	PHY	—	—	Input
MIPI_DSI_CLK_N	A11	VDD_MIPI_1P8	PHY	—	—	Output low
MIPI_DSI_CLK_P	B11	VDD_MIPI_1P8	PHY	—	—	Output low
MIPI_DSI_D0_N	A9	VDD_MIPI_1P8	PHY	—	—	Output low
MIPI_DSI_D0_P	B9	VDD_MIPI_1P8	PHY	—	—	Output low
MIPI_DSI_D1_N	A10	VDD_MIPI_1P8	PHY	—	—	Output low
MIPI_DSI_D1_P	B10	VDD_MIPI_1P8	PHY	—	—	Output low
MIPI_DSI_D2_N	A12	VDD_MIPI_1P8	PHY	—	—	Output low
MIPI_DSI_D2_P	B12	VDD_MIPI_1P8	PHY	—	—	Output low
MIPI_DSI_D3_N	A13	VDD_MIPI_1P8	PHY	—	—	Output low
MIPI_DSI_D3_P	B13	VDD_MIPI_1P8	PHY	—	—	Output low
MIPI_VREG_CAP	D15	0.35 - 0.45 V	PHY	—	—	Output
NAND_ALE	N22	NVCC_NAND	GPIO	ALT5	GPIO3.IO[0]	Input with PD
NAND_CE0_B	N24	NVCC_NAND	GPIO	ALT5	GPIO3.IO[1]	Input with PU
NAND_CE1_B	P27	NVCC_NAND	GPIO	ALT5	GPIO3.IO[2]	Input with PD
NAND_CE2_B	M27	NVCC_NAND	GPIO	ALT5	GPIO3.IO[3]	Input with PD
NAND_CE3_B	L27	NVCC_NAND	GPIO	ALT5	GPIO3.IO[4]	Input with PD
NAND_CLE	K27	NVCC_NAND	GPIO	ALT5	GPIO3.IO[5]	Input with PD
NAND_DATA00	P23	NVCC_NAND	GPIO	ALT5	GPIO3.IO[6]	Input with PD
NAND_DATA01	K24	NVCC_NAND	GPIO	ALT5	GPIO3.IO[7]	Input with PD
NAND_DATA02	K23	NVCC_NAND	GPIO	ALT5	GPIO3.IO[8]	Input with PD
NAND_DATA03	N23	NVCC_NAND	GPIO	ALT5	GPIO3.IO[9]	Input with PD
NAND_DATA04	M26	NVCC_NAND	GPIO	ALT5	GPIO3.IO[10]	Input with PD
NAND_DATA05	L26	NVCC_NAND	GPIO	ALT5	GPIO3.IO[11]	Input with PD

Table 65. i.MX 8M Nano 14 x 14 mm functional contact assignments (continued)

Ball name	Ball	Power group	Ball type	Reset condition		
				Default mode	Default function	Input/ Output status
NAND_DATA06	K26	NVCC_NAND	GPIO	ALT5	GPIO3.IO[12]	Input with PD
NAND_DATA07	N26	NVCC_NAND	GPIO	ALT5	GPIO3.IO[13]	Input with PD
NAND_DQS	R22	NVCC_NAND	GPIO	ALT5	GPIO3.IO[14]	Input with PD
NAND_RE_B	N27	NVCC_NAND	GPIO	ALT5	GPIO3.IO[15]	Input with PU
NAND_READY_B	P26	NVCC_NAND	GPIO	ALT5	GPIO3.IO[16]	Input with PD
NAND_WE_B	R26	NVCC_NAND	GPIO	ALT5	GPIO3.IO[17]	Input with PD
NAND_WP_B	R27	NVCC_NAND	GPIO	ALT5	GPIO3.IO[18]	Input with PD
ONOFF	A25	NVCC_SNVS_1P8	GPIO	ALT0	snvsmix.ONOFF	Input without PU/PD
PMIC_ON_REQ	A24	NVCC_SNVS_1P8	GPIO	ALT0	snvsmix.PMIC_ON_REQ	Open-drain output high with PU
PMIC_STBY_REQ	E24	NVCC_SNVS_1P8	GPIO	ALT0	ccmsrcgpcmix.PMIC_STBY_REQ	Output low with PD
POR_B	B24	NVCC_SNVS_1P8	GPIO	ALT0	snvsmix.POR_B	Input without PU/PD
RTC_XTALI	A26	NVCC_SNVS_1P8	ANALOG	ALT0	snvsmix.RTC	Input
RTC_XTALO	B25	NVCC_SNVS_1P8	ANALOG	—	—	Output, inverted of RTC_XTALI
RTC_RESET_B	F24	NVCC_SNVS_1P8	GPIO	ALT0	snvsmix.RTC_POR_B	Input without PU/PD
SAI2_MCLK	AD19	NVCC_SAI2	GPIO	ALT5	GPIO4.IO[27]	Input with PD
SAI2_RXC	AB22	NVCC_SAI2	GPIO	ALT5	GPIO4.IO[22]	Input with PD
SAI2_RXD0	AC24	NVCC_SAI2	GPIO	ALT5	GPIO4.IO[23]	Input with PD
SAI2_RXFS	AC19	NVCC_SAI2	GPIO	ALT5	GPIO4.IO[21]	Input with PD
SAI2_TXC	AD22	NVCC_SAI2	GPIO	ALT5	GPIO4.IO[25]	Input with PD
SAI2_TXD0	AC22	NVCC_SAI2	GPIO	ALT5	GPIO4.IO[26]	Input with PD
SAI2_TXFS	AD23	NVCC_SAI2	GPIO	ALT5	GPIO4.IO[24]	Input with PD
SAI3_MCLK	AD6	NVCC_SAI3	GPIO	ALT5	GPIO5.IO[2]	Input with PD
SAI3_RXC	AG7	NVCC_SAI3	GPIO	ALT5	GPIO4.IO[29]	Input with PD
SAI3_RXD	AF7	NVCC_SAI3	GPIO	ALT5	GPIO4.IO[30]	Input with PD
SAI3_RXFS	AG8	NVCC_SAI3	GPIO	ALT5	GPIO4.IO[28]	Input with PD

Table 65. i.MX 8M Nano 14 x 14 mm functional contact assignments (continued)

Ball name	Ball	Power group	Ball type	Reset condition		
				Default mode	Default function	Input/ Output status
SAI3_TXC	AG6	NVCC_SAI3	GPIO	ALT5	GPIO5.IO[0]	Input with PD
SAI3_TXD	AF6	NVCC_SAI3	GPIO	ALT5	GPIO5.IO[1]	Input with PD
SAI3_TXFS	AC6	NVCC_SAI3	GPIO	ALT5	GPIO4.IO[31]	Input with PD
SAI5_MCLK	AD15	NVCC_SAI5	GPIO	ALT5	GPIO3.IO[25]	3
SAI5_RXC	AC15	NVCC_SAI5	GPIO	ALT5	GPIO3.IO[20]	Input with PD
SAI5_RXD0	AD18	NVCC_SAI5	GPIO	ALT5	GPIO3.IO[21]	Input with PD
SAI5_RXD1	AC14	NVCC_SAI5	GPIO	ALT5	GPIO3.IO[22]	Input with PD
SAI5_RXD2	AD13	NVCC_SAI5	GPIO	ALT5	GPIO3.IO[23]	Input with PD
SAI5_RXD3	AC13	NVCC_SAI5	GPIO	ALT5	GPIO3.IO[24]	Input with PD
SAI5_RXFS	AB15	NVCC_SAI5	GPIO	ALT5	GPIO3.IO[19]	Input with PD
SD1_CLK	V26	NVCC_SD1	GPIO	ALT5	GPIO2.IO[0]	Input with PD
SD1_CMD	V27	NVCC_SD1	GPIO	ALT5	GPIO2.IO[1]	Input with PD
SD1_DATA0	Y27	NVCC_SD1	GPIO	ALT5	GPIO2.IO[2]	Input with PD
SD1_DATA1	Y26	NVCC_SD1	GPIO	ALT5	GPIO2.IO[3]	Input with PD
SD1_DATA2	T27	NVCC_SD1	GPIO	ALT5	GPIO2.IO[4]	Input with PD
SD1_DATA3	T26	NVCC_SD1	GPIO	ALT5	GPIO2.IO[5]	Input with PD
SD1_DATA4	U27	NVCC_SD1	GPIO	ALT5	GPIO2.IO[6]	Input with PD
SD1_DATA5	U26	NVCC_SD1	GPIO	ALT5	GPIO2.IO[7]	Input with PD
SD1_DATA6	W27	NVCC_SD1	GPIO	ALT5	GPIO2.IO[8]	Input with PD
SD1_DATA7	W26	NVCC_SD1	GPIO	ALT5	GPIO2.IO[9]	Input with PD
SD1_RESET_B	R23	NVCC_SD1	GPIO	ALT5	GPIO2.IO[10]	Input with PD
SD1_STROBE	R24	NVCC_SD1	GPIO	ALT5	GPIO2.IO[11]	Input with PD
SD2_CD_B	AA26	NVCC_SD2	GPIO	ALT5	GPIO2.IO[12]	Input with PD
SD2_CLK	W23	NVCC_SD2	GPIO	ALT5	GPIO2.IO[13]	Input with PD
SD2_CMD	W24	NVCC_SD2	GPIO	ALT5	GPIO2.IO[14]	Input with PD
SD2_DATA0	AB23	NVCC_SD2	GPIO	ALT5	GPIO2.IO[15]	Input with PD
SD2_DATA1	AB24	NVCC_SD2	GPIO	ALT5	GPIO2.IO[16]	Input with PD
SD2_DATA2	V24	NVCC_SD2	GPIO	ALT5	GPIO2.IO[17]	Input with PD
SD2_DATA3	V23	NVCC_SD2	GPIO	ALT5	GPIO2.IO[18]	Input with PD
SD2_RESET_B	AB26	NVCC_SD2	GPIO	ALT5	GPIO2.IO[19]	Input with PD

Table 65. i.MX 8M Nano 14 x 14 mm functional contact assignments (continued)

Ball name	Ball	Power group	Ball type	Reset condition		
				Default mode	Default function	Input/ Output status
SD2_WP	AA27	NVCC_SD2	GPIO	ALT5	GPIO2.IO[20]	Input with PD
SPDIF_EXT_CLK	AF8	NVCC_SAI3	GPIO	ALT5	GPIO5.IO[5]	Input with PD
SPDIF_RX	AG9	NVCC_SAI3	GPIO	ALT5	GPIO5.IO[4]	Input with PD
SPDIF_TX	AF9	NVCC_SAI3	GPIO	ALT5	GPIO5.IO[3]	Input with PD
TSENSOR_TEST_OUT	J23	VDD_ANA1_1P8	ANALOG	—	—	Output low
TSENSOR_REST_EXT	J24	VDD_ANA1_1P8	ANALOG	—	—	—
UART1_RXD	E14	NVCC_UART	GPIO	ALT5	GPIO5.IO[22]	Input with PD
UART1_TXD	F13	NVCC_UART	GPIO	ALT5	GPIO5.IO[23]	Input with PD
UART2_RXD	F15	NVCC_UART	GPIO	ALT5	GPIO5.IO[24]	Input with PD
UART2_TXD	E15	NVCC_UART	GPIO	ALT5	GPIO5.IO[25]	Input with PD
UART3_RXD	E18	NVCC_UART	GPIO	ALT5	GPIO5.IO[26]	Input with PD
UART3_TXD	D18	NVCC_UART	GPIO	ALT5	GPIO5.IO[27]	Input with PD
UART4_RXD	F19	NVCC_UART	GPIO	ALT5	GPIO5.IO[28]	Input with PD
UART4_TXD	F18	NVCC_UART	GPIO	ALT5	GPIO5.IO[29]	Input with PD
USB1_DN	A22	VDD_USB_3P3	PHY	—	—	Input
USB1_DP	B22	VDD_USB_3P3	PHY	—	—	Input
USB1_ID	D22	VDD_USB_1P8	PHY	—	—	Input
USB1_TXRTUNE	E19	VDD_USB_1P8	PHY	—	—	—
USB1_VBUS	F22	VDD_USB_3P3	PHY	—	—	—

1 During reset: output high without PU/PD; After reset: input with PU

2 Mandatory requirement: JTAG_TMS pin must be connected with a 50 ohm serial resistor near the component.

3 During reset: input without PU/PD; After reset: input with PD

5.1.3 i.MX 8M Nano 14 x 14 mm 0.5 mm pitch ball map

Table 66 shows the i.MX 8M Nano 14 x 14 mm 0.5 mm pitch ball map.

Table 66. 14 x 14 mm, 0.5 mm pitch ball map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27
A	VSS	DRAM_DQS0_P	DRAM_DQ06	DRAM_DM0	DRAM_DQ00	ECSPI2_SS0	ECSPI1_MISO	ECSPI2_MISO	MIPI_DSI_D0_N	MIPI_DSI_D1_N	MIPI_DSI_CLK_N	MIPI_DSI_D2_N	MIPI_DSI_D3_N	MIPI_CSI_D0_N	MIPI_CSI_D1_N	MIPI_CSI_CLK_N	MIPI_CSI_D2_N	MIPI_CSI_D3_N				USB1_DN		PMIC_ON_REQ	ONOFF	RTC_XTALI	VSS
B	DRAM_DQ05	DRAM_DQS0_N	VSS	DRAM_DQ07	DRAM_DQ01	ECSPI1_SS0	ECSPI1_MOSI	ECSPI2_MOSI	MIPI_DSI_D0_P	MIPI_DSI_D1_P	MIPI_DSI_CLK_P	MIPI_DSI_D2_P	MIPI_DSI_D3_P	MIPI_CSI_D0_P	MIPI_CSI_D1_P	MIPI_CSI_CLK_P	MIPI_CSI_D2_P	MIPI_CSI_D3_P				USB1_DP		POR_B	RTC_XTALO	VSS	24M_XTALI
C	DRAM_DQ04	VSS			VSS	VSS			VSS	VSS			VSS	VSS	VSS			VSS	VSS			VSS	VSS			24M_XTALO	BOOT_MODE2
D	DRAM_DQ03	DRAM_DQ02			DRAM_AC11	ECSPI1_SCLK			I2C2_SDA	I2C2_SCL			I2C4_SCL		MIPI_VREG_CAP			UART3_TXD				USB1_ID				BOOT_MODE3	JTAG_MOD
E	DRAM_DQ14	DRAM_DQ15	VSS	DRAM_AC10		ECSPI2_SCLK			I2C1_SCL	I2C3_SCL			I2C4_SDA	UART1_RXD	UART2_TXD			UART3_RXD	USB1_TXRTUNE					PMIC_STBY_REQ	VSS	JTAG_TDO	JTAG_TDI
F	DRAM_DM1	DRAM_DQ08	VSS	DRAM_AC00	DRAM_AC01	DRAM_AC06			I2C1_SDA	I2C3_SDA			UART1_TXD		UART2_RXD			UART4_TXD	UART4_RXD			USB1_VBUS		RTC_RESET_B	VSS	JTAG_TCK	JTAG_TMS
G	DRAM_DQS1_P	DRAM_DQ09					VSS		VSS	VSS			VSS		VSS			VSS	VSS		VSS					BOOT_MODE0	BOOT_MODE1

Table 66. 14 x 14 mm, 0.5 mm pitch ball map (continued)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27
H	DRAM_DQS1_N	VSS								NVCC_ESCPI			VDD_MIPI_1P8		VDD_USB_1P8			VSS								CLKOUT1	CLKIN1
J	DRAM_DQ10	DRAM_DQ11	VSS	DRAM_AC03	DRAM_AC07	DRAM_AC08	VSS			VDD_DRAM	NVCC_I2C	NVCC_UART	PVCC2_1P8	VDD_MIPI_0P8	VDD_MIPI_1P2		VDD_USB_0P8				VSS	NVCC_SNVS_1P8	TSENSOR_TEST_OUT	TESENSOR_RES_EXT	VSS	CLKOUT2	CLKIN2
K	DRAM_DQ13	DRAM_DQ12	VSS	DRAM_AC02	DRAM_AC14	DRAM_AC09	VSS	NVCC_DRAM	NVCC_DRAM						VDD_SOC	VDD_SOC			VDD_USB_3P3	VSS	VSS	VDD_SNVS_0P8	NAND_DATA02	NAND_DATA01	VSS	NAND_DATA06	NAND_CLE
L	DRAM_AC05	DRAM_AC04							NVCC_DRAM	VDD_DRAM		VSS			VDD_SOC	VSS	VDD_ANA_0P8	VDD_SOC	NVCC_JTAG							NAND_DATA05	NAND_CE3_B
M	DRAM_A165	DRAM_AC17							NVCC_DRAM			VSS			VDD_SOC	VSS			NVCC_CLK							NAND_DATA04	NAND_CE2_B
N	DRAM_AC26	DRAM_AC19	VSS	DRAM_AC12	DRAM_AC13	DRAM_AC15	VSS	NVCC_DRAM	NVCC_DRAM	VDD_DRAM		VSS	VDD_SOC		VDD_SOC	VSS	VDD_ANA_0P8	VDD_SOC	VDD_24M_XTAL_1P8	VDD_ANA1_1P8	VSS	NAND_ALE	NAND_DATA03	NAND_CE0_B	VSS	NAND_DATA07	NAND_RE_B
P	DRAM_VREF	DRAM_ZN	VSS		VDD_DRAM_PLL_1P8		NVCC_DRAM		VDD_DRAM_PLL_0P8			VDD_GPU	VSS		VSS	VDD_ARM_PLL_0P8			VDD_ANA1_1P8		VSS		NAND_DATA00		VSS	NAND_READY_B	NAND_CE1_B

Table 66. 14 x 14 mm, 0.5 mm pitch ball map (continued)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27
R	DRAM_RESET_N	DRAM_ALERT_N	VSS	DRAM_AC32	DRAM_AC33	DRAM_AC27	VSS	NVCC_DRAM	NVCC_DRAM	VDD_DRAM	VDD_GPU	VSS	VDD_ARM		VDD_ARM	VSS	VDD_SOC	VDD_SOC	VDD_ARM_PLL_1P8	VSS	VSS	NAND_DQS	SD1_RESET_B	SD1_STROBE	VSS	NAND_WE_B	NAND_WP_B
T	DRAM_AC34	DRAM_AC35							NVCC_DRAM			VSS	VDD_ARM	VDD_ARM	VDD-ARM	VSS			PVCC1_1P8							SD1_DATA3	SD1_DATA2
U	DRAM_AC25	DRAM_AC24							NVCC_DRAM	VDD_DRAM	VDD_GPU	VSS	VDD_ARM		VDD_ARM	VSS	VDD_SOC	VDD_SOC	NVCC_NAND							SD1_DATA5	SD1_DATA4
V			VSS	DRAM_AC23	DRAM_AC36	DRAM_AC29	VSS	NVCC_DRAM	NVCC_DRAM			VDD_GPU	VDD_ARM		VDD_ARM	VDD_ARM			NVCC_SAI2	NVCC_SD1	VSS	NVCC_SD2	SD2_DATA3	SD2_DATA2	VSS	SD1_CLK	SD1_CMD
W			VSS	DRAM_AC22	DRAM_AC37	DRAM_AC28	VSS			VDD_DRAM	VDD_GPU	NVCC_GPIO1	VDD_ARM	VDD_ARM	VDD_ARM	VDD_ARM	NVCC_SAI5					NVCC__ENET	SD2_CLK	SD2_CMD	VSS	SD1_DATA7	SD1_DATA6
Y		VSS								NVCC_SAI3			VSS	VDD_ANA0_1P8	VDD_ANA0_1P8			VSS								SD1_DATA1	SD1_DATA0
AA			VSS	DRAM_AC20	DRAM_AC21	DRAM_AC38	VSS		GPIO1_IO15	GPIO1_IO12			PVCC0_1P8	VDD_ANA0_1P8	SAI5_RXFS						VSS					SD2_RESET_B	ENET_MDIO
AB																						SAI2_RXC	SD2_DATA0	SD2_DATA1	VSS		

Table 66. 14 x 14 mm, 0.5 mm pitch ball map (continued)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27
AC			VSS	DRAM_AC30		SAI3_TXFS			GPIO1_IO14	GPIO1_IO11			SAI5_RXD3	SAI5_RXD1	SAI5_RXC				SAI2_RXFS			SAI2_TXD0		SAI2_RXD0	VSS	ENENT_RD3	ENET_MDC
AD					DRAM_AC31	SAI3_MCLK			GPIO1_IO13	GPIO1_IO10			SAI5_RXD2		SAI5_MCLK			SAI5_RXD0	SAI2_MCLK			SAI2_TXC	SAI2_TXFS			ENET_RD2	ENET_RD1
AE		VSS			VSS	VSS			VSS	VSS			VSS	VSS	VSS			VSS	VSS			VSS	VSS			ENET_RXC	ENET_RD0
AF			VSS			SAI3_TXD	SAI3_RXD	SPDIF_EXT_CLK	SPDIF_TX	GPIO1_IO09	GPIO1_IO07	GPIO1_IO05	GPIO1_IO03	GPIO1_IO01										ENET_TX_CTL	ENET_TD3	ENET_TD1	ENET_RX_CTL
AG	VSS					SAI3_TXC	SAI3_RXC	SAI3_RXFS	SPDIF_RX	GPIO1_IO08	GPIO1_IO06	GPIO1_IO04	GPIO1_IO02	GPIO1_IO00										ENET_TXC	ENET_TD2	ENET_TD0	VSS

5.2 DDR pin function list

Table 67 shows the DDR pin function list.

Table 67. DDR pin function list

Ball name	LPDDR4	DDR4	DDR3/3L
DRAM_DQS0_P	DQS0_t_A	DQSL_t_A	DQSL_A
DRAM_DQS0_N	DQS0_c_A	DQSL_c_A	DQSL#_A
DRAM_DM0	DMI0_A	DML_n_A / DBIL_n_A	DML_A
DRAM_DQ00	DQ0_A	DQL0_A	DQL0_A
DRAM_DQ01	DQ1_A	DQL1_A	DQL1_A
DRAM_DQ02	DQ2_A	DQL2_A	DQL2_A
DRAM_DQ03	DQ3_A	DQL3_A	DQL3_A
DRAM_DQ04	DQ4_A	DQL4_A	DQL4_A
DRAM_DQ05	DQ5_A	DQL5_A	DQL5_A
DRAM_DQ06	DQ6_A	DQL6_A	DQL6_A

Table 67. DDR pin function list (continued)

DRAM_DQ07	DQ7_A	DQL7_A	DQL7_A
DRAM_DQS1_P	DQS1_t_A	DQSU_t_A	DQSU_A
DRAM_DQS1_N	DQS1_c_A	DQSU_c_A	DQSU#_A
DRAM_DM1	DMI1_A	DMU_n_A / DBIU_n_A	DMU_A
DRAM_DQ08	DQ08_A	DQU0_A	DQU0_A
DRAM_DQ09	DQ09_A	DQU1_A	DQU1_A
DRAM_DQ10	DQ10_A	DQU2_A	DQU2_A
DRAM_DQ11	DQ11_A	DQU3_A	DQU3_A
DRAM_DQ12	DQ12_A	DQU4_A	DQU4_A
DRAM_DQ13	DQ13_A	DQU5_A	DQU5_A
DRAM_DQ14	DQ14_A	DQU6_A	DQU6_A
DRAM_DQ15	DQ15_A	DQU7_A	DQU7_A
DRAM_RESET_N	RESET_N	RESET_n	RESET#
DRAM_ALERT_N	MTEST1	ALERT_n / MTEST1	MTEST1
DRAM_AC00	CKE0_A	CKE0	CKE0
DRAM_AC01	CKE1_A	CKE1	CKE1
DRAM_AC02	CS0_A	CS0_n	CS0#
DRAM_AC03	CS1_A	C0	—
DRAM_AC04	CK_t_A	BG0	BA2
DRAM_AC05	CK_c_A	BG1	A14
DRAM_AC06	—	ACT_n	A15
DRAM_AC07	—	A9	A9
DRAM_AC08	CA0_A	A12	A12 / BC#
DRAM_AC09	CA1_A	A11	A11
DRAM_AC10	CA2_A	A7	A7
DRAM_AC11	CA3_A	A8	A8
DRAM_AC12	CA4_A	A6	A6
DRAM_AC13	CA5_A	A5	A5
DRAM_AC14	ODT_CA_A	A4	A4
DRAM_AC15	—	A3	A3
DRAM_AC16	—	CK_t_A	CK_A
DRAM_AC17	—	CK_c_A	CK#_A
DRAM_AC19	MTEST	MTEST	MTEST
DRAM_AC20	CKE0_B	CK_t_B	CK_B

Table 67. DDR pin function list (continued)

DRAM_AC21	CKE1_B	CK_c_B	CK#_B
DRAM_AC22	CS1_B	—	—
DRAM_AC23	CS0_B	—	—
DRAM_AC24	CK_t_B	A2	A2
DRAM_AC25	CK_c_B	A1	A1
DRAM_AC26	—	BA1	BA1
DRAM_AC27	—	PARITY	—
DRAM_AC28	CA0_B	A13	A13
DRAM_AC29	CA1_B	BA0	BA0
DRAM_AC30	CA2_B	A10 / AP	A10 / AP
DRAM_AC31	CA3_B	A0	A0
DRAM_AC32	CA4_B	C2	—
DRAM_AC33	CA5_B	CAS_n / A15	CAS#
DRAM_AC34	ODT_CA_B	WE_n / A14	WE#
DRAM_AC35	—	RAS_n / A16	RAS#
DRAM_AC36	—	ODT0	ODT0
DRAM_AC37	—	ODT1	ODT1
DRAM_AC38	—	CS1_n	CS1#
DRAM_ZN	ZQ	ZQ	ZQ
DRAM_VREF	VREF	VREF	VREF

6 Revision history

Table 68 provides a revision history for this data sheet.

Table 68. Revision history

Rev.number	Date	Substantive change(s)
Rev. 0	10/2019	• Initial version

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Document Number: IMX8MNCEC
10/2019