LT1761 100mA Low Noise Micropower LDO Regulators

DESCRIPTION

Demonstration circuit DC330 comprises two low noise micropower voltage regulators using the LT®1761 in the 5-lead SOT-23 package. These circuits are primarily used in cellular phones, voltage controlled oscillators, RF power supplies and as local regulators in larger systems. Their ability to tolerate a wide variety of output capacitors makes them ideal in space- and cost-sensitive systems.

PERFORMANCE SUMMARY

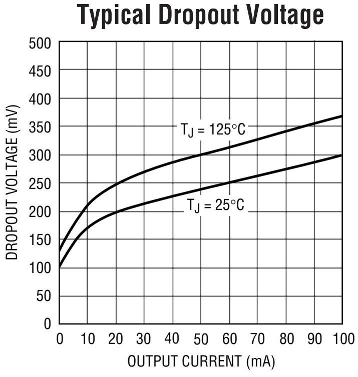
T_A = 25°C, V_{IN} = 2.3V, V_{SHDN} = 5V, I_{LOAD} = 1mA, V_{OUT} = 1.22V (JP1 or JP3 set on pins 1 and 2), unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range		2.3		20	V
Output Voltage (Note 1)		1.205	1.220	1.235	V
Output Voltage (Note 1)	V_{IN} = 2.8V, JP1 or JP3 on Pins 5 and 6	1.764	1.802	1.839	V
Output Voltage (Note 1)	V_{IN} = 3V, JP1 or JP3 on Pins 7 and 8	1.954	1.999	2.044	V
Output Voltage (Note 1)	V_{IN} = 3.5V, JP1 or JP3 on Pins 9 and 10	2.455	2.506	2.571	V
Output Voltage (Note 1)	V_{IN} = 3.8V, JP1 or JP3 on Pins 11 and 12	2.742	2.817	2.894	V
Output Voltage (Note 1)	V_{IN} = 4V, JP1 or JP3 on Pins 13 and 14	2.936	3.019	3.103	V
Output Voltage (Note 1)	V_{IN} = 4.3V, JP1 or JP3 on Pins 15 and 16	3.207	3.300	3.396	V
Output Voltage (Note 1)	V_{IN} = 5V, JP1 or JP3 on Pins 17 and 18	4.848	5.006	5.167	V
Line Regulation	ΔV_{IN} = 2.3V to 20V		1	5	mV
Quiescent Current	I_{LOAD} = 0mA		20	35	µA
Load Regulation	ΔI_{LOAD} = 1mA to 100mA		0.2	1	%
$\overline{SHDN}$ Pin Threshold (LT1761-SD)	On-to-Off Off-to-On, I_{LOAD} = 100mA	0.45	0.65 0.8	 1.8	V V
Output Voltage Noise (LT1761-BYP)	I_{LOAD} = 100mA, BW = 10Hz to 100kHz		20		μV_{RMS}

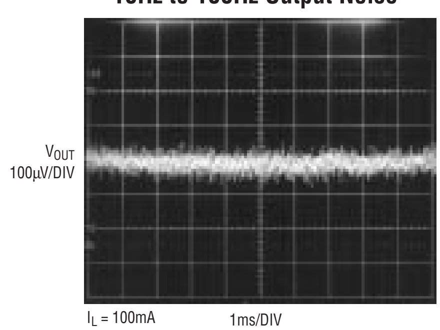
Note 1: Output voltage variations include ±1% tolerance of feedback divider network. For tighter voltage range, use lower tolerance resistors or use fixed voltage output devices.

TYPICAL PERFORMANCE CHARACTERISTICS AND BOARD PHOTO

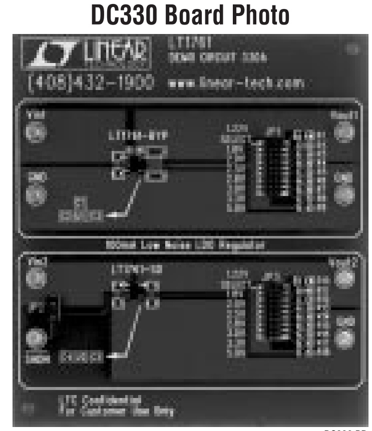
Typical Dropout Voltage



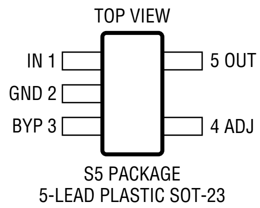
LT1761-BYP (5V Output)
10Hz to 100Hz Output Noise



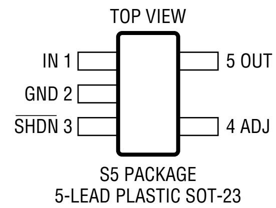
DC330 Board Photo



PACKAGE AND SCHEMATIC DIAGRAMS



LT1761ES5-BYP



LT1761ES5-SD

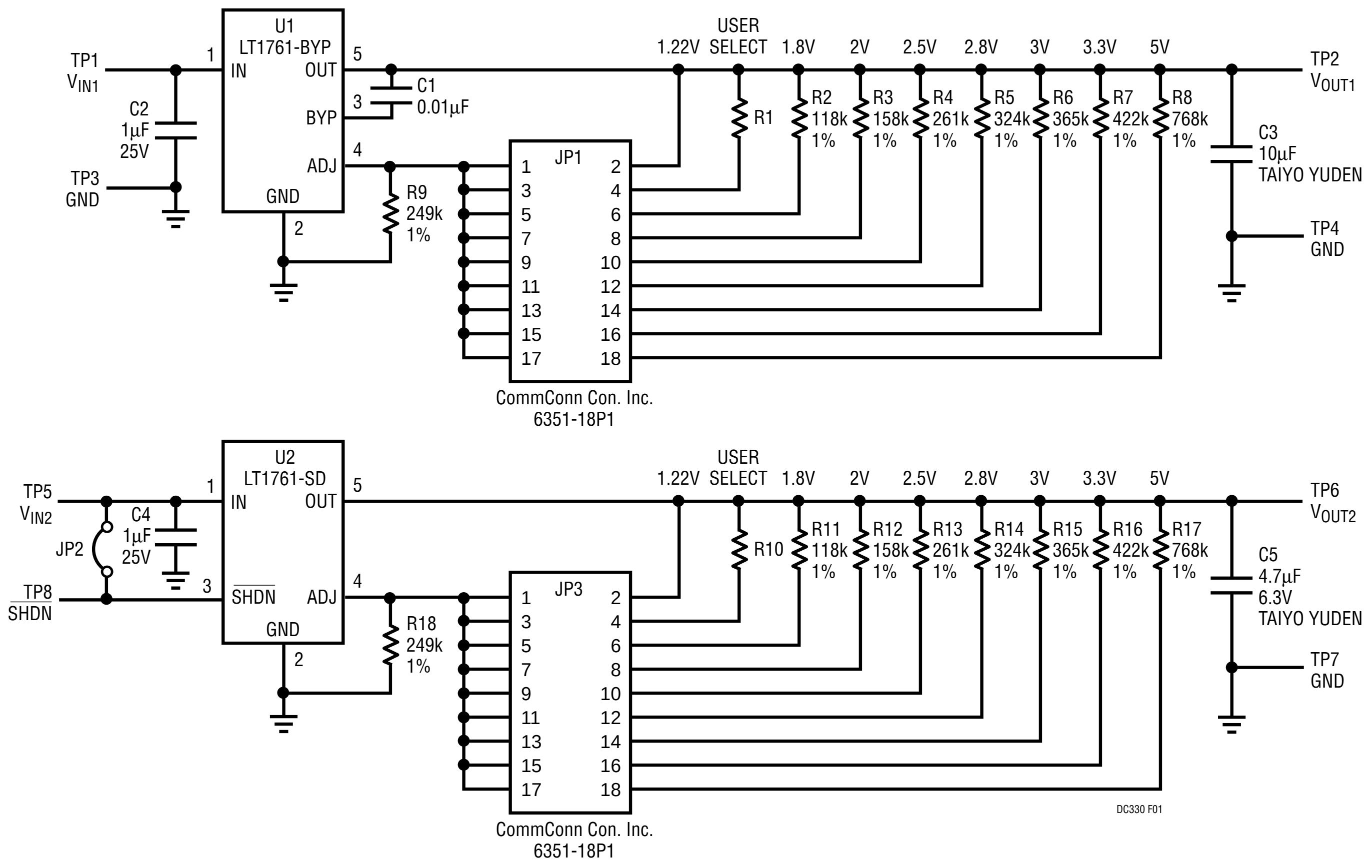


Figure 1. 100mA Low Noise LDO Regulator

PARTS LIST

REFERENCE DESIGNATOR	QUANTITY	PART NUMBER	DESCRIPTION	VENDOR	TELEPHONE
C1	1	0402YC103KAT2A	0.01µF 16V 10% X7R Capacitor	AVX	(843) 946-0362
C2, C4	2	GRM40Y5U105Z025AL	1µF 25V 80% Ceramic Capacitor	Murata Erie	(770) 436-1300
C3	1	LMK325BJ106MN-T	10µF 25V XX% Ceramic Capacitor	Taiyo Yuden	(408) 573-4150
C5	1	JMK212BJ475MG-T	4.7µF 6.3V 20% X7R Capacitor	Taiyo Yuden	(408) 573-4150
JP1, JP3	2	50971	1mm Ctr Double Row Header	Comm Con	(626) 301-4200
JP2	1	2802S-02G2	2mm 2-Pin Ctr. Jumper	Comm Con	(626) 301-4200
JP1, JP3	2	CTAIJ1MM-G	1mm Single Insulated Shunts	Comm Con	(626) 301-4200
R1, R10 Optional	0	CJ06-0R0JM	0Ω 5% 0.1W Chip Resistor	AAC	(800) 508-1521
R2, R11	2	CR05-1183FM	118k 1% 1/16W Chip Resistor	AAC	(800) 508-1521
R3, R12	2	CR05-1583FM	158k 1% 1/16W Chip Resistor	AAC	(800) 508-1521
R4, R13	2	CR05-2613FM	261k 1% 1/16W Chip Resistor	AAC	(800) 508-1521
R5, R14	2	CR05-3243FM	324k 1% 1/16W Chip Resistor	AAC	(714) 255-9186
R6, R15	2	CR05-3653FM	365k 1% 1/16W Chip Resistor	AAC	(714) 255-9186
R7, R16	2	CR05-4223FM	422k 1% 1/16W Chip Resistor	AAC	(714) 255-9186
R8, R17	2		768k 1% 1/16W Chip Resistor	Panasonic	(714) 373-7334
R9, R18	2		249k 1% 1/16W Chip Resistor	AAC	(714) 255-9186
TP1-TP8	8	2308-2	Turret, Testpoint	Mill-Max	(516) 922-6000
U1	1	LT1761-BYP	LDO Regulator IC	LTC	(408) 432-1900
U2	1	LT1761-SD	LDO Regulator IC	LTC	(408) 432-1900

OPERATION

Part Selection

Two versions of the LT1761 are provided for evaluation. Both are adjustable versions, one with the low noise option, and the other with the low current shutdown option. Both allow selection of a number of common output voltages or a custom output voltage. Fixed voltage parts operate similarly to the adjustable parts, except that fixed voltage LT1761 regulators feature both low current shutdown and low noise operation.

Hook-Up

Solid turret terminals are provided for easy connection to supplies and test equipment. Connect a 0V to 20V, 0.2A power supply across the V_{IN} and GND terminals and the load across the V_{OUT} and GND terminals. The $\overline{SHDN}$ pin can be disconnected from V_{IN} by removing JP2 to allow separate shutdown control via a secondary control line. JP1 and JP3 can be used to select a number of common fixed output voltages or, in conjunction with R1 or R10, to create a custom output voltage using the formula:

R1 or R10 = $(V_{OUT} – 1.22V)/4.93\mu A$

Output Capacitor Selection

The output capacitor C3 is a 10µF X7R ceramic chip capacitor and C5 is a 3.3µF X7R ceramic chip capacitor. Care must be exercised in the selection of output capacitors should a different output capacitor be desired. Many ceramic capacitor dielectrics exhibit undesirable temperature and voltage characteristics that reduce their effective capacitance to as low as 10% to 20% of nominal value. For further information, see Linear Technology Application Note 83, “Performance Verification of Low Noise, Low Dropout Regulators,” Appendix B, “Capacitor Selection Considerations”; see also the Applications Information Section of this manual.

Output Voltage Noise

Measuring output voltage noise can be a tricky process, further complicated by the low levels of noise inherent in a circuit such as this. Consideration must be given to regulator operating conditions, as well as the noise bandwidth of interest. Linear Technology has invested an enormous amount of time to provide accurate, relevant data to customers regarding noise performance. For further information on measuring output voltage noise, see Linear Technology Application Note 83, “Performance Verification of Low Noise, Low Dropout Regulators.”

APPLICATIONS INFORMATION

Noise Testing Considerations

What noise bandwidth is of interest and why is it interesting? In most systems, the range of 10Hz to 100kHz is the information signal processing area of concern. Additionally, linear regulators produce little noise energy outside this region.[1] These considerations suggest a measurement bandpass of 10Hz to 100kHz, with steep slopes at the band limits. Figure 2 shows a conceptual filter for LDO noise testing. The Butterworth sections are the key to steep slopes and flatness in the passband. The small input level requires 60dB of low noise gain to provide adequate signal for the Butterworth filters. Figure 3 details the filter scheme. The regulator under test is at the diagram’s center.[2] A1–A3 make up a 60dB gain highpass section. A1 and A2, extremely low noise devices ($<1nV/\sqrt{Hz}$), comprise a 60dB gain stage with a 5Hz highpass input. A3 provides a 10Hz, 2nd order Butterworth highpass characteristic. The LTC®1562 filter block is arranged as a 4th order Butterworth lowpass. Its output is delivered via the 330µF-100Ω highpass network. The circuit’s output drives a thermally responding RMS voltmeter.[3] Note that all circuit power is furnished by batteries, precluding ground loops from corrupting the measurement.

Note 1: Switching regulators are an entirely different proposition, requiring very broadband noise measurement. See Reference 1.

Note 2: Component choice for the regulator, more critical than might be supposed, is discussed in Appendix B, “Capacitor Selection Considerations.”

Note 3: The choice of the RMS voltmeter is absolutely crucial to obtaining meaningful measurements. See Application Note 83 Appendix C, “Understanding and Selecting RMS Voltmeters.”

APPLICATIONS INFORMATION

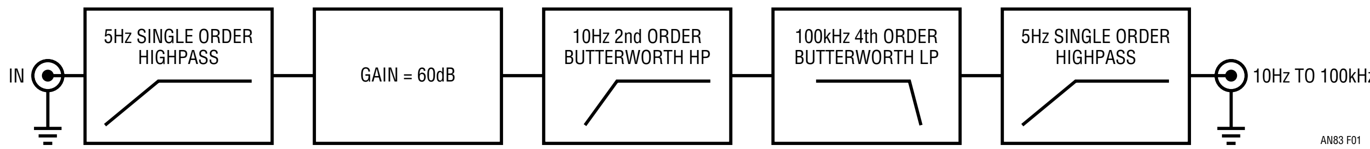


Figure 2. Filter Structure for Noise Testing LDOs. Butterworth Sections Provide Appropriate Response in Desired Frequency Range

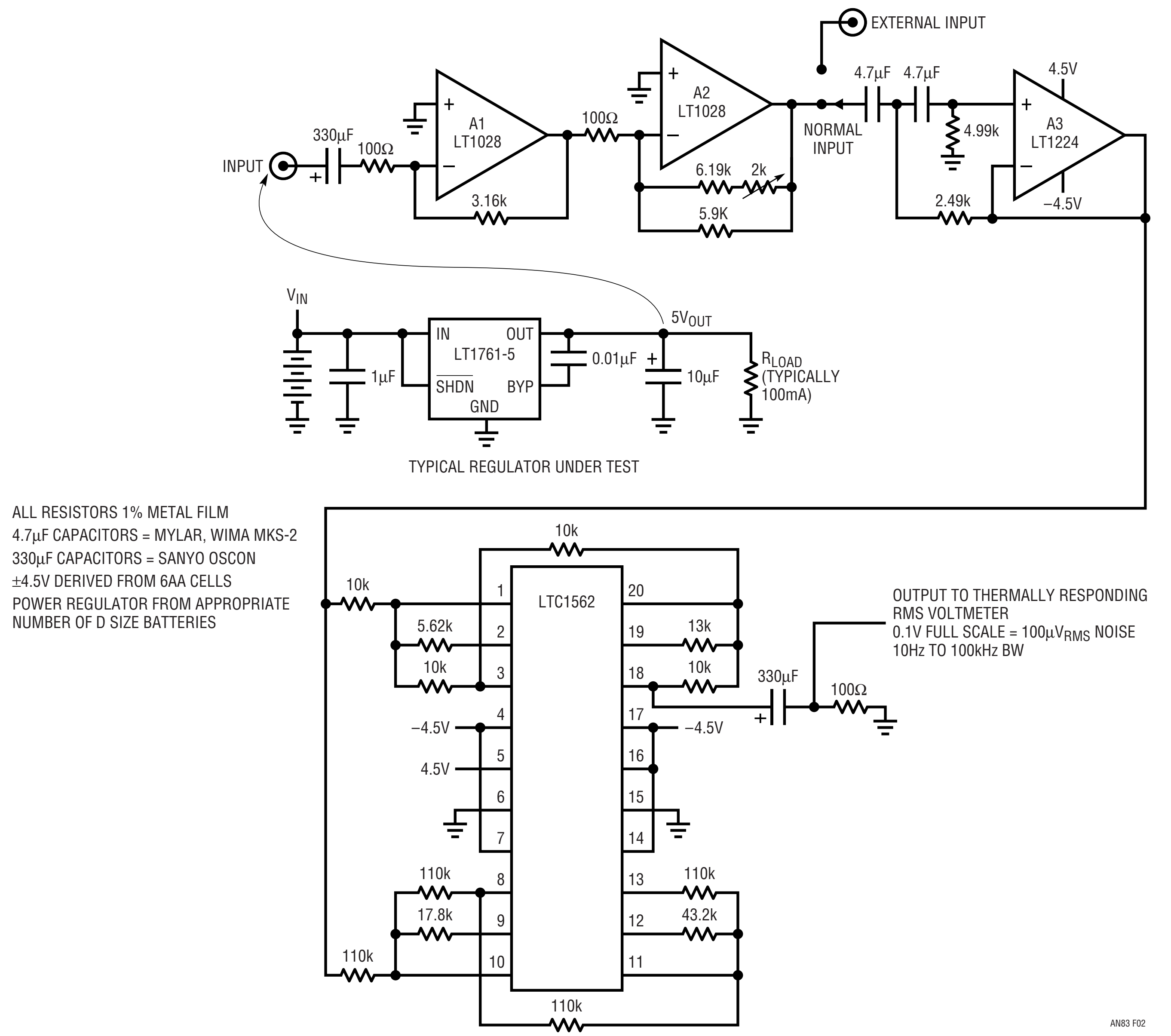


Figure 3. Implementation of Figure 2. Low Noise Amplifiers Provide Gain and Initial Highpass Shaping. LTC1562 Filter Supplies 4th Order Butterworth Lowpass Characteristic

APPLICATIONS INFORMATION

APPENDIX B

CAPACITOR SELECTION CONSIDERATIONS

Bypass Capacitance and Low Noise Performance

Adding a capacitor between the regulator's OUT and BYP pins lowers output noise. A good quality low leakage capacitor is recommended. This capacitor bypasses the regulator's reference, providing a low frequency noise pole. A 0.01μF capacitor lowers the output voltage noise to $20\mu V_{RMS}$. Using a bypass capacitor also improves transient response. With no bypassing and a 10μF output capacitor, a 10mA to 500mA load step settles to within 1% of final value in under 100μs. With a 0.01μF bypass capacitor, the output settles to within 1% for the same load step in under 10μs; total output deviation is inside 2.5%. Regulator start-up time is inversely proportional to bypass capacitor size, slowing to 15ms with a 0.01μF bypass capacitor and 10μF at the output.

Output Capacitance and Transient Response

The regulators are designed to be stable with a wide range of output capacitors. Output capacitor ESR affects stability, most notably with small capacitors. A 3.3μF minimum output value with ESR of 3Ω or less is recommended to prevent oscillation. Transient response is a function of output capacitance. Larger values of output capacitance decrease peak deviations, providing improved transient response for large load current changes. Bypass capacitors, used to decouple individual components powered by the regulator, increase the effective output capacitor value. Larger values of reference bypass capacitance dictate larger output capacitors. For 100pF of bypass capacitance, 4.7μF of output capacitor is recommended. With 1000pF of bypass capacitance or larger, a 6.8μF output capacitor is required.

Figure B1's shaded region defines the regulator's stability range. Minimum ESR needed is set by the amount of bypass capacitance used, while maximum ESR is 3Ω.

Ceramic Capacitors

Ceramic capacitors require extra consideration. They are manufactured with a variety of dielectrics, each with different behavior across temperature and applied voltage. The most common dielectrics are Z5U, Y5V, X5R and X7R. The Z5U and Y5V dielectrics provide high capacitance in a small package, but exhibit strong voltage and temperature coefficients as shown in Figures B2 and B3. Used with a 5V regulator, a 10μF Y5V capacitor shows values as low as 1μF to 2μF over the operating temperature range. The X5R and X7R dielectrics have more stable characteristics and are more suitable for output capacitor use. The X7R type has better stability over temperature, while the X5R is less expensive and available in higher values.

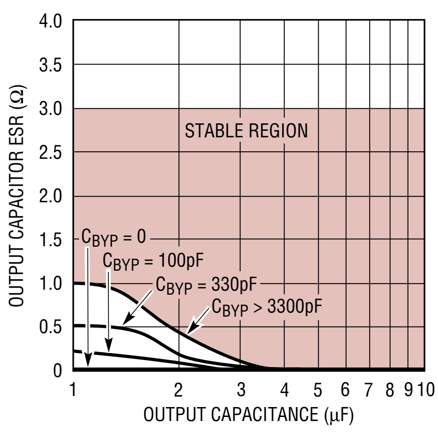


Figure B1. Regulator Stability for Various Output and Bypass (C_{BYP}) Capacitor Characteristics

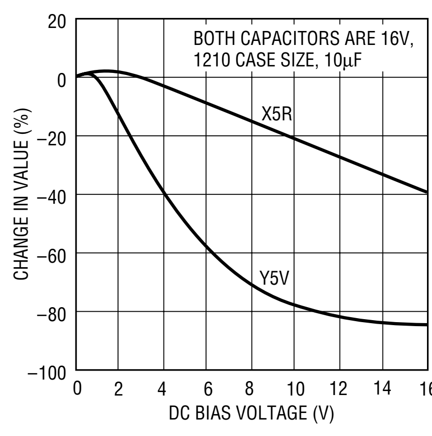


Figure B2. Ceramic Capacitor DC Bias Characteristics Indicate Pronounced Voltage Dependence. Device Must Provide Desired Capacitance Value at Operating Voltage

APPLICATIONS INFORMATION

Voltage and temperature coefficients are not the only problem sources. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress, similar to the way a piezoelectric accelerometer or microphone works. For a ceramic capacitor the stress can be induced by vibrations in the system or thermal transients. The resulting voltages produced can cause appreciable amounts of noise, especially when a ceramic capacitor is used for noise bypassing. A ceramic capacitor produced Figure B4's trace in response to light tapping from a pencil. Similar vibration-induced behavior can masquerade as increased output voltage noise.

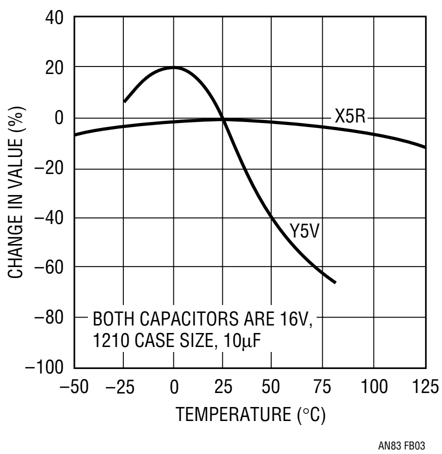


Figure B3. Ceramic Capacitor Temperature Characteristics Show Large Capacitance Shift. Effect Should Be Considered When Determining Circuit Error Budget

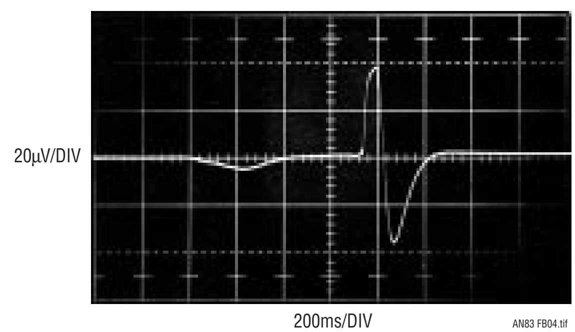
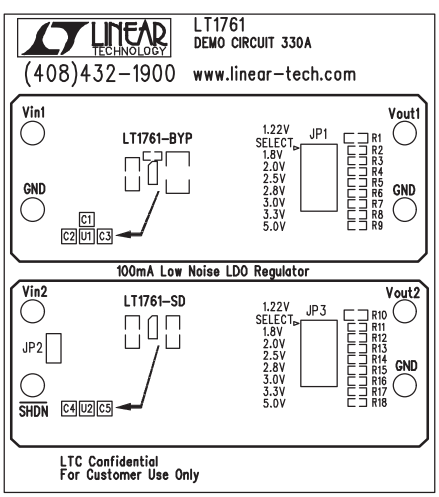
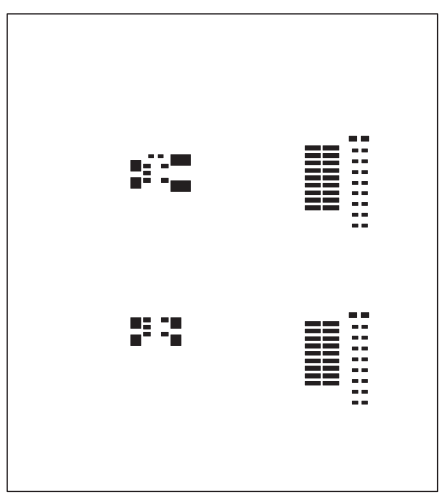


Figure B4. A Ceramic Capacitor Responds to Light Pencil Tapping. Piezoelectric Based Response Approaches 80µV_{P-P}

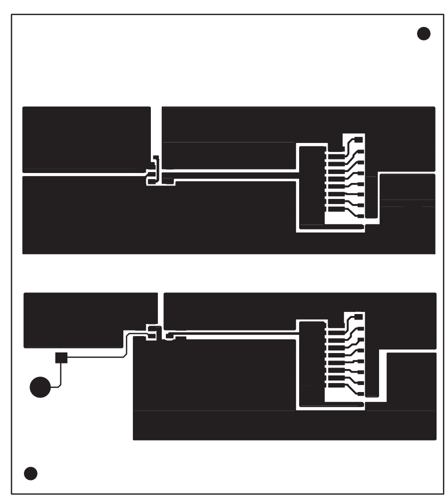
PCB LAYOUT AND FILM



Silkscreen Top

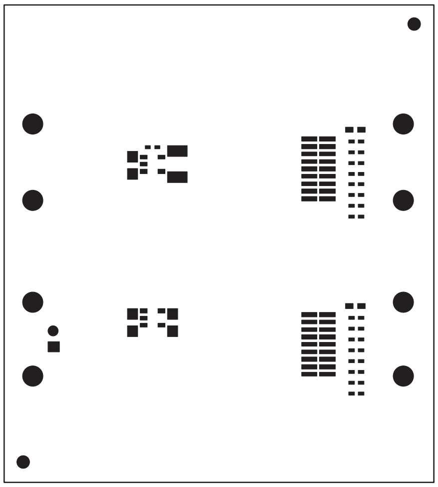


Paste Mask Top

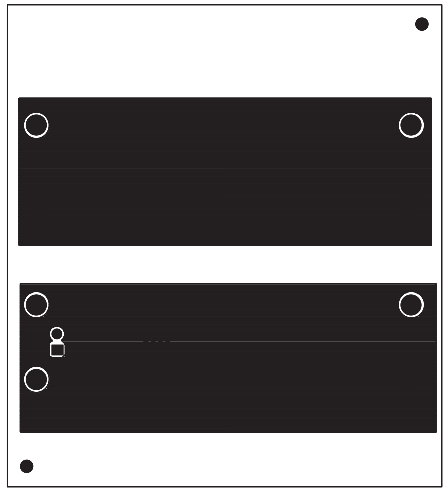


Component Side

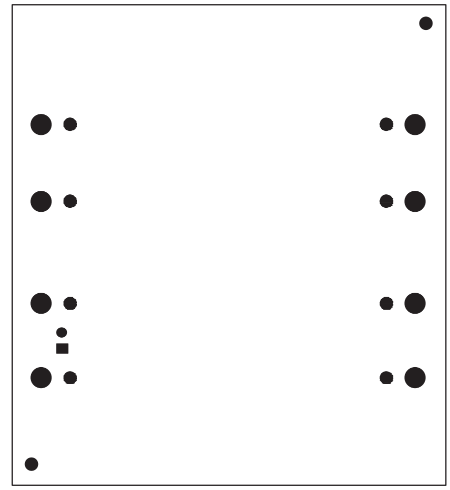
PCB LAYOUT AND FILM



Solder Mask Top

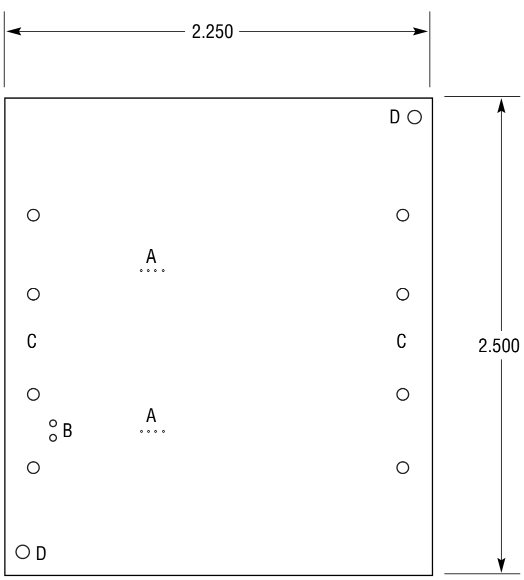


Solder Side



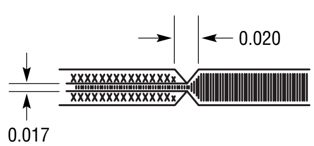
Solder Mask Bottom

PC FAB DRAWING



NOTES: UNLESS OTHERWISE SPECIFIED

1. MATERIAL: 2 LAYERS, 0.062" THK. FR-4 GLASS EPOXY, 2 0Z COPPER CLAD
2. ALL HOLES SHALL BE PLATED THRU.
3. PLATE THRU HOLES WITH COPPER 0.0014 MIN THICKNESS. ALL HOLE SIZES IN HOLE TABLE ARE AFTER PLATING.
4. SILKSCREEN: WITH WHITE EPOXY NON-CONDUCTIVE INK.
5. NO SILKSCREEN ALLOWED ON PADS LANDS.
6. SOLDER MASK: LPI, GREEN.
7. NO BLOCK SOLDERMASKING OF PAD ROWS.
8. SCORING:



SYMBOL	DIAMETER	NUMBER OF HOLES	PLATED
A	0.010	8	YES
B	0.035	2	YES
C	0.061	8	YES
D	0.070	2	NO
TOTAL HOLES		20	

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