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NTE7495
Integrated Circuit
TTL – 4–Bit Parallel–Access Shift Register

Description:

The NTE7495 is 4–bit register in a 14–Lead DIP type package that features parallel and serial inputs, parallel outputs, mode control, and two clock inputs. This device hs three output modes of operation:

Parallel (broadside) Load
Shift Right (the direction Q_A toward Q_D)
Shift Left (the direction Q_D toward Q_A)

Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip–flops and appears at the outputs after the high–to–low transition of the clock–2 input. During loading, the entry of serial data is inhibited.

Shift right is accomplished on the high–to–low transition of clock 1 when the mode control is low; shift left is accomplished on the high–to–low transition of clock 2 when the mode control is high by connecting the output of each flip–flop to the parallel input of the previous flip–flop (Q_D to input C, etc.) and serial data is entered at input D. The clock input may be applied commonly to clock 1 and clock 2 if both modes can be clocked from the same source. Changes at the mode control input should normally be made while both clock inputs are low; however, conditions described in the last three lines of the function table will also ensure that register contents are protected.

Absolute Maximum Ratings: (Note 1)

Supply Voltage, V_{CC} 7V
Input Voltage, V_{IN} 5.5V
Interemitter Voltage (Note 2) 5.5V
Power Dissipation 195mW
Operating Temperature Range, T_A . . . . . 0°C to +70°C
Storage Temperature Range, T_{stg} . . . . . –65°C to +150°C

Note 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
Note 2. This is the voltage between two emitters of a multiple–emitter input transistor. This rating applies between the clock–2 and th mode control input.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
High−Level Output Current	I_{OH}	–	–	−800	μA
Low−Level Output Current	I_{OL}	–	–	16	mA
Clock Frequency	f_{clock}	0	–	25	MHz
Width of Clock Pulse	$t_{w(clock)}$	20	–	_	ns
Setup Time, High Level or Low−Level Data	t_{su}	15	–	–	ns
Hold Time, High Level or Low−Level Data	t_h	0	–	–	ns
Time to Enable Clock 1	$t_{enable\ 1}$	15	–	–	ns
Time to Enable Clock 2	$t_{enable\ 2}$	15	–	–	ns
Time to Inhibit Clock 1	$t_{inhibit\ 1}$	5	–	–	ns
Time to Inhibit Clock 2	$t_{inhibit\ 2}$	5	–	–	ns
Operating Temperature Range	T_A	0	–	+70	°C

Electrical Characteristics: (Note 2, Note 3)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
High−Level Input Voltage	V_{IH}		2	–	–	V
Low−Level Input Voltage	V_{IL}		–	–	0.8	V
Input Clamp Voltage	V_{IK}	V_{CC} = MIN, I_I = −12mA	–	–	−1.5	V
High Level Output Voltage	V_{OH}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −800μA	2.4	3.4	–	V
Low Level Output Voltage	V_{OL}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16mA	–	0.2	0.4	V
Input Current	I_I	V_{CC} = MAX, V_I = 5.5V	–	–	1	mA
High Level Input Current Serial, A, B, C, D	I_{IH}	V_{CC} = MAX, V_I = 2.7V	–	–	40	μA
Clock 1 or 2			–	–	40	μA
Mode Control			–	–	80	μA
Low Level Input Current Serial, A, B, C, D	I_{IL}	V_{CC} = MAX, V_I = 0.4V	–	–	−1.6	mA
Clock 1 or 2			–	–	−1.6	mA
Mode Control			–	–	−3.2	mA
Short−Circuit Output Current	I_{OS}	V_{CC} = MAX, Note 4	−18	–	−57	mA
Supply Current	I_{CC}	V_{CC} = MAX, Note 5	–	39	63	mA

Note 2. .For conditions shown as MIN or MAX, use the appropriate value specified under “Recommended Operation Conditions”.

Note 3. All typical values are at V_{CC} = 5V, T_A = +25°C.

Note 4. Not more than one output should be shorted at a time.

Note 5. I_{CC} is measured with all outputs and serial input open; A, B, C, and D inputs grounded; mode control at 4.5V; and a momentary 3V, then ground, applied to both clock inputs.

Switching Characteristics: (V_{CC} = 5V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum Clock Frequency	f_{max}	R_L = 400Ω, C_L = 15pF	25	36	–	MHz
Propagation Delay Time	t_{PLH}		–	18	27	ns
	t_{PHL}		–	21	32	ns

Function Table:

Inputs								Outputs			
Mode Control	Clocks		Serial	Parallel				Q_A	Q_B	Q_C	Q_D
	2 (L)	1 (R)		A	B	C	D				
H	H	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	↓	X	X	a	b	c	d	a	b	c	d
H	↓	X	X	Q_B †	Q_C †	Q_D †	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d
L	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	X	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	X	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
↑	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

† = Shifting left requires external connection of Q_B to A, Q_C to B, and Q_D to C. Serial data is entered at input D.

H = HIGH Level (Steady State)

L = LOW Level (Steady State)

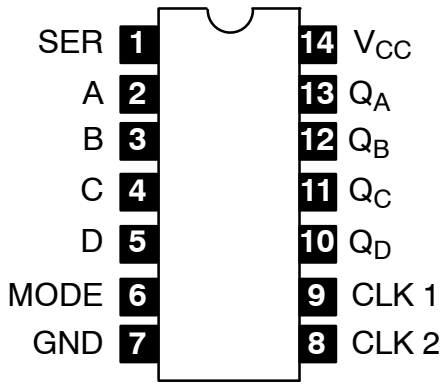
X = Irrelevant (Any input, including transitions)

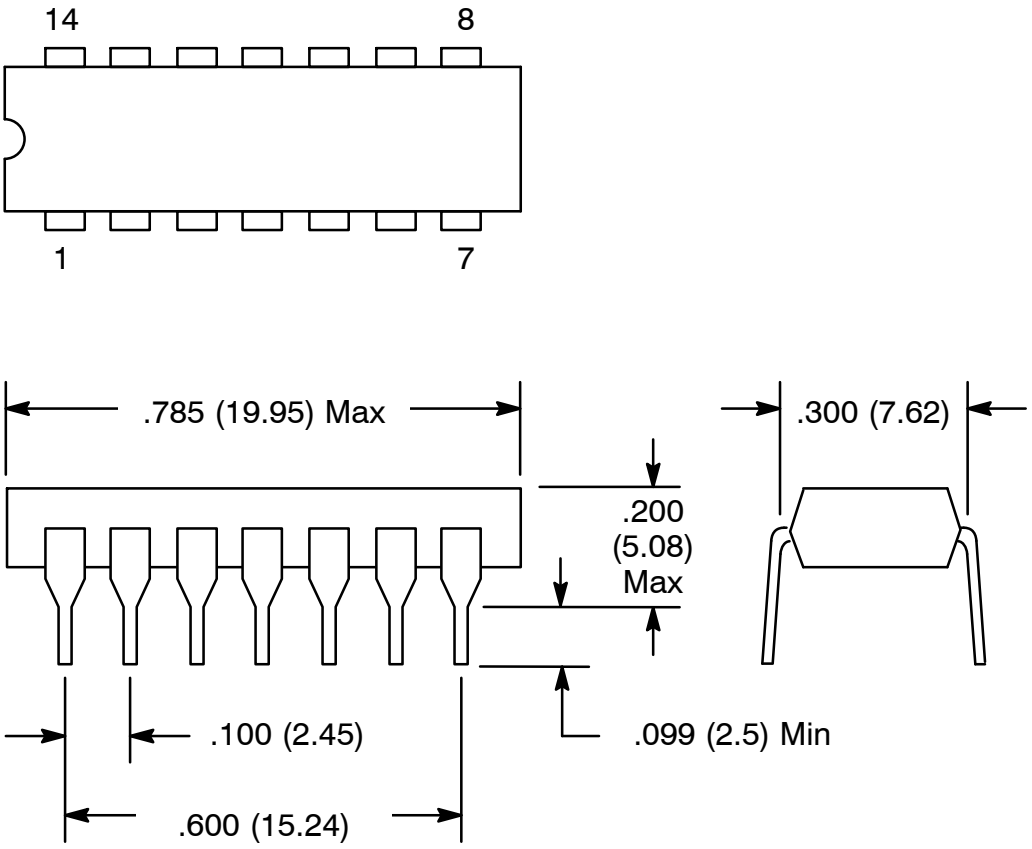
a, b, c, d = The level of steady−state input at inputs A, B, C, or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = The level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady−state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = The level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most−recent ↓ transition of the clock.

Pin Connection Diagram




14
8
1
7
.785 (19.95) Max
.300 (7.62)
.200
(5.08)
Max
.100 (2.45)
.099 (2.5) Min
.600 (15.24)