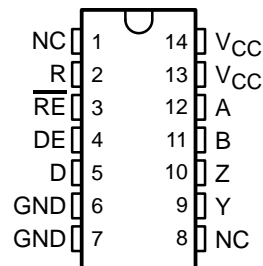


SN65ALS180, SN75ALS180 DIFFERENTIAL DRIVER AND RECEIVER PAIRS

SLLS052G – AUGUST 1987 – REVISED APRIL 2003

- Meet or Exceed the Requirements of TIA/EIA-422-B, TIA/EIA-485-A† and ITU Recommendation V.11
- High-Speed Advanced Low-Power Schottky Circuitry
- Designed for 25-Mbaud Operation in Both Serial and Parallel Applications
- Low Skew Between Devices . . . 6 ns Max
- Low Supply-Current Requirements . . . 30 mA Max
- Individual Driver and Receiver I/O Pins With Dual V_{CC} and Dual GND
- Wide Positive and Negative Input/Output Bus Voltage Ranges
- Driver Output Capacity . . . ±60 mA
- Thermal Shutdown Protection
- Driver Positive- and Negative-Current Limiting
- Receiver Input Impedance . . . 12 kΩ Min
- Receiver Input Sensitivity . . . ±200 mV Max
- Receiver Input Hysteresis . . . 60 mV Typ
- Operate From a Single 5-V Supply
- Glitch-Free Power-Up and Power-Down Protection

SN65ALS180 . . . D PACKAGE
SN75ALS180 . . . D OR N PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The SN65ALS180 and SN75ALS180 differential driver and receiver pairs are integrated circuits designed for bidirectional data communication on multipoint bus-transmission lines. They are designed for balanced transmission lines and meet TIA/EIA-422-B, TIA/EIA-485-A, and ITU Recommendation V.11.

ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP (N)	Tube of 25	SN75ALS180N	SN75ALS180N
	SOIC (D)	Tube of 50	SN75ALS180D	75ALS180
		Reel of 2500	SN75ALS180DR	
–40°C to 85°C	SOIC (D)	Tube of 50	SN65ALS180D	65ALS180
		Reel of 2500	SN65ALS180DR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

† These devices meet or exceed the requirements of TIA/EIA-485-A, except for the Generator Contention Test (para. 3.4.2) and the Generator Current Limit (para. 3.4.3). The applied test voltage ranges are –6 V to 8 V for the SN75ALS180 and –4 V to 8 V for the SN65ALS180.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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SN65ALS180, SN75ALS180 DIFFERENTIAL DRIVER AND RECEIVER PAIRS

SLLS052G – AUGUST 1987 – REVISED APRIL 2003

description/ordering information (continued)

The SN65ALS180 and SN75ALS180 combine a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be connected together externally to function as a direction control. The driver differential outputs and the receiver differential inputs are connected to separate terminals for greater flexibility and are designed to offer minimum loading to the bus when the driver is disabled or $V_{CC} = 0$.

These ports feature wide positive and negative common-mode voltage ranges, making the device suitable for party-line applications.

Function Tables

DRIVER

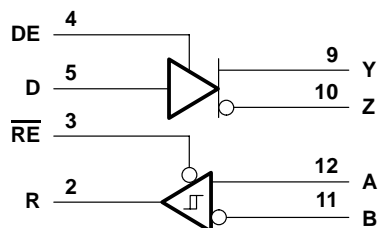
INPUT D	ENABLE DE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

RECEIVER

DIFFERENTIAL INPUTS A-B	ENABLE RE	OUTPUT R
$V_{ID} \geq 0.2\text{ V}$	L	H
$-0.2\text{ V} < V_{ID} < 0.2\text{ V}$	L	?
$V_{ID} \leq -0.2\text{ V}$	L	L
X	H	Z
Open	L	H

H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

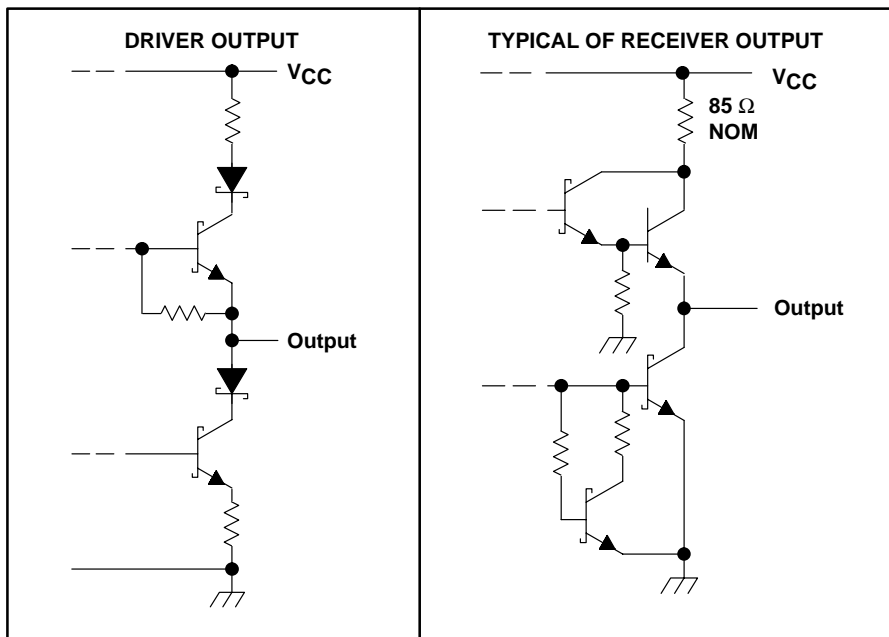
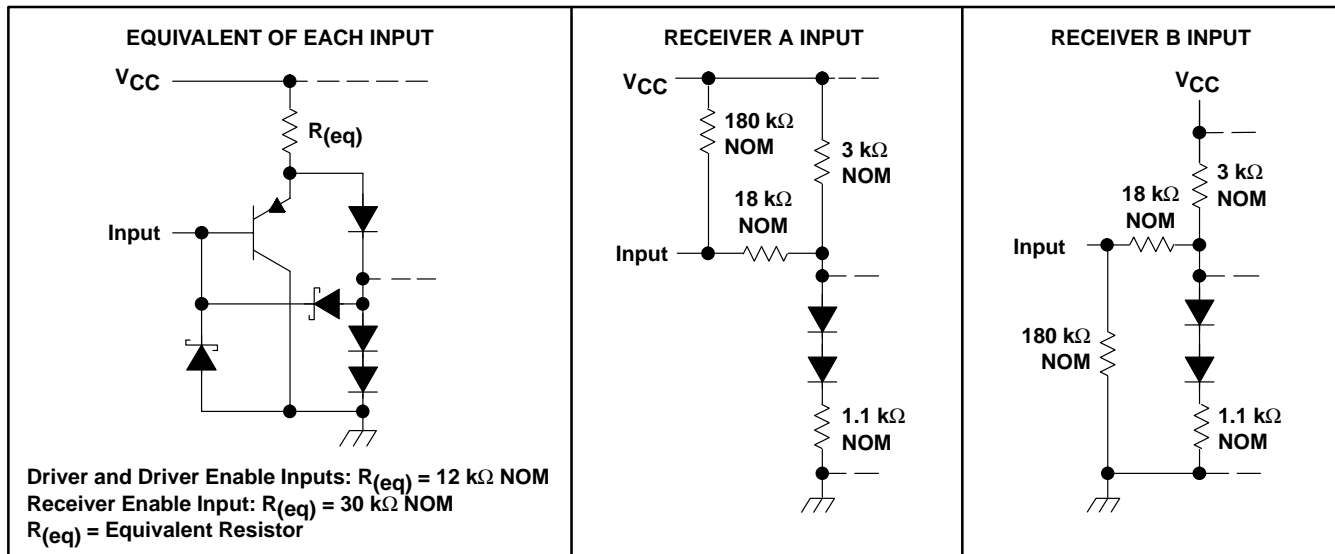
logic diagram (positive logic)



SN65ALS180, SN75ALS180 DIFFERENTIAL DRIVER AND RECEIVER PAIRS

SLLS052G – AUGUST 1987 – REVISED APRIL 2003

schematics of inputs and outputs



SN65ALS180, SN75ALS180 DIFFERENTIAL DRIVER AND RECEIVER PAIRS

SLLS052G – AUGUST 1987 – REVISED APRIL 2003

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	7 V
Voltage range at any bus terminal	-10 V to 15 V
Enable input voltage, V_I	5.5 V
Package thermal impedance, θ_{JA} (see Notes 2 and 3): D package	86°C/W
N package	80°C/W
Operating virtual junction temperature, T_J	150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T_{st}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.
 2. Maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} - T_A) / \theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		MIN	NOM	MAX	UNIT	
V_{CC}	Supply voltage	4.75	5	5.25	V	
V_I or V_{IC}	Voltage at any bus terminal (separately or common mode)	12			V	
		-7				
V_{IH}	High-level input voltage	D, DE, and \overline{RE}		2	V	
V_{IL}	Low-level input voltage	D, DE, and \overline{RE}		0.8	V	
V_{ID}	Differential input voltage (see Note 4)				±12	V
I_{OH}	High-level output current	Driver		-60	mA	
		Receiver		-400	µA	
I_{OL}	Low-level output current	Driver		60	mA	
		Receiver		8		
T_A	Operating free-air temperature	SN65ALS180		-40	85	°C
		SN75ALS180		0	70	

NOTE 4: Differential-input/output bus voltage is measured at the noninverting terminal, A/Y, with respect to the inverting terminal, B/Z.



SN65ALS180, SN75ALS180 DIFFERENTIAL DRIVER AND RECEIVER PAIRS

SLLS052G – AUGUST 1987 – REVISED APRIL 2003

DRIVERS

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITION†	MIN	TYP‡	MAX	UNIT	
V _{IK}	Input clamp voltage	I _I = -18 mA		-1.5	V	
V _O	Output voltage	I _O = 0		0	6	V
V _{OD1}	Differential output voltage	I _O = 0		1.5	6	V
V _{OD2}	Differential output voltage	R _L = 100 Ω,	See Figure 1	1/2 V _{OD1} or 2§		V
		R _L = 54 Ω,	See Figure 1	1.5	2.5	
V _{OD3}	Differential output voltage	V _{test} = -7 V to 12 V, See Figure 2		1.5	5	V
Δ V _{OD}	Change in magnitude of differential output voltage¶	R _L = 54 Ω or 100 Ω, See Figure 1		±0.2		V
V _{OC}	Common-mode output voltage	R _L = 54 Ω or 100 Ω, See Figure 1		3	-1	V
Δ V _{OC}	Change in magnitude of common-mode output voltage¶	R _L = 54 Ω or 100 Ω, See Figure 1		±0.2		V
I _O	Output current	Output disabled (see Note 5)	V _O = 12 V	1		mA
			V _O = -7 V	-0.8		
I _{IH}	High-level input current	V _I = 2.4 V		20		μA
I _{IL}	Low-level input current	V _I = 0.4 V		-400		μA
I _{OS}	Short-circuit output current#	V _O = -6 V	SN75ALS180	-250		mA
		V _O = -4 V	SN65ALS180	-250		
		V _O = 0	All	-150		
		V _O = V _{CC}	All	250		
		V _O = 8 V	All	250		
I _{CC}	Supply current	No load	Driver outputs enabled, Receiver disabled	25	30	mA
			Outputs disabled	19	26	

† The power-off measurement in TIA/EIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ The minimum V_{OD2} with 100-Ω load is either 1/2 V_{OD2} or 2 V, whichever is greater.

¶ Δ|V_{OD}| and Δ|V_{OC}| are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

Duration of the short circuit should not exceed one second for this test.

NOTE 5: This applies for both power on and off; refer to TIA/EIA-485-A for exact conditions. The TIA/EIA-422-B limit does not apply for a combined driver and receiver terminal.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT			
t _{d(OD)}	Differential output delay time	R _L = 54 Ω,	C _L = 50 pF,	See Figure 3	3	8	13	ns
	Pulse skew (t _{d(ODH)} - t _{d(ODL)})	R _L = 54 Ω,	C _L = 50 pF,	See Figure 3	1		6	ns
t _{t(OD)}	Differential output transition time	R _L = 54 Ω,	C _L = 50 pF,	See Figure 3	3	8	13	ns
t _{pZH}	Output enable time to high level	R _L = 110 Ω,	See Figure 4		23		50	ns
t _{pZL}	Output enable time to low level	R _L = 110 Ω,	See Figure 5		19		24	ns
t _{PHZ}	Output disable time from high level	R _L = 110 Ω,	See Figure 4		8		13	ns
t _{PLZ}	Output disable time from low level	R _L = 110 Ω,	See Figure 5		8		13	ns

‡ All typical values are at V_{CC} = 5 V and T_A = 25°C.



SN65ALS180, SN75ALS180 DIFFERENTIAL DRIVER AND RECEIVER PAIRS

SLLS052G – AUGUST 1987 – REVISED APRIL 2003

SYMBOL EQUIVALENTS

DATA-SHEET PARAMETER	TIA/EIA-422-B	TIA/EIA-485-A
V_O	V_{Oa}, V_{Ob}	V_{Oa}, V_{Ob}
$ V_{OD1} $	V_o	V_o
$ V_{OD2} $	$V_t (R_L = 100 \Omega)$	$V_t (R_L = 54 \Omega)$
$ V_{OD3} $		V_t (test termination measurement 2)
V_{test}		V_{tst}
$\Delta V_{OD} $	$ V_t - \bar{V}_t $	$ V_t - \bar{V}_t $
V_{OC}	$ V_{os} $	$ V_{os} $
$\Delta V_{OC} $	$ V_{os} - \bar{V}_{os} $	$ V_{os} - \bar{V}_{os} $
I_{OS}	$ I_{sa} , I_{sb} $	
I_O	$ I_{xa} , I_{xb} $	I_{ia}, I_{ib}

RECEIVERS

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT	
V_{IT+}	Positive-going input threshold voltage	$V_O = 2.7 V, I_O = -0.4 mA$			0.2	V	
V_{IT-}	Negative-going input threshold voltage	$V_O = 0.5 V, I_O = 8 mA$	-0.2‡			V	
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)			60		mV	
V_{IK}	Enable-input clamp voltage	$I_I = -18 mA$			-1.5	V	
V_{OH}	High-level output voltage	$V_{ID} = 200 mV, I_{OH} = -400 \mu A,$ See Figure 6	2.7			V	
V_{OL}	Low-level output voltage	$V_{ID} = -200 mV, I_{OL} = 8 mA,$ See Figure 6			0.45	V	
I_{OZ}	High-impedance-state output current	$V_O = 0.4 V$ to 2.4 V			± 20	μA	
I_I	Line input current	Other input = 0 V (see Note 6)			1	mA	
					-0.8		
I_{IH}	High-level enable-input current	$V_{IH} = 2.7 V$			20	μA	
I_{IL}	Low-level enable-input current	$V_{IL} = 0.4 V$			-100	μA	
r_i	Input resistance		12			k Ω	
I_{OS}	Short-circuit output current	$V_{ID} = 200 mV, V_O = 0$	-15		-85	mA	
I_{CC}	Supply current	No load	Receiver outputs enabled, Driver inputs disabled		19	30	mA
			Outputs disabled		19	26	

† All typical values are at $V_{CC} = 5 V, T_A = 25^\circ C$.

‡ The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

NOTE 6: This applies for both power on and power off. Refer to TIA/EIA-485-A for exact conditions.



switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH} Propagation delay time, low- to high-level output	$V_{ID} = -1.5\text{ V to }1.5\text{ V}$, See Figure 7	9	14	19	ns
t_{PHL} Propagation delay time, high- to low-level output	$V_{ID} = -1.5\text{ V to }1.5\text{ V}$, See Figure 7	9	14	19	ns
Skew ($ t_{PHL} - t_{PLH} $)	$V_{ID} = -1.5\text{ V to }1.5\text{ V}$, See Figure 7		2	6	ns
t_{PZH} Output enable time to high level	$C_L = 15\text{ pF}$, See Figure 8		7	14	ns
t_{PZL} Output enable time to low level	$C_L = 15\text{ pF}$, See Figure 8		7	14	ns
t_{PHZ} Output disable time from high level	$C_L = 15\text{ pF}$, See Figure 8		20	35	ns
t_{PLZ} Output disable time from low level	$C_L = 15\text{ pF}$, See Figure 8		8	17	ns

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

PARAMETER MEASUREMENT INFORMATION

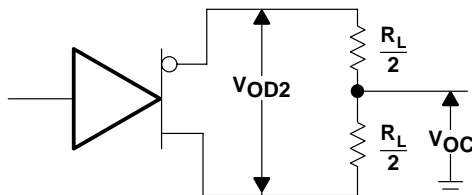


Figure 1. Driver V_{OD} and V_{OC}

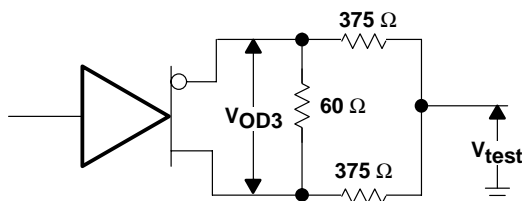
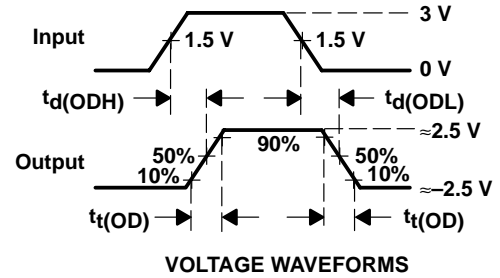
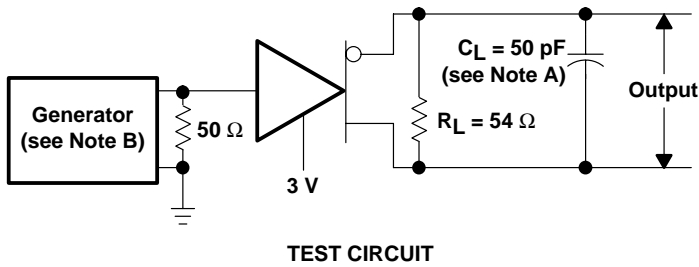


Figure 2. Driver V_{OD3}

SN65ALS180, SN75ALS180 DIFFERENTIAL DRIVER AND RECEIVER PAIRS

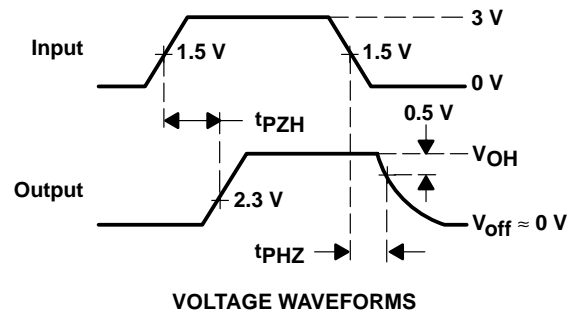
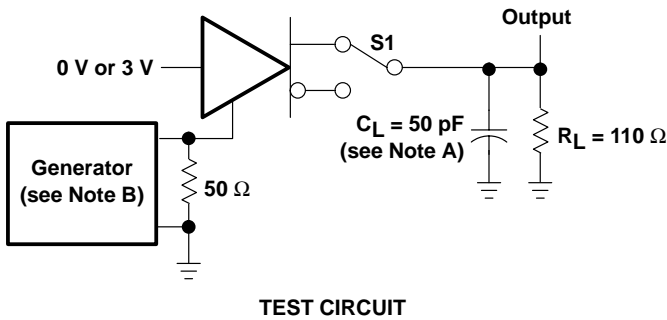
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PARAMETER MEASUREMENT INFORMATION



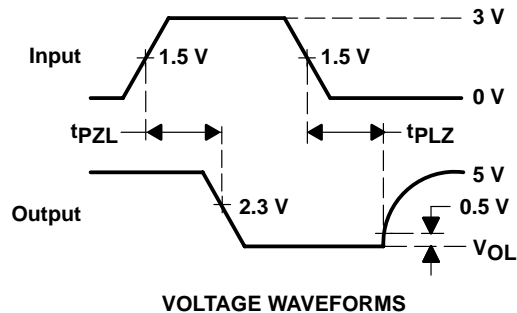
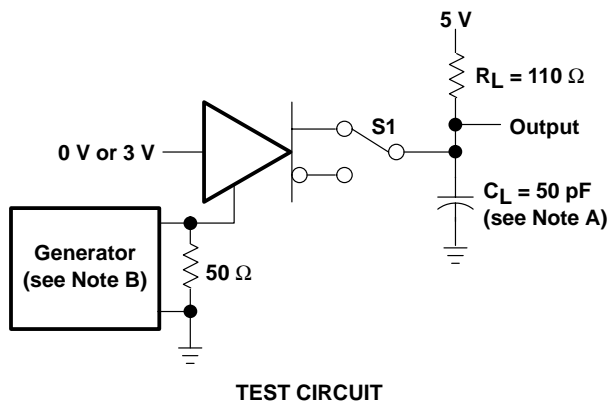
- NOTES: A. C_L includes probe and jig capacitance.
 B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_0 = 50 \Omega$.

Figure 3. Driver Test Circuit and Voltage Waveforms



- NOTES: A. C_L includes probe and jig capacitance.
 B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_0 = 50 \Omega$.

Figure 4. Driver Test Circuit and Voltage Waveforms



- NOTES: A. C_L includes probe and jig capacitance.
 B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_0 = 50 \Omega$.

Figure 5. Driver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

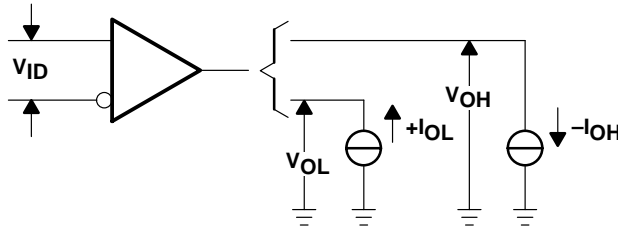
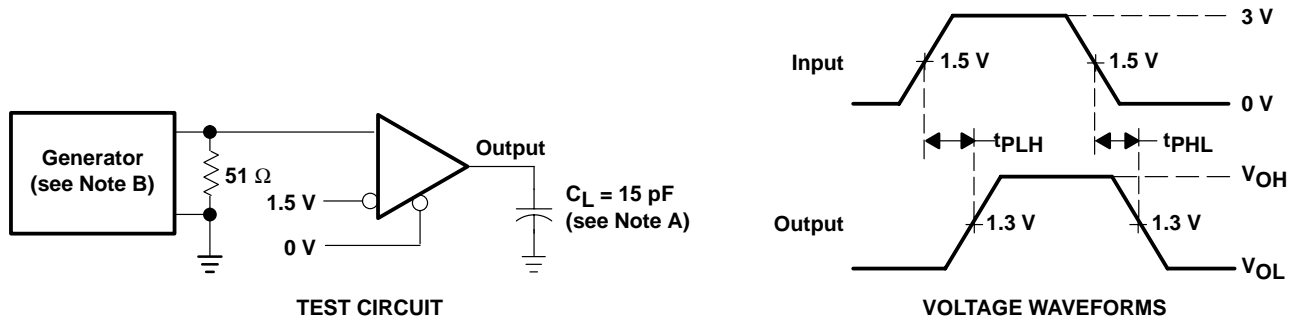


Figure 6. Receiver V_{OH} and V_{OL}



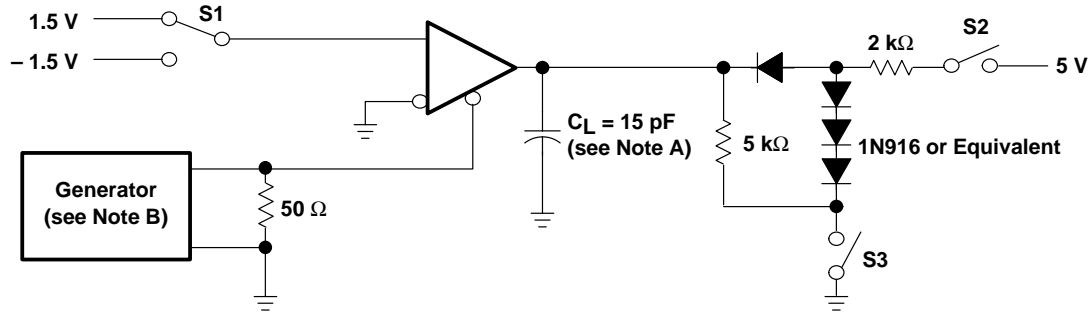
- NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1\text{ MHz}$, 50% duty cycle, $t_r \leq 6\text{ ns}$, $t_f \leq 6\text{ ns}$, $Z_O = 50\ \Omega$.

Figure 7. Receiver Test Circuit and Voltage Waveforms

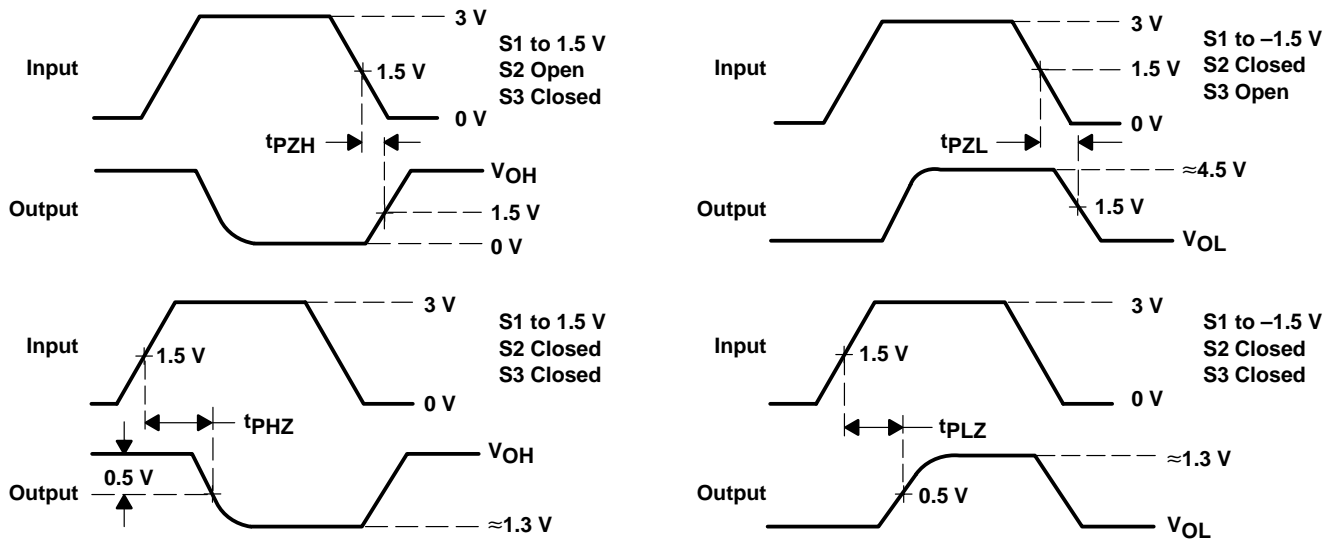
SN65ALS180, SN75ALS180 DIFFERENTIAL DRIVER AND RECEIVER PAIRS

SLLS052G – AUGUST 1987 – REVISED APRIL 2003

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

- NOTES: A. C_L includes probe and jig capacitance.
 B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1 \text{ MHz}$, 50% duty cycle, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$, $Z_O = 50 \Omega$.

Figure 8. Receiver Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS – DRIVERS

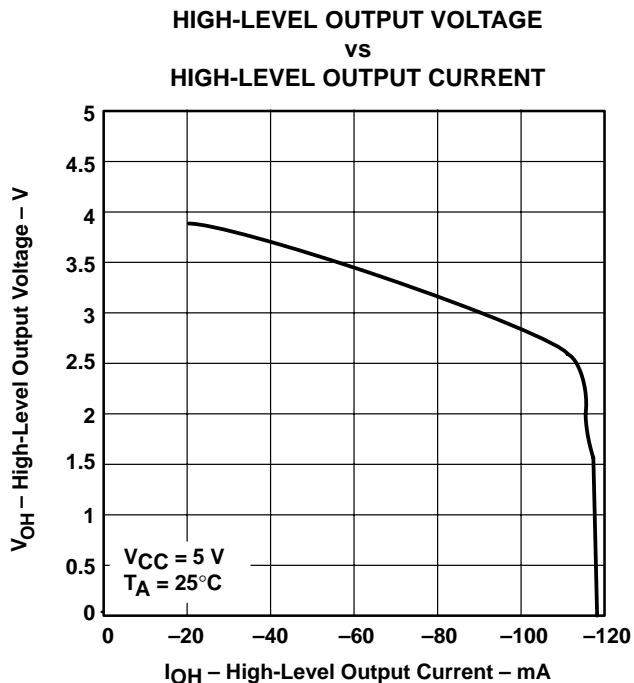


Figure 9

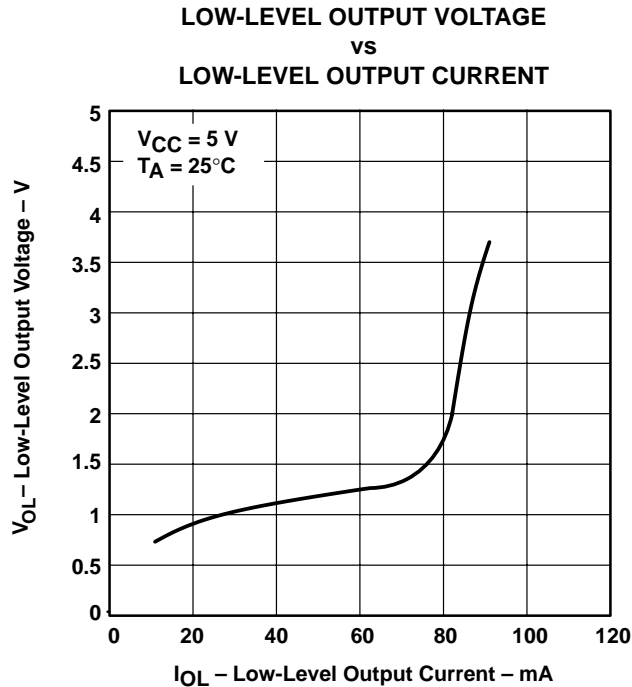


Figure 10

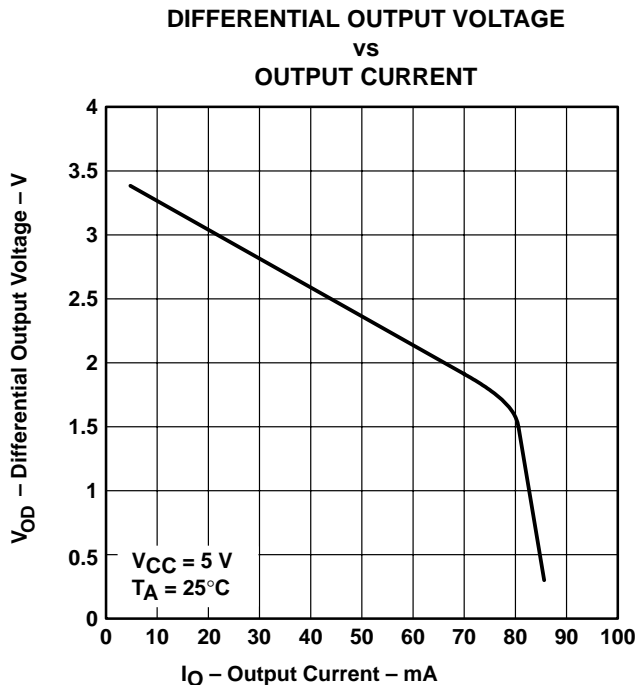


Figure 11

SN65ALS180, SN75ALS180 DIFFERENTIAL DRIVER AND RECEIVER PAIRS

SLLS052G – AUGUST 1987 – REVISED APRIL 2003

TYPICAL CHARACTERISTICS – RECEIVERS

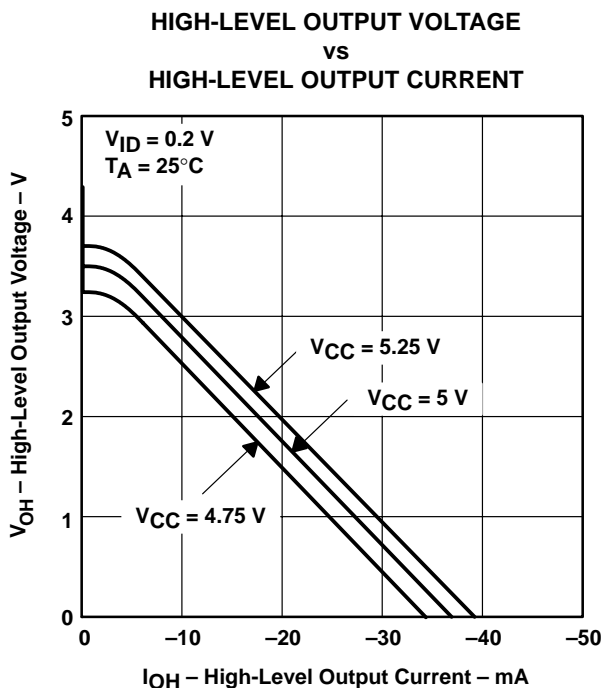


Figure 12

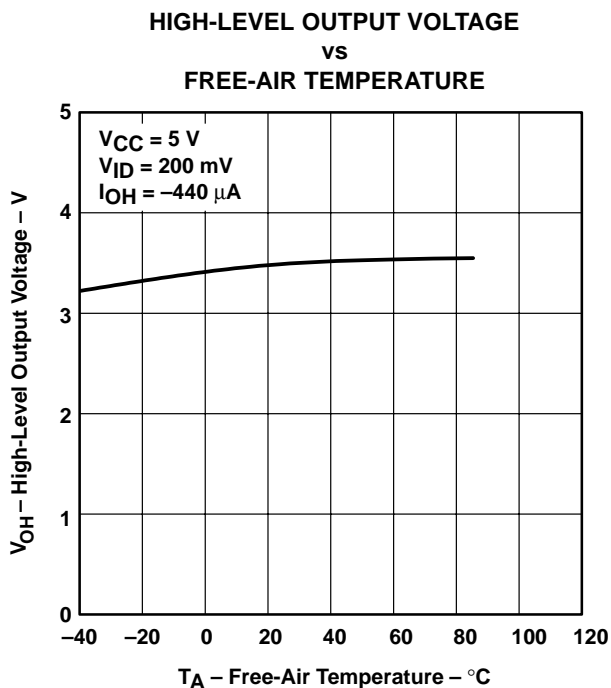


Figure 13

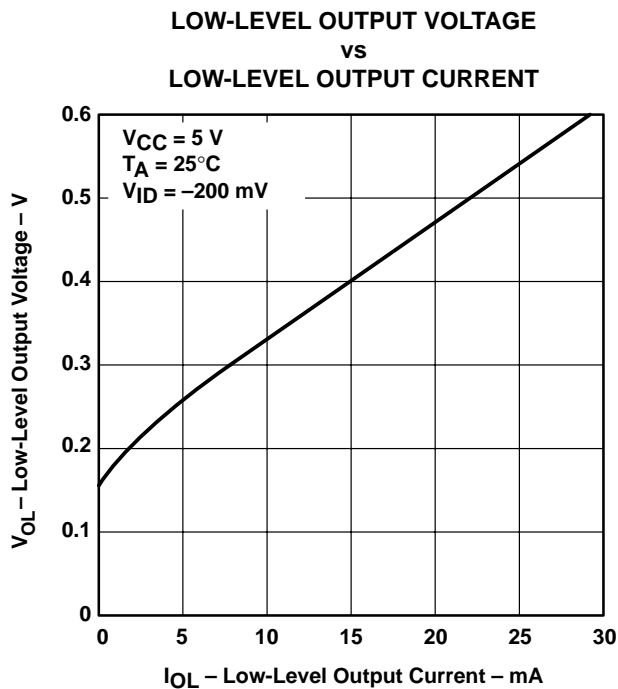


Figure 14

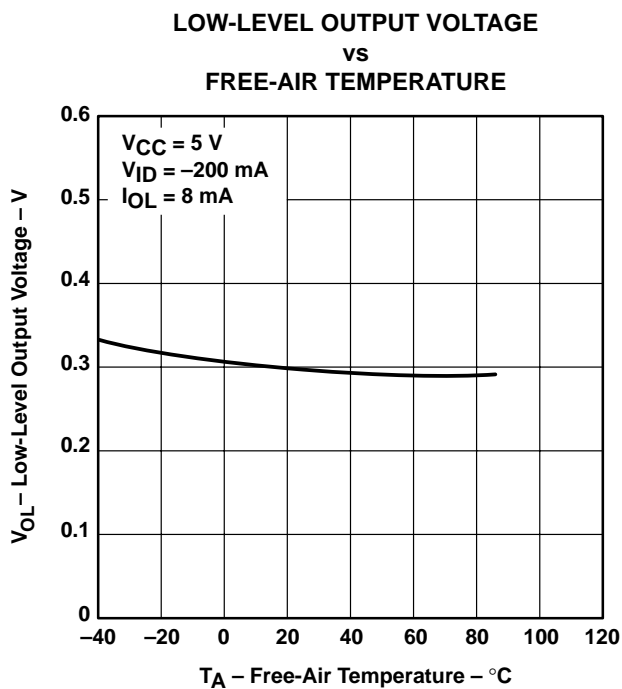


Figure 15



TYPICAL CHARACTERISTICS – RECEIVERS

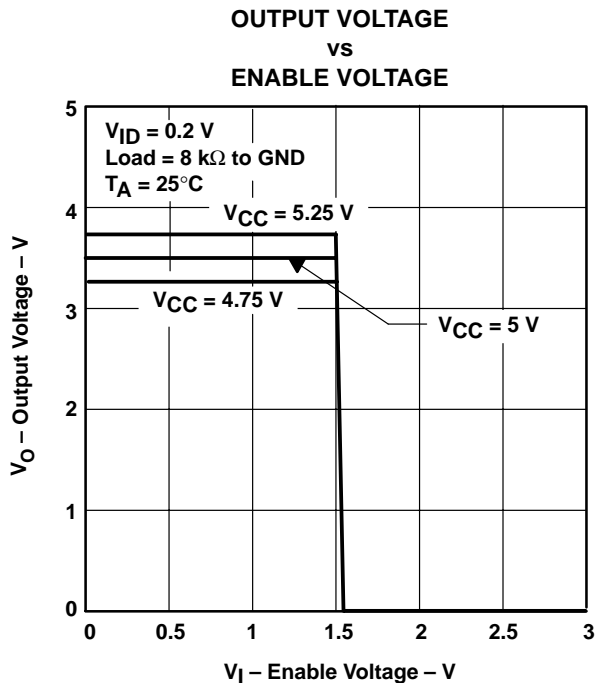


Figure 16

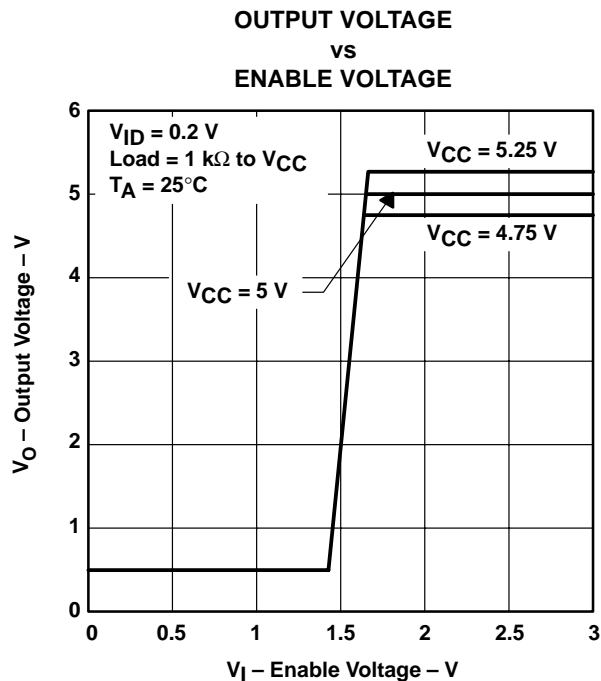
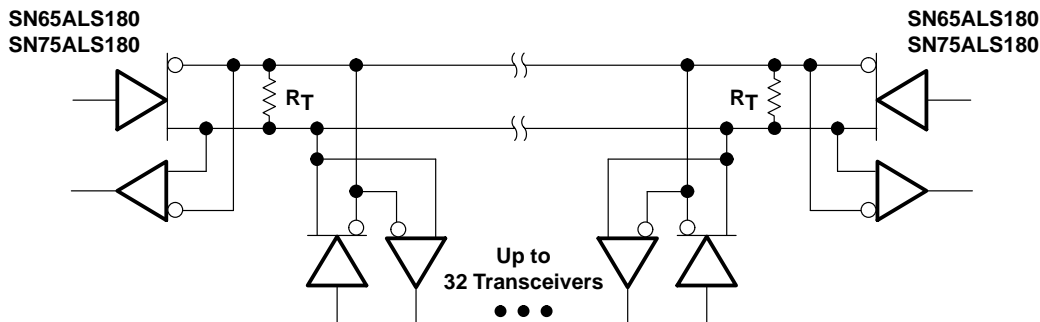


Figure 17

APPLICATION INFORMATION



NOTE A: The line should terminate at both ends in its characteristic impedance ($R_T = Z_0$). Stub lengths off the main line should be kept as short as possible.

Figure 18. Typical Application Circuit

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65ALS180D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	65ALS180	Samples
SN65ALS180DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	65ALS180	Samples
SN65ALS180DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	65ALS180	Samples
SN65ALS180DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	65ALS180	Samples
SN65ALS180N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	-40 to 85		
SN75ALS180D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS180	Samples
SN75ALS180DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS180	Samples
SN75ALS180DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS180	Samples
SN75ALS180DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS180	Samples
SN75ALS180DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS180	Samples
SN75ALS180N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75ALS180N	Samples
SN75ALS180NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75ALS180N	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65ALS180DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN75ALS180DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65ALS180DR	SOIC	D	14	2500	367.0	367.0	38.0
SN75ALS180DR	SOIC	D	14	2500	367.0	367.0	38.0

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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