PRODUCT INFORMATION LETTER

PIL AMS-APD/12/7659
Dated 27 Dec 2012

Production line extension within ST Ang Mo Kio (Singapore) for AMS Group products

Sales Type/product family label	See here attached
Type of change	Waferfab additional location
Reason for change	Production capacity increase
Description	Progressing on the activities related to JFet diffusion manufacturing processes, ST is glad to announce line extension, for AMS products produced in JFet process within the same ST plant Ang Mo Kio in Singapore.
Forecasted date of implementation	20-Dec-2012
Forecasted date of samples for customer	20-Dec-2012
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	20-Dec-2012
Involved ST facilities	ST Ang Mo Kio in Singapore

DOCUMENT APPROVAL

Name	Function
Camiolo, Jean	Marketing Manager
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Bugnard, Jean-Marc	Q.A. Manager

PRODUCT/PROCESS
CHANGE NOTIFICATION

PIL AMS-APD/12/7659

Analog, MEMS and Sensor Group

Line extension for JFET production in ST Singapore for AMS products

WHAT:

Progressing on the activities related to bipolar diffusion manufacturing processes, ST is glad to announce line extension, for AMS products produced in Jfet process.

Material	Current process JFET	Modified process JFET
Diffusion location	ST Singapore	ST Singapore
Building	AMK6	AMJ9
Facilities	No change	
Equipments type	No Change	
Material	No change	

For the complete list of the part numbers affected by the change, please refer to the attached Products list.

WHY:
To increase our production capacity for bipolar process in ST Singapore.

HOW:
The change that covers AMS products is already qualified through attached report.
Here below you'll find the details of qualification plan.

Qualification program and results:

The qualification program consists mainly of comparative electrical characterization and reliability tests. Please refer to Appendix 1 for all the details.

WHEN:
Production in ST Singapore AMJ9 for AMS is already started.

Marking and traceability:

Unless otherwise stated by customer specific requirement, the traceability of the parts assembled with the new material set will be ensured by new internal sales types.

The changes here reported will not affect the electrical, dimensional and thermal parameters keeping unchanged all information reported on the relevant datasheets.
There is as well no change in the packing process or in the standard delivery quantities.

Report ID 2012-W40 AMJ9

Reliability Report

AMJ9 JFET Technology Xfer Qualification

General Information	
Product Line	*006401, 008401*
Product Description	Low power JFET quad operational amplifier / General purpose JFET quad operational amplifiers
P/N	*TL064CDT / TL084CN*
Product Group	*AMS*
Product division	*Analog*
Package	*SO14 / DIP14*
Silicon Process technology	*JFET*
Production mask set rev.	*1*
Maturity level step	*from 10 to 30*

Locations	
Wafer fab	*AMJ9*
Assembly plant	*Bouskoura (SO14)* *LGG (DIP14)*
Reliability Lab	*Grenoble*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	03-Oct-2012	21	X. Gagnard	JM Bugnard	First issue

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
This report does not imply for STMicroelectronics expressly or implicitly any contractual obligations other than as set forth in STMicroelectronics general terms and conditions of Sale. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics.

TABLE OF CONTENTS

1 **APPLICABLE AND REFERENCE DOCUMENTS** **5**
2 **GLOSSARY** **5**
3 **RELIABILITY EVALUATION OVERVIEW** **5**
3.1 OBJECTIVES 5
3.2 CONCLUSION 5
4 **DEVICE CHARACTERISTICS** **6**
4.1 DEVICE DESCRIPTION 6
4.2 CONSTRUCTION NOTE 8
5 **TESTS RESULTS SUMMARY** **9**
5.1 TEST VEHICLE 9
5.2 TEST PLAN AND RESULTS SUMMARY 9
6 **ANNEXES** **10**
6.1 DEVICE DETAILS 10
6.2 TESTS DESCRIPTION 17
6.3 ESD CERTIFICATES 18
6.4 LU CERTIFICATES 20

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q100	Stress test qualification for automotive grade integrated circuits
AEC-Q101	Stress test qualification for automotive grade discrete semiconductors
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
PCB	Printed Circuit Board
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

The objective of this qualification is the transfer of the BIPOLAR/JFET technology in 6 inches, from AMK6 to AMJ9.
The transfer is based in a copy paste transfer of the equipments and the recipes.
In term of building the AMJ9 is located in the AMK5 building, but using the same informatics tracking systems than AMK6, the same facilities, and the same management of documentations & process control.
The qualification is using 2 tests vehicles in PRO and 2 tests vehicles in JFET. The qualification of AMJ9 is also based on 0431 product qualified by IPC/APM.
This report concerns only the JFET/BIPOLAR technology, the PRO/BIPOLAR being already qualified.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

COMPANY CONFIDENTIAL

4 DEVICE CHARACTERISTICS

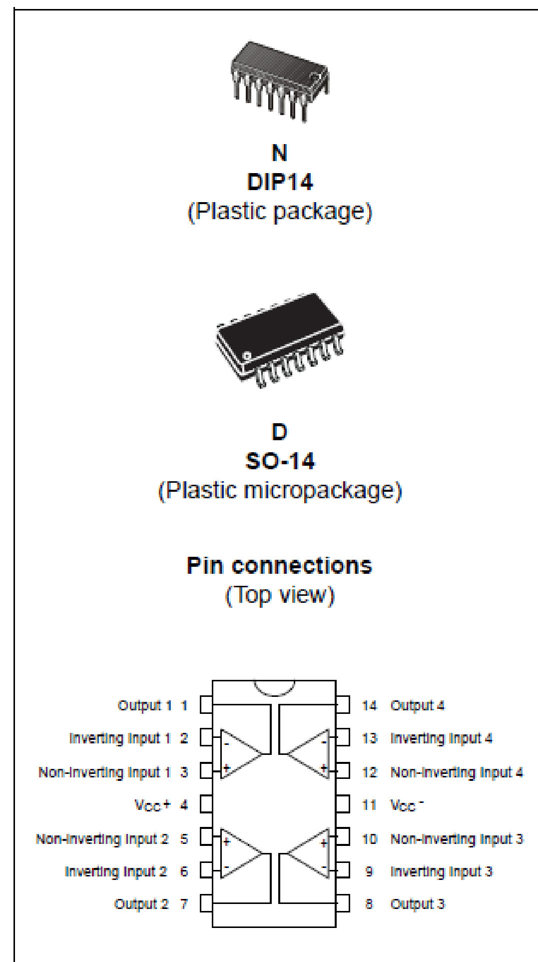
4.1 Device description

TL064

Low power JFET quad operational amplifier

Features

- Very low power consumption: 200 µA
- Wide common-mode (up to V_{CC}^{+}) and differential voltage ranges
- Low input bias and offset currents
- Output short-circuit protection
- High input impedance JFET input stage
- Internal frequency compensation
- Latch up free operation
- High slew rate: 3.5 V/µs



Description

The TL064, TL064A and TL064B are high-speed JFET input single operational amplifiers. Each of these JFET input operational amplifiers incorporates well matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit.

The devices feature high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient.

TL084

General purpose JFET quad operational amplifiers

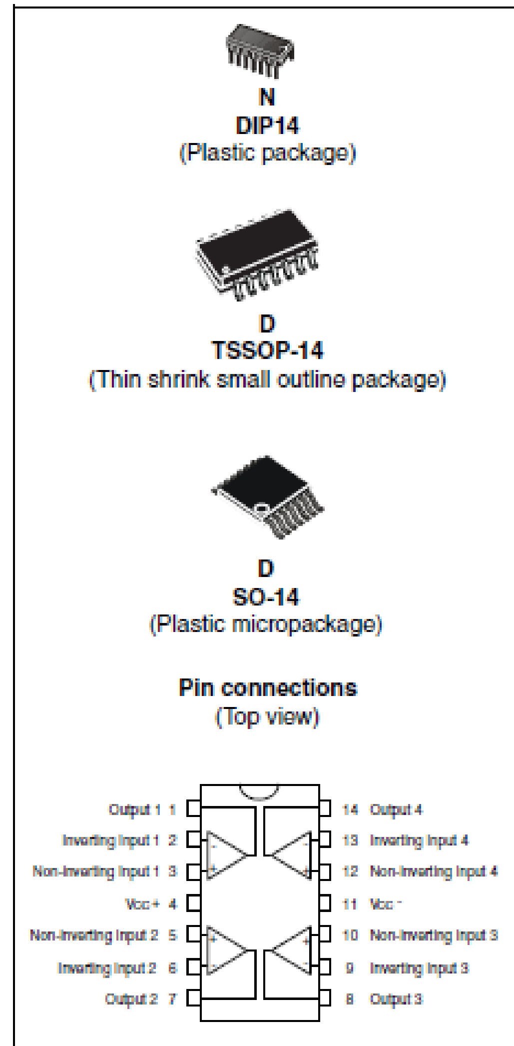
Features

- Wide common-mode (up to V_{CC}^{+}) and differential voltage range
- Low input bias and offset current
- Output short-circuit protection
- High input impedance JFET input stage
- Internal frequency compensation
- Latch up free operation
- High slew rate: 16 V/µs (typical)

Description

The TL084, TL084A and TL084B are high-speed JFET input quad operational amplifiers incorporating well matched, high voltage JFET and bipolar transistors in a monolithic integrated circuit.

The devices feature high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient.



4.2 Construction note

	Site AMJ9	
	P/N TL064CDT	**P/N TL084CN**
Wafer/Die fab. information		
Wafer fab manufacturing location	AMJ9	
Technology	JFET	
Process family	JFET421A	
Die finishing back side	Raw silicon	
Die size	2940 x 1520 µm²	2480 x 1460 µm²
Bond pad metallization layers	AlSiCu	
Passivation type	PVAPOX/SiN	
Poly silicon layers	NA	
Wafer Testing (EWS) information		
Electrical testing manufacturing location	Singapore	
Tester	AOT	Not yet defined
Test program	H0064CW.01	Not yet defined
Assembly information		
Assembly site	BSK	LGG
Package description	SO14	DIP14
Molding compound	EME-G700K	GR360A-ST
Frame material	Cu	Cu
Die attach process	Glue	Glue
Die attach material	8601S-25	8390S25
Die pad size	132 x 132 µm²	81 x 81 µm²
Wire bonding process	Wire	Wire
Wires bonding materials/diameters	Cu 1 mil	Cu 1 mil
Lead finishing process	Pre plated	Plating
Lead finishing/bump solder material	NiPdAu	Sn
Substrate supplier for BGA	NA	NA
Final testing information		
Testing location	BSK	LGG
Tester	ASL1000	ASL1000
Test program	T0064AF4	T0084AF5

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Diffusion Lot	Assy Lot	Trace Code	Process/ Package	Product Line	Comments
1	W212NK7	CA1221N140	CZ2250EU	SO14	006401	TL064CDT$DFWH
2	W129NTJ	0084QLAMJ9	G4145088	DIP14	008401	TL084CN$LIW
3						

Detailed results in below chapter will refer to P/N and Lot #.

5.2 Test plan and results summary

P/N TL064CDT (lot 1) & TL084CN (lot 2)

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS			Note
						Lot 1	Lot 2	Lot 3	
Die Oriented Tests									
HTB	N	JESD22 A-108	Tj = 125°C, BIAS 30V	158	168 H	0/78	0/80		
					1000 H		0/80		
HTSL	N	JESD22 A-103	Ta = 150°C	78	168 H				
					1000 H		0/78		
Package Oriented Tests									
PC		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Over Reflow @ Tpeak=260°C 3 times		Final		NA		
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121°C	158	96 H		0/158		(1)
					168 H				
TC	Y	JESD22 A-104	Ta = -65°C to 150°C	78	100 cy		0/78		
					1000 cy		0/78		
Env Seq	Y	no	Ta = -65°C to 150°C Then Pa=2Atm / Ta=121°C	78	100 cy		0/78		
					96h		0/78		(1)
THB	Y	JESD22 A-101	Ta = 85°C, RH = 85%, BIAS 30V	80	168 H		0/80		
					1000 H		0/80		
Other Tests									
ESD	N	JESD22-A114/A115 ANSI	HBM	3	In V	900	800		
			CDM	3	1500V	Pass	Pass		
			MM	3	In V	200	150		
LU	N	JESD78C	Current Inj. Overvoltage		±200mA	Pass	Pass		

Note (1): Still strong difficulties to test DIP after PPT, due to Sn oxidation and mechanism of contact of DIP socket. After cleaning, test is functional.

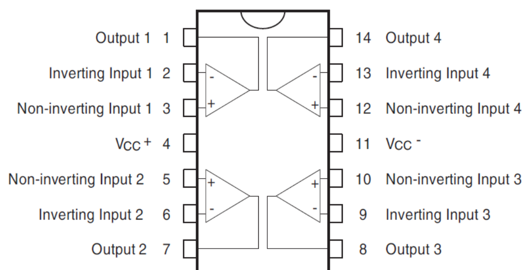
In case of rejects include a short description of the failure analysis and corrective actions.

6 ANNEXES

6.1 Device details

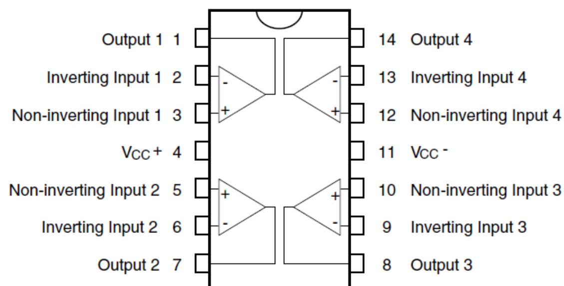
6.1.1 Pin connection

For SO14 package:



For DIP14 package:

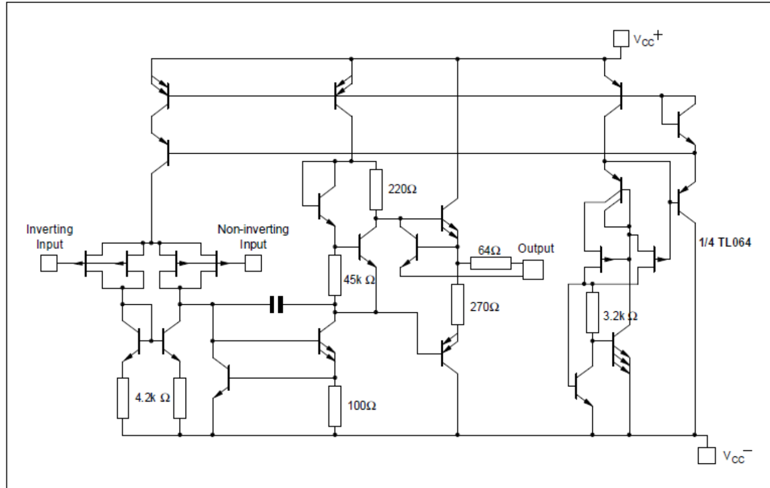
Pin connections
(Top view)



6.1.2 Block diagram

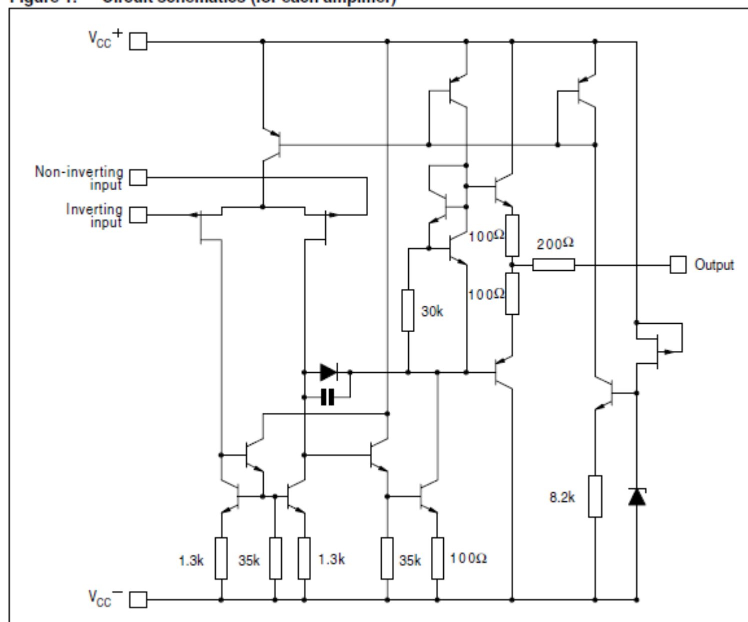
For TL064CDT product:

Figure 1. Circuit schematics



For TL084CN product:

Figure 1. Circuit schematics (for each amplifier)



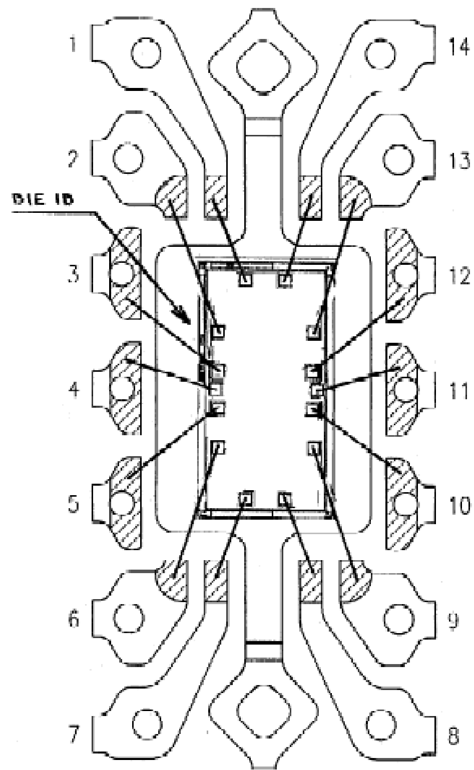
6.1.3 Bonding diagram

For SO14 package:

BONDING DIAGRAM FOR LINE : ØØ64 PACKAGE : K 7

FRAME PAD : .094 x .125 inch / 2,388 x 3,175 mm DIE SIZE : ______ inch

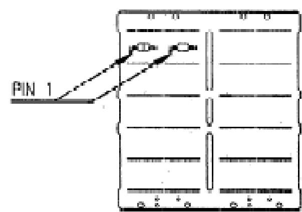
Dimensions in the bsa



BE CAREFUL

(JFET) BALL BONDING CONTROL REFER TO: 0032665/3thd OPTICAL SPEC.

PIN 1



SOP 14L MATRIX

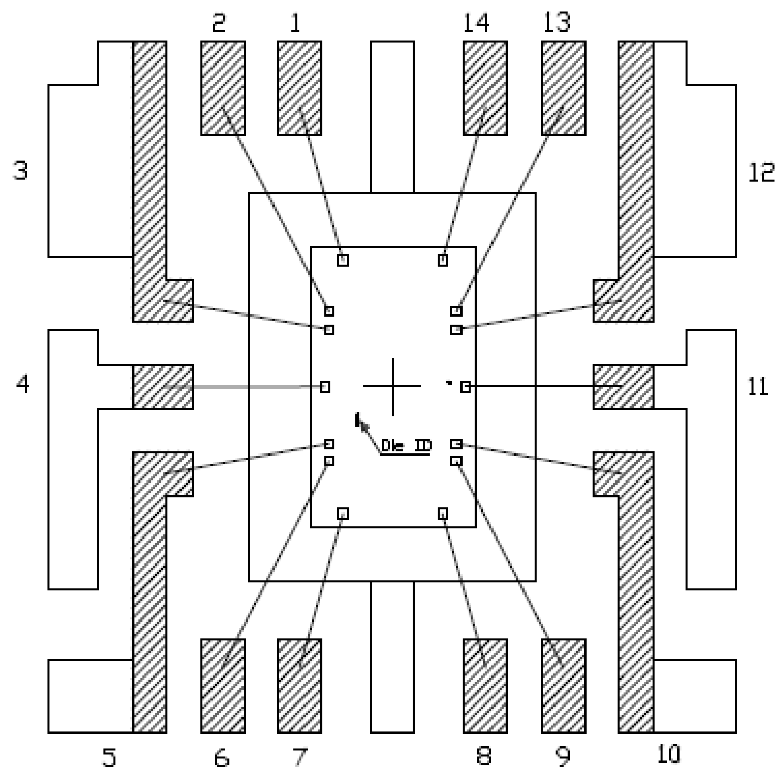
BLANK BOND. DIAG. REF. : 0100405

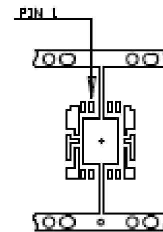
For DIP14 package:

BONDING DIAGRAM FOR LINE : 0084 PACKAGE : X 7

FRAME PAD : $\frac{.100 \times .135 \quad \text{Inch}}{2,540 \times 3,429 \quad \text{mm}}$

SCALE :

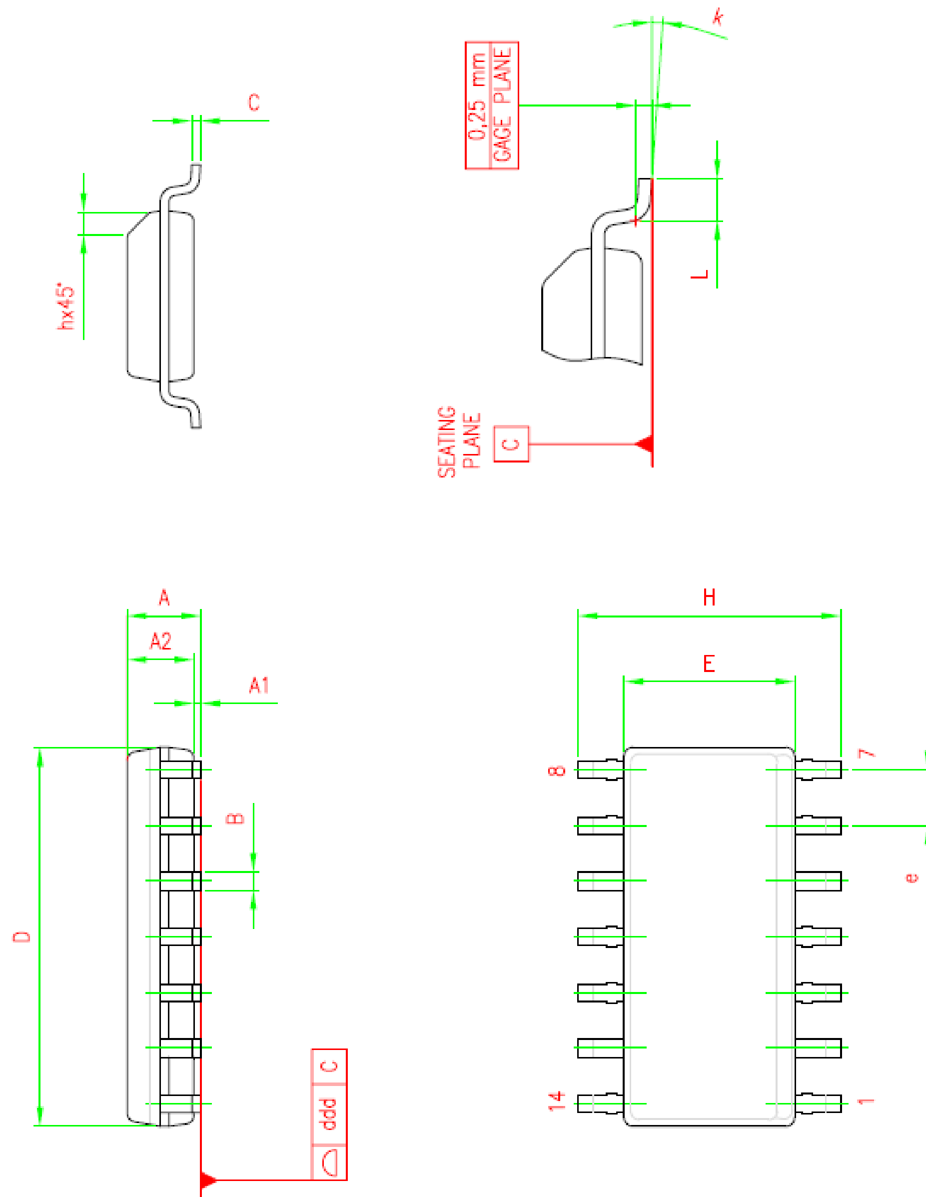




PDIP 14L

Package outline/Mechanical data

For SO14 package :



TITLE: PLASTIC SMALL OUTLINE PACKAGE 14L

PACKAGE CODE: K7

JEDEC/EIAJ REFERENCE NUMBER: JEDEC MS012-VARIATION AB

	DIMENSIONS						
	DATABOOK (mm)			DRAWING (mm)			
REF.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	NOTES
A	1.35		1.75			1.75	
A1	0.10		0.25	0.10	0.15	0.20	
A2	1.10		1.65	1.48	1.52	1.60	
B	0.33		0.51	0.35	0.40	0.455	
C	0.19		0.25	0.19	0.20	0.238	
D	8.55		8.75	8.60	8.65	8.70	(1)
E	3.80		4.00	3.80	3.90	4.00	
e		1.27			1.27		
H	5.80		6.20	5.90	6.00	6.10	
h	0.25		0.50	0.425		0.50	
L	0.40		1.27	0.50	0.635	0.685	
k	0		8	2	4	8	DEGREES
e		0.40			0.40		
ddd			0.10			0.04	

NOTES:

(1) – Dimension "D" does not include mold flash, protrusions or gate burrs.
Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.

(2) – Drawing dimensions include Single and Matrix versions.

For DIP14 package:

TITLE: PLASTIC DIP 14 LEADS STD

PACKAGE CODE: X7

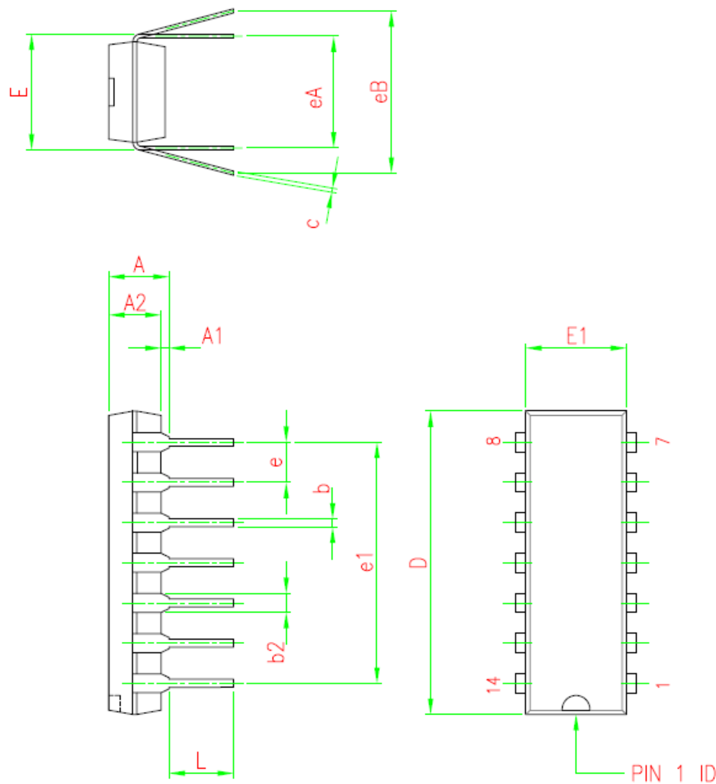
JEDEC/EIAJ REFERENCE NUMBER: JEDEC MS-001 VARIATION AA

	DIMENSIONS						
	DATABOOK (mm)			DRAWING (mm)			
REF.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	NOTES
A			5.33			5.10	
A1	0.38			0.51			
A2	2.92	3.30	4.95	3.18	3.30	3.43	
b	0.36	0.46	0.56	0.38	0.50	0.53	
b2	1.14	1.52	1.78	1.39		1.65	
c	0.20	0.25	0.36	0.20	0.25	0.30	
D	18.67	19.05	19.69	18.92	19.18	19.56	(1)
E	7.62	7.87	8.26		7.87		
E1	6.10	6.35	7.11	6.22	6.35	6.50	(1)
e		2.54		2.29	2.54	2.79	
e1		15.24		14.98	15.24	15.49	
eA		7.62		7.36	7.62	7.87	
eB			10.92	7.80	8.50	9.10	
L	2.92	3.30	3.81	3.00	3.30	3.70	

NOTES:

1- “D” AND “E1” DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTUSIONS. MOLD FLASH OR PROTUSIONS SHALL NOT EXCEED 0.25mm.

POA TITLE: PLASTIC DIP 14L STANDARD
PACKAGE CODE: X7



6.2 Tests Description

Test name	Description	Purpose
Die Oriented		
HTOL High Temperature Operating Life **HTB** High Temperature Bias	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
ELFR Early Life Failure Rate	The device is stressed in biased conditions at the max junction temperature.	To evaluate the defects inducing failure in early life.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
Other		
ESD Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. CBM: Charged Device Model HBM: Human Body Model MM: Machine Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.
LU Latch-Up	The device is submitted to a direct current forced/sunk into the input/output pins. Removing the direct current no change in the supply current must be observed.	To verify the presence of bulk parasitic effect inducing latch-up.

6.3 ESD certificates

ESD CERTIFICATE

According to ST 0061692

Date : 05/10/2012
Line : 008401
Raw Line : WLX7*0084BIW
Die code : P0084BIW
Traceability code: G4145088
Package(s) : DIP14
Laboratory Site : ST Grenoble / Catane (CDM)

■ **HBM (Human Body Model)**

Equipment reference: Zapmaster MK2- S/N: 0507277
Number of units: 3
This product meets the electrostatic discharge sensitivity specification of 1 KV and is compliant with :

- ☐ **MIL-883-H**
- ☐ **AEC_Q100-002D** ☐ **by pin group**
- ■ **JEDEC : JESD22-A114F** ■ **by pin group**

■ **MM (Machine Model)**

Equipment reference: Zapmaster MK2- 2 S/N: 0507277
Number of units: 3
This product meets the electrostatic discharge sensitivity specification of 150 V and is compliant with :

- ☐ **MIL-883-H**
- ☐ **AEC_Q100-003E** ☐ **by pin group**
- ■ **JEDEC : JESD22-A115A** ☐ **by pin group**

■ **CDM (Charged Device Model)**

Equipment reference: : ORION CDM Test System S/N: 200 23
Number of units: 3
This product meets the electrostatic discharge sensitivity specification of 1.5 KV and is compliant with :

- ☐ **MIL-883-H**
- ☐ **AEC_Q100-011B**
- ■ **ANSI /ESD STM5.3.1** ☐ **by pin group**

ESD CERTIFICATE

According to ST 0061692

Date : 05/10/2012
Line : 006401
Finished Good : TL064CDT$DFWH
Die code : P0064AFW
Traceability code: CZ2250EU
Package(s) : SO14
Laboratory Site : ST Grenoble / Catane (CDM)

■ **HBM (Human Body Model)**

Equipment reference: Zapmaster MK2- S/N: 0507277
Number of units: 3
This product meets the electrostatic discharge sensitivity specification of 900 V and is compliant with :

- ☐ **MIL-883-H**
- ☐ **AEC_Q100-002D** ☐ **by pin group**
- ■ **JEDEC : JESD22-A114F** ☐ **by pin group**

■ **MM (Machine Model)**

Equipment reference: Zapmaster MK2- 2 S/N: 0507277
Number of units: 3
This product meets the electrostatic discharge sensitivity specification of 200 V and is compliant with :

- ☐ **MIL-883-H**
- ☐ **AEC_Q100-003E** ☐ **by pin group**
- ■ **JEDEC : JESD22-A115A** ☐ **by pin group**

■ **CDM (Charged Device Model)**

Equipment reference: : ORION CDM Test System S/N: 200 23
Number of units: 3
This product meets the electrostatic discharge sensitivity specification of 1.5 KV and is compliant with :

- ☐ **MIL-883-H**
- ☐ **AEC_Q100-011B**
- ■ **ANSI /ESD STM5.3.1** ☐ **by pin group**

6.4 LU certificates

LATCH-UP CERTIFICATE

According to ST 0018695 & JEDEC JESD78C STANDARDS

Date : 05/10/2012
Line : 008401
Raw Line : WLX7*0084BIW
Die code : P0084BIW
Traceability code: G4145088
Package(s) : DIP14

Laboratory Site: Grenoble
Latch-up tester reference: MK2-2 S/N: 0507277
Latch-up testing classification: Class I

TEST CONDITIONS AND RESULTS

Current Injection						
Device	Sample N°	Pin numbers		Negative Current Injection	Positive Current Injection	**Class**
WLX7*0084 BIW	1-6	INPUTS	2-3-5-6	-200 mA	+ 200 mA	**A+**
			9-10-12-13	-200 mA	+ 200 mA	**A+**
		OUTPUTS	1-7-8-14	-200 mA	+ 200 mA	**A+**

Supply Overvoltage					
Device	Sample N°	Pin numbers		Overvoltage Test	**Class**
WLX7*0084BIW	1-6	SUPPLY	4	36V	**A**

REFERENCE LEVELS

Test type	Trigger polarity	Quality Level	Trigger stress
Current injection	Positive	A+	+200 mA
		A	+100 mA
	Negative	A+	-200 mA
		A	-100 mA
Supply Overvoltage		A	1.5*Vmax

Class I	Latchup tested at room temperature.

LATCH-UP CERTIFICATE

According to ST 0018695 & JEDEC JESD78C STANDARDS

Date : 05/10/2012
Line : 006401
Finished Good : TL064CDT$DFWH
Die code : P0064AFW
Traceability code: CZ2250EU
Package(s) : SO14

Laboratory Site: Grenoble
Latch-up tester reference: MK2-2 S/N: 0507277
Latch-up testing classification: Class I

TEST CONDITIONS AND RESULTS

Current Injection						
Device	Sample N°	Pin numbers		Negative Current Injection	Positive Current Injection	**Class**
TL064CDT $DFWH	1-6	INPUTS	2-3-5-6	-200 mA	+ 200 mA	**A+**
			9-10-12-13	-200 mA	+ 200 mA	**A+**
		OUTPUTS	1-7-8-14	-200 mA	+ 200 mA	**A+**

Supply Overvoltage					
Device	Sample N°	Pin numbers		Overvoltage Test	**Class**
TL064CDT$DFWH	1-6	SUPPLY	4	36V	**A**

REFERENCE LEVELS

Test type	Trigger polarity	Quality Level	Trigger stress
Current injection	Positive	A+	+200 mA
		A	+100 mA
	Negative	A+	-200 mA
		A	-100 mA
Supply Overvoltage		A	1.5*Vmax

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