Bidirectional PolyPhase Synchronous Buck or Boost Controller

FEATURES

- **Unique Architecture Allows Dynamic Regulation of Input Voltage, Output Voltage or Current**
- **V_{HIGH} Voltages Up to 100V**
- **V_{LOW} Voltages Up to 30V**
- **Synchronous Rectification: Up to 97% Efficiency**
- **ADI-Proprietary Advanced Current Mode Control**
- **±1% Voltage Regulation Accuracy Over Temperature**
- **Accurate, Programmable Output Current Monitoring and Regulation for Both Buck and Boost Operation**
- **Selectable Buck and Boost Current Sense Limits**
- Programmable DRV_{CC}/$EXTV_{CC}$ Optimizes Efficiency
- Programmable V_{HIGH} UV and OV Thresholds
- Programmable V_{LOW} OV Threshold
- Phase-Lockable Frequency: 60kHz to 460kHz
- Multiphase/Multi-ICs Operation Up to 12 Phases
- Selectable CCM/DCM Modes
- Thermally Enhanced 48-Lead LQFP Package
- AEC-Q100 Qualified for Automotive Applications

APPLICATIONS

- Automotive 48V/12V Dual Battery Systems
- Backup Power Systems

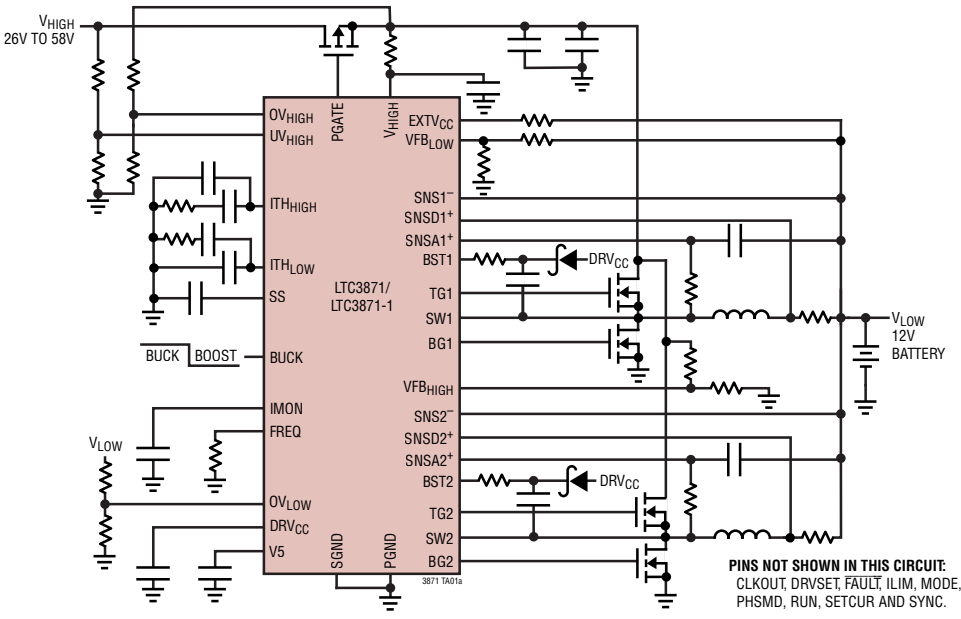
DESCRIPTION

The LTC®3871/LTC3871-1 is a high performance bidirectional buck or boost switching regulator controller that operates in either buck or boost mode on demand. It regulates in buck mode from V_{HIGH}-to-V_{LOW} and boost mode from V_{LOW}-to-V_{HIGH} depending on a control signal, making it ideal for 48V/12V automotive dual battery systems. An accurate current programming loop regulates the maximum current that can be delivered in either direction. The LTC3871/LTC3871-1 allows both batteries to supply energy to the load simultaneously by converting energy from one battery to the other.

Its proprietary constant-frequency current mode architecture enhances the signal-to-noise ratio enabling low noise operation and provides excellent current matching between phases. Additional features include discontinuous or continuous mode of operation, OV/UV monitors, independent loop compensation for buck and boost operation, accurate output current monitoring and overcurrent protection. The LTC3871 and LTC3871-1 have different current limit foldback characteristics.

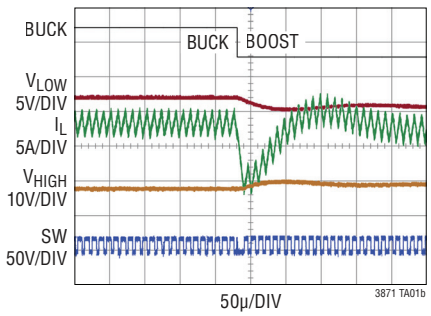
TYPICAL APPLICATION

High Efficiency Bidirectional Charger/Power Supply



PINS NOT SHOWN IN THIS CIRCUIT: CLKOUT, DRVSET, $\overline{FAULT}$, ILIM, MODE, PHSMD, RUN, SETCUR AND SYNC.

Buck-to-Boost Transition



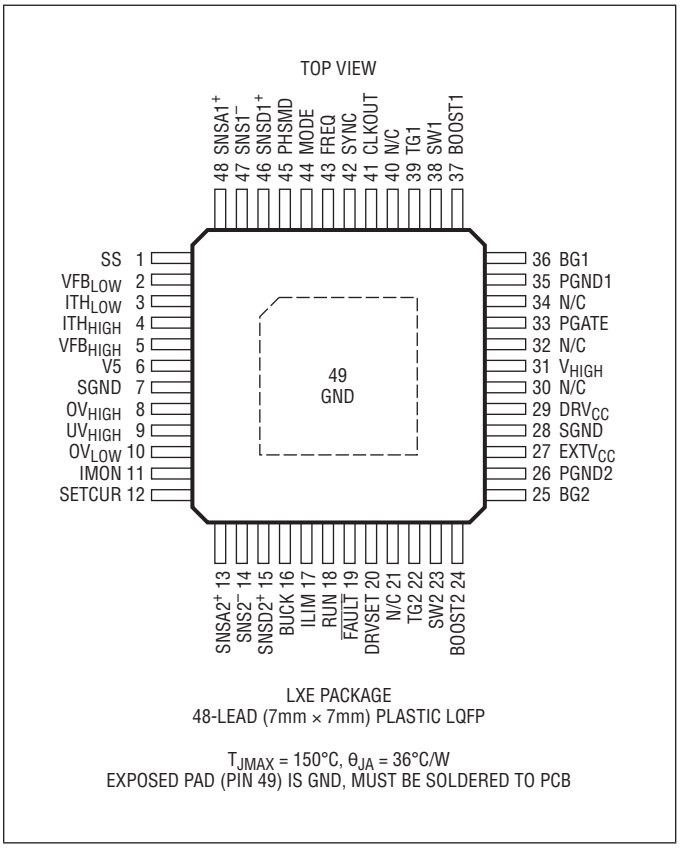
Rev. C

ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{HIGH} ..... –0.3V to 100V
Top Side Driver Voltages
(BOOST1, BOOST2) ..... –0.3V to 111V
Switch Voltage (SW1, SW2) ..... –5V to 100V
Current Sense Voltages
($SNSA^+$, SNS^-, $SNSD^+$ Channels 1 and 2) ... –0.3V to 34V,
–2V to 34V for < 100µsec
(BOOST1-SW1), (BOOST2-SW2) ..... –0.3V to 11V
$EXTV_{CC}$ ..... –0.3V to 34V,
–0.8V to 34V for < 100µsec
DRV_{CC} ..... –0.3V to 11V
VFB_{HIGH}, VFB_{LOW} ..... –0.3V to V5
MODE, SS Voltages..... –0.3V to V5
RUN ..... –0.3V to 6V
$\overline{FAULT}$, SETCUR, Voltages ..... –0.3V to V5
ILIM, DRVSET, BUCK Voltages ..... –0.3V to V5
OV_{HIGH}, UV_{HIGH}, OV_{LOW} Voltages..... –0.3V to 6V
SYNC, PHSMD Voltages ..... –0.3V to V5
Operating Junction Temperature
Range (Notes 2, 3)..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
$DRV_{CC}/EXTV_{CC}$ Peak Current.....100mA

PIN CONFIGURATION



LXE PACKAGE
48-LEAD (7mm × 7mm) PLASTIC LQFP

T_{JMAX} = 150°C, θ_{JA} = 36°C/W
EXPOSED PAD (PIN 49) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3871ELXE#PBF	LTC3871	48-Lead (7mm × 7mm) Plastic LQFP	–40°C to 125°C
LTC3871ILXE#PBF	LTC3871	48-Lead (7mm × 7mm) Plastic LQFP	–40°C to 125°C
LTC3871HLXE#PBF	LTC3871	48-Lead (7mm × 7mm) Plastic LQFP	–40°C to 150°C
LTC3871ELXE-1#PBF	LTC3871-1	48-Lead (7mm × 7mm) Plastic LQFP	–40°C to 125°C
LTC3871ILXE-1#PBF	LTC3871-1	48-Lead (7mm × 7mm) Plastic LQFP	–40°C to 125°C
LTC3871HLXE-1#PBF	LTC3871-1	48-Lead (7mm × 7mm) Plastic LQFP	–40°C to 150°C
AUTOMOTIVE PRODUCTS**			
LTC3871ILXE#WPBF	LTC3871	48-Lead (7mm × 7mm) Plastic LQFP	–40°C to 125°C
LTC3871HLXE#WPBF	LTC3871	48-Lead (7mm × 7mm) Plastic LQFP	–40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C, V_{HIGH} = 50V, V_{RUN} = 5V unless otherwise noted (Note 2).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{HIGH}	V_{HIGH} Supply Voltage Range			5		100	V
V_{LOW}	V_{LOW} Supply Voltage Range	V_{HIGH} > 5V		1.2		30	V
	V_{LOW} Regulated Feedback Voltage	(Note 4); ITH_{LOW} Voltage = 1.5V	●	1.188	1.200	1.212	V
	V_{HIGH} Regulated Feedback Voltage	(Note 4); ITH_{HIGH} Voltage = 0.5V	●	1.185	1.200	1.215	V
	V_{LOW} EA Feedback Current	(Note 4)			–115	–200	nA
	V_{HIGH} EA Feedback Current	(Note 4)			–115	–200	nA
	Reference Voltage Line Regulation	(Note 4); V_{HIGH} = 7V to 80V			0.02	0.2	%
	V_{LOW}/V_{HIGH} Voltage Load Regulation	Measured in Servo Loop; ΔI_{TH} Voltage = 1V to 1.5V			0.01	0.2	%
		Measured in Servo Loop; ΔI_{TH} Voltage = 1V to 0.5V			–0.01	–0.2	%
$g_{m\text{-}buck}$	Transconductance Amplifier $g_{m\text{-}buck}$	(Note 4); ITH_{LOW} = 1.5V; Sink/Source 5µA			2		mmho
$g_{m\text{-}boost}$	Transconductance Amplifier $g_{m\text{-}boost}$	(Note 4); ITH_{HIGH}= 0.5V; Sink/Source 5µA			1		mmho
I_Q	V_{HIGH} DC Supply Current	(Note 5)			8	14	mA
	Shutdown (V_{HIGH})	V_{RUN} = 0V; V_{HIGH} = 50V			140		µA
	Undervoltage Lockout	V5 Ramping Down		3.7	4.15	4.5	V
	Undervoltage Hysteresis				0.5		V
	RUN Pin On Threshold	V_{RUN} Rising		1.1	1.22	1.35	V
	RUN Pin On Hysteresis				80		mV
	RUN Pin Source Current	V_{RUN} < 1.2	●	1	2		µA
	RUN Pin Source Current	V_{RUN} > 1.3	●	3	6.5		µA
I_{SS}	Soft-Start Charging Current	V_{SS} = 1.2V		0.9	1.25	1.7	µA
$I_{SNSA^+\,1,2}$	Current Sensing Pins Current				0.1	±1	µA
$I_{SNSD^+\,1,2}$	Current Sensing Pins Current				0.01	±1	µA
$I_{SNS^-\,1,2}$	Current Sensing Pins Current				1.5		mA
	Total DC Sense Signal Gain	DCR Configuration			5		V/V
	ILIM Pin Input Resistance				100		kΩ
I_{SETCUR}	Current to Program Initial Current Limit		●	6.75	7.5	8.25	µA
	IMON Current Proportional to V_{LOW} at Max Current	V_{ILIM} = Float; R_{SENSE} = 3mΩ				±10	%
	IMON Zero Current Voltage		●	1.125	1.25	1.375	V
	Sense Pin to IMON Gain	V_{ILIM} = 0V, 1/4 V_{V5}, Float			38		V/V
		V_{ILIM} = 3/4 V_{V5}, V_{V5}			19		V/V
	TG Pull-Up On-Resistance				5		Ω
	TG Pull-Down On-Resistance				2.5		Ω
	BG Driver Pull-Up On-Resistance				5		Ω
	BG Driver Pull-Down On-Resistance				2.5		Ω
	Total DC Sense Signal Gain	R_{SENSE} Configuration			4		V/V
	Maximum Duty Cycle	Buck Mode Boost Mode		96	98 92		% %

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C, V_{HIGH} = 50V, V_{RUN} = 5V unless otherwise noted (Note 2).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{SENSE(MAX)}$ (DCR Sensing)	Maximum Current Sense Threshold (Buck and Boost Mode)	0°C to 150°C					
		V_{ILIM} = 0V	●	8	10	14.5	mV
		V_{ILIM} = 1/4 V_{V5}	●	17	20	24	mV
		V_{ILIM} = Float	●	26.5	30	33.5	mV
		V_{ILIM} = 3/4 V_{V5}	●	36	40	44.5	mV
		V_{ILIM} = V_{V5} (LTC3871)	●	44.5	50	55.5	mV
		V_{ILIM} = V_{V5} (LTC3871-1)	●	44.5	50	58.5	mV
$V_{SENSE(MAX)}$ (R_{SENSE} Sensing)	Maximum Current Sense Threshold (Buck and Boost Mode)	0°C to 150°C					
		V_{ILIM} = 0V	●	10	12.5	18.2	mV
		V_{ILIM} = 1/4 V_{V5}	●	21.3	25	30	mV
		V_{ILIM} = Float	●	33.2	37.5	41.9	mV
		V_{ILIM} = 3/4 V_{V5}	●	45	50	55.6	mV
		V_{ILIM} = V_{V5} (LTC3871)	●	55.6	62.5	69.4	mV
		V_{ILIM} = V_{V5} (LTC3871-1)	●	55.6	62.5	73.1	mV
$V_{SENSE(MAX)}$ (DCR Sensing)	Maximum Current Sense Threshold (Buck and Boost Mode)	–40°C to 150°C					
		V_{ILIM} = 0V	●	7	10	14.5	mV
		V_{ILIM} = 1/4 V_{V5}	●	16	20	24	mV
		V_{ILIM} = Float	●	26	30	33.5	mV
		V_{ILIM} = 3/4 V_{V5}	●	35	40	44.5	mV
		V_{ILIM} = V_{V5} (LTC3871)	●	42	50	55.5	mV
		V_{ILIM} = V_{V5} (LTC3871-1)	●	42	50	58.5	mV
$V_{SENSE(MAX)}$ (R_{SENSE} Sensing)	Maximum Current Sense Threshold (Buck and Boost Mode)	–40°C to 150°C					
		V_{ILIM} = 0V	●	8.8	12.5	18.2	mV
		V_{ILIM} = 1/4 V_{V5}	●	20	25	30	mV
		V_{ILIM} = Float	●	32.5	37.5	41.9	mV
		V_{ILIM} = 3/4 V_{V5}	●	43.8	50	55.6	mV
		V_{ILIM} = V_{V5} (LTC3871)	●	52.5	62.5	69.4	mV
		V_{ILIM} = V_{V5} (LTC3871-1)	●	52.5	62.5	73.1	mV
TG t_r TG t_f	Top Gate Rise Time Top Gate Fall Time	(Note 6)			60		ns
BG t_r BG t_f	Bottom Gate Rise Time Bottom Gate Fall Time	(Note 6)			60		ns
	Top Gate Off to Bottom Gate On Delay Synchronous Switch-On Delay Time	(Note 6) C_{LOAD} = 3300pF Each Driver			60		ns
	Bottom Gate Off to Top Gate On Delay Top Switch-On Delay Time	(Note 6) C_{LOAD} = 3300pF Each Driver			60		ns
	V5 Regulation Voltage	6V < V_{DRVCC} < 10V		5.3	5.5	5.7	V
	V5 Load Regulation	I_{V5} = 0mA to 20mA			0.5	1	%
V_{DRVCC}	DRV_{CC} Regulation Voltage	12V < V_{EXTVCC} < 30V, V_{DRVSET} = V_{V5}		9.5	10	10.5	V
		12V < V_{EXTVCC} < 30V, V_{DRVSET} = 3/4 V_{V5}		8.5	9	9.5	V
		12V < V_{EXTVCC} < 30V, V_{DRVSET} = Float		7.5	8	8.5	V
		12V < V_{EXTVCC} < 30V, V_{DRVSET} = 1/4 V_{V5}		6.5	7	7.5	V
		12V < V_{EXTVCC} < 30V, V_{DRVSET} = 0V		5.5	6	6.5	V
	DRV_{CC} Load Regulation	I_{CC} = 0mA to 20mA, V_{EXTVCC} = 10V			0.2	1	%
V_{EXTVCC}	$EXTV_{CC}$ Switchover Voltage	$EXTV_{CC}$ Ramping Positive			DRV_{CC} –0.5V		V
	$EXTV_{CC}$ Hysteresis				10		%
CLKOUT Phasing	Phase Relative to Channel 1	V_{PHSMD} = 0V			60		Deg
		V_{PHSMD} = 1/4 V_{V5}			60		Deg
		V_{PHSMD} = Float			90		Deg
		V_{PHSMD} = 3/4 V_{V5}			45		Deg
		V_{PHSMD} = V_{V5}			240		Deg

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C, V_{HIGH} = 50V, V_{RUN} = 5V unless otherwise noted (Note 2).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SYNC Phasing	Phase Relative to Channel 1	V_{PHSMD} = 0V			0		Deg
		V_{PHSMD} = 1/4 V_{V5}			90		Deg
		V_{PHSMD} = Float			0		Deg
		V_{PHSMD} = 3/4 V_{V5}			0		Deg
		V_{PHSMD} = V_{V5}			0		Deg
Channel to Channel Phasing	Channel 1 to Channel 2	V_{PHSMD} = 0V			180		Deg
		V_{PHSMD} = 1/4 V_{V5}			180		Deg
		V_{PHSMD} = Float			180		Deg
		V_{PHSMD} = 3/4 V_{V5}			180		Deg
		V_{PHSMD} = V_{V5}			120		Deg
$CLKOUT_{HI}$	Clock Output High Voltage	I_{LOAD} = 0.5mA		5.2	5.5		V
$CLKOUT_{LO}$	Clock Output Low Voltage	I_{LOAD} = –0.5mA			0	0.2	V
V_{SYNC}	Sync Input Threshold	V_{SYNC} Rising		2			V
		V_{SYNC} Falling				1.2	V
	Nominal Frequency	R_{FREQ} = 51.1kΩ		180	200	220	kHz
f_{LOW}	Low Fixed Frequency	R_{FREQ} = ≤20kΩ		40	50	60	kHz
f_{HIGH}	High Fixed Frequency	R_{FREQ} = 117kΩ		450	500	550	kHz
	Synchronizable Frequency	SYNC = External Clock	●	60		460	kHz
	SYNC Input Resistance				100		kΩ
I_{FREQ}	Frequency Setting Current		●	18	20	22	µA
	$\overline{FAULT}$ Voltage Low	$I_{\overline{FAULT}}$ = 2mA			0.1	0.3	V
	$\overline{FAULT}$ Leakage Current	$V_{\overline{FAULT}}$ = 5.5V				±1	µA
	$\overline{FAULT}$ Delay	Going Low			125		µs
	V_{LOW} OV Comparator Threshold			1.15	1.2	1.25	V
	V_{LOW} OV Comparator Hysteresis	V_{OVLOW} > 1.2V			5		µA
	V_{HIGH} OV Comparator Threshold			1.15	1.2	1.25	V
	V_{HIGH} OV Comparator Hysteresis	V_{OVHIGH} > 1.2V			5		µA
	V_{HIGH} UV Comparator Threshold			1.15	1.2	1.25	V
	V_{HIGH} UV Comparator Hysteresis	V_{UVHIGH} < 1.2V			5		µA
	BUCK Pin Pull-Up Resistance	BUCK Pin to V5			200		kΩ

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Ratings for extended periods may affect device reliability and lifetime.

Note 2: The LTC3871/LTC3871-1 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3871/LTC3871-1E is guaranteed to meet performance specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3875I is guaranteed over the –40°C to 125°C operating junction temperature range. The LTC3871/LTC3871-1H is guaranteed over the full –40°C to 150°C operating junction temperature range. High junction temperature degrades operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula: $T_J = T_A + (P_D \bullet 36°C/W)$.

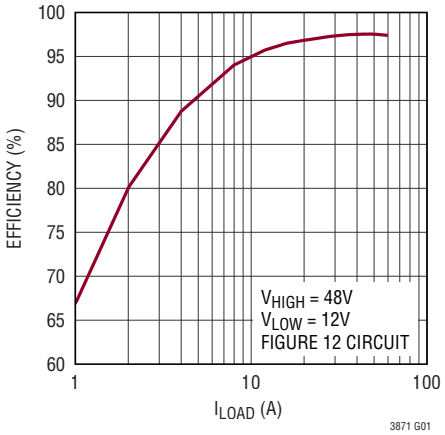
Note 4: The LTC3871/LTC3871-1 is tested in a feedback loop that servos $V_{ITHHIGH}$ and V_{ITHLOW} to a specified voltage and measures the resultant V_{FBHIGH} and V_{FBLOW}, respectively.

Note 5: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications Information.

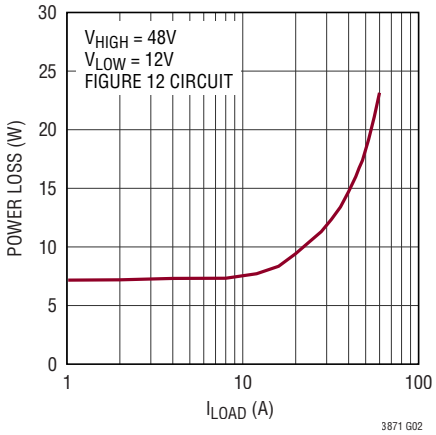
Note 6: Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

TYPICAL PERFORMANCE CHARACTERISTICS

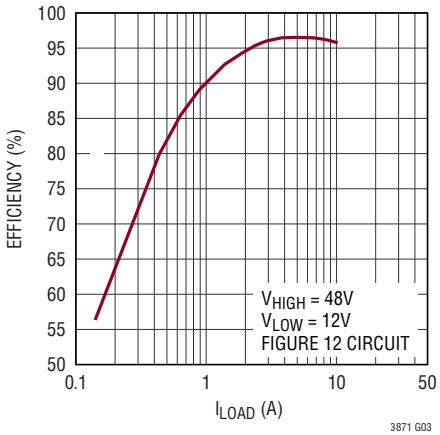
Efficiency Buck Mode



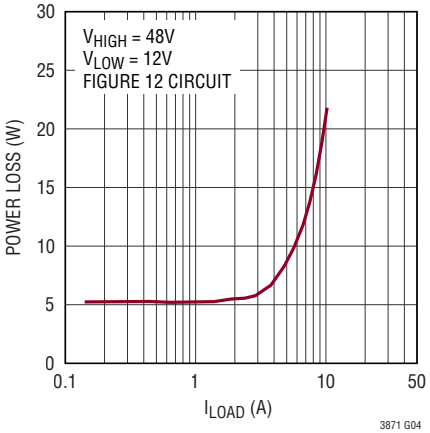
Power Loss Buck Mode



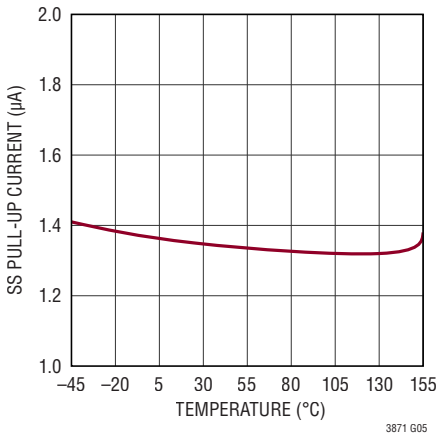
Efficiency Boost Mode



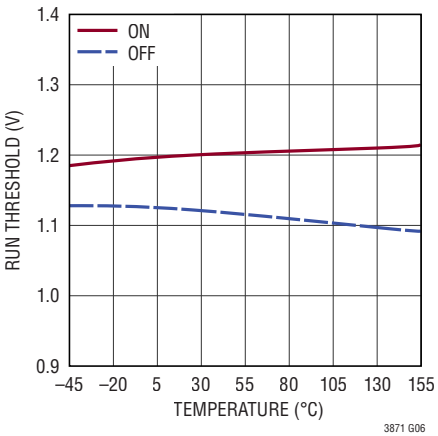
Power Loss Boost Mode



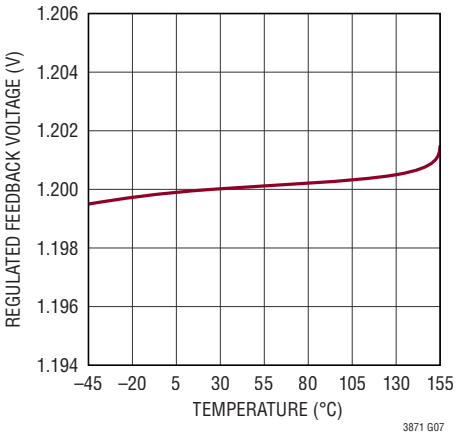
SS Pull-Up Current vs Temperature



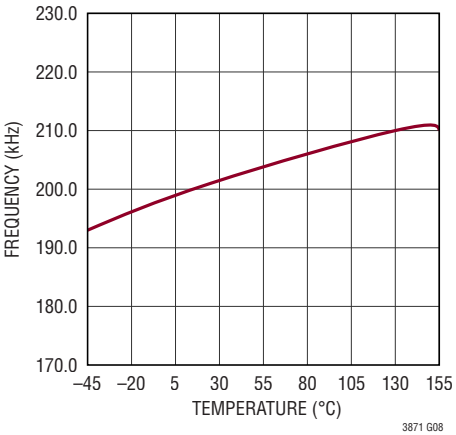
RUN Threshold vs Temperature



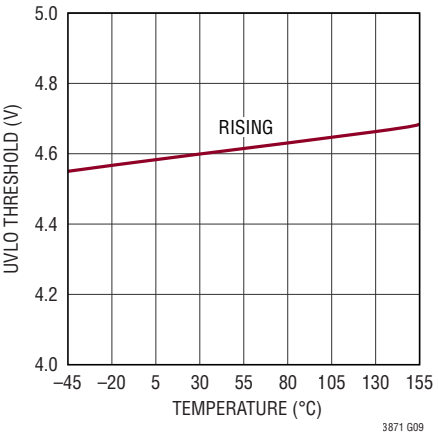
Regulated Feedback Voltage vs Temperature



Oscillator Frequency vs Temperature



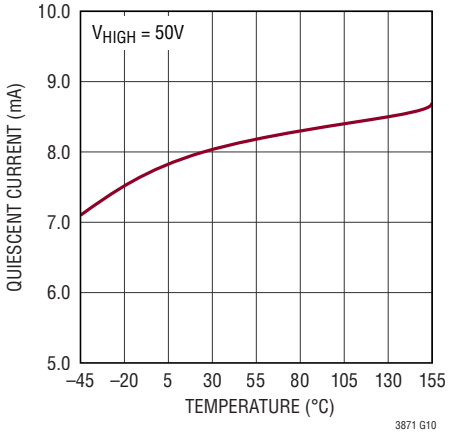
Undervoltage Lockout Threshold (V_5) vs Temperature



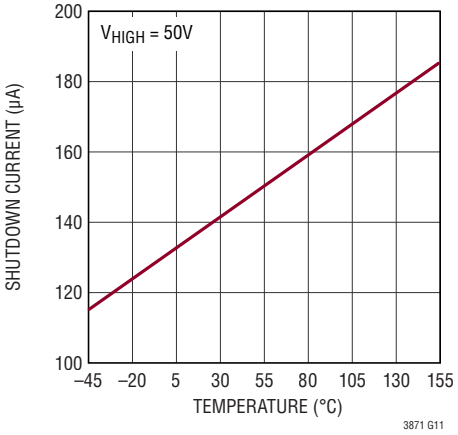
Rev. C

TYPICAL PERFORMANCE CHARACTERISTICS

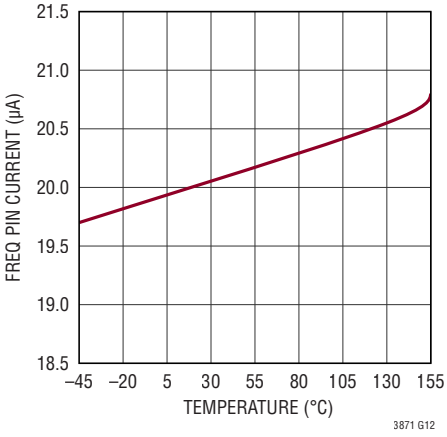
Quiescent Current vs Temperature



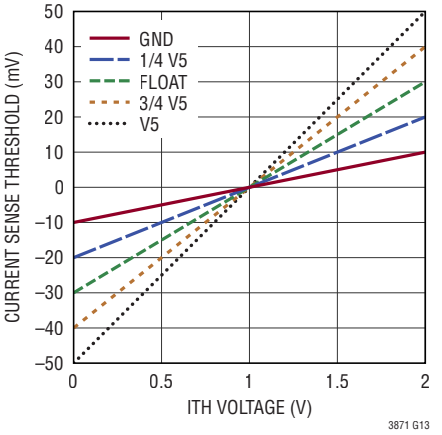
Shutdown Current vs Temperature



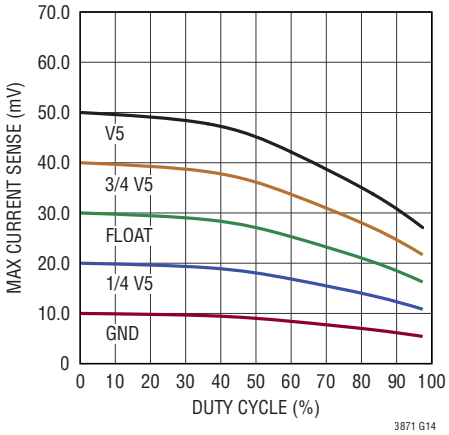
FREQ Pin Source Current vs Temperature



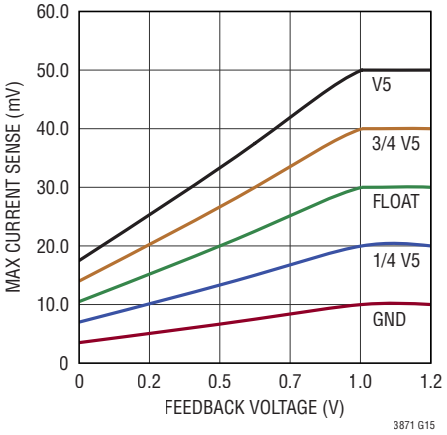
Current Sense Threshold vs ITH Voltage (DCR)



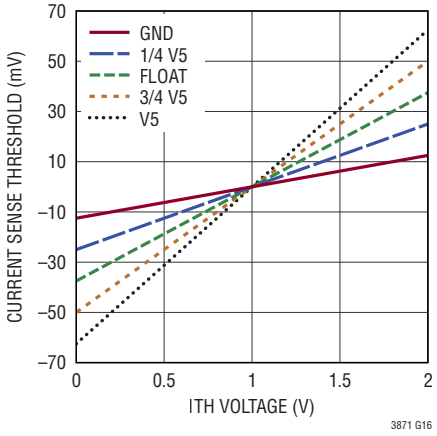
Maximum Current Sense Threshold vs Duty Cycle – BUCK (DCR)



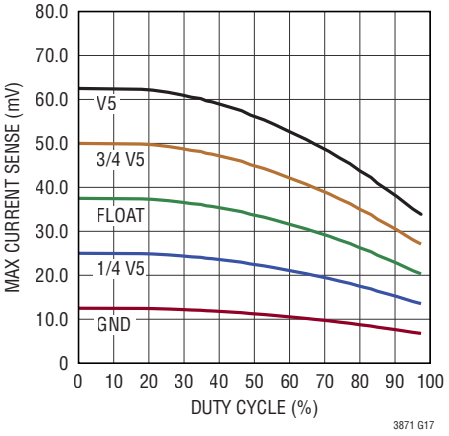
Maximum Current Sense Threshold vs Feedback Voltage (DCR) (LTC3871)



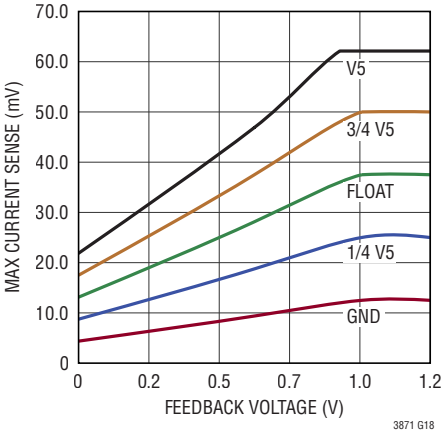
Current Sense Threshold vs ITH Voltage (R_{SENSE})



Maximum Current Sense Threshold vs Duty Cycle – BUCK (R_{SENSE})

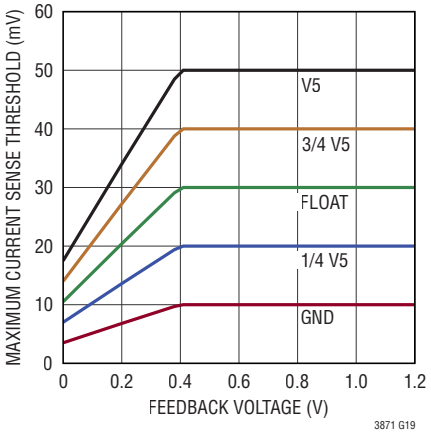


Maximum Current Sense Threshold vs Feedback Voltage (R_{SENSE}) (LTC3871)

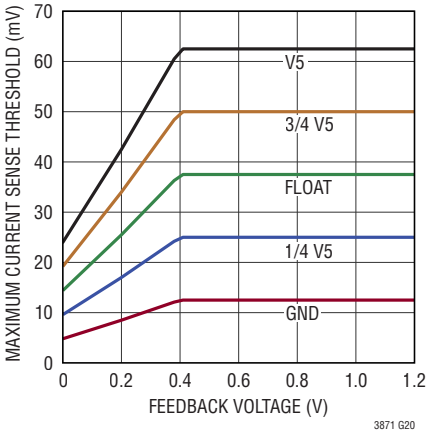


TYPICAL PERFORMANCE CHARACTERISTICS

Maximum Current Sense Threshold vs Feedback Voltage (DCR) (LTC3871-1)



Maximum Current Sense Threshold vs Feedback Voltage (R_{SENSE}) (LTC3871-1)



PIN FUNCTIONS

SS (Pin 1): Soft-Start Input. The voltage ramp rate at this pin sets the voltage ramp rate of the regulated voltage. A capacitor to ground accomplishes soft-start in buck mode. This pin has a 1.25µA pull-up current.

VFB_{LOW} (Pin 2): V_{LOW} Voltage Sensing Error Amplifier Inverting Input.

ITH_{LOW}/ITH_{HIGH} (Pins 3 and 4): Current Control Threshold and Error Amplifier Compensation Point. The current comparator's threshold varies with the ITH control voltage.

VFB_{HIGH} (Pin 5): V_{HIGH} Voltage Sensing Error Amplifier Inverting Input.

V5 (Pin 6): Internal 5.5V Regulator Output. The control circuits are powered from this voltage. Bypass this pin to SGND with a minimum of 4.7µF low ESR tantalum or ceramic capacitor.

SGND (Pins 7 and 28): Signal Ground Pins.

OV_{HIGH} (Pin 8): V_{HIGH} Overvoltage Threshold Set Pin. A resistor divider from V_{HIGH} is needed to set this threshold. When the voltage on this pin rises past the 1.2V trip point, a 5µA current is sourced out of the pin to provide externally adjustable hysteresis. When OV_{HIGH} voltage is above 3V, the controller stops switching.

UV_{HIGH} (Pin 9): V_{HIGH} Undervoltage Threshold Set Pin. A resistor divider from V_{HIGH} is needed to set this threshold. This pin also controls the state of the PGATE pin. When the voltage on this pin falls below the 1.2V trip point, a 5µA current is sunk into the pin to provide externally adjustable hysteresis.

OV_{LOW} (Pin 10): V_{LOW} Overvoltage Threshold Set Pin. A resistor divider from V_{LOW} is needed to set this threshold. When the voltage on this pin rises past the 1.2V trip point, a 5µA current is sourced out of the pin to provide externally adjustable hysteresis.

IMON (Pin 11): The voltage on this pin is directly proportional to the average inductor currents of the 2 channels. 1.25V indicates zero average inductor current per phase.

SETCUR (Pin 12): This pin sets the maximum average inductor current in buck or boost mode. This pin sources 7.5µA.

$SNSA1^+$/$SNSA2^+$ (Pins 13 and 48): AC Positive Current Sense Comparator Inputs. These inputs amplify the AC portion of the current signal to the IC's current comparator.

$SNS1^-$/$SNS2^-$(Pins 14 and 47): Negative Current Sense Comparator Inputs. The negative input of the current comparator is normally connected to V_{LOW}.

PIN FUNCTIONS

SNSD1+/SNSD2+(Pins 15 and 46): DC Positive Current Sense Comparator Inputs. These inputs amplify the DC portion of the current signal to the IC's current comparator.

BUCK (Pin 16): The voltage on this pin determines if the IC is regulating the V_{LOW} or V_{HIGH} voltage/current. Float or tie this pin to V5 for buck mode operation. Ground this pin for boost mode operation.

ILIM (Pin 17): Current Comparator Sense Voltage Limit Selection Pin. The input impedance of this pin is 100kΩ.

RUN (Pin 18): Enable Control Input. A voltage above 1.22V turns on the IC. There is a 2µA pull-up current on this pin. Once the RUN pin rises above the 1.22V threshold the pull-up current increases to 6µA.

$\overline{\text{FAULT}}$ (Pin 19): Fault Indicator Output. Open-drain output that pulls to ground during a fault condition.

DRVSET (Pin 20): The voltage setting on this pin programs the DRV_{CC} output voltage. The input impedance of this pin is 100kΩ.

NC (Pins 21, 30, 32, 34, 40): No Connect Pins.

TG1/TG2 (Pins 22 and 39): Top Gate Driver Outputs. This is the output of the floating driver with a voltage swing equal to DRV_{CC} superimposed on the SW voltage.

SW1/SW2 (Pins 23 and 38): Switch Node Connections to the Inductors. Voltage swing at this pin is from a Schottky diode (external) voltage drop below ground to V_{HIGH}.

BOOST1/BOOST2 (Pins 24 and 37): Boosted Floating Driver Supplies. The (+) terminal of the bootstrap capacitor connects to this pin. This pin swings from a diode drop below DRV_{CC} up to V_{HIGH}+DRV_{CC}.

BG1/BG2 (Pins 25 and 36): Bottom Gate Driver Outputs. This pin drives the gate(s) of the bottom N-channel MOSFET(s) between PGND and DRV_{CC}.

PGND1/PGND2 (Pins 26 and 35): Power Ground Pin. Connect this pin closely to the source(s) of the bottom N-channel MOSFET(s), the (–) terminal of $CDRV_{CC}$ and (–) terminal of CV_{HIGH}.

$EXTV_{CC}$ (Pin 27): External Power Input to an Internal LDO Connected to DRV_{CC}. When the voltage on this pin is greater than the DRV_{CC} LDO setting minus 500mV, this LDO bypasses the internal LDO powered from V_{HIGH}. In applications where the supply $EXTV_{CC}$ is connected to is expected to go below ground, such as V_{LOW}, a Schottky diode on the pin and a 10Ω resistor in between and the external supply is strongly recommended.

DRV_{CC} (Pin 29): Gate Driver Current Supply LDO Output. The voltage on this pin can be set from 6V to 10V in 1V increments. Bypass this pin to PGND with a minimum of 4.7µF low ESR tantalum or ceramic capacitor.

V_{HIGH} (Pin 31): Main V_{HIGH} supply. Bypass this pin to PGND with a capacitor (0.1µF to 1µF)

PGATE (Pin 33): Gate Drive for Input Short Protection. If a UV_{HIGH} fault is detected, PGATE drives the gate of an external PMOS in series with the V_{HIGH} rail high. Signal swings is from V_{HIGH} to V_{HIGH} –15V.

CLKOUT (Pin 41): Clock Output Pin. Use this pin to synchronize multiple LTC3871/LTC3871-1 ICs. Signal swing is from V5 to ground.

SYNC (Pin 42): Applying a clock signal to this pin causes the internal PLL to synchronize the internal oscillator to the clock signal. The PLL compensation network is integrated onto the IC. This pin has a 100k internal resistor to ground.

FREQ (Pin 43): Frequency Set Pin. A resistor between this pin and SGND sets the switching frequency.

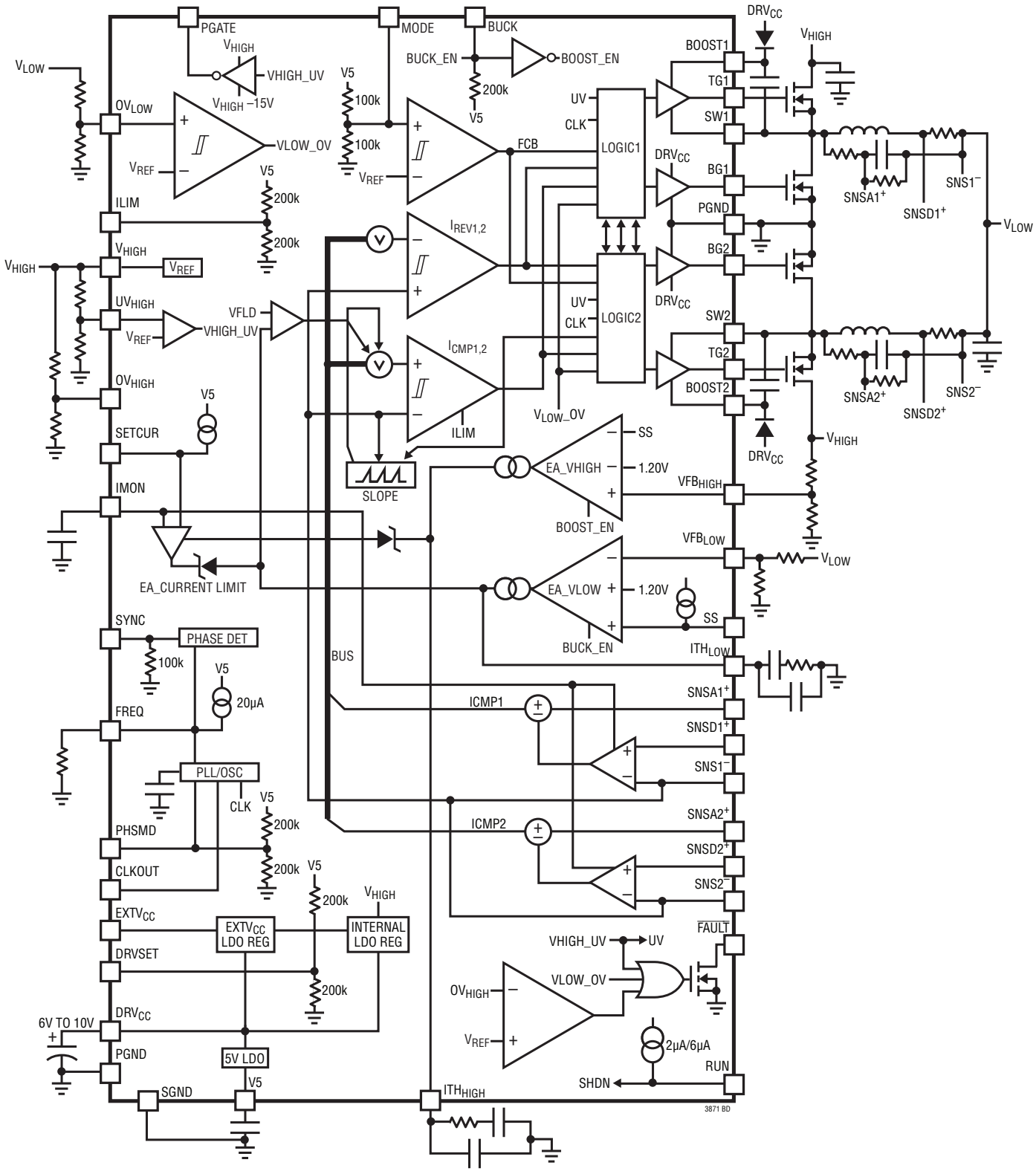
MODE (Pin 44): Tying this pin to SGND enables forced continuous mode in buck or boost modes. Floating this pin results in discontinuous mode when in buck mode and forced continuous mode in boost mode. Tying this pin to V5 enables discontinuous mode in buck mode and non-synchronous operation in boost mode. The input impedance of this pin is 50kΩ.

PHSMD (Pin 45): Phase Mode Pin. This pin selects CH1 – CH2 and CH1 – CLKOUT phasing.

GND (Exposed Pad Pin 49): Ground. Must be soldered to PCB ground for rated thermal performance. Connect this pin closely to the sources of the bottom N-channel MOSFETs and negative terminal of V_{HIGH}, DRV_{CC}, V_5 bypass capacitors. All small signal components and compensation components should connect here. Signal ground pin should be connected to this exposed pad.

BLOCK DIAGRAM

Bidirectional Controller with Current Programming and Monitoring Functions



OPERATION

Main Control Loop

The LTC3871/LTC3871-1 is a bidirectional, constant-frequency, current mode step-down controller with two channels operating 180° or 120° out of phase. The LTC3871/LTC3871-1 is capable of delivering power from V_{HIGH} to V_{LOW} as well as from V_{LOW} back to V_{HIGH}. When power is delivered from V_{HIGH} to V_{LOW}, the LTC3871/LTC3871-1 operates as a peak-current mode constant-frequency buck regulator; and when power delivery is reversed, it operates as a valley current mode constant-frequency boost regulator. Four control loops, two for current and two for voltage, allow control of voltage or current on either V_{HIGH} or V_{LOW}. The LTC3871/LTC3871-1 uses an LTC-proprietary current sensing, current mode architecture. During normal buck mode operation, the top MOSFET is turned on every cycle when the oscillator sets the RS latch, and turned off when the main current comparator, I_{CMP}, resets the RS latch. The peak inductor current at which I_{CMP} resets the RS latch is controlled by the voltage on the ITH pin, which is the output of the error amplifier, EA. The error amplifier receives the feedback signal and compares it to the internal 1.2V reference. When the load current increases, it causes a slight change in the feedback pin voltage relative to the 1.2V reference, which in turn causes the ITH voltage to change until the inductor's average current equals the new load current. After the top MOSFET has turned off, the bottom synchronous MOSFET is turned on until the beginning of the next cycle.

The main control loop is shut down by pulling the RUN pin low. Releasing RUN allows an internal 2µA current source to pull-up the RUN pin. When the RUN pin reaches 1.22V, the main control loop is enabled and the IC is powered up and the pull-up current increases to 6.5µA. When the RUN pin is low, all functions are kept in a controlled shutdown state.

Current Sensing with Low DCR

The LTC3871/LTC3871-1 employs a unique architecture to enhance the signal-to-noise ratio with low current sense offsets. That enables it to operate with a small current sense signal of a very low value inductor DCR to improve power efficiency, and reduce jitter due to switching noise which could corrupt the signal. The LTC3871/LTC3871-1 uses two positive current sense pins, $SNSD^+$ and $SNSA^+$, to acquire signals and process them internally to provide the response equivalent to a DCR sense signal that has a 14dB (5 times) signal-to-noise ratio. Accordingly, the current limit threshold is still a function of the inductor peak-current and its DCR value, and can be accurately set from 10mV to 50mV in 10mV steps with the ILIM pin. The filter time constant, R1 • C1, of the $SNSD^+$ pin should match the L/DCR of the output inductor, while the filter at $SNSA^+$ pin should have a bandwidth of five times larger than $SNSD^+$, R2 • C2 equals R1 • C1/5 (refer to Figure 3).

Current Sensing with Low Value R_{SENSE}

The LTC3871/LTC3871-1 can also be used with an external low value R_{SENSE} resistor for increased accuracy. To accomplish this, the $SNSA^+$ pin needs a filter time constant R2 • C2 that has a bandwidth that is four times larger than the L/(R_{SENSE}). The $SNSD^+$ pin is now connected to the R_{SENSE} resistor as shown in Figure 1. A small filter cap may be used to filter out high frequency noise (refer to Figure 4).

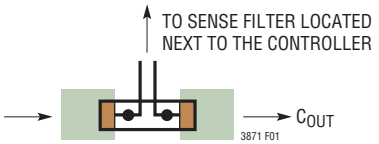


Figure 1. Sense Lines Placement with Sense Resistor

$DRV_{CC}/EXTV_{CC}/V5$ Power

Power for the top and bottom MOSFET drivers is derived from the DRV_{CC} pin. The DRV_{CC} voltage can be set to anywhere from 6V to 10V in 1V steps using the DRVSET pin. When the $EXTV_{CC}$ pin is left open or tied to a voltage less than (DRV_{CC} – 1V), an internal linear regulator supplies DRV_{CC} power from V_{HIGH}. When $EXTV_{CC}$ is taken above (DRV_{CC} – 500mV), the internal regulator between DRV_{CC} and V_{HIGH} is turned off, and a second internal regulator is turned on between $EXTV_{CC}$ and DRV_{CC}. Each top MOSFET driver is biased from a floating bootstrap capacitor, which normally recharges during each off cycle through an external diode when the top MOSFET turns off. If the input voltage, V_{HIGH}, decreases to a voltage close to V_{LOW}, the loop may enter dropout and attempt to turn

OPERATION

on the top MOSFET continuously. The dropout detector detects this and forces the top MOSFET off for about one-twelfth of the clock period plus 100ns every fifth cycle to allow the bootstrap capacitor to recharge.

Most of the internal circuitry is powered from the V5 rail that is generated by an internal linear regulator from DRV_{CC}. The V5 pin needs to be bypassed with a 2.2µF to 10µF external capacitor between V5 and SGND. This pin provides a 5.5V output that can supply up to 20mA of current. See the Applications Information section for more details.

Soft-Start (Buck Mode)

By default, the start-up of the V_{LOW} voltage is normally controlled by an internal soft-start ramp. The internal soft-start ramp represents a non-inverting input to the error amplifier. The VFB_{LOW} pin is regulated to the lower of the error amplifier's three non-inverting inputs (the internal soft-start ramp, the SS pin or the internal 1.2V reference). As the ramp voltage rises from 0V to 1.2V over approximately 1ms, the V_{LOW} voltage rises smoothly from its pre-biased value to its final set value. Certain applications can require the start-up of the converter into a non-zero load voltage, where residual charge is stored on the V_{LOW} capacitor at the onset of converter switching. In order to prevent the V_{LOW} from discharging under these conditions, the top and bottom MOSFETs are disabled until soft-start is greater than VFB_{LOW}.

Soft-Start (Boost Mode)

The same internal soft-start capacitor and external soft-start capacitor are also active if the controller starts with boost mode of operation. The error amplifier for boost mode also tries to regulate to the lowest reference during start-up. However, the topology of the boost converter limits the effectiveness of this soft-start mechanism until the boost output voltage reaches its input voltage level. Therefore, it is recommended that the controller starts in buck mode of operation.

Shutdown and Start-Up (RUN and SS Pins)

The LTC3871/LTC3871-1 can be shut down using the RUN pin. Pulling the RUN pin below 1.14V shuts down the main control loop for the controller and most internal circuits, including the DRV_{CC} and V5 regulators. Releasing the RUN pin allows an internal 2µA current to pull-up the pin and enable the controller. Alternatively, the RUN pin may be externally pulled up or driven directly by logic. Be careful not to exceed the absolute maximum rating of 6V on this pin. The start-up of the controller's V_{LOW} voltage is controlled by the voltage on the SS pin. When the voltage on the SS pin is less than the 1.2V internal reference, the LTC3871/LTC3871-1 regulates the VFB_{LOW} voltage to the SS pin voltage instead of the 1.2V reference. This allows the SS pin to be used to program a soft-start by connecting an external capacitor from the SS pin to GND. An internal 1.25µA pull-up current charges this capacitor, creating a voltage ramp on the SS pin. As the SS voltage rises linearly from 0V to 1.2V (and beyond), the V_{LOW} voltage, rises smoothly from zero to its final value. When the RUN pin is pulled low to disable the controller, or when V5 drops below its undervoltage lockout threshold of 4.15V, the SS pin is pulled low by an internal MOSFET. When in undervoltage lockout, the controller is disabled and the external MOSFETs are held off. External circuitry can be added to discharge the soft-start capacitor during fault conditions to ensure a soft-start when the faults are cleared.

Frequency Selection and Phase-Locked Loop (FREQ and SYNC Pins)

The selection of switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage.

If the SYNC pin is not being driven by an external clock source, the FREQ pin can be used to program the controller's operating frequency from 50kHz to 500kHz. There is a precision 20µA current flowing out of the FREQ pin so that the user can program the controller's switching frequency with a single resistor to SGND. A curve is provided later in the Applications Information section showing the relationship between the voltage on the FREQ pin and switching frequency (Figure 8).

OPERATION

A phase-locked loop (PLL) is available on the LTC3871/LTC3871-1 to synchronize the internal oscillator to an external clock source that is connected to the SYNC pin. The PLL loop filter network is integrated inside the LTC3871/LTC3871-1. The phase-locked loop is capable of locking any frequency within the range of 60kHz to 460kHz. The frequency setting resistor should always be present to set the controller's initial switching frequency before locking to the external clock. The controller operates in the user selected mode when it is synchronized.

Multiphase Operation

For output loads that demand high current, multiple LTC3871/LTC3871-1s can be daisy chained to run out of phase to provide more output current without increasing input and output voltage ripple. The SYNC pin allows the LTC3871/LTC3871-1 to synchronize to the CLKOUT signal of another LTC3871/LTC3871-1. The CLKOUT signal can be connected to the SYNC pin of the following LTC3871/LTC3871-1 stage to line up both the frequency and the phase of the entire system. Tying the PHSMD pin to V5, GND or floating, generates a phase difference (between CH1 and CLKOUT) of 240°, 60° or 90° respectively, and a phase difference (between CH1 and CH2) of 120°, 180° or 180°. Tying PHSMD to 1/4 or 3/4 of V5 generates a phase difference of 60° or 45° between CH1 and CLKOUT. Figure 2 shows the PHSMD connections necessary for 3-, 4-, 6-, 8- or 12-phase operation. A total of 12 phases can be daisy chained to run simultaneously out of phase with respect to each other. When paralleling multiple ICs, please be aware of the input impedance of pins connected to the same node.

Undervoltage Lockout

The LTC3871/LTC3871-1 has two functions that help protect the controller in case of undervoltage conditions. A precision UVLO comparator constantly monitors the V5 voltage to ensure that an adequate voltage is present. It locks out the switching action when V5 is below 4.15V. To prevent oscillation when there is a disturbance on the V5, the UVLO comparator has 500mV of precision hysteresis.

Another way to detect an undervoltage condition is to monitor the V_{HIGH} supply. Because the RUN pin has a precision turn-on reference of 1.22V, one can use a resistor divider to V_{HIGH} to turn on the IC when V_{HIGH} is high enough. An extra 4.5µA of current flows out of the RUN pin once the RUN pin voltage passes 1.22V. The RUN comparator itself has about 80mV of hysteresis. Additional hysteresis for the RUN comparator can be programmed by adjusting the values of the resistive divider. For accurate V_{HIGH} undervoltage detection, V_{HIGH} needs to be higher than 5V.

Fault Flag ($\overline{FAULT}$, OV_{HIGH}, OV_{LOW} and UV_{HIGH} Pins)

The $\overline{FAULT}$ pin is connected to the open-drain of an internal N-channel MOSFET. It can be pulled high with an external resistor connected to a voltage up to 6V, such as V5 or an external bias voltage. The $\overline{FAULT}$ pin is pulled low when:

a. The RUN pin is below its turn on threshold.

b. When V5 is below its UVLO threshold.

c. Any of the three OV/UV comparators have been tripped.

d. During a startup sequence until the SS pin charges up past 1.2V.

The OV_{LOW} and OV_{HIGH} thresholds are set using an external resistor dividers off of V_{LOW} and V_{HIGH}, respectively. When the voltage at the pin exceeds the comparator threshold of 1.2V, a 5µA hysteresis current is sourced out of the respective pin and the $\overline{FAULT}$ signal goes low after a 125µs delay. The UV_{HIGH} threshold is also set using an external resistor divider off V_{HIGH}. When the voltage at the pin falls below the comparator threshold of 1.2V, a 5µA hysteresis current is sunk in to the UV_{HIGH} pin and the $\overline{FAULT}$ signal goes low after a 125µs delay. The amount of hysteresis can be adjusted by changing the total impedance of the resistor divider, while the resistor ratio sets the UV/OV trip point.

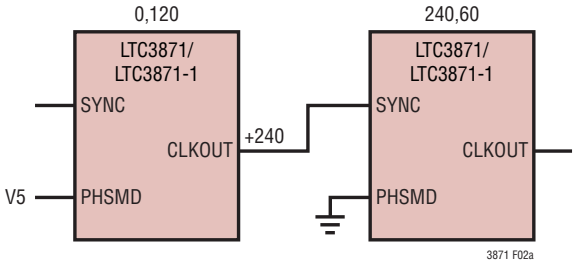
Besides flagging the $\overline{FAULT}$ pin, the UV/OV comparators also affect the operation of the controller, as shown in Table 1.

When the OV_{LOW} comparator crosses its 1.2V threshold:

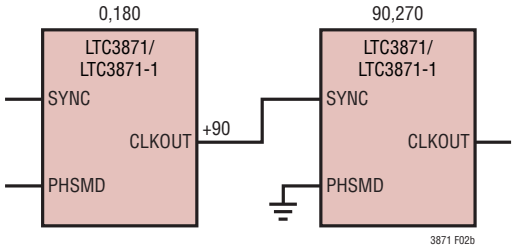
a. In buck mode, the controller stops switching.

b. In boost mode, the controller continues to switch.

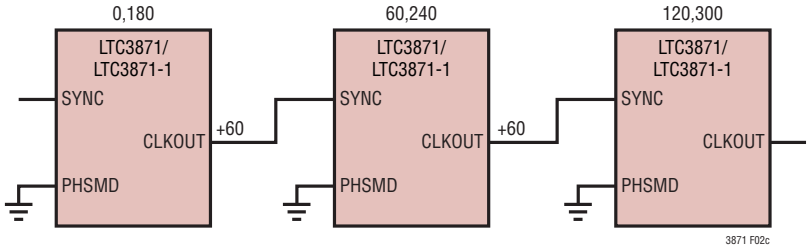
OPERATION



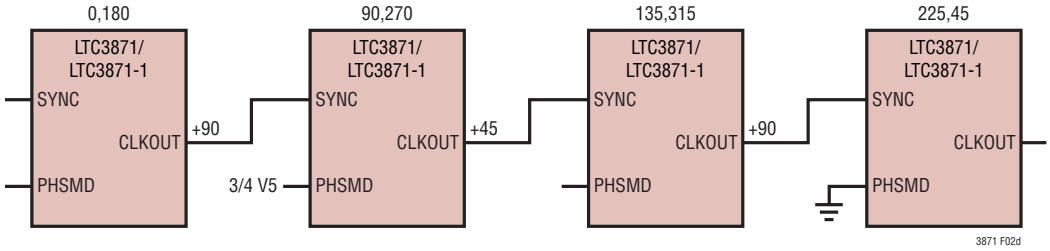
(2a) 3-Phase Operation



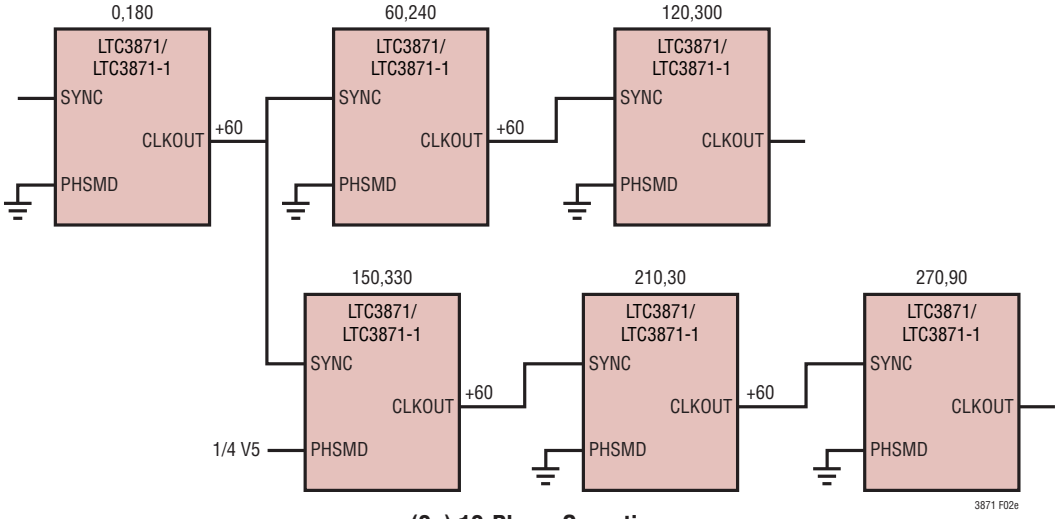
(2b) 4-Phase Operation



(2c) 6-Phase Operation



(2d) 8-Phase Operation



(2e) 12-Phase Operation

Figure 2. Phase Operations

OPERATION

c. ITH and SS are unaffected in both buck and boost modes. Whenever a fault is detected, discharge the SS pin as needed externally.

When the OV_{HIGH} comparator crosses its 1st threshold of 1.2V:

a. The controller stops switching in both buck and boost modes.

b. ITH and SS are unaffected in both buck and boost modes. Whenever a fault is detected, discharge the SS pin as needed externally.

When the OV_{HIGH} comparator crosses its 2nd threshold of 3V:

a. The controller stops switching in both buck and boost modes.

b. Both ITH and IMON pins are driven into high impedance. This feature allows the users to isolate one LTC3871/LTC3871-1 from a multiphase system in the case a fault is detected on one particular IC.

c. The SS pin is unaffected.

When the UV_{HIGH} comparator crosses its 1.2V threshold:

a. In buck mode, the controller stops switching after a 125µsec delay and disconnects V_{HIGH} from V_{LOW} with an external P-channel MOSFET via the PGATE pin.

b. In boost mode, the controller continues to switch, but it disconnects V_{HIGH} from V_{LOW} with an external P-channel MOSFET after a 125µsec delay. The voltage at the source side of the P-channel MOSFET is still regulated.

c. ITH and SS are unaffected in both buck and boost modes. Whenever a fault is detected, discharge the SS pin as needed externally.

Input Disconnect (PGATE Pin)

In a typical boost controller, the synchronous diode or the body diode of the synchronous MOSFET conducts current from the input to the output until the output is a diode drop below the input. As a result an output (V_{HIGH}) short will drag the input (V_{LOW}) down without a blocking diode or MOSFET to block the current. The LTC3871/LTC3871-1 uses an external low RDS(ON) P-channel MOSFET for input short-circuit protection when V_{HIGH} is shorted to ground.

The PGATE pin drives the gate of an external MOSFET between V_{IN} and V_{HIGH}–15V—this pin is internally clamped to V_{HIGH}–15V to protect the gate oxide of the external MOSFET. In normal operation, the P-channel MOSFET is always on, with its gate-source voltage clamped to 15V maximum. When the UV_{HIGH} pin voltage goes below its 1.2V threshold, $\overline{FAULT}$ goes low 125µs later. At this point, the PGATE pin voltage transitions from V_{HIGH}–15V to V_{HIGH}, turning off the external P-channel MOSFET. The MOSFET needs to be connected such that its body diode will block the current path from V_{LOW} to V_{HIGH}. In buck mode, the switching action stops when PGATE is off and a fault condition is reported; In boost mode, the controller will still switch and regulate the programmed boost voltage on the source side of the PGATE. Output cap should be present at the source side of the PGATE. A fault condition is also reported in this case. The external P-channel MOSFET remains disconnected until V_{HIGH} rises high enough to un-trip the UV_{HIGH} comparator.

Table 1. OV/UV Faults

$\overline{FAULT}$	MODE	SWITCHING	ITH PINS	IMON	SS	PGATE PIN
OV_{LOW} 1.2V Threshold	Buck	Stops	No Effect	No Effect	No Effect	Low
	Boost	Continues	No Effect	No Effect	No Effect	Low
OV_{HIGH} 1.2V Threshold	Buck	Stops	No Effect	No Effect	No Effect	Low
	Boost	Stops	No Effect	No Effect	No Effect	Low
OV_{HIGH} 3V Threshold	Buck	Stops	Hi-Z	Hi-Z	No Effect	Low
	Boost	Stops	Hi-Z	Hi-Z	No Effect	Low
UV_{HIGH} 1.2V Threshold	Buck	Stops	No Effect	No Effect	No Effect	High
	Boost	Continues	No Effect	No Effect	No Effect	High

OPERATION

Current Monitoring and Regulation (IMON, SETCUR Pins)

The inductor current can be sensed using either its DCR or a R_{SENSE} resistor. The current monitoring pin, IMON, outputs a voltage that is proportional to the average inductor current of the two channels sensed by the LTC3871/LTC3871-1. The operational range of IMON is 0.5V to 2.5V. When the average inductor current is zero, the IMON pin voltage rests at 1.25V. As the inductor current increases in buck mode, the I_{MON} voltage proportionally increases. The current sense signal to I_{MON} gain is 38 for the 10mV, 20mV and 30mV ILIM settings, and 19 for the 40mV and 50mV ILIM settings. An external voltage can be applied to the SETCUR pin to regulate the average output current. Because SETCUR and IMON are the two inputs to the current loop gain amplifier with SETCUR acting as the reference, as the IMON pin voltage approaches SETCUR, the ITH pin control is taken over by the current regulation error amplifier from the voltage loop error amplifier.

In boost mode, the inductor current polarity is reversed, so the corresponding IMON and SETCUR ranges are 1.25V to 0.5V with 0.5V being the maximum boost current. The SETCUR pin sources an accurate 7.5µA current in both modes, allowing this voltage to be set with a single resistor for convenience. The SETCUR value defaults to the zero current value internally if the SETCUR pin sees a voltage that is out of range for the selected mode. The valid range of SETCUR is 1.25V to 2.5V for buck mode and 1.25V to 0.5V for boost mode. Therefore, if SETCUR voltage is set below 1.25V in buck mode, the internal SETCUR voltage is forced at 1.25V. If SETCUR voltage is set above 1.25V in boost mode, the internal SETCUR voltage is also forced at 1.25V. For battery charging applications, SETCUR can be programmed dynamically on-the-fly to set the charging currents to the batteries in either buck or boost mode. SETCUR can be used at start-up to limit the in-rush current in both buck mode and boost mode.

Use the following equation to calculate the voltages on IMON:

$V_{IMON} = V_{ZERO} + K \bullet I_{OUT} \bullet R_{SENSE}/m$; Buck Mode

$V_{IMON} = V_{ZERO} – K \bullet I_{OUT} \bullet R_{SENSE}/m$; Boost Mode

Where:

V_{IMON}, the phase current voltage appears on IMON pin;

V_{ZERO}, the IMON voltage when average output current is zero; V_{ZERO} = 1.25V typically

K = 38 if ILIM = 10mV; 20mV; or 30mV

K = 19 if ILIM = 40mV; or 50mV

I_{OUT}, the total average output current,

R_{SENSE}, the current sensing element value;

m, the number of phases.

To defeat the current programming operation, tie the SETCUR pin to V_5 in buck mode and ground the SETCUR pin in boost mode.

Buck and Boost Modes (BUCK Pin)

The LTC3871/LTC3871-1 can be dynamically and seamlessly switched from buck mode to boost mode and vice versa via the BUCK pin. Tie this pin to V5 to select buck mode and to ground to select boost mode operation. This pin has an internal pull up resistor that defaults to buck mode if left floating. There are two separate error amplifiers for V_{HIGH} or V_{LOW} regulation. Having two error amplifiers allows fine tuning of the loop compensation for the buck and boost modes independently to optimize transient response. When buck mode is selected, the corresponding error amplifier is enabled, and ITH_{LOW} voltage controls the peak inductor current. The other error amplifier is disabled and ITH_{HIGH} is parked at its zero current level. In boost mode, ITH_{HIGH} is enabled while ITH_{LOW} is

Table 2. ITH PIN Parking Conditions

PIN	MODE	PARKING STATE	COMMENTS
ITH_{HIGH}	Buck	Parked	OV_{HIGH} 3V Threshold Overrides Park
	Boost	Parked in Prebias	OV_{HIGH} 3V Threshold Overrides Park
ITH_{LOW}	Buck	Parked in Prebias	OV_{LOW} and OV_{HIGH} 3V Threshold Overrides Park
	Boost	Parked	OV_{LOW} and OV_{HIGH} 3V Threshold Overrides Park

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parked at its zero current level. During a buck to boost or a boost to buck transition, the internal soft-start is reset. Resetting soft-start and parking the ITH pin at the zero current level ensures a smooth transition to the newly selected mode. Refer to Table 2 for a summary.

To further minimize any transients, SETCUR can be programmed to 1.25V or zero current level before switching between boost and buck modes.

Buck Mode Light Load Current Operation (DCM/CCM)

In buck mode, the LTC3871/LTC3871-1 can be enabled to enter discontinuous conduction mode or forced continuous conduction mode. To select forced continuous operation, tie the MODE pin to GND. To select discontinuous conduction mode of operation, tie the MODE pin to V5 or float it.

In forced continuous operation, the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined by the voltage on the ITH_{LOW} pin, just as in normal operation. In this mode, the efficiency at light loads is lower than in DCM mode operation. However, continuous mode has the advantages of lower output ripple and less interference with audio circuitry.

When the MODE pin is connected to V5 or left floating, the LTC3871/LTC3871-1 operates in discontinuous conduction mode at light loads. At very light loads, the current comparator, I_{CMP}, may remain tripped for several cycles and force the external top MOSFET to stay off for the same number of cycles (i.e., skipping-pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple as well as low audio noise and reduced RF interference. It provides higher low current efficiency than forced continuous mode.

Boost Mode Light Load Current Operation (DCM/CCM)

In boost mode, the LTC3871/LTC3871-1 can be enabled to enter constant-frequency discontinuous conduction mode or forced continuous conduction mode. To select forced-continuous operation, tie the MODE pin to GND or float it. To select discontinuous conduction mode of operation, tie the MODE pin to V5.

In forced continuous operation, the inductor current is allowed to reverse at light loads or under large transient conditions. The inductor current valley is determined by the voltage on the ITH_{HIGH} pin, just as in normal operation. In this mode, the efficiency at light loads is lower. However, continuous mode has the advantages of lower output ripple.

When the MODE pin is connected to V5, the LTC3871/LTC3871-1 operates with the synchronous N-channel MOSFET disabled, using the body diode of the MOSFET as the synchronous diode to reduce switching losses, and prevent reverse current. To reduce the MOSFET heat dissipation in this mode, parallel Schottky diodes are recommended.

Thermal Shutdown

The LTC3871/LTC3871-1 has a temperature sensor integrated on the IC, to sense the die temperature near the gate driver circuits. When the die temperature exceeds 175°C, all switching actions stop, and the driver gate pins are held low, thus turning off all external MOSFETs. At the same time, the channels are disconnected from the IMON pins, and SS and ITH_{HIGH}/ITH_{LOW} pins continue to function normally, so as not to interfere with other LTC3871/LTC3871-1 chips that may reference the common pins. When the temperature drops 10°C below the trip threshold, normal operation resumes.

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The Typical Application on the first page of this data sheet is a basic LTC3871/LTC3871-1 application circuit. In general, external component selection is driven by the load requirements, and begins with the DCR or R_{SENSE} and inductor value. Next, power MOSFETs are selected. Finally, V_{HIGH} and V_{LOW} capacitors are selected.

Slope Compensation and Inductor Peak Current

Slope compensation provides stability in constant frequency architectures by preventing sub-harmonic oscillations at high duty cycles. It is accomplished internally by adding a compensating ramp to the inductor current signal at duty cycles in excess of 40%. For high duty cycle applications, the maximum current is reduced. A curve of maximum peak current vs. duty cycle is given in the Typical Performance Characteristics section.

Current Limit Programming

The ILIM pin is a 5-level logic input which sets the maximum current limit of the controller. Table 3 shows the five ILIM settings. Please note that these settings represent the peak inductor current setting. Because of the inductor ripple current, the average output current is lower than the peak current. Setting ILIM using a resistor divider off of V5 will allow the maximum current sense threshold setting to not change when the 5.5V LDO is in dropout at start-up. Please note that the ILIM pin has an internal 200k pull-down to SGND and a 200k pull-up to V5.

Table 3. ILIM Settings

ILIM Pin Voltage	Max Current Sense Threshold	
	DCR Sensing	R_{SENSE}
0	10mV	12.5mV
1/4 V5	20mV	25mV
Float	30mV	37.5mV
3/4 V5	40mV	50mV
V5	50mV	62.5mV

SNSD+, SNSA+ and SNS– Pins

The SNSA+ and SNS– pins are the inputs to the current comparators, while the SNSD+ pin is the input of an internal DC amplifier. The operating input voltage range is 0V to 30V for all three sense pins. All the positive sense pins that are connected to the current comparator or the amplifier are high impedance with input bias currents of less than 1µA. The SNS– pin is not a high impedance pin. For V_{LOW} voltages greater than V5, the current comparators derive their bias currents directly off of SNS–. The SNS– pins should be connected directly to V_{LOW}. Care must be taken not to float these pins during normal operation. Filter components, especially capacitors, must be placed close to the LTC3871/LTC3871-1, and the sense lines should run close together to a Kelvin connection underneath the current sense element (Figure 1). Because the LTC3871/LTC3871-1 is designed to be used with a very low value sensing element to sense inductor current, without proper care, the parasitic resistance, capacitance and inductance will degrade the current sense signal integrity, making the programmed current limit unpredictable. As shown in Figure 3, resistors R1 and R2 are placed close to the output inductor and capacitors C1 and C2 are close to the IC pins to prevent noise coupling to the sense signal.

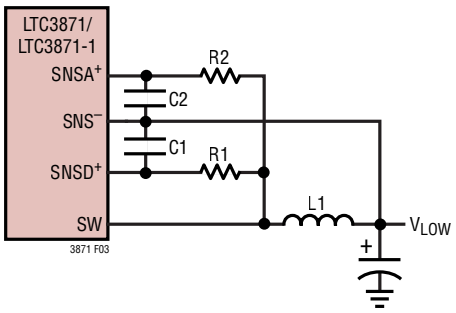

Figure 3. Inductor DCR Sensing

Inductor DCR Sensing

The LTC3871/LTC3871-1 is specifically designed for high load current applications requiring the highest possible efficiency; it is capable of sensing the signal of an inductor DCR in the milliohm range (Figure 3). The DCR is the DC winding resistance of the inductor's copper, which is often 1mΩ for high current inductors. In high current applications, the conduction loss of a high DCR or a sense resistor will cause a significant reduction in power efficiency. The SNSD+ pin connects to the filter that has a R1 • C1 time constant matched to L/DCR of the inductor. The SNSA+ pin is connected to the second filter with the time constant one-fifth that of R1 • C1. For a specific output

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requirement, choose the inductor with the DCR that satisfies the maximum desired sense voltage, and uses the relationship of the sense pin filters to output inductor characteristics as depicted below.

$$DCR = \frac{V_{SENSE(MAX)}}{I_{MAX} + \frac{\Delta I_L}{2}}$$

$$L/DCR = R1 \bullet C1 = 5 \bullet R2 \bullet C2$$

where:

$V_{SENSE(MAX)}$: Maximum sense voltage for a given ILIM threshold

ΔI_L: Inductor ripple current

L, DCR: Output inductor characteristics

R1 • C1: Filter time constant of the $SNSD^+$ pin

R2 • C2: Filter time constant of the $SNSA^+$ pin

To ensure that the load current will be delivered over the full operating temperature range, the temperature coefficient of DCR resistance, approximately 0.4%/°C, should be taken into account.

Typically, C1 and C2 are selected in the range of 0.047µF to 0.47µF. If C1 and C2 are chosen to be 0.47µF, and an inductor of 10µH with 3mΩ DCR is selected, R1 and R2 will be 6.98kΩ and 1.4kΩ respectively. The bias current at $SNSD^+$ and $SNSA^+$ is less than 1µA, and it introduces a small error to the sense signal.

There will be some power loss in R1 and R2 that relates to the duty cycle, and will be the most in continuous mode at the maximum V_{HIGH} voltage:

$$P_{LOSS}(R) = \frac{\left(V_{HIGH(MAX)} - V_{LOW}\right) \bullet V_{LOW}}{R}$$

Ensure that R1 and R2 have a power rating higher than this value. Care has to be taken for voltage coefficients of these resistors at high V_{HIGH} voltages. Multiple resistors can be used in series to minimize this effect. However, DCR sensing eliminates the conduction loss of a sense resistor; and provides better efficiency at heavy loads. To maintain a good signal-to-noise ratio for the current sense signal, use a minimum of 10mV between $SNSA^+$ and SNS^- pins or the equivalent of 2mV ripple on the current sense signal for duty cycles less than 40%. The actual ripple voltage across $SNSA^+$ and SNS^- pins will be determined by the following equation:

$$\Delta V_{SENSE} = \frac{V_{LOW}}{V_{HIGH}} \bullet \frac{V_{HIGH} - V_{LOW}}{R1 \bullet C1 \bullet f_{OSC}}$$

Sensing Using an R_{SENSE} Resistor

The LTC3871/LTC3871-1 can be used with an external R_{SENSE} resistor to sense current accurately. The external components required to accomplish this are shown in Figure 4. The $SNSD^+$ pin senses directly across the R_S resistor. The R1, C1 network provides the current signal path to the $SNSA^+$ pin. Internally the signals from the AC and DC paths are combined for accurate current sensing and low jitter performance. Resistor R2 is used to divide down the DC component of the signal seen by $SNSA^+$ due to the DCR of the inductor. As a rule of thumb, R2 needs to be 10 times smaller than R1 so the DCR value can be safely ignored.

The R1 • C1 time constant should be selected such that:

$$L/R_S = 4 \bullet R1 \bullet C1 \text{ for } R1 = 10 \bullet R2$$

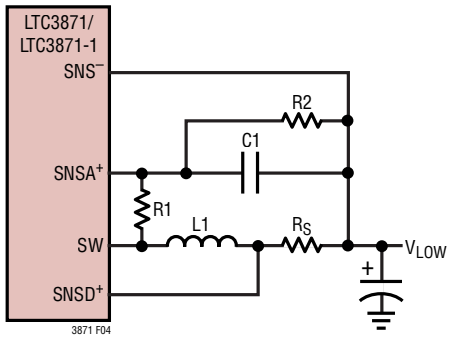

Figure 4. R_{SENSE} Resistor Sensing

Pre-Biased Output Start-Up

There may be situations that require the power supply to start up with a pre-bias on the V_{LOW} output capacitors. In this case, it is desirable to start up without discharging that output pre-bias. The LTC3871/LTC3871-1 can safely power up into a pre-biased output without discharging it.

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The LTC3871/LTC3871-1 accomplishes this by disabling both the top and bottom MOSFETs until the SS pin voltage and the internal soft-start voltage are above the VFB_{LOW} pin voltage. When VFB_{LOW} is higher than SS or the internal soft-start voltage, the error amp output is parked at its zero current level. Disabling both top and bottom MOSFETs prevents the pre-biased output voltage from being discharged. When SS and the internal soft-start both cross 1.32V or V_{FB}, whichever is lower, both top and bottom MOSFETs are enabled.

Buck Mode Overcurrent Fault

When the output of the power supply is loaded beyond its preset current limit, the regulated output voltage will collapse depending on the load. The V_{LOW} rail may be shorted to ground through a very low impedance path or it may be a resistive short, in which case the output will collapse partially, until the load current equals the preset current limit. The controller will continue to source current into the short. The amount of current sourced depends on the ILIM pin setting and the VFB_{LOW} voltage as shown in the Current Foldback graph in the Typical Performance Characteristics section.

Upon removal of the short, V_{LOW} soft starts using the internal soft-start, thus reducing output overshoot. In the absence of this feature, the output capacitors would have been charged at current limit, and in applications with minimal output capacitance this may have resulted in output overshoot. Current limit foldback is not disabled during an overcurrent recovery. The load must drop below the folded back current limit threshold in order to restart from a hard short.

Boost Mode Overcurrent Fault

When in boost mode, if the overcurrent situation persists and discharges V_{HIGH} below the preset UV_{HIGH} trip point, The PGATE pin turns off the external disconnect P-channel MOSFET, preventing V_{LOW} from getting discharged via the top MOSFET body diode. For both buck and boost mode of operation, current regulation loop can be used to limit the current by forcing a voltage on SETCUR pin. The zero average inductor current can be obtained by forcing 1.25V on SETCUR. If the SETCUR voltage is set to an invalid range for the selected mode of operation, the effective SETCUR voltage is internally set to 1.25V.

One way of protecting against an input V_{HIGH} soft short in boost mode is to monitor the I_{MON} voltage. If the I_{MON} voltage indicates excessive current, an external circuit can be added to simulate an UV condition at the input and turn off PGATE.

Inductor Value Calculation

Given the desired input and output voltages, the inductor value and operating frequency, f_{OSC}, directly determine the inductor's peak-to-peak ripple current:

$$I_{RIPPLE} = \frac{V_{LOW}}{V_{HIGH}}\left(\frac{V_{HIGH} - V_{LOW}}{f_{OSC} \bullet L}\right)$$

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors, and output voltage ripple. Thus, highest efficiency operation is obtained at low frequency with a small ripple current. Achieving this, however, requires a large inductor.

A reasonable starting point is to choose a ripple current that is about 40% of the maximum inductor current. Note that the largest ripple current occurs at the highest V_{HIGH} voltage. To guarantee that ripple current does not exceed a specified maximum, the inductor should be chosen according to:

$$L \geq \frac{V_{HIGH} - V_{LOW}}{f_{OSC} \bullet I_{RIPPLE}} \bullet \frac{V_{LOW}}{V_{HIGH}}$$

Inductor Core Selection

Once the inductance value is determined, the type of inductor must be selected. Core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that

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inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Power MOSFET and Schottky Diode (Optional) Selection

At least two external power MOSFETs need to be selected: One N-channel MOSFET for the top switch and one or more N-channel MOSFET(s) for the bottom switch. The number, type and on-resistance of all MOSFETs selected take into account the voltage step-down ratio as well as the actual position (main or synchronous) in which the MOSFET will be used. A much smaller and much lower input capacitance MOSFET should be used for the top MOSFET in applications that have an V_{LOW} that is less than one-third of V_{HIGH}. In applications where $V_{HIGH} >> V_{LOW}$, the top MOSFETs' on-resistance is normally less important for overall efficiency than its input capacitance at operating frequencies above 300kHz. MOSFET manufacturers have designed special purpose devices that provide reasonably low on-resistance with significantly reduced input capacitance for the main switch application in switching regulators.

The peak-to-peak MOSFET gate drive levels are set by the internal DRV_{CC} regulator voltage. Pay close attention to the BV_{DSS} specification for the MOSFETs as well. Selection criteria for the power MOSFETs include the on-resistance $R_{DS(ON)}$, input capacitance, input voltage and maximum output current. MOSFET input capacitance is a combination of several components but can be taken from the typical gate charge curve included on most data sheets (Figure 5). The curve is generated by forcing a constant input current into the gate of a common source, current source loaded stage and then plotting the gate voltage versus time.

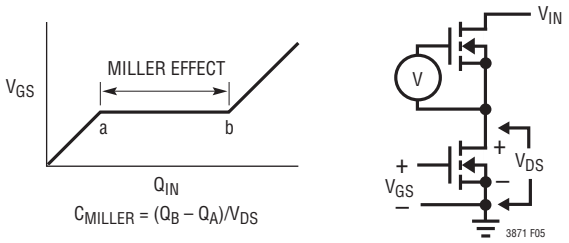

Figure 5. Gate Charge Characteristic

The initial slope is the effect of the gate-to-source and the gate-to-drain capacitance. The flat portion of the curve is the result of the Miller multiplication effect of the drain-to-gate capacitance as the drain drops the voltage across the current source load. The upper sloping line is due to the drain-to-gate accumulation capacitance and the gate-to-source capacitance. The Miller charge (the increase in coulombs on the horizontal axis from a to b while the curve is flat) is specified for a given V_{DS} drain voltage, but can be adjusted for different V_{DS} voltages by multiplying the ratio of the application V_{DS} to the curve specified V_{DS} values. A way to estimate the C_{MILLER} term is to take the change in gate charge from points a and b on a manufacturer's data sheet and divide by the stated V_{DS} voltage specified. C_{MILLER} is the most important selection criteria for determining the transition loss term in the top MOSFET but is not directly specified on MOSFET data sheets. C_{RSS} and C_{OS} are specified sometimes but definitions of these parameters are not included. When the controller is operating in continuous mode the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Main Switch Duty Cycle} = \frac{V_{LOW}}{V_{HIGH}}$$

$$\text{Synchronous Switch Duty Cycle} = \left(\frac{V_{HIGH} - V_{LOW}}{V_{HIGH}}\right)$$

The power dissipation for the main and synchronous MOSFETs at maximum output current are given by:

$$P_{MAIN} = \frac{V_{LOW}}{V_{HIGH}}\left(I_{MAX}\right)^2(1+\delta)R_{DS(ON)} + (V_{HIGH})^2\left(\frac{I_{MAX}}{2}\right)(R_{DR})(C_{MILLER})\bullet \left[\frac{1}{DRV_{CC} - V_{TH(MIN)}} + \frac{1}{V_{TH(MIN)}}\right]\bullet f$$

$$P_{SYNC} = \frac{V_{HIGH} - V_{LOW}}{V_{HIGH}}\left(I_{MAX}\right)^2(1+\delta)R_{DS(ON)}$$

I_{MAX} = Maximum Inductor Current.

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where δ is the temperature dependency of $R_{DS(ON)}$, RDR is the effective top driver resistance (approximately 5Ω at $V_{GS} = V_{MILLER}$); V_{HIGH} is the drain potential and the change in drain potential in the particular application. $V_{TH(MIN)}$ is the data sheet specified typical gate threshold voltage specified in the power MOSFET data sheet at the specified drain current. C_{MILLER} is the calculated capacitance using the gate charge curve from the MOSFET data sheet and the technique described above.

Both MOSFETs have I^2R losses while the topside N-channel equation includes an additional term for transition losses, which peak at the highest input voltage. The bottom MOSFET losses are greatest at high V_{HIGH} voltage when the top switch duty factor is low or during a V_{LOW} short-circuit when the bottom switch is on close to 100% of the period.

The term $(1 + \delta)$ is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs temperature curve, but $\delta = 0.005/°C$ can be used as an approximation for low voltage MOSFETs.

An optional Schottky diode across the bottom MOSFET conducts during the dead time between the conduction of the two large power MOSFETs in buck mode. This prevents the body diode of the bottom MOSFET from turning on, storing charge during the dead time and requiring a reverse-recovery period which could cost as much as several percent in efficiency. A 2A to 8A Schottky is generally a good compromise for both regions of operation due to the relatively small average current. Larger diodes result in additional transition loss due to their larger junction capacitance.

An optional Schottky diode across the top MOSFET is also recommended for Boost DCM operation. This will increase efficiency and reduce heat dissipation for large output currents.

C_{HIGH} and MOSFETs Selection (on V_{HIGH} and V_{LOW})

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle $(V_{LOW})/(V_{HIGH})$. To prevent large voltage transients, a low ESR capacitor sized for the maximum RMS current of one channel must be used. In the following discussion, it is assumed that C_{IN} is C_{HIGH}, C_{OUT} is C_{LOW}, V_{IN} is V_{HIGH}, and V_{OUT} is V_{LOW}. The maximum RMS capacitor current is given by:

$$C_{IN}\ \text{Required}\ I_{RMS} \approx \frac{I_{MAX}}{V_{IN}}\left[(V_{OUT})(V_{IN} - V_{OUT}) \right]^{1/2}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours of life.

This makes it advisable to further de-rate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may be paralleled to meet size or height requirements in the design. Ceramic capacitors can also be used for C_{IN}. Always consult the manufacturer if there is any question.

Ceramic capacitors are becoming very popular for small designs but several cautions should be observed. X7R, X5R and Y5V are examples of a few of the ceramic materials used as the dielectric layer, and these different dielectrics have very different effect on the capacitance value due to the voltage and temperature conditions applied. Physically, if the capacitance value changes due to applied voltage change, there is a concomitant piezo effect which results in radiating sound! A load that draws varying current at an audible rate may cause an attendant varying input voltage on a ceramic capacitor, resulting in an audible signal. A secondary issue relates to the energy flowing back into a ceramic capacitor whose capacitance value is being reduced by the increasing charge. The voltage can increase at a considerably higher rate than the constant current being supplied because the capacitance value is decreasing as the voltage is increasing! Nevertheless, ceramic capacitors, when properly selected and used, can provide the lowest overall loss due to their extremely low ESR.

A small (0.1µF to 1µF) bypass capacitor, C_{IN}, between the chip V_{IN} pin and ground, placed close to the LTC3871/LTC3871-1, is also suggested. A 2.2Ω to 10Ω resistor placed between C_{IN} and V_{IN} pin provides further isolation.

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The selection of C_{OUT} at V_{OUT} is driven by the required effective series resistance (ESR). Typically once the ESR requirement is satisfied the capacitance is adequate for filtering. The steady-state output ripple (ΔV_{OUT}) is determined by:

$$\Delta V_{OUT} \approx \Delta I_{RIPPLE}\left(ESR+\frac{1}{8fC_{OUT}}\right)$$

where f = operating frequency, C_{OUT} = output capacitance and ΔI_{RIPPLE} = ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI_{RIPPLE} increases with input voltage (V_{HIGH}). The output ripple will be less than 50mV at maximum V_{IN} with ΔI_{RIPPLE} = $0.4I_{OUT(MAX)}$ assuming:

C_{OUT} required ESR < N • R_{SENSE}

and

$$C_{OUT} > \frac{1}{(8f)(R_{SENSE})}$$

The emergence of very low ESR capacitors in small, surface mount packages makes very small physical implementations possible. The ability to externally compensate the switching regulator loop using the ITH pin allows a much wider selection of output capacitor types. The impedance characteristic of each capacitor type is significantly different than an ideal capacitor and therefore requires accurate modeling or bench evaluation during design. Manufacturers such as Nichicon, Nippon Chemi-Con and Sanyo should be considered for high performance through-hole capacitors. The OS-CON semiconductor dielectric capacitors available from Sanyo and the Panasonic SP surface mount types have a good (ESR) (size) product.

Once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement. Ceramic capacitors from AVX, Taiyo Yuden, Murata and TDK offer high capacitance value and very low ESR, especially applicable for low output voltage applications.

In surface mount applications, multiple capacitors may have to be paralleled to meet the ESR or RMS current handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. New special polymer surface mount capacitors offer very low ESR also but have much lower capacitive density per unit volume. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. Several excellent choices are the AVX TPS, AVX TPSV, the KEMET T510 series of surface mount tantalums or the Panasonic SP series of surface mount special polymer capacitors available in case heights ranging from 2mm to 4mm. Other capacitor types include Sanyo POSCAP, Sanyo OS-CON, Nichicon PL series and Sprague 595D series. Consult the manufacturers for other specific recommendations.

C_{HIGH} Capacitor Selection for Boost Operation

Contributions of ESR (equivalent series resistance), ESL (equivalent series inductance) and the bulk capacitance must be considered when choosing the correct combination of output capacitors for a boost converter application.

The choice of component(s) begins with the maximum acceptable ripple voltage (expressed as a percentage of the output voltage), and how this ripple should be divided between the ESR step and the charging/discharging ΔV. For the purpose of simplicity we will choose 2% for the maximum output ripple, to be divided equally between the ESR step and the charging/discharging ΔV. This percentage ripple will change, depending on the requirements of the application, and the equations provided below can easily be modified.

One of the key benefits of multiphase operation is a reduction in the peak current supplied to the output capacitor by the boost diodes. As a result, the ESR requirement of the capacitor is relaxed. For a 1% contribution to the total ripple voltage, the ESR of the output capacitor can be determined using the following equation:

$$ESR_{COUT} \le \frac{0.01 \bullet V_{OUT}}{I_{D(PEAK)}}$$

where:

$$I_{D(PEAK)} = \frac{1}{n} \bullet \left(1+\frac{\chi}{2}\right) \bullet \frac{I_{O(MAX)}}{1-D_{MAX}}$$

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The factor n represents the number of phases and the factor χ represents the percentage inductor ripple current.

For the bulk capacitance, which we assume contributes 1% to the total output ripple, the minimum required capacitance is approximately:

$$C_{OUT} \geq \frac{I_{O(MAX)}}{0.01 \bullet n \bullet V_{OUT} \bullet f}$$

For many designs it will be necessary to use one type of capacitor to obtain the required ESR, and another type to satisfy the bulk capacitance. For example, using a low ESR ceramic capacitor can minimize the ESR step, while an electrolytic capacitor can be used to supply the required bulk C.

The voltage rating of the output capacitor must be greater than the maximum output voltage, with sufficient derating to account for the maximum capacitor temperature.

Because the ripple current in the output capacitor is a square wave, the ripple current requirements for this capacitor depend on the duty cycle, the number of phases and the maximum output current. In order to choose a ripple current rating for the output capacitor, first establish the duty cycle range, based on the output voltage and range of input voltage.

The output ripple current is divided between the various capacitors connected in parallel at the output voltage. Although ceramic capacitors are generally known for low ESR (especially X5R and X7R), these capacitors suffer from a relatively high voltage coefficient. Therefore, it is not safe to assume that the entire ripple current flows in the ceramic capacitor. Aluminum electrolytic capacitors are generally chosen because of their high bulk capacitance, but they have a relatively high ESR. As a result, some amount of ripple current will flow in this capacitor. If the ripple current flowing into a capacitor exceeds its RMS rating, the capacitor will heat up, reducing its effective capacitance and adversely affecting its reliability. After the output capacitor configuration has been determined using the equations provided, measure the individual capacitor case temperatures in order to verify good thermal performance.

Setting Output Voltage

The LTC3871/LTC3871-1 output voltage is set by two external feedback resistive dividers carefully placed across V_{HIGH} to ground and V_{LOW} to ground, as shown in Figure 6. The regulated output voltage is determined by:

$$V_{LOW} = 1.2V \bullet \left(1 + \frac{R_B}{R_A}\right) \text{ and } V_{HIGH} = 1.2V \bullet \left(1 + \frac{R_D}{R_C}\right)$$

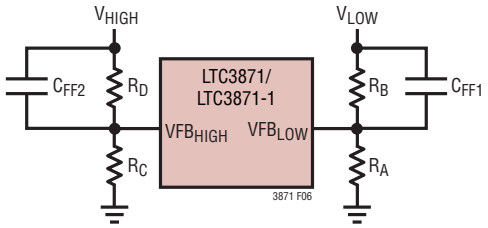

Figure 6. Setting Output Voltage

To improve the frequency response, a feed forward capacitor, C_{FF1}/C_{FF2}, may be used. Great care should be taken to route the feedback line away from noise sources, such as the inductor or the SW line.

External Soft-Start

The LTC3871/LTC3871-1 has the ability to soft-start by itself using the internal soft-start or at a slower rate with an external capacitor on the SS pin. The controller is in the shutdown state if its RUN pin voltage is below 1.14V and its SS pin is actively pulled to ground in this shutdown state. If the RUN pin voltage is above 1.22V, the controller powers up. Once V5 passes its UVLO threshold and power on reset delay expires, a soft-start current of 1.25μA then starts to charge the SS soft-start capacitor. Note that soft-start is achieved not by limiting the maximum V_{LOW} output current of the controller but by controlling the output ramp voltage according to the ramp rate on the SS pin. Current foldback is disabled until the SS pin charges up and external soft-start is complete. However, current foldback is always enabled when internal soft-start is used. The soft-start range is defined to be the voltage range from 0V to 1.2V on the SS pin. The total soft-start time can be calculated as:

$$t_{SOFTSTART} = 1.2 \bullet \frac{C_{SS}}{1.25\mu A}$$

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The Internal LDOs

The LTC3871/LTC3871-1 features three internal PMOS LDOs that supplies power to DRV_{CC} from either the V_{HIGH} or V_{LOW} supply, and also generates the V5 rail from DRV_{CC}. DRV_{CC} powers the top and bottom gate drive circuits, and V5 powers the LTC3871/LTC3871-1's internal circuitry.

There are two DRV_{CC} LDOs—one that generates DRV_{CC} from V_{HIGH} (LDO1) and another that generates DRV_{CC} from V_{LOW} (LDO2), thus allowing the part to start up with just one of the two rails present! Only one of them is active at any given time. If V_{LOW} is higher than the $EXTV_{CC}$ switchover threshold, LDO2 is active; if it is below the switchover threshold, LDO1 is active. The DRV_{CC} pin regulation voltage is determined by the state of the DRVSET pin. The DRVSET pin is a 5-level logic. When DRVSET is either grounded, floated or tied to V5, the typical value for the DRV_{CC} voltage will be 6V, 8V and 10V respectively. Use the 10V setting with careful PCB layout. This is because any overshoot between BOOST and SW would exceed the ABS max voltage of 11V for the floating driver. Set DRV_{CC} to one-fourth of V5 and three-fourths of V5 for 7V and 9V DRV_{CC} voltages. Setting DRVSET using a resistor divider off of V5 will allow the DRVSET setting to not change when the 5.5V LDO is in dropout at start-up. Please note that the DRVSET pin has an internal 200k pull-down to SGND and a 200k pull-up to V5. The $EXTV_{CC}$ turn on threshold is the selected DRV_{CC} regulation voltage minus 500mV. The turn off threshold is 500mV below the turn on threshold.

The V5 LDO regulates the voltage at the V5 pin to 5.5V when DRV_{CC} is at least 6V. The LDO can supply a peak current of 20mA and must be bypassed to ground with a minimum of 4.7µF ceramic capacitor or low ESR electrolytic capacitor. No matter what type of bulk capacitor is used, an additional 0.1µF ceramic capacitor placed directly adjacent to the V5 and SGND pins is highly recommended.

Fault Conditions: Current Limit and Current Foldback

In buck mode, the LTC3871/LTC3871-1 includes current foldback to help limit power dissipation when the V_{LOW} is shorted to ground. On the LTC3871, if the V_{LOW} falls below 85% of its nominal output level, then the maximum sense voltage is progressively lowered from its maximum programmed value to one-third of the maximum value. On the LTC3871-1, current foldback begins when V_{LOW} falls below 33% of its nominal output level, and the maximum sense voltage is progressively lowered to one-third of the maximum value. Under short-circuit conditions with very low duty cycles, the LTC3871/LTC3871-1 will begin cycle skipping in order to limit the short-circuit current. In this situation the bottom MOSFET will be dissipating most of the power but less than in normal operation. The short circuit ripple current is determined by the minimum on-time $t_{ON(MIN)}$ of the LTC3871/LTC3871-1, the V_{HIGH} voltage and inductor value:

$$\Delta I_{L(SC)} = t_{ON(MIN)} \bullet \frac{V_{HIGH}}{L}$$

The resulting short-circuit current is:

$$I_{SC} = \left(\frac{1/3 V_{SENSE(MAX)}}{R_{SENSE}} - \frac{1}{2} \Delta I_{L(SC)} \right)$$

After a short, or while starting up, make sure that the load current takes the folded-back current limit into account. Current foldback is disabled in boost mode.

Phase-Locked Loop and Frequency Synchronization

The LTC3871/LTC3871-1 has a phase-locked loop (PLL) comprised of an internal voltage-controlled oscillator (VCO) and a phase detector. This allows the turn-on of the top MOSFET to be locked to the rising edge of an external clock signal applied to the SYNC pin. The phase detector is an edge sensitive digital type that provides zero degrees phase shift between the external and internal oscillators. This type of phase detector does not exhibit false lock to harmonics of the external clock.

The output of the phase detector is a pair of complementary current sources that charge or discharge the internal filter network. There is a precision 20µA current flowing out of the FREQ pin. This allows the user to use a single resistor to SGND to set the switching frequency when no external clock is applied to the SYNC pin. The internal switch between the FREQ pin and the integrated PLL filter network is on, allowing the filter network to be pre-charged at the same voltage as of the FREQ pin. The relationship between the voltage on the FREQ pin and

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operating frequency is shown in Figure 8 and specified in the Electrical Characteristics table. If an external clock is detected on the SYNC pin, the internal switch mentioned above turns off and isolates the influence of the FREQ pin. Note that the LTC3871/LTC3871-1 can only be synchronized to an external clock whose frequency is within range of the LTC3871/LTC3871-1's internal VCO. A simplified block diagram is shown in Figure 7.

If the external clock frequency is greater than the internal oscillator's frequency, f_{OSC}, then current is sourced continuously from the phase detector output, pulling up the filter network. When the external clock frequency is less than f_{OSC}, current is sunk continuously, pulling down the filter network. If the external and internal frequencies

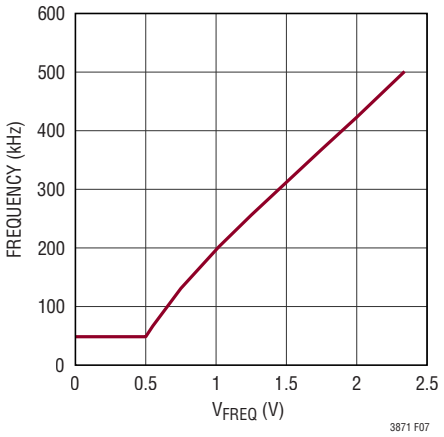

Figure 7. Relationship Between Oscillator Frequency and Voltage at the FREQ Pin

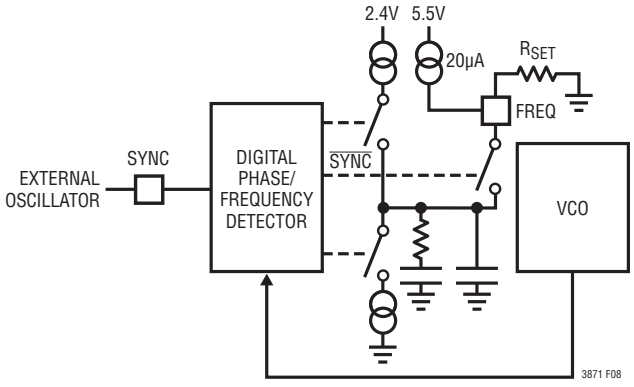

Figure 8. Phase-Locked Loop Block Diagram

are the same but exhibit a phase difference, the current sources turn on for an amount of time corresponding to the phase difference. The voltage on the filter network is adjusted until the phase and frequency of the internal and external oscillators are identical. At the stable operating point, the phase detector output is high impedance and the filter capacitor holds the voltage.

Typically, the external clock (on the SYNC pin) input high threshold is 2V, while the input low threshold is 1.2V.

The LTC3871/LTC3871-1 switching frequency is determined by:

$$\text{Frequency} = [335.8k \bullet V_{(FREQ)}] - [32.7k \bullet V_{(FREQ)}{}^2] - 106.5k$$

Where, $V_{(FREQ)} = I_{FREQ}$ (from spec table) $\bullet R_{(FREQ)}$

Or,

$$\text{Frequency} = [6.72 \bullet R_{(FREQ)}] - [1.3E\text{-}5 \bullet R_{(FREQ)}{}^2] - 106.5k$$

This assumes a perfect 20µA I_{FREQ}.

Shared Pin Connections in Multi-Chip Applications

When multiple LTC3871/LTC3871-1 ICs are used together in high current applications, a number of pins may or may not be connected together at the customer's discretion, trying to balance better communication between the ICs versus increasing the probability of preventing a single point failure.

The LTC3871/LTC3871-1 features CLKOUT and PHSMD pins that allow multiple ICs to be daisy chained together. The clock output signal on the CLKOUT pin can be used to synchronize additional ICs in a 3-, 4-, 6-, 8-, 10- or 12-phase power supply solution feeding a single high current output, or even several outputs from the same input supply. The PHSMD pin is used to adjust the phase relationship between channel 1 and channel 2, as well as the phase relationship between channel 1 and CLKOUT. The phases are calculated relative to zero degrees, defined as the rising edge of TG1. Refer to the Operation section and Figure 2 for more details on PHSMD settings and connections for multiphase applications.

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The SS pins should be tied together to enable every LTC3871/LTC3871-1 IC to startup together. Not connecting them together may result in some phases sourcing a lot of current and others sinking current.

The IMON pins may or may not be tied together, depending on whether the customer wants to monitor the average current per IC or the total average current in the application.

The ILIM, SETCUR, FREQ, MODE, BUCK and DRVSET pins may or may not be tied together based on convenience. When tying these pins together, please be aware of the pull-up/down currents/resistors on these pins! Any external resistor or resistor divider network must take those into account. For example, each FREQ pin sources 20µA. When four LTC3871/LTC3871-1 ICs have their FREQ pins tied together, that is 80µA.

The OV_{LOW}, OV_{HIGH} and UV_{HIGH} pins must be tied together. This enables the entire system to react to an OV/UV condition appropriately. The resistor divider used on these pins must be scaled based on the number of LTC3871/LTC3871-1s paralleled, as these pins have 5µA hysteresis currents that turn on and off.

The ITH_{LOW} and ITH_{HIGH} pins of multiple LTC3871/LTC3871-1s should be tied together. Tying the ITH_{LOW} pins together and the ITH_{HIGH} pins together gives the best current sharing between phases. Each error amplifier's compensation network has to be placed local to the specific IC to minimize jitter and stability issues.

The RUN pins must be tied together – this is very critical for boost mode operation. In boost mode, when multiple LTC3871/LTC3871-1 have their RUN pins connected together, care must be taken to ensure that the logic signal on the RUN pin is a clean fast rising/falling signal so all ICs are enabled at the same instant. If a resistor divider is used on the RUN pin, then the part must be started up in buck mode. Using a resistor divider on the RUN pin off V_{HIGH}, set for a start-up voltage higher than the UV_{HIGH} set point allows the part to soft start cleanly after a UV_{HIGH} fault is cleared.

Minimum On-Time Considerations

Minimum on-time, $t_{ON(MIN)}$, is the smallest time duration that the LTC3871/LTC3871-1 is capable of turning on the top MOSFET. It is determined by internal timing delays, power stage timing delays and the gate charge required to turn on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that:

$$t_{ON(MIN)} < \frac{V_{LOW}}{V_{HIGH}(f)}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the controller will begin to skip cycles. The output voltage and current will continue to be regulated, but the voltage ripple and current ripple will increase. The minimum on-time for the LTC3871/LTC3871-1 is approximately 150ns, with good PCB layout, minimum 30% inductor current ripple and at least 2mV ripple on the current sense signal or equivalent 10mV between $SNSA^+$ and SNS^- pins.

The minimum on-time can be affected by PCB switching noise in the voltage and current loop. As the peak sense voltage decreases, the minimum on-time gradually increases. This is of particular concern in forced continuous applications with low ripple current at light loads. If the duty cycle drops below the minimum on-time limit in this situation, a significant amount of cycle skipping can occur with correspondingly larger current and voltage ripple.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\%Efficiency = 100\% - (L1 + L2 + L3 + ...)$$

where L1, L2, etc. are the individual losses as a percentage of input power.

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Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC3871/LTC3871-1 circuits: 1) IC V_{HIGH} current, 2) MOSFET driver current, 3) I^2R losses, 4) topside MOSFET transition losses.

1. The V_{HIGH} current is the DC supply current given in the Electrical Characteristics table. V_{HIGH} current typically results in a small (<0.1%) loss.

2. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge d_Q moves from the driver supply to ground. The resulting d_Q/d_t is a current out of the driver supply that is typically much larger than the control circuit current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the topside and bottom side MOSFETs.

3. I^2R losses are predicted from the DC resistances of the fuse (if used), MOSFET, inductor and current sense resistor. In continuous mode, the average output current flows through L and R_{SENSE}, but is chopped between the topside MOSFET and the synchronous MOSFET. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L and R_{SENSE} to obtain I^2R losses. For example, if each $R_{DS(ON)} = 10m\Omega$, $R_L = 10m\Omega$, $R_{SENSE} = 5m\Omega$, then the total resistance is $25m\Omega$. This results in losses ranging from 0.6% to 3% as the output current increases from 3A to 15A for a 12V output.

   Efficiency varies as the inverse square of V_{LOW} for the same external components and output power level. The combined effects of increasingly lower output voltages and higher currents required by high performance digital systems is not doubling but quadrupling the importance of loss terms in the switching regulator system!

4. Transition losses apply only to the topside MOSFET(s), and become significant only when operating at high input voltages (typically 15V or greater). Transition losses can be estimated from:

   Transition Loss = $(1.7)\ V_{HIGH}^2 \bullet I_{O(MAX)} \bullet C_{RSS} \bullet f$
   $I_{O(MAX)}$ = Maximum Load on V_{LOW}

Other hidden losses such as copper trace and internal battery resistances can account for an additional 5% to 10% efficiency degradation in portable systems. It is very important to include these system level losses during the design phase. The internal battery and fuse resistance losses can be minimized by making sure that C_{HIGH} has adequate charge storage and very low ESR at the switching frequency. Other losses including Schottky conduction losses during dead time and inductor core losses generally account for less than 2% total additional loss.

Checking Transient Response

The regulator loop response can be checked by looking at the load current transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{LOW} shifts by an amount equal to $\Delta I_{LOAD} \bullet ESR$, where ESR is the effective series resistance of C_{OUT} at V_{LOW}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating the feedback error signal that forces the regulator to adapt to the current change and return V_{LOW} to its steady-state value. During this recovery time V_{LOW} can be monitored for excessive overshoot or ringing, which would indicate a stability problem. The availability of the ITH pin not only allows optimization of control loop behavior but also provides a DC-coupled and AC-filtered closed-loop response test point. The DC step, rise time and settling at this test point truly reflects the closed-loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin. The ITH external components shown in the Typical Application circuit will provide an adequate starting point for most applications. The ITH series RC-CC filter sets the dominant pole-zero loop compensation. The values can be modified slightly (from 0.5 to 2 times their suggested values) to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because the various types and values determine the loop gain and phase. An output current pulse of 20% to 80% of full-load current having a rise time of 1µs to 10µs will produce output voltage and ITH pin waveforms

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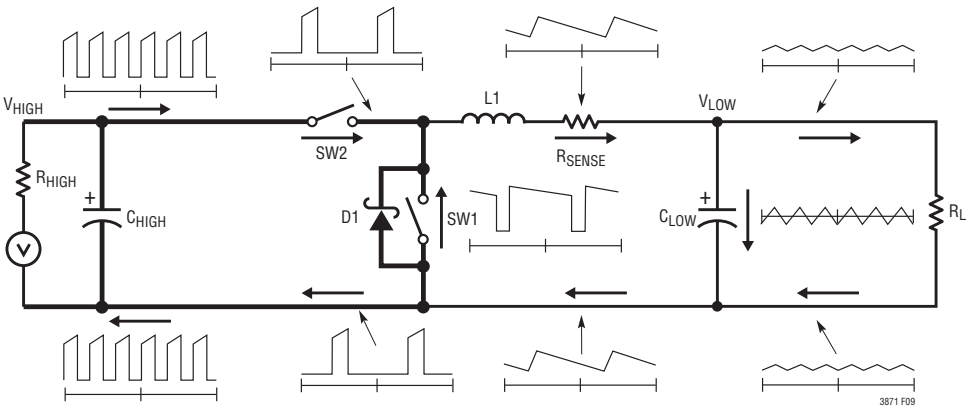
that will give a sense of the overall loop stability without breaking the feedback loop. Placing a power MOSFET directly across the output capacitor and driving the gate with an appropriate signal generator is a practical way to produce a realistic load step condition. The initial output voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop, so this signal cannot be used to determine phase margin. This is why it is better to look at the ITH pin signal which is in the feedback loop and is the filtered and compensated control loop response. The gain of the loop will be increased by increasing RC and the bandwidth of the loop will be increased by decreasing CC. If RC is increased by the same factor that CC is decreased, the zero frequency will be kept the same, thereby keeping the phase shift the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{LOW}, causing a rapid drop in V_{LOW}. No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage if the load switch resistance is low and it is driven quickly. If the ratio of C_{LOAD} to C_{OUT} is greater than 1:50, the switch rise time should be controlled so that the load rise time is limited to approximately 25 • C_{LOAD}. Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC. These items are also illustrated graphically in the layout diagram of Figure 9. Check the following in the PC layout:

1. The DRV_{CC} bypass capacitor should be placed immediately adjacent to the IC between the DRV_{CC} pin and the GND plane. A 1µF ceramic capacitor of the X7R or X5R type is small enough to fit very close to the IC. An additional 4.7µF to 10µF of ceramic, tantalum or other very low ESR capacitance is recommended in order to keep the internal IC supply quiet.
2. The V5 bypass capacitor should be placed immediately adjacent to the IC between the V5 and the SGND pins. A 4.7µF to 10µF capacitor of ceramic, tantalum or other very low ESR capacitance is recommended.
3. Place the feedback divider between the + and – terminals of C_{LOW}/C_{HIGH}. Route VFB_{LOW}/VFB_{HIGH} with minimum PC trace spacing from the IC to the feedback dividers.
4. Are the $SNSA^+$, $SNSD^+$ and SNS^- printed circuit traces routed together with minimum PC trace spacing? The filter capacitors between $SNSA^+$, $SNSD^+$ and SNS^- should be as close as possible to the pins of the IC.
5. Do the (+) plates of C_{HIGH} decoupling cap connect to the drain of the topside MOSFET as closely as possible? This capacitor provides the pulsed current to the MOSFET.



BOLD LINES INDICATE HIGH, SWITCHING CURRENTS. KEEP LINES TO A MINIMUM LENGTH

Figure 9. Branch Current Waveforms (Buck Mode Shown)

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6. Keep the switching nodes away from sensitive small-signal nodes ($SNSD^+$, $SNSA^+$, SNS^-, V_{FB}). Ideally the switch nodes printed circuit traces should be routed away and separated from the IC and especially the quiet side of the IC. Separate the high d_V/d_t traces from sensitive small-signal nodes with ground traces or ground planes.

7. Use a low impedance source such as a logic gate to drive the SYNC pin and keep the PCB trace as short as possible.

8. The 47pF to 330pF ceramic capacitor between the ITH pins and signal ground should be placed as close as possible to the IC. Figure 9 illustrates all branch currents in a switching regulator. It becomes very clear after studying the current waveforms why it is critical to keep the high switching current paths to a small physical size. High electric and magnetic fields will radiate from these loops just as radio stations transmit signals. The output capacitor ground should return to the negative terminal of the input capacitor and not share a common ground path with any switched current paths. The left half of the circuit gives rise to the noise generated by a switching regulator. The ground terminations of the synchronous MOSFET and Schottky diode should return to the bottom plate(s) of the input capacitor(s) with a short isolated PC trace since very high switched currents are present. External OPTI-LOOP® compensation allows overcompensation for PC layouts which are not optimized, but this is not the recommended design procedure.

Special Layout Consideration

1. Exceeding ABS Max ratings on the sense pins can result in damage to the controller. As the $SNS1^-$/$SNS2^-$ pins are connected directly to V_{LOW}, it is recommended that a fast acting diode with an appropriately high voltage rating be used to clamp these pins to reduce voltage spiking below ground. The diodes should be placed close to the controller IC, with the cathode connected to $SNS1^-$ or $SNS2^-$ and the anode connected to ground.

2. The TG traces from the controller IC to the gate of the external MOSFET should be kept as short as possible to minimize the parasitic inductance. This inductance can cause voltage spikes that can potentially exceed the ABS Max rating of the drivers and damage them. A 3Ω resistor and 1nF capacitor can be used to filter these spikes as shown in Figure 10. When using the 9V/10V DRV_{SET} settings, or if the TG traces are longer than 25mm, this filter network must be used on both TG1 and TG2. The 1nF capacitor should be placed as close to the TG/SW pins as possible.

3. Exceeding Absolute Max ratings on the $EXTV_{CC}$ pin can result in damage to the controller. As the $EXTV_{CC}$ pin is normally connected to V_{LOW}, it is recommended to put a Schottky diode with an appropriately high voltage rating between the V_{LOW} and the $EXTV_{CC}$ pins as shown in Figure 11a. Choose the right Schottky diode with the forward voltage less than 0.5V at the maximum $EXTV_{CC}$ pin current.

4. Another method to protect the $EXTV_{CC}$ pin is to use a Schottky diode to clamp the $EXTV_{CC}$ pin to reduce voltage spiking below ground. The Schottky diode should be placed close to the controller IC, with the cathode connected to the $EXTV_{CC}$ pin and the anode connected to ground as shown in the Figure 11b. Choose a 10Ω R_{FLTR} and keep the maximum voltage drop across the R_{FLTR} less than 0.5V.

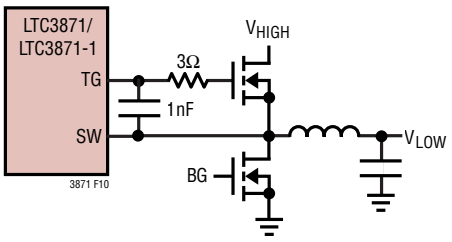

Figure 10. Filter for TG Traces > 25mm

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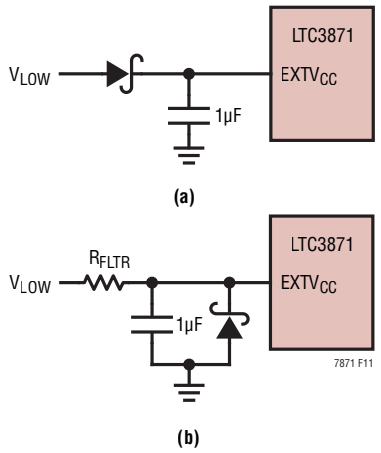

Figure 11. Methods to Protect the $EXTV_{CC}$ Pin

Design Example

As a design example for a two-phase single output high current regulator, assume V_{HIGH} = 48V (nominal), V_{HIGH} = 60V (maximum), V_{LOW} = 12V, $V_{LOW}I_{MAX}$ = 40A (20A/phase), and f = 120kHz (see Figure 12). The regulated output voltages are determined by: V_{LOW} = 1.2V • (1 + RB/RA).

Using 10k 1% resistors from VFB_{LOW} node to ground, the top feedback resistors are (to the nearest 1% standard value) 90.9k and 10k. The frequency is set by biasing the FREQ pin to 0.7V (see Figure 8). The inductance values are based on a 35% maximum ripple current assumption (7A for each phase). The highest value of ripple current occurs at the maximum V_{HIGH} voltage:

$$L = \frac{V_{LOW}}{f \bullet \Delta I_{L(MAX)}} \bullet \left(1 - \frac{V_{LOW}}{V_{HIGH(MAX)}}\right)$$

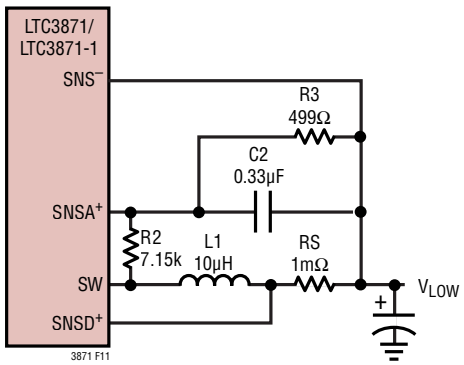

Figure 12. Design Example

Each phase will require 11.4µH. The Coilcraft SER2918H-103, 10µH, 2.6mΩ inductor is chosen. At the nominal V_{HIGH} voltage (48V), the ripple current will be:

$$\Delta I_{L(NOM)} = \frac{V_{LOW}}{f \bullet L} \bullet \left(1 - \frac{V_{LOW}}{V_{HIGH(NOM)}}\right)$$

Each phase will have 7.5A (37.5%) ripple. The peak inductor current will be the maximum DC value plus one-half the ripple current, or 23.8A. The minimum on-time at the maximum V_{HIGH}, and should not be less than 150ns:

$$T_{ON(MIN)} = \frac{V_{LOW}}{V_{HIGH(MAX)} \bullet f} = \frac{12V}{60V \bullet 120kHz} = 1.7\mu s$$

With ILIM floating, the equivalent R_{SENSE} resistor value can be calculated by using the minimum value for the maximum current sense threshold (33.2mV).

$$R_{SENSE(EQUIV)} = \frac{V_{SENSE(MIN)}}{I_{LOAD(MAX)} + \frac{\Delta I_{L(NOM)}}{2}}$$

The equivalent required R_{SENSE} value is 1.4mΩ. Choose R_S = 1mΩ to allow some design margin. Set R3 to be below 1/10th of the R2. Therefore, the DC component of the $SNSA^+$ filter is small enough to be omitted. R2 • C2 should have a bandwidth that is four times as high as the L/R_S.

Typically, C2 is selected in the range of 0.047µF to 0.47µF. If C2 is chosen to be 0.33µF, R2 and R3 will be 7.15k and 499Ω respectively. The bias current at $SNSD^+$ and $SNSA^+$ is about 10nA and 100nA respectively, and it causes some small error to the current sense signal.

The power dissipation on the topside MOSFET can be easily estimated. Set the gate drive voltage (DRV_{CC}) to be 9V. Choosing an Infineon BSC097N06NS MOSFET results in:

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$R_{DS(ON)}$ = 9.7mΩ (max), V_{MILLER} = 5.2V, $C_{MILLER} \cong$ 32pF. At maximum input voltage with T_J (estimated) = 75°C:

$$P_{MAIN} = \left(\frac{12V}{48V} \bullet (20A)^2 \bullet (1 + 0.005(75°C - 25°C)) \bullet 0.0097\Omega\right) + \left(\frac{(48V)^2 \bullet 23.8A}{2} \bullet 2\Omega \bullet 32pF \bullet \left(\frac{1}{9V - 5.2V} + \frac{1}{5.2V}\right) \bullet 120kHz\right)$$

$$= 1.21W + 96mW$$

$$= 1306mW$$

An Infineon BSC028N06NS, $R_{DS(ON)}$ = 2.8mΩ, C_{OSS} = 660pF is chosen for the bottom FET. The resulting power loss is:

$$PSYNC = \frac{48V - 12V}{48V} \bullet 20A^2 \bullet (1 + ((0.005) \bullet (75°C - 25°C))) \bullet 0.0028\Omega$$

$$P_{SYNC} = 1.05W$$

The power to charge the MOSFET's output capacitance is imposed on the topside MOSFET as well:

$$PC_{OSS} = 660pF \bullet (48V)^2 \bullet \frac{120kHz}{2} = 91mW$$

C_{IN} at V_{HIGH} is chosen for an equivalent RMS current rating of at least 20A. C_{OUT} at V_{LOW} is chosen with an equivalent ESR of 10mΩ for low output ripple. The V_{LOW} output ripple in continuous mode will be highest at the maximum V_{HIGH} voltage. The V_{LOW} output voltage ripple due to ESR is approximately:

$$V_{LOWRIPPLE} = R_{ESR(\Delta IL)} = 0.01\Omega \bullet 7.5A = 75mV_{P-P}$$

Further reductions in V_{LOW} output voltage ripple can be made by placing a 100µF ceramic capacitor across C_{LOW}.

If the output load is a battery, the voltage loop is first set for the desired output voltage and then the charge current can be regulated using the current regulation loop – via the SETCUR and IMON pins. Selecting a maximum charge current of 20A, the desired SETCUR pin voltage is calculated using:

$$V_{SETCUR} = 1.25V + \frac{[38 \bullet 20A \bullet 1m\Omega]}{2} = 1.63V$$

The SETCUR pin can be driven by an ADC's output to 1.63V for the best accuracy. If one is not available, the 7.5µA current sourced out of the SETCUR pin can be used to set the voltage with a resistor from SETCUR to ground, calculated using:

$$R_{SETCUR} = \frac{1.63V}{7.5\mu A} = 217k\Omega$$

A 1% or more accurate 217kΩ resistor should be used.

TYPICAL APPLICATIONS

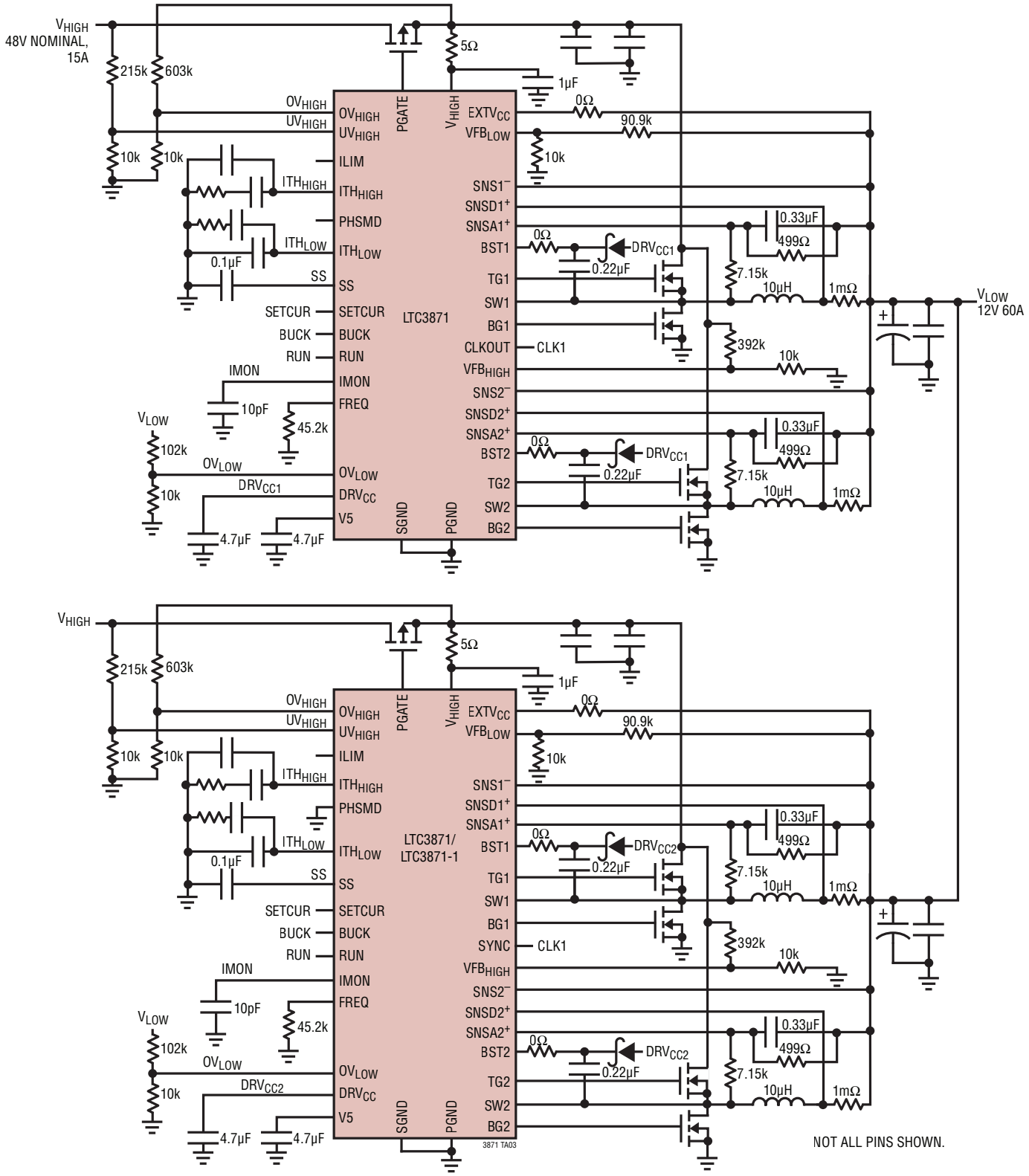
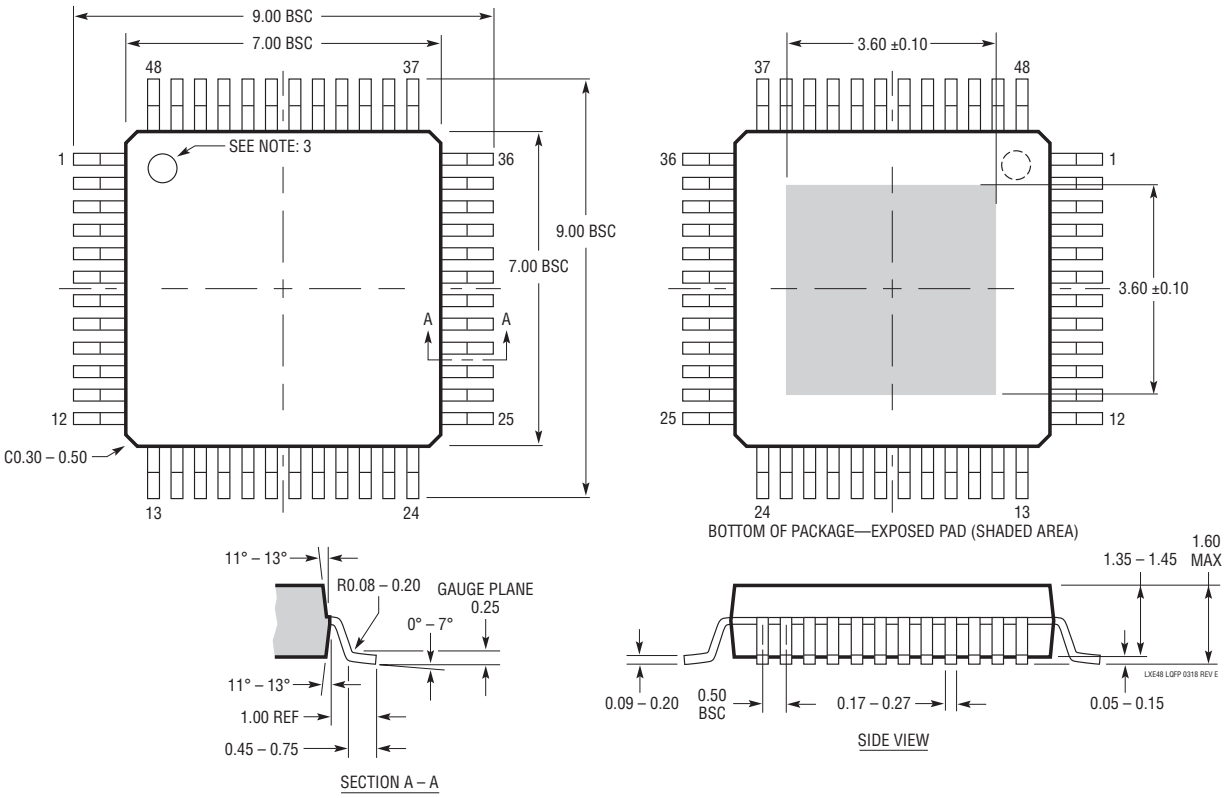


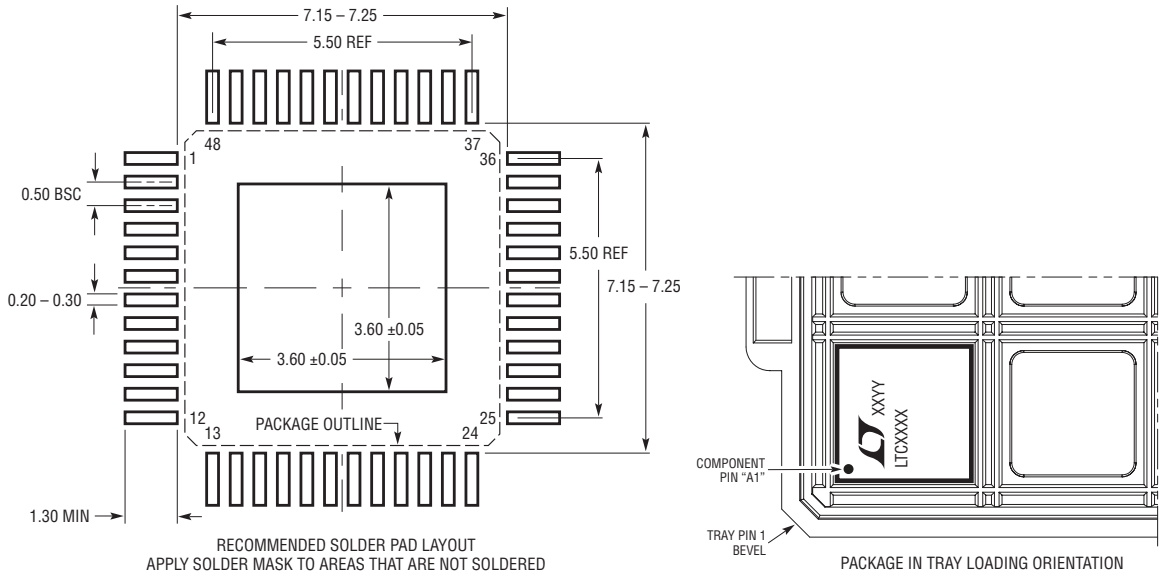
Figure 13. High Efficiency 12V, 60A 4-Phase Supply

PACKAGE DESCRIPTION

LXE Package
48-Lead Plastic Exposed Pad LQFP (7mm × 7mm)
(Reference LTC DWG #05-08-1832 Rev E)
Exposed Pad Variation BB



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DIMENSIONS OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.25mm (10 MILS) BETWEEN THE LEADS AND ON ANY SIDE OF EXPOSED PAD, MAX 0.50mm (20 MILS) AT CORNER OF EXPOSED PAD, IF PRESENT
3. PIN-1 INDENTIFIER IS A MOLDED INDENTATION
4. DRAWING IS NOT TO SCALE



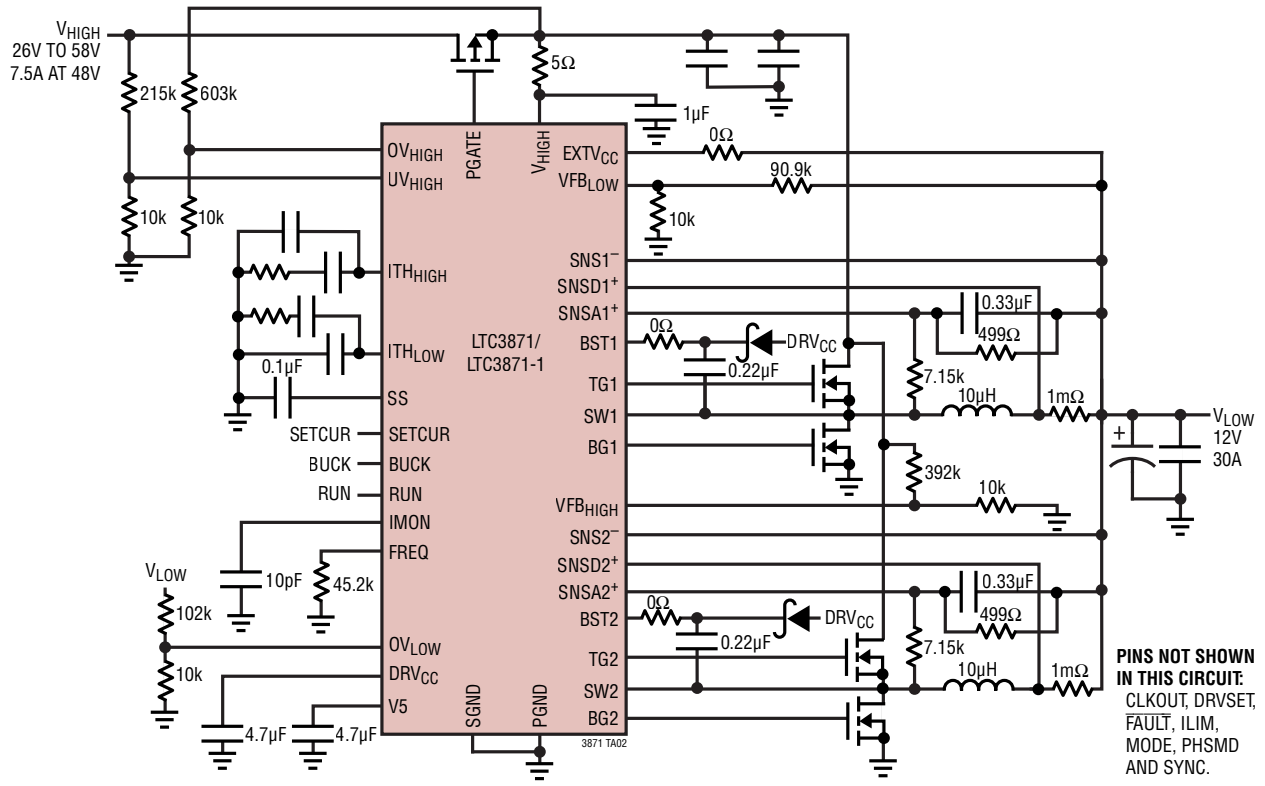
Rev. C

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	12/18	Added LTC3871-1	1, 2, 3, 7, 14, 25
B	10/19	Modified Current Sense Voltages Max Ratings Changed V_{SETCUR} Equation	2 32
C	04/24	Included AECQ Statement Automotive Flow Devices Listed in Order Information	1 2

TYPICAL APPLICATION

High Efficiency PolyPhase Bidirectional Charger/Supply



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3784	60V PolyPhase® Synchronous Boost Controller	4.5V (Down to 2.3V After Start-Up) ≤ V_{IN} ≤ 60V, V_{OUT} Up to 60V, I_Q = 28µA PLL Fixed Frequency 50kHz to 900kHz, 3mm × 3mm QFN-16, MSOP-16E
LTC3769	60V Synchronous Boost Controller	4.5V (Down to 2.5V After Start-Up) ≤ V_{IN} ≤ 60V, V_{OUT} Up to 60V, I_Q = 28µA PLL Fixed Frequency 50kHz to 900kHz, 4mm × 4mm QFN-24, TSSOP-20E
LTC3899	Triple Output, Buck/Buck/Boost Synchronous Controller with Adjustable Gate Drive Voltage	4.5V (Down to 2.2V After Start-Up) ≤ V_{IN} ≤ 60V, V_{OUT} Up to 60V, I_Q = 29µA Buck V_{OUT} Range: 0.8V to 0.99V_{IN}, Boost V_{OUT} Up to 60V
LTC3890/LTC3890-1/ LTC3890-2	60V, Low I_Q, Dual 2-Phase Synchronous Step-Down DC/DC Controller with 99% Duty Cycle	PLL Fixed Frequency 50kHz to 900kHz, 4V ≤ V_{IN} ≤ 60V, 0.8V ≤ V_{OUT} ≤ 24V, I_Q = 50µA
LTC3892/ LTC3892-1	60V Low I_Q, Dual, 2-Phase Synchronous Step-Down DC/DC Controller with Adjustable Gate Drive	PLL Fixed Frequency 50kHz to 900kHz, 4.5V ≤ V_{IN} ≤ 60V, 0.8V ≤ V_{OUT} ≤ 0.99V_{IN}, I_Q = 29µA
LT®8710	Synchronous SEPIC/Inverting/Boost Controller with Output Current Control	4.5V ≤ V_{IN} ≤ 80V, Rail-to-Rail Output Current Monitor and Control, Power Good
LT8705	80V V_{IN} and V_{OUT} Synchronous 4-Switch Buck-Boost DC/DC Controller	PLL Fixed Frequency 100kHz to 400kHz, 2.8V ≤ V_{IN} ≤ 80V, 1.3V ≤ V_{OUT} ≤ 80V
LTM®8056	58V_{IN}, 48V_{OUT} Buck-Boost µModule® Regulator	PLL Fixed Frequency 200kHz to 700kHz, 5V ≤ V_{IN} ≤ 58V, 1.2V ≤ V_{OUT} ≤ 48V, Input/Output Current Monitors