



## Product Change Notification / SYST-12DFRS700

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**Date:**

13-May-2022

**Product Category:**

Linear Op Amps

**PCN Type:**

Document Change

**Notification Subject:**

Data Sheet - MCP6V51 Data Sheet Document Revision

**Affected CPNs:**

[SYST-12DFRS700\\_Affected\\_CPN\\_05132022.pdf](#)

[SYST-12DFRS700\\_Affected\\_CPN\\_05132022.csv](#)

**Notification Text:**

SYST-12DFRS700

Microchip has released a new Product Documents for the MCP6V51 Data Sheet of devices. If you are using one of these devices please read the document located at [MCP6V51 Data Sheet](#).

**Notification Status:** Final

**Description of Change:** Added MCP6V52 and MCP6V54 devices.

**Impacts to Data Sheet:** See above details.

**Reason for Change:** To Improve Productivity

**Change Implementation Status:** Complete

**Date Document Changes Effective:** 13 May 2022

**NOTE:** Please be advised that this is a change to the document only the product has not been changed.

**Markings to Distinguish Revised from Unrevised Devices:** N/A

## Attachments:

[MCP6V51 Data Sheet](#)

Please contact your local [Microchip sales office](#) with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

MCP6V51-E/MS

MCP6V51-I/WMMOD

MCP6V51T-E/MS

MCP6V51T-E/OT

MCP6V52-E/MS

MCP6V52-E/SN

MCP6V52T-E/MS

MCP6V52T-E/SN

MCP6V54-E/SL

MCP6V54T-E/SL

## 45V, 2 MHz Zero-Drift Op Amp with EMI Filtering

### Features

- High DC Precision:
  - $V_{OS}$  Drift: 36 nV/°C (max.)
  - $V_{OS}$ : 15  $\mu$ V (max.)
  - Open-Loop Gain: 140 dB (min.)
  - PSRR: 134 dB (min.)
  - CMRR: 135 dB (min.)
- Low Noise:
  - 10.2 nV/ $\sqrt{\text{Hz}}$  at 1 kHz
  - $E_{ni}$ : 0.21  $\mu$ V<sub>P-P</sub>, f = 0.1 Hz to 10 Hz
- Low Power:
  - $I_Q$ : 470  $\mu$ A/Amplifier (typ.)
  - Wide Single or Dual Supply Voltage Range: 4.5V to 45V,  $\pm 2.25$ V to  $\pm 22.5$ V
- Easy to Use:
  - Input Range incl. Negative Rail
  - Rail-to-Rail Output
  - EMI Filtered Inputs
  - Gain Bandwidth Product: 2 MHz
  - Slew Rate 1.2V/ $\mu$ s
  - Unity Gain Stable
- Small Packages:
  - Single: SOT-23-5, MSOP-8
  - Dual: MSOP-8, SOIC-8
  - Quad: SOIC-14
- Extended Temperature Range: -40°C to +125°C

### Typical Applications

- Industrial Instrumentation, PLC
- Process Control
- Power Control Loops
- Sensor Conditioning
- Electronic Weight Scales
- Medical Instrumentation
- Automotive Monitors
- High/Low-Side Current Sensing

### Design Aids

- Microchip Advanced Part Selector (MAPS)
- SPICE Macro Models
- Application Notes

### Related Parts

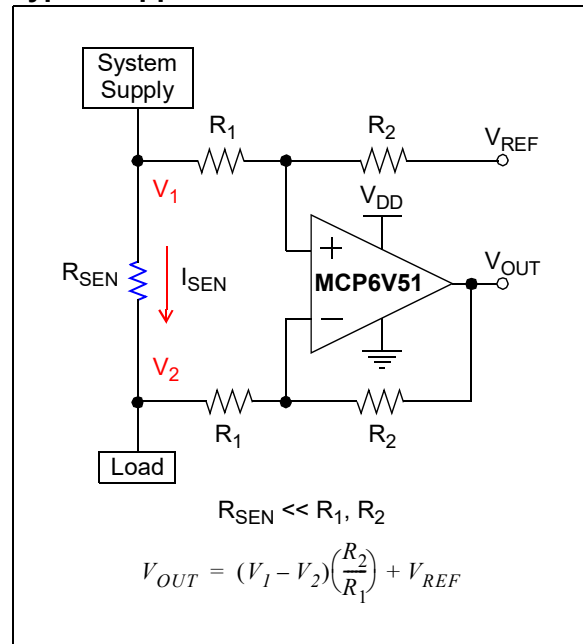
- [MCP6V71/1U/2/4: Zero-Drift, 2 MHz, 1.8V to 5V](#)
- [MCP6V81/1U/2/4: Zero-Drift, 5 MHz, 1.8V to 5V](#)

### General Description

The Microchip Technology MCP6V51/2/4 operational amplifiers employ dynamic offset correction for very low offset and offset drift. These devices have a gain bandwidth product of 2 MHz (typical). They are unity gain stable, have virtually no 1/f noise and excellent Power Supply Rejection Ratio (PSRR) and Common-Mode Rejection Ratio (CMRR). These products operate with a single or dual supply voltage that can range from 4.5V to 45V ( $\pm 2.25$ V to  $\pm 22.5$ V), while drawing 470  $\mu$ A/amp (typical) of quiescent current.

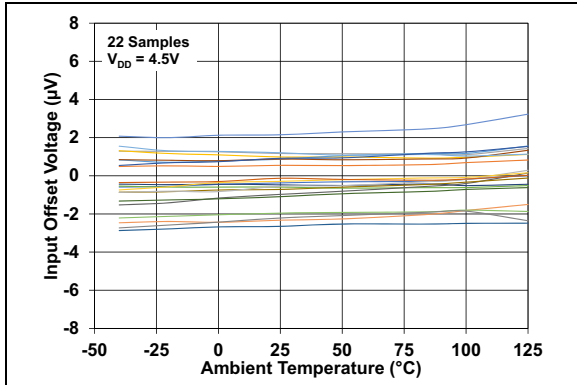
The MCP6V51/2/4 op amps are offered as single, dual and quad channel amplifiers, and are designed using an advanced CMOS process.

### Typical Application Circuit

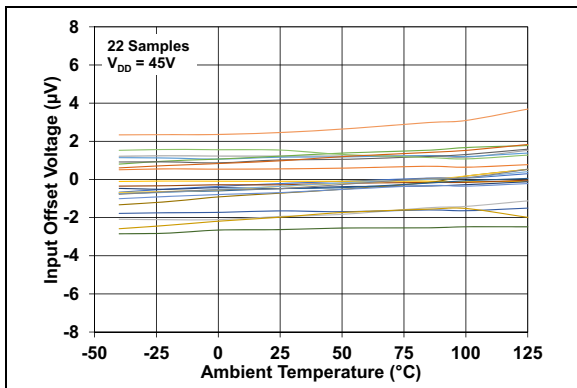


# MCP6V51/2/4

Figure 1 and Figure 2 show input offset voltage versus ambient temperature for different power supply voltages.



**FIGURE 1:** *Input Offset Voltage vs. Ambient Temperature with  $V_{DD} = 4.5V$ .*



**FIGURE 2:** *Input Offset Voltage vs. Ambient Temperature with  $V_{DD} = 45V$ .*

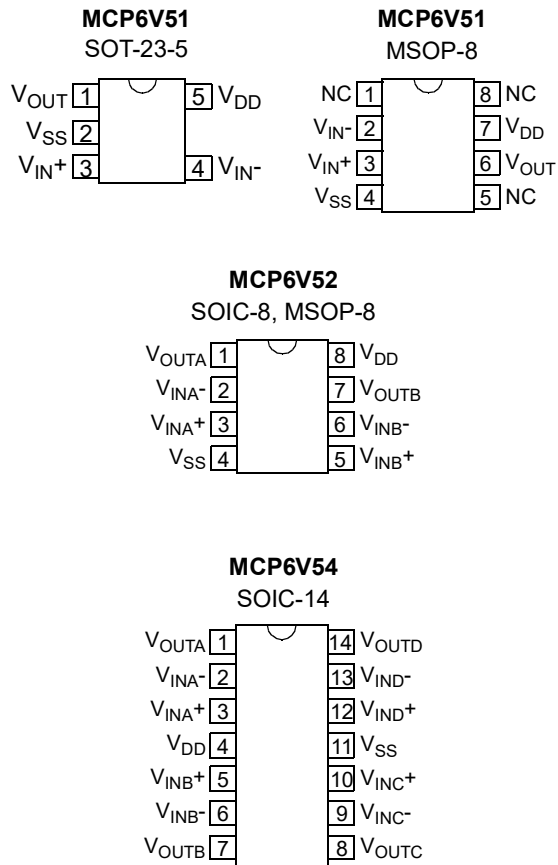
As seen in Figure 1 and Figure 2, the MCP6V51/2/4 op amps have excellent performance across temperature.

The input offset voltage temperature drift ( $TC_1$ ) shown is well within the specified maximum values of:

31 nV/°C at  $V_{DD} = 4.5V$  and 36 nV/°C at  $V_{DD} = 45V$ .

This performance supports applications with stringent DC precision requirements. In many cases, it will not be necessary to correct for temperature effects (i.e., calibrate) in a design. In the other cases, the correction will be small.

## Package Types



## 1.0 ELECTRICAL CHARACTERISTICS

### 1.1 Absolute Maximum Ratings<sup>†</sup>

$V_{DD} - V_{SS}$ .....	49.5V
Current at Input Pins ( <b>Note 1</b> ) .....	±5 mA
Analog Inputs ( $V_{IN+}$ and $V_{IN-}$ ) .....	$V_{SS} - 0.5V$ to $V_{DD} + 0.5V$
All Other Inputs and Outputs .....	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
Differential Input Voltage ( <b>Note 1</b> ) .....	±9V
Output Short-Circuit Current .....	Continuous
Current at Output and Supply Pins .....	±50 mA
Storage Temperature .....	-65°C to +150°C
Maximum Junction Temperature .....	+150°C
ESD Protection on All Pins (HBM, CDM, MM) .....	≥ 2 kV, 750V, 200V

**† Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Note 1:** The inputs are clamped by internal back-to-back diodes. If differential input voltages exceed ±9V, the current must be limited to 5 mA or less. Also, see [Section 4.2.1 “Input Protection”](#).

### 1.2 Electrical Specifications

#### DC ELECTRICAL SPECIFICATIONS

**Electrical Characteristics:** Unless otherwise indicated,  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = +4.5V$  to  $+45V$ ,  $V_{SS} = \text{GND}$ ,  $V_{CM} = V_{DD}/3$ ,  $V_{OUT} = V_{DD}/2$ ,  $V_L = V_{DD}/2$ ,  $R_L = 10\text{ k}\Omega$  to  $V_L$  and  $C_L = 100\text{ pF}$  (refer to [Figure 1-4](#) and [Figure 1-5](#)).

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
<b>Input Offset</b>						
Input Offset Voltage	$V_{OS}$	-15	±2.4	+15	μV	$T_A = +25^\circ\text{C}$
Input Offset Voltage Drift with Temperature (Linear Temp. Co.)	$TC_1$	-31	±5	+31	nV/°C	$T_A = -40$ to $+125^\circ\text{C}$ , $V_{DD} = 4.5V$ ( <b>Note 1</b> )
	$TC_1$	-36	±7	+36	nV/°C	$T_A = -40$ to $+125^\circ\text{C}$ , $V_{DD} = 45V$ ( <b>Note 1</b> )
Input Offset Voltage Quadratic Temperature Co.	$TC_2$	—	±42	—	nV/°C <sup>2</sup>	$T_A = -40$ to $+125^\circ\text{C}$ , $V_{DD} = 4.5V$
	$TC_2$	—	±38	—	nV/°C <sup>2</sup>	$T_A = -40$ to $+125^\circ\text{C}$ , $V_{DD} = 45V$
Input Offset Voltage Aging	$\Delta V_{OS}$	—	±2	—	μV	408 hours Life Test at $+150^\circ\text{C}$ , measured at $+25^\circ\text{C}$
Power Supply Rejection Ratio	PSRR	134	160	—	dB	
		124	138	—	dB	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ , $V_{DD} = 45V$ ( <b>Note 1</b> )

**Note 1:** Not production tested. Limits set by characterization and/or simulation and provided as design guidance only.

**2:** [Figure 2-17](#) shows how  $V_{CML}$  and  $V_{CMH}$  changed across temperature for the first production lot.

# MCP6V51/2/4

## DC ELECTRICAL SPECIFICATIONS (CONTINUED)

**Electrical Characteristics:** Unless otherwise indicated,  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = +4.5\text{V}$  to  $+45\text{V}$ ,  $V_{SS} = \text{GND}$ ,  $V_{CM} = V_{DD}/3$ ,  $V_{OUT} = V_{DD}/2$ ,  $V_L = V_{DD}/2$ ,  $R_L = 10\text{ k}\Omega$  to  $V_L$  and  $C_L = 100\text{ pF}$  (refer to [Figure 1-4](#) and [Figure 1-5](#)).

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
<b>Input Bias Current and Impedance</b>						
Input Bias Current	$I_B$	-250	$\pm 60$	+250	pA	$V_{DD} = 45\text{V}$
Input Bias Current across Temperature	$I_B$	—	$\pm 80$	—	pA	$T_A = +85^\circ\text{C}$
	$I_B$	-4	$\pm 1.4$	+4	nA	$T_A = +125^\circ\text{C}$ ( <a href="#">Note 1</a> )
Input Offset Current	$I_{OS}$	-1	$\pm 0.28$	+1	nA	$V_{DD} = 45\text{V}$
Input Offset Current across Temperature	$I_{OS}$	—	$\pm 0.32$	—	nA	$T_A = +85^\circ\text{C}$
	$I_{OS}$	-8	$\pm 0.45$	+8	nA	$T_A = +125^\circ\text{C}$ ( <a href="#">Note 1</a> )
Common-Mode Input Impedance	$Z_{CM}$	—	120G  3	—	$\Omega$   pF	
Differential Input Impedance	$Z_{DIFF}$	—	2.5M  5.2	—	$\Omega$   pF	
<b>Common-Mode</b>						
Common-Mode Input Voltage Range Low	$V_{CML}$	—	—	$V_{SS} - 0.3$	V	<a href="#">Note 2</a>
Common-Mode Input Voltage Range High	$V_{CMH}$	$V_{DD} - 2.1$	—	—	V	<a href="#">Note 2</a>
Common-Mode Rejection Ratio	CMRR	110	125	—	dB	$V_{DD} = 4.5\text{V}$ , $V_{CM} = -0.3\text{V}$ to $2.4\text{V}$ ( <a href="#">Note 2</a> )
		106	116	—	dB	$V_{DD} = 4.5\text{V}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ ( <a href="#">Note 1</a> )
	CMRR	135	150	—	dB	$V_{DD} = 45\text{V}$ , $V_{CM} = -0.3\text{V}$ to $42.9\text{V}$ ( <a href="#">Note 2</a> )
		128	140	—	dB	$V_{DD} = 45\text{V}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ ( <a href="#">Note 1</a> )
<b>Open-Loop Gain</b>						
DC Open-Loop Gain	$A_{OL}$	124	142	—	dB	$V_{DD} = 4.5\text{V}$ , $V_{OUT} = 0.3\text{V}$ to $4.2\text{V}$
		120	139	—	dB	$V_{DD} = 4.5\text{V}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ ( <a href="#">Note 1</a> )
	$A_{OL}$	140	164	—	dB	$V_{DD} = 45\text{V}$ , $V_{OUT} = 0.3\text{V}$ to $44.7\text{V}$
		134	160	—	dB	$V_{DD} = 45\text{V}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ ( <a href="#">Note 1</a> )

**Note 1:** Not production tested. Limits set by characterization and/or simulation and provided as design guidance only.

**2:** [Figure 2-17](#) shows how  $V_{CML}$  and  $V_{CMH}$  changed across temperature for the first production lot.

## DC ELECTRICAL SPECIFICATIONS (CONTINUED)

**Electrical Characteristics:** Unless otherwise indicated,  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = +4.5\text{V}$  to  $+45\text{V}$ ,  $V_{SS} = \text{GND}$ ,  $V_{CM} = V_{DD}/3$ ,  $V_{OUT} = V_{DD}/2$ ,  $V_L = V_{DD}/2$ ,  $R_L = 10\text{ k}\Omega$  to  $V_L$  and  $C_L = 100\text{ pF}$  (refer to [Figure 1-4](#) and [Figure 1-5](#)).

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
<b>Output</b>						
Minimum Output Voltage Swing	$V_{OL}$	—	$V_{SS} + 45$	$V_{SS} + 60$	mV	$R_L = 1\text{ k}\Omega$ , $V_{DD} = 4.5\text{V}$
		—	$V_{SS} + 500$	$V_{SS} + 1000$		$R_L = 1\text{ k}\Omega$ , $V_{DD} = 45\text{V}$
		—	$V_{SS} + 6$	$V_{SS} + 20$		$R_L = 10\text{ k}\Omega$ , $V_{DD} = 4.5\text{V}$
		—	$V_{SS} + 50$	$V_{SS} + 70$		$R_L = 10\text{ k}\Omega$ , $V_{DD} = 45\text{V}$
Maximum Output Voltage Swing	$V_{OH}$	$V_{DD} - 150$	$V_{DD} - 100$	—	mV	$R_L = 1\text{ k}\Omega$ , $V_{DD} = 4.5\text{V}$
		$V_{DD} - 2500$	$V_{DD} - 1500$	—		$R_L = 1\text{ k}\Omega$ , $V_{DD} = 45\text{V}$
		$V_{DD} - 20$	$V_{DD} - 12$	—		$R_L = 10\text{ k}\Omega$ , $V_{DD} = 4.5\text{V}$
		$V_{DD} - 200$	$V_{DD} - 100$	—		$R_L = 10\text{ k}\Omega$ , $V_{DD} = 45\text{V}$
Output Short-Circuit Current	$I_{SC}^+$	—	46	—	mA	
	$I_{SC}^-$	—	36	—	mA	
Closed-Loop Output Resistance	$R_{OUT}$	—	16	—	$\Omega$	$f = 0.1\text{ MHz}$ , $I_O = 0$ , $G = 1$
Capacitive Load Drive	$C_L$	—	100	—	pF	$G = 1$
<b>Power Supply</b>						
Supply Voltage	$V_{DD}$	4.5	—	45	V	
Quiescent Current per Amplifier	$I_Q$	310	460	590	$\mu\text{A}$	$V_{DD} = 4.5\text{V}$ , $I_O = 0$
		310	470	590	$\mu\text{A}$	$V_{DD} = 45\text{V}$ , $I_O = 0$
		—	540	670	$\mu\text{A}$	$I_O = 0$ , $T_A = -40$ to $+125^\circ\text{C}$ , see <a href="#">Figure 2-22 (Note 1)</a>
Power-on Reset (POR) Trip Voltage	$V_{POR}$	—	2.3	—	V	

**Note 1:** Not production tested. Limits set by characterization and/or simulation and provided as design guidance only.

**2:** [Figure 2-17](#) shows how  $V_{CML}$  and  $V_{CMH}$  changed across temperature for the first production lot.



# MCP6V51/2/4

## AC ELECTRICAL SPECIFICATIONS

**Electrical Characteristics:** Unless otherwise indicated,  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = +4.5\text{V}$  to  $+45\text{V}$ ,  $V_{SS} = \text{GND}$ ,  $V_{CM} = V_{DD}/3$ ,  $V_{OUT} = V_{DD}/2$ ,  $V_L = V_{DD}/2$ ,  $R_L = 10\text{ k}\Omega$  to  $V_L$  and  $C_L = 100\text{ pF}$  (refer to [Figure 1-4](#) and [Figure 1-5](#)).

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
<b>Amplifier AC Response</b>						
Gain Bandwidth Product	GBWP	—	1.8	—	MHz	$V_{DD} = 4.5\text{V}$ , $V_{IN} = 10\text{ mVpp}$ , Gain = 100
		—	2	—	MHz	$V_{DD} = 45\text{V}$ , $V_{IN} = 10\text{ mVpp}$ , Gain = 100
Slew Rate	SR	—	1.2	—	V/ $\mu\text{s}$	See <a href="#">Figure 2-45</a>
Phase Margin	PM	—	66	—	deg.	$V_{DD} = 45\text{V}$
<b>Amplifier Noise Response</b>						
Input Noise Voltage	$E_{ni}$	—	0.1	—	$\mu\text{V}_{P-P}$	$f = 0.01\text{ Hz}$ to $1\text{ Hz}$
		—	0.21	—	$\mu\text{V}_{P-P}$	$f = 0.1\text{ Hz}$ to $10\text{ Hz}$
Input Noise Voltage Density	$e_{ni}$	—	10.2	—	nV/ $\sqrt{\text{Hz}}$	$f = 1\text{ kHz}$
Input Noise Current Density	$i_{ni}$	—	4	—	fA/ $\sqrt{\text{Hz}}$	
<b>Amplifier Step Response</b>						
Start-Up Time	$t_{STR}$	—	200	—	$\mu\text{s}$	$G = +1$ , 1% $V_{OUT}$ settling ( <a href="#">Note 1</a> )
Offset Correction Settling Time	$t_{STL}$	—	45	—	$\mu\text{s}$	$G = +1$ , $V_{IN}$ step of 2V, $V_{OS}$ within $\pm 100\text{ }\mu\text{V}$ of its final value
Output Overdrive Recovery Time	$t_{ODR}$	—	65	—	$\mu\text{s}$	$G = -10$ , $\pm 0.5\text{V}$ input overdrive to $V_{DD}/2$ , $V_{IN}$ 50% point to $V_{OUT}$ 90% point ( <a href="#">Note 2</a> )
<b>EMI Protection</b>						
EMI Rejection Ratio	EMIRR	—	80	—	dB	$V_{IN} = 0.1\text{ V}_{PK}$ , $f = 400\text{ MHz}$ , $V_{DD} = 45\text{V}$
		—	95	—		$V_{IN} = 0.1\text{ V}_{PK}$ , $f = 900\text{ MHz}$ , $V_{DD} = 45\text{V}$
		—	108	—		$V_{IN} = 0.1\text{ V}_{PK}$ , $f = 1800\text{ MHz}$ , $V_{DD} = 45\text{V}$
		—	109	—		$V_{IN} = 0.1\text{ V}_{PK}$ , $f = 2400\text{ MHz}$ , $V_{DD} = 45\text{V}$
		—	109	—		$V_{IN} = 0.1\text{ V}_{PK}$ , $f = 5600\text{ MHz}$ , $V_{DD} = 45\text{V}$

**Note 1:** Behavior may vary with different gains; see [Section 4.3.3 "Offset at Power-up"](#).

**2:**  $t_{STL}$  and  $t_{ODR}$  include some uncertainty due to clock edge timing.

## TEMPERATURE SPECIFICATIONS

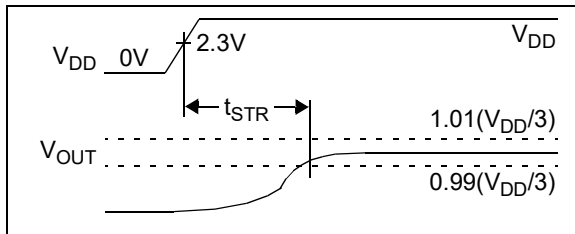
**Electrical Characteristics:** Unless otherwise indicated, all limits are specified for:  $V_{DD} = +4.5\text{V}$  to  $+45\text{V}$ ,  $V_{SS} = \text{GND}$ .

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
<b>Temperature Ranges</b>						
Specified Temperature Range	$T_A$	-40	—	+125	$^\circ\text{C}$	
Operating Temperature Range	$T_A$	-40	—	+125	$^\circ\text{C}$	<a href="#">Note 1</a>
Storage Temperature Range	$T_A$	-65	—	+150	$^\circ\text{C}$	
<b>Thermal Package Resistances</b>						
Thermal Resistance, 8-Lead MSOP	$\theta_{JA}$	—	206	—	$^\circ\text{C/W}$	
Thermal Resistance, 5-Lead SOT-23	$\theta_{JA}$	—	115	—	$^\circ\text{C/W}$	
Thermal Resistance, 8-Lead SOIC	$\theta_{JA}$	—	150	—	$^\circ\text{C/W}$	
Thermal Resistance, 14-Lead SOIC	$\theta_{JA}$	—	91	—	$^\circ\text{C/W}$	

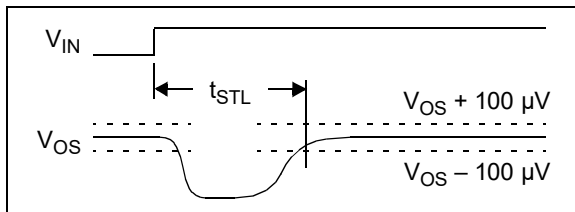
**Note 1:** Operation must not cause  $T_J$  to exceed Maximum Junction Temperature specification ( $+150^\circ\text{C}$ ).

## 1.3 Timing Diagrams

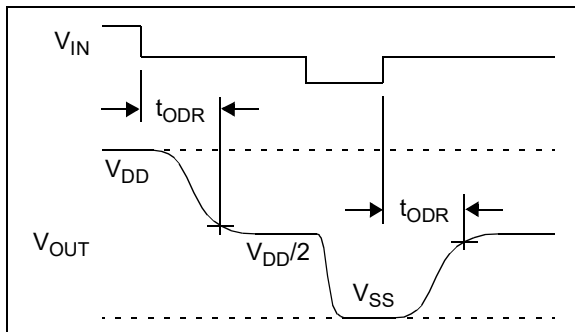
The Timing Diagrams provide a depiction of the Amplifier Step Response specifications listed under the **AC Electrical Specifications** table.



**FIGURE 1-1:** Amplifier Start-up.



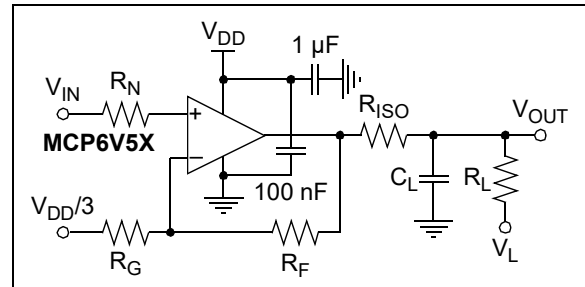
**FIGURE 1-2:** Offset Correction Settling Time.



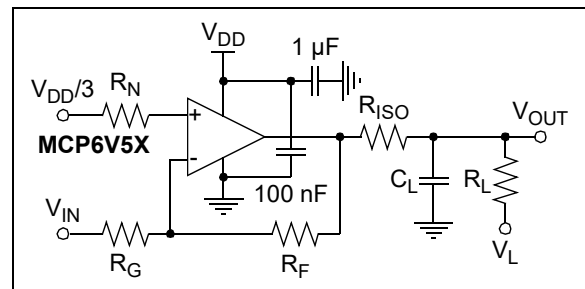
**FIGURE 1-3:** Output Overdrive Recovery.

## 1.4 Test Circuits

The circuits used for most DC and AC tests are shown in **Figure 1-4** and **Figure 1-5**. Lay the bypass capacitors out as discussed in **Section 4.3.10 “Supply Bypassing and Filtering”**.  $R_N$  is equal to the parallel combination of  $R_F$  and  $R_G$  to minimize bias current effects.

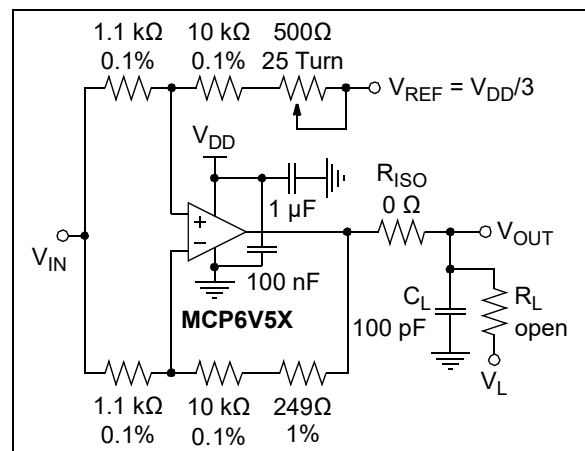


**FIGURE 1-4:** AC and DC Test Circuit for Most Noninverting Gain Conditions.



**FIGURE 1-5:** AC and DC Test Circuit for Most Inverting Gain Conditions.

The circuit in **Figure 1-6** tests the input's dynamic behavior (i.e.,  $t_{STR}$ ,  $t_{STL}$  and  $t_{ODR}$ ). The potentiometer balances the resistor network ( $V_{OUT}$  should equal  $V_{REF}$  at DC). The op amp's Common-Mode Input Voltage is  $V_{CM} = V_{IN}/3$ . The error at the input ( $V_{ERR}$ ) appears at  $V_{OUT}$  with a noise gain of approximately 10 V/V.



**FIGURE 1-6:** Test Circuit for Dynamic Input Behavior.

# MCP6V51/2/4

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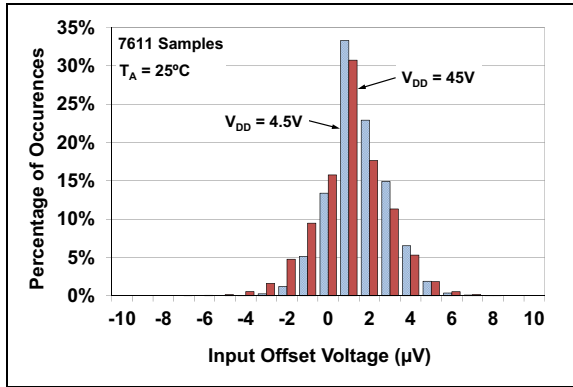
NOTES:

## 2.0 TYPICAL PERFORMANCE CURVES

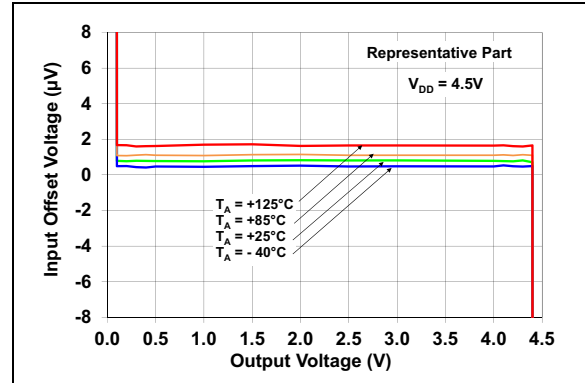
**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

**Note:** Unless otherwise indicated,  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = +4.5\text{V to } +45\text{V}$ ,  $V_{SS} = \text{GND}$ ,  $V_{CM} = V_{DD}/3$ ,  $V_{OUT} = V_{DD}/2$ ,  $V_L = V_{DD}/2$ ,  $R_L = 10\text{ k}\Omega$  to  $V_L$  and  $C_L = 100\text{ pF}$ .

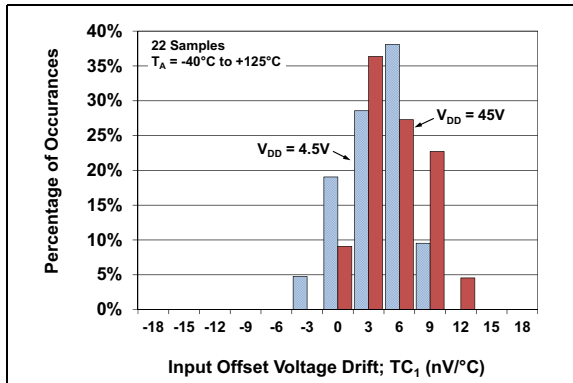
### 2.1 DC Input Precision



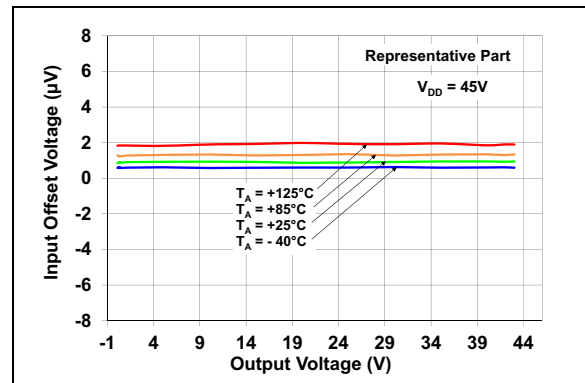
**FIGURE 2-1:** Input Offset Voltage.



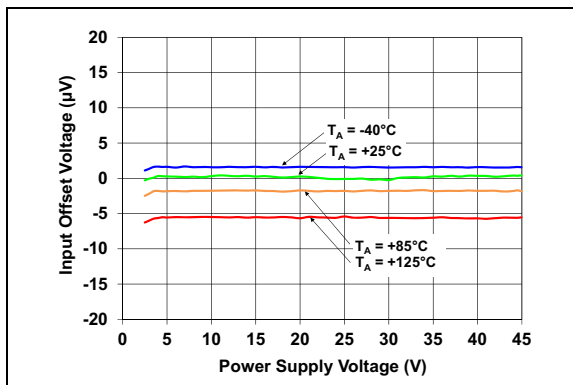
**FIGURE 2-4:** Input Offset Voltage vs. Output Voltage with  $V_{DD} = 4.5\text{V}$ .



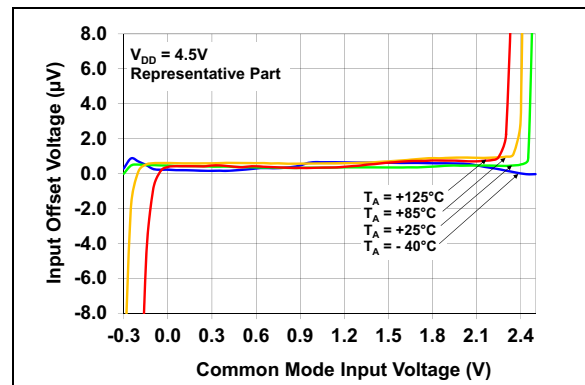
**FIGURE 2-2:** Input Offset Voltage Drift.



**FIGURE 2-5:** Input Offset Voltage vs. Output Voltage with  $V_{DD} = 45\text{V}$ .

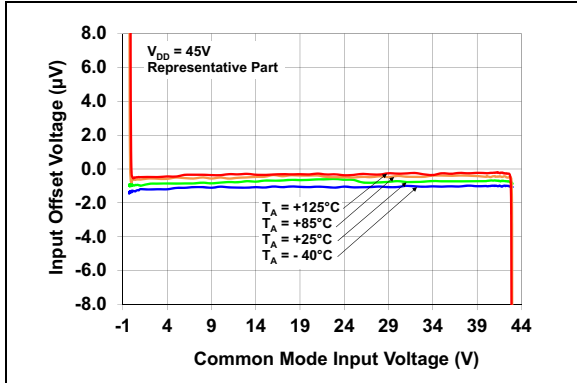


**FIGURE 2-3:** Input Offset Voltage vs. Power Supply Voltage.

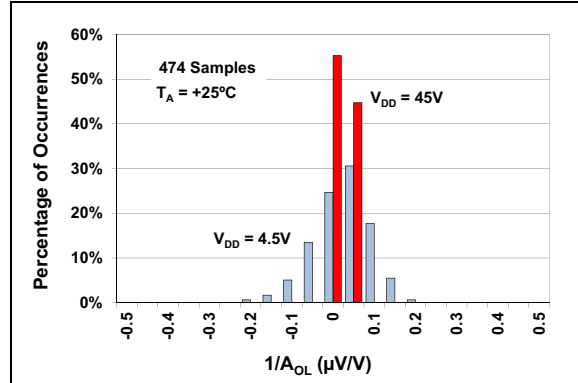


**FIGURE 2-6:** Input Offset Voltage vs. Common-Mode Voltage with  $V_{DD} = 4.5\text{V}$

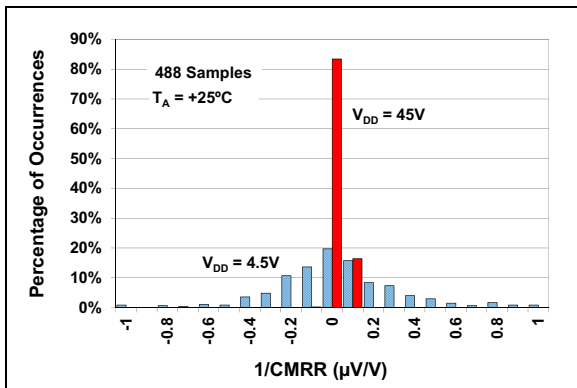
# MCP6V51/2/4



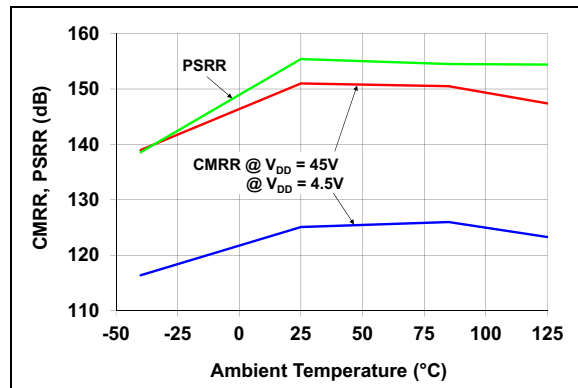
**FIGURE 2-7:** Input Offset Voltage vs. Common-Mode Voltage with  $V_{DD} = 45V$ .



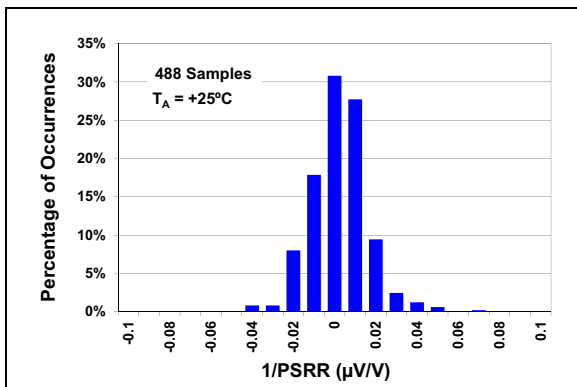
**FIGURE 2-10:** DC Open-Loop Gain.



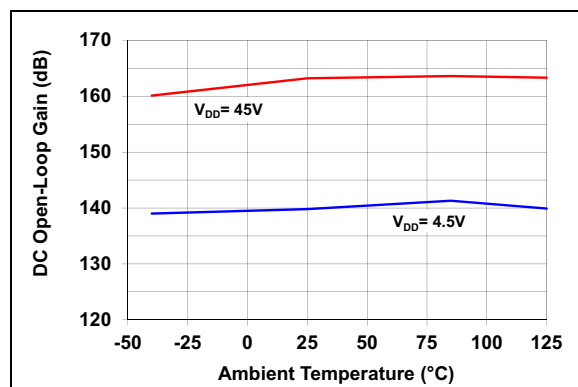
**FIGURE 2-8:** CMRR.



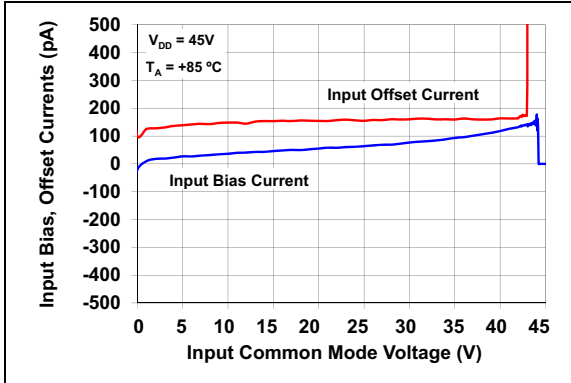
**FIGURE 2-11:** CMRR and PSRR vs. Ambient Temperature.



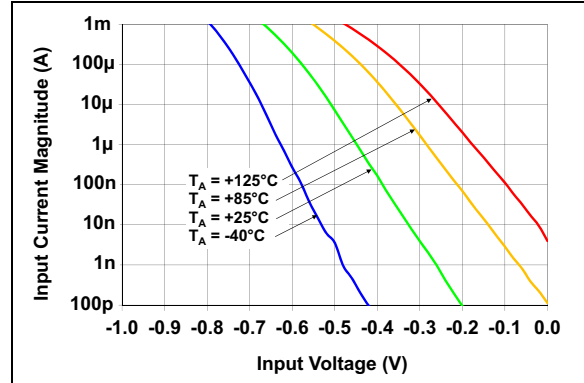
**FIGURE 2-9:** PSRR.



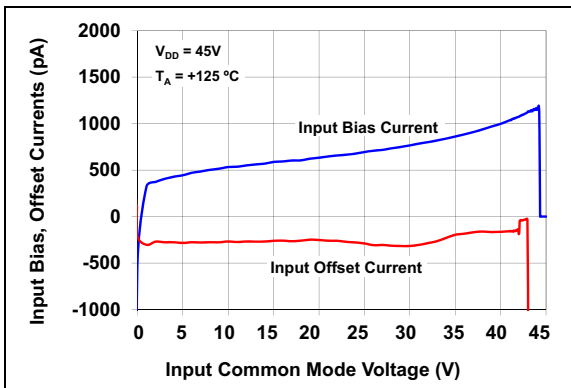
**FIGURE 2-12:** DC Open-Loop Gain vs. Ambient Temperature.



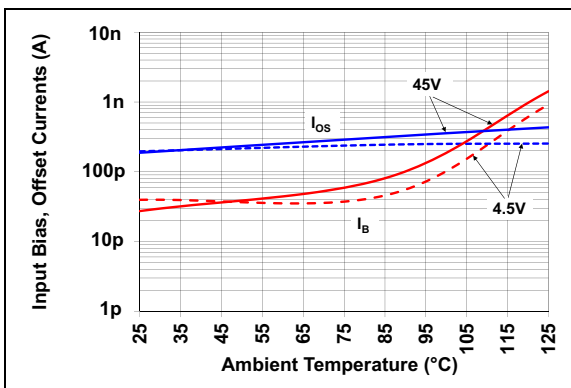
**FIGURE 2-13:** Input Bias and Offset Currents vs. Common-Mode Input Voltage with  $T_A = +85^\circ\text{C}$ .



**FIGURE 2-16:** Input Bias Current vs. Input Voltage (Below  $V_{SS}$ ).



**FIGURE 2-14:** Input Bias and Offset Currents vs. Common-Mode Input Voltage with  $T_A = +125^\circ\text{C}$ .

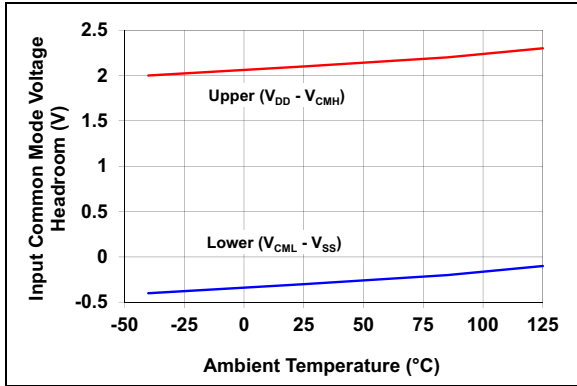


**FIGURE 2-15:** Input Bias and Offset Currents vs. Ambient Temperature with  $V_{DD} = 45\text{V}$ .

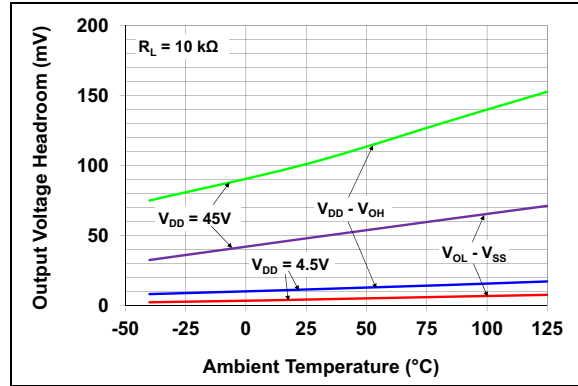
# MCP6V51/2/4

**Note:** Unless otherwise indicated,  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = +4.5\text{V}$  to  $+45\text{V}$ ,  $V_{SS} = \text{GND}$ ,  $V_{CM} = V_{DD}/3$ ,  $V_{OUT} = V_{DD}/2$ ,  $V_L = V_{DD}/2$ ,  $R_L = 10\text{ k}\Omega$  to  $V_L$  and  $C_L = 100\text{ pF}$ .

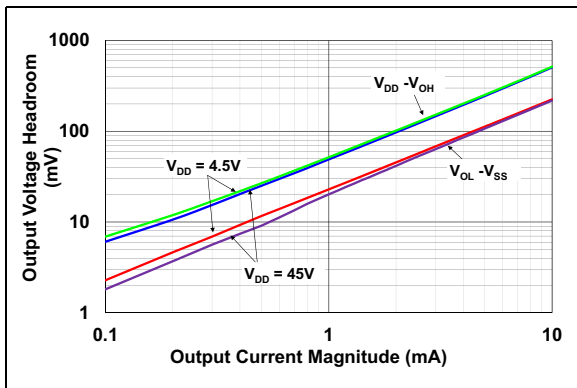
## 2.2 Other DC Voltages and Currents



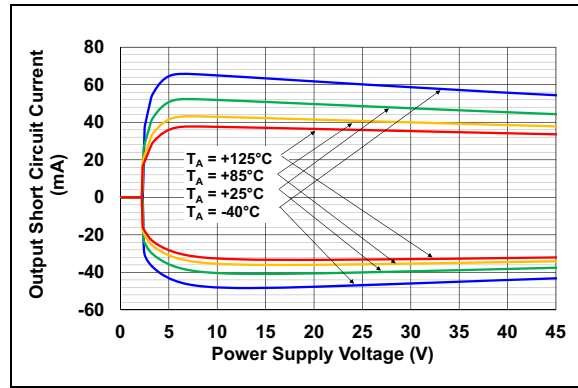
**FIGURE 2-17:** Input Common-Mode Voltage Headroom (Range) vs. Ambient Temperature.



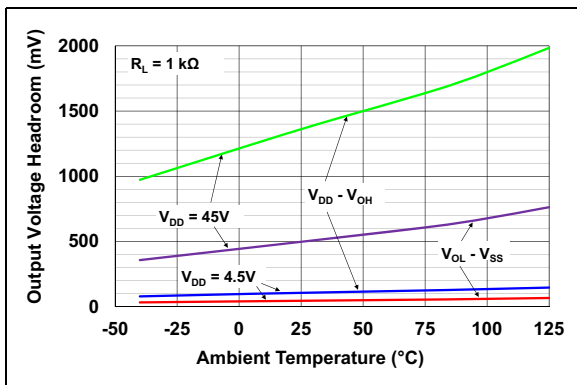
**FIGURE 2-20:** Output Voltage Headroom vs. Temperature  $R_L = 10\text{ k}\Omega$ .



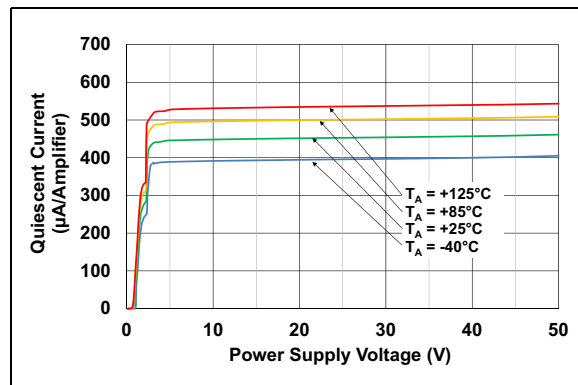
**FIGURE 2-18:** Output Voltage Headroom vs. Output Current.



**FIGURE 2-21:** Output Short-Circuit Current vs. Power Supply Voltage.



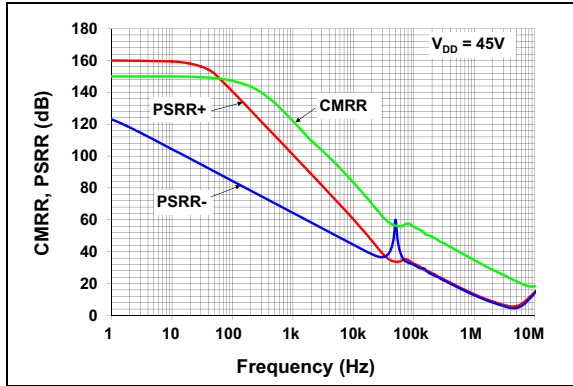
**FIGURE 2-19:** Output Voltage Headroom vs. Ambient Temperature.



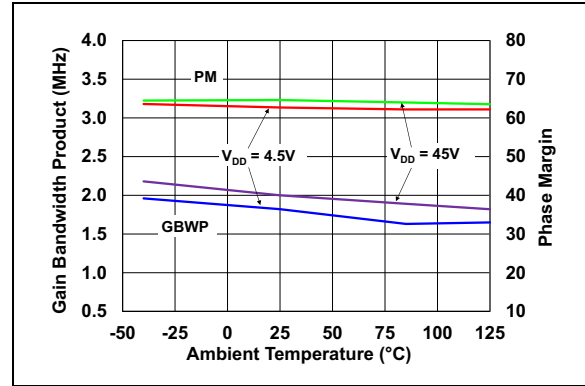
**FIGURE 2-22:** Supply Current vs. Power Supply Voltage.

**Note:** Unless otherwise indicated,  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = +4.5\text{V}$  to  $+45\text{V}$ ,  $V_{SS} = \text{GND}$ ,  $V_{CM} = V_{DD}/3$ ,  $V_{OUT} = V_{DD}/2$ ,  $V_L = V_{DD}/2$ ,  $R_L = 10\text{ k}\Omega$  to  $V_L$  and  $C_L = 100\text{ pF}$ .

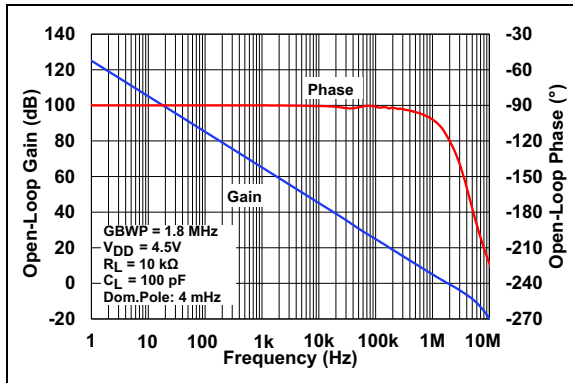
## 2.3 Frequency Response



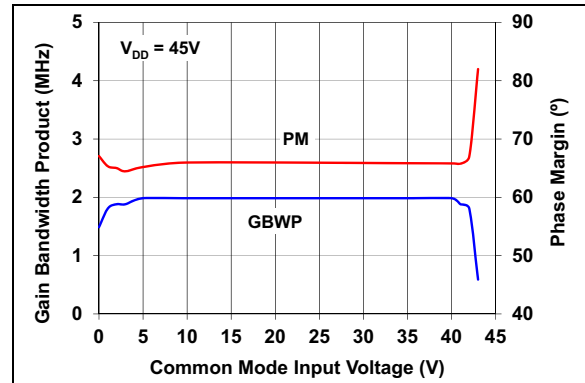
**FIGURE 2-23:** CMRR and PSRR vs. Frequency.



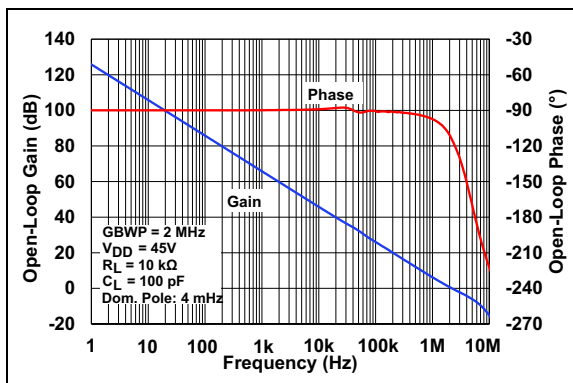
**FIGURE 2-26:** Gain Bandwidth Product and Phase Margin vs. Ambient Temperature.



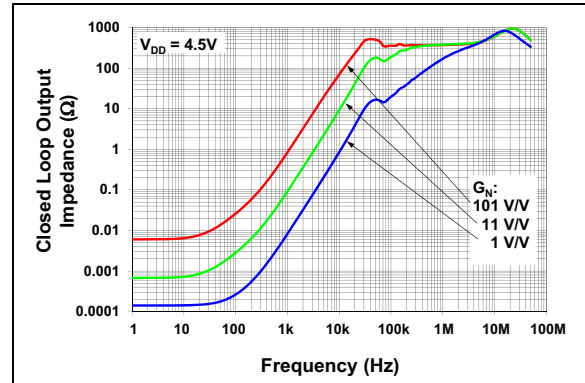
**FIGURE 2-24:** Open-Loop Gain vs. Frequency with  $V_{DD} = 4.5\text{V}$ .



**FIGURE 2-27:** Gain Bandwidth Product and Phase Margin vs. Common-Mode Input Voltage.



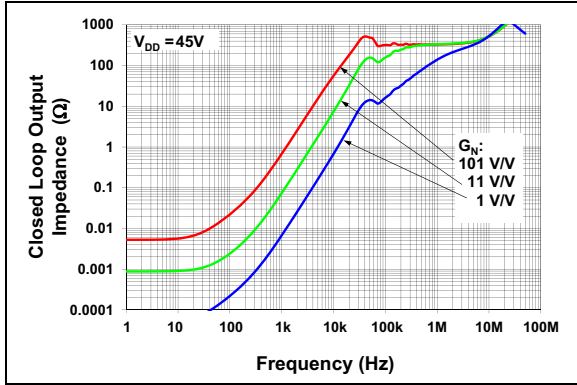
**FIGURE 2-25:** Open-Loop Gain vs. Frequency with  $V_{DD} = 45\text{V}$ .



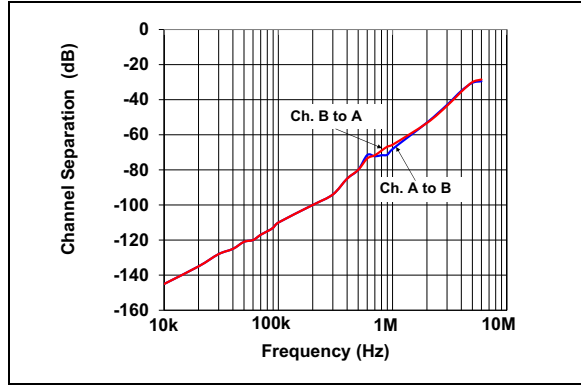
**FIGURE 2-28:** Closed-Loop Output Impedance vs. Frequency with  $V_{DD} = 4.5\text{V}$ .



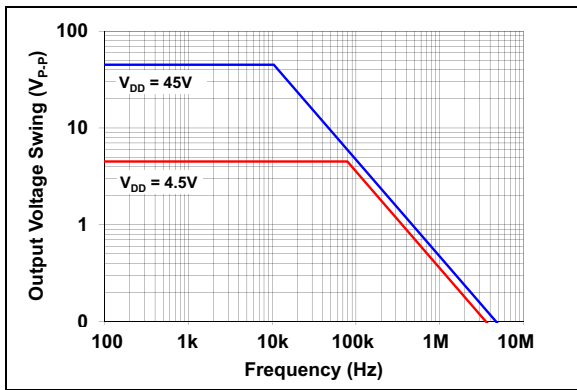
# MCP6V51/2/4



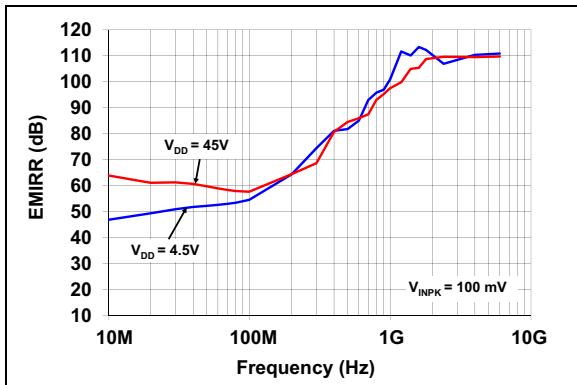
**FIGURE 2-29:** Closed-Loop Output Impedance vs. Frequency with  $V_{DD} = 45V$ .



**FIGURE 2-32:** Channel-to-Channel Crosstalk (MCP6V52).



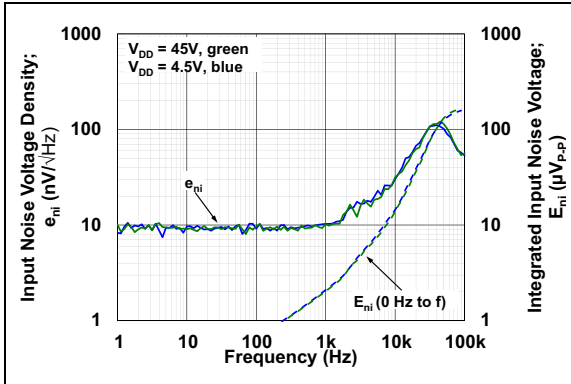
**FIGURE 2-30:** Maximum Output Voltage Swing vs. Frequency.



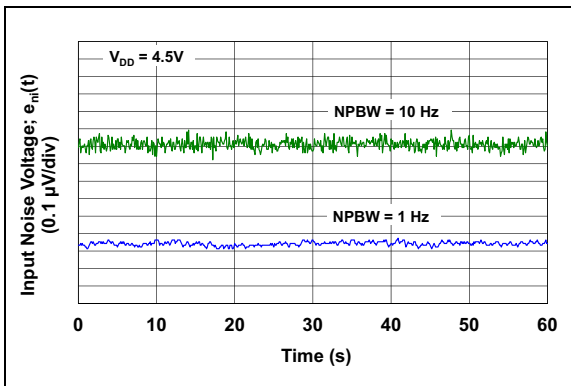
**FIGURE 2-31:** EMIRR vs. Frequency.

**Note:** Unless otherwise indicated,  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = +4.5\text{V}$  to  $+45\text{V}$ ,  $V_{SS} = \text{GND}$ ,  $V_{CM} = V_{DD}/3$ ,  $V_{OUT} = V_{DD}/2$ ,  $V_L = V_{DD}/2$ ,  $R_L = 10\text{ k}\Omega$  to  $V_L$  and  $C_L = 100\text{ pF}$ .

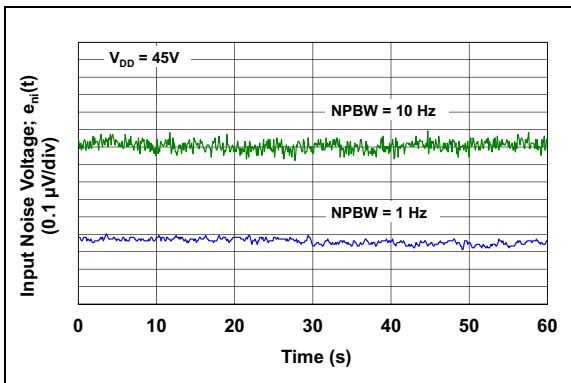
## 2.4 Input Noise



**FIGURE 2-33:** Input Noise Voltage Density and Integrated Input Noise Voltage vs. Frequency.



**FIGURE 2-34:** Input Noise vs. Time with 1 Hz and 10 Hz Filters and  $V_{DD} = 4.5\text{V}$ .

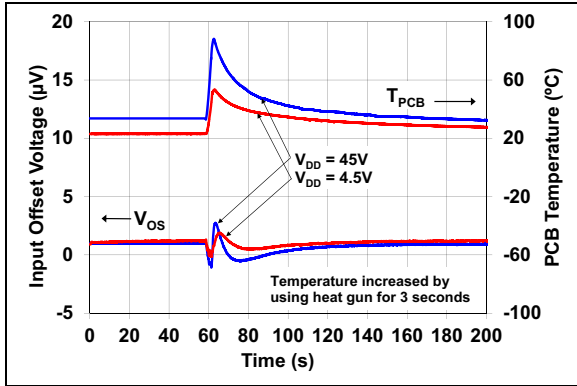


**FIGURE 2-35:** Input Noise vs. Time with 1 Hz and 10 Hz Filters and  $V_{DD} = 45\text{V}$ .

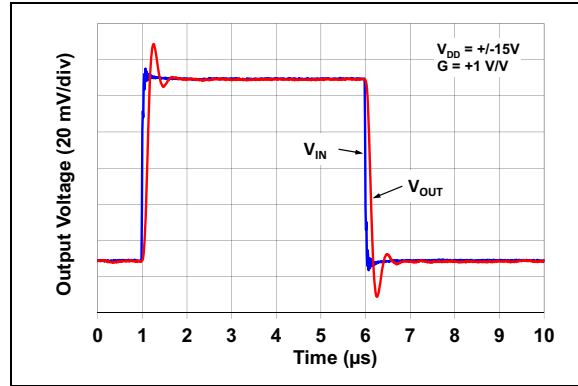
# MCP6V51/2/4

**Note:** Unless otherwise indicated,  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = +4.5\text{V}$  to  $+45\text{V}$ ,  $V_{SS} = \text{GND}$ ,  $V_{CM} = V_{DD}/3$ ,  $V_{OUT} = V_{DD}/2$ ,  $V_L = V_{DD}/2$ ,  $R_L = 10\text{ k}\Omega$  to  $V_L$  and  $C_L = 100\text{ pF}$ .

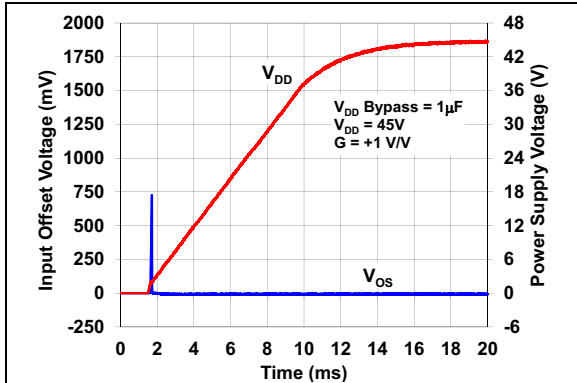
## 2.5 Time Response



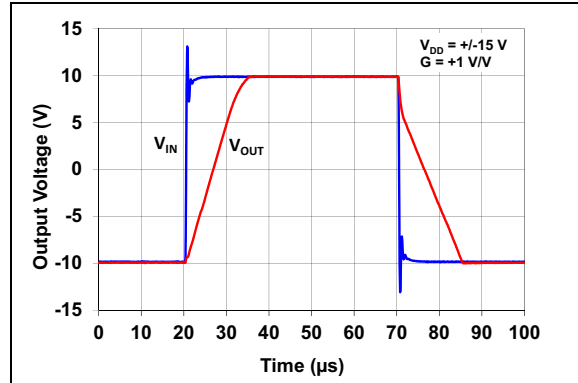
**FIGURE 2-36:** Input Offset Voltage vs. Time with Temperature Change.



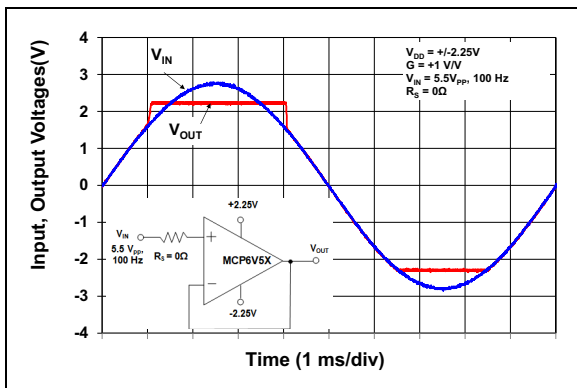
**FIGURE 2-39:** Noninverting Small Signal Step Response.



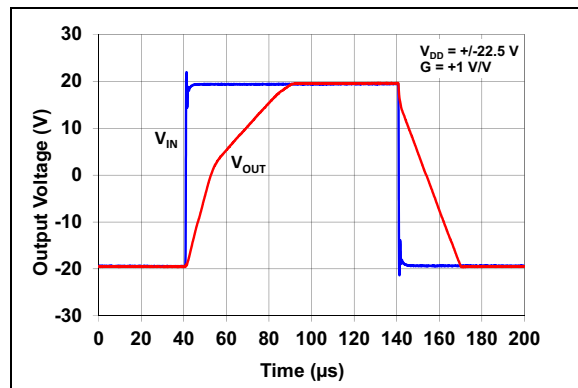
**FIGURE 2-37:** Input Offset Voltage vs. Time at Power-up.



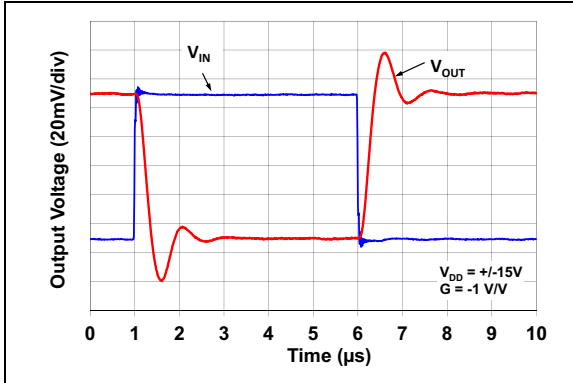
**FIGURE 2-40:** Noninverting Large Signal Step Response.



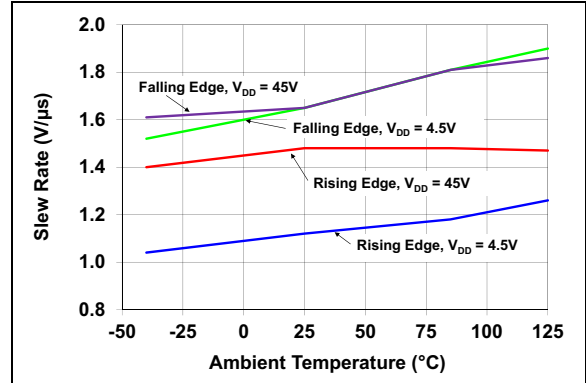
**FIGURE 2-38:** The MCP6V51/2/4 Shows No Input Phase Reversal with Overdrive.



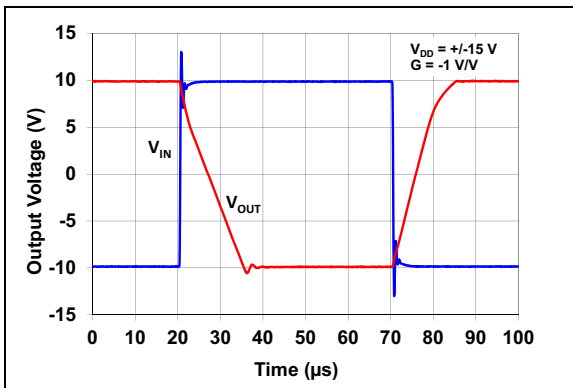
**FIGURE 2-41:** Noninverting 40  $V_{PP}$  Step Response.



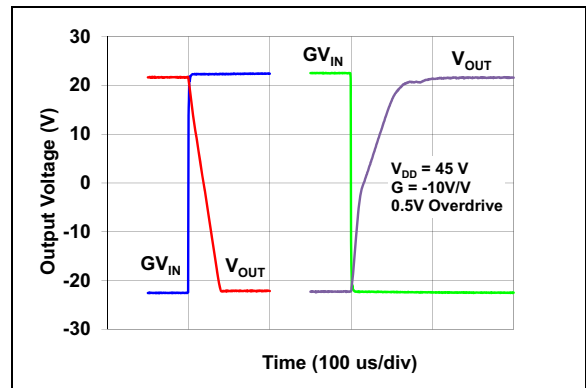
**FIGURE 2-42:** Inverting Small Signal Step Response.



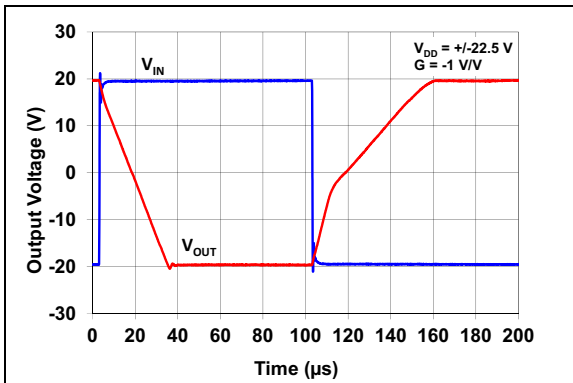
**FIGURE 2-45:** Slew Rate vs. Ambient Temperature.



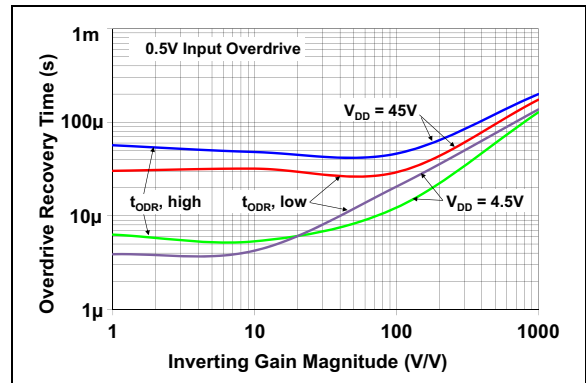
**FIGURE 2-43:** Inverting Large Signal Step Response.



**FIGURE 2-46:** Output Overdrive Recovery vs. Time with  $G = -10$  V/V.



**FIGURE 2-44:** Inverting 40  $V_{PP}$  Step Response.



**FIGURE 2-47:** Output Overdrive Recovery Time vs. Inverting Gain.

# MCP6V51/2/4

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NOTES:

## 3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in [Table 3-1](#).

**TABLE 3-1: PIN FUNCTION TABLE**

MCP6V51		MCP6V52		MCP6V54	Symbol	Description
SOT23-5	MSOP-8	SOIC-8	MSOP-8	SOIC-14		
1	6	1	1	1	$V_{OUT}$	Output
4	2	2	2	2	$V_{IN-}$	Inverting Input
3	3	3	3	3	$V_{IN+}$	Noninverting Input
5	7	8	8	4	$V_{DD}$	Positive Power Supply
—	—	5	5	5	$V_{INB+}$	Noninverting Input (Op Amp B)
—	—	6	6	6	$V_{INB-}$	Inverting Input (Op Amp B)
—	—	7	7	7	$V_{OUTB}$	Output (Op Amp B)
—	—	—	—	8	$V_{OUTC}$	Output (Op Amp C)
—	—	—	—	9	$V_{INC-}$	Inverting Input (Op Amp C)
—	—	—	—	10	$V_{INC+}$	Noninverting Input (Op Amp C)
2	4	4	4	11	$V_{SS}$	Negative Power Supply
—	—	—	—	12	$V_{IND+}$	Noninverting Input (Op Amp D)
—	—	—	—	13	$V_{IND-}$	Inverting Input (Op Amp D)
—	—	—	—	14	$V_{OUTD}$	Output (Op Amp D)
—	1, 5, 8	—	—	—	NC	Do Not Connect (no internal connection)

### 3.1 Analog Outputs ( $V_{OUT}$ , $V_{OUTA}$ , $V_{OUTB}$ , $V_{OUTC}$ , $V_{OUTD}$ )

The analog output pins ( $V_{OUT}$ ) are low-impedance voltage sources.

### 3.2 Analog Inputs ( $V_{IN+}$ , $V_{IN-}$ , $V_{INB+}$ , $V_{INB-}$ , $V_{INC-}$ , $V_{INC+}$ , $V_{IND-}$ , $V_{IND+}$ )

The noninverting and inverting inputs ( $V_{IN+}$ ,  $V_{IN-}$ , ...) are high-impedance CMOS inputs with low bias currents.

### 3.3 Power Supply Pins

The positive power supply ( $V_{DD}$ ) is 4.5V to 45V higher than the negative power supply ( $V_{SS}$ ). For normal operation, the other pins are between  $V_{SS}$  and  $V_{DD}$ .

Typically, these parts are used in a single (positive) supply configuration. In this case,  $V_{SS}$  is connected to ground and  $V_{DD}$  is connected to the supply.  $V_{DD}$  will need bypass capacitors.

# MCP6V51/2/4

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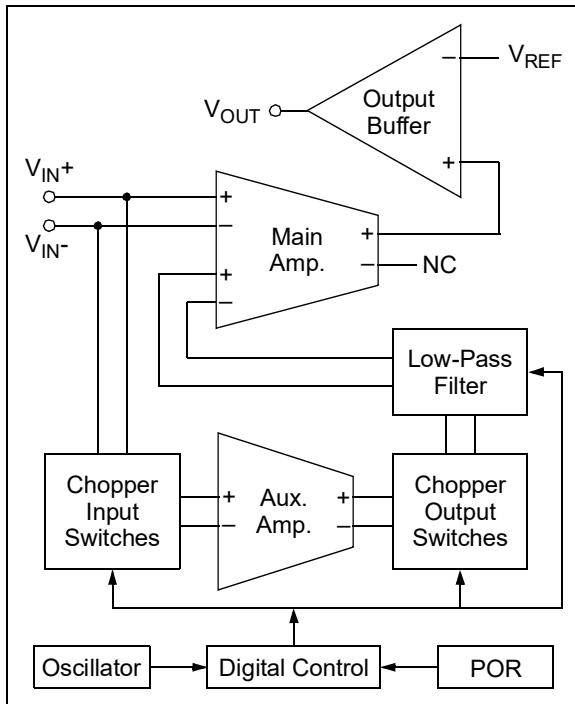
NOTES:

## 4.0 APPLICATIONS

The MCP6V51/2/4 devices are designed for precision applications with requirements for small packages and low power. Their wide supply voltage range and low quiescent current make the MCP6V51/2/4 devices ideal for industrial applications.

### 4.1 Overview of Zero-Drift Operation

Figure 4-1 shows a simplified diagram of the MCP6V5X zero-drift op amp. This diagram will be used to explain how slow voltage errors are reduced in this architecture (much better  $V_{OS}$ ,  $\Delta V_{OS}/\Delta T_A$  ( $TC_1$ ), CMRR, PSRR,  $A_{OL}$  and  $1/f$  noise).



**FIGURE 4-1:** Simplified Zero-Drift Op Amp Functional Diagram.

#### 4.1.1 BUILDING BLOCKS

The main amplifier is designed for high gain and bandwidth, with a differential topology. Its main input pair (+ and – pins at the top left) is used for the higher frequency portion of the input signal. Its auxiliary input pair (+ and – pins at the bottom left) is used for the low-frequency portion of the input signal and corrects the op amp's input offset voltage. Both inputs are added together internally.

The auxiliary amplifier, chopper input switches and chopper output switches provide a high DC gain to the input signal. DC errors are modulated to higher frequencies, while white noise is modulated to low frequency.

The low-pass filter reduces high-frequency content, including harmonics of the chopping clock.

The output buffer drives external loads at the  $V_{OUT}$  pin ( $V_{REF}$  is an internal reference voltage).

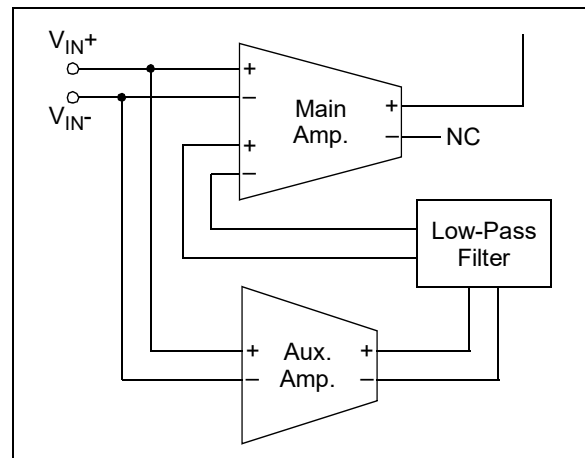
The oscillator runs at  $f_{OSC1} = 200$  kHz. Its output is divided by two, to produce the chopping clock rate of  $f_{CHOP} = 100$  kHz.

The internal Power-on Reset (POR) starts the part in a known good state, protecting against power supply brown-outs.

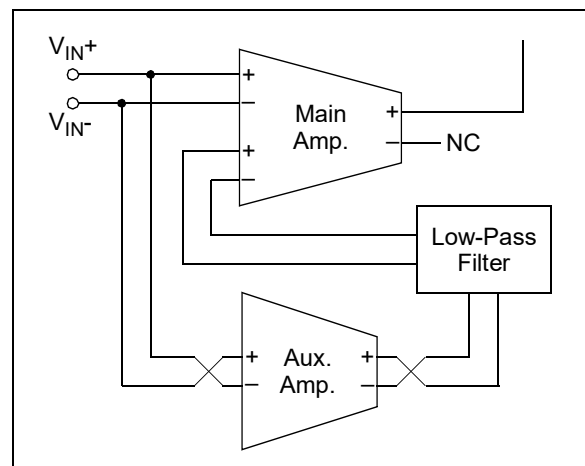
The digital control block controls switching and POR events.

#### 4.1.2 CHOPPING ACTION

Figure 4-2 shows the amplifier connections for the first phase of the chopping clock and Figure 4-3 shows the connections for the second phase. Its slow voltage errors alternate in polarity, making the average error small.



**FIGURE 4-2:** First Chopping Clock Phase; Equivalent Amplifier Diagram.



**FIGURE 4-3:** Second Chopping Clock Phase; Equivalent Amplifier Diagram.



# MCP6V51/2/4

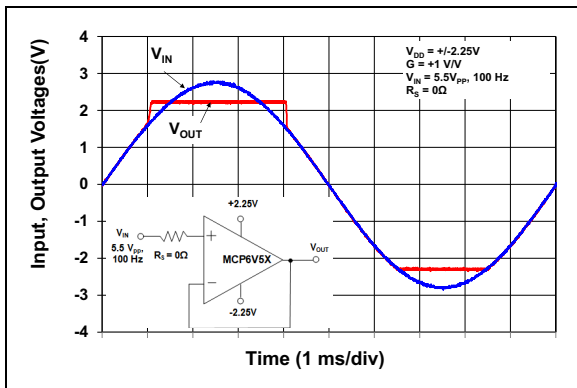
## 4.2 Other Functional Blocks

### 4.2.1 INPUT PROTECTION

The MCP6V5X op amps can be operated on a single supply, voltage ranging from 4.5V to 45V, or in a split-supply application ( $\pm 2.25V$  to  $\pm 22.5V$ ). The input Common-Mode range extends below the negative rail,  $V_{CML} = V_{SS} - 0.3V$  at  $+25^\circ C$ , while maintaining high CMRR (135 dB min. at  $45 V_{DD}$ ). The upper range of the input Common-Mode is limited to  $V_{CMH} = V_{DD} - 2.1V$ . To ensure proper operation, these  $V_{CM}$  limits, along with any potential overvoltage/current conditions as described in the following paragraphs, should be taken into consideration.

#### 4.2.1.1 Phase Reversal

The input circuitry of the MCP6V5X amplifiers is designed to not exhibit phase reversal when the input pins ( $V_{IN+}$ ,  $V_{IN-}$ ) exceed the supply voltages. Typically, an amplifier is most susceptible to phase reversal when operated in a unity gain buffer configuration, where the input is prone to be driven beyond the specified Common-Mode voltage range.



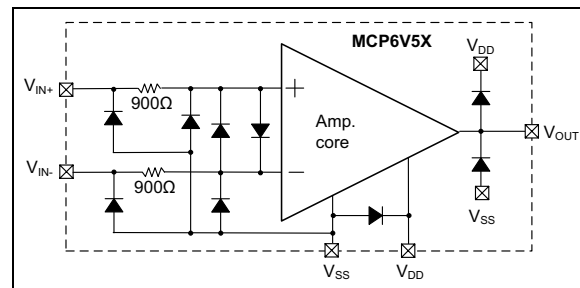
**FIGURE 4-4:** No Phase Reversal.

Figure 4-4 shows an input voltage exceeding the supply voltages by 0.5V for each rail. The output voltage remains railed with no phase inversion while the input is overdriven. For this particular example, the supply voltage was kept lower in order to help visualize the relationship between the input and output voltages during an Overvoltage condition.

#### 4.2.1.2 Input Voltage Limits

In order to prevent damage and/or improper operation of these amplifiers, the surrounding circuit must limit the voltage levels seen by the amplifier's input pins to within the specified limits (see [Section 1.1 "Absolute Maximum Ratings"](#)). This input voltage limit requirement is independent of the current limits discussed later on.

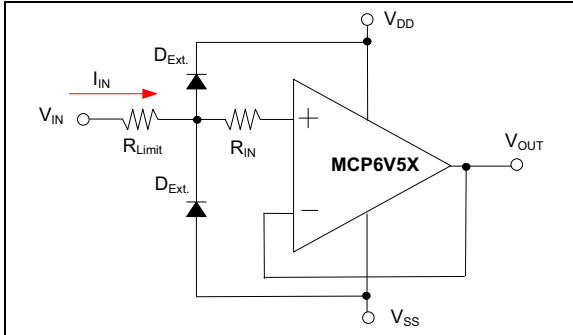
Figure 4-5 illustrates the principle ESD protection scheme used for the MCP6V5X amplifiers. Each input is protected by a set of primary and secondary steering diodes in addition to series resistance. Furthermore, a set of anti-parallel diodes protect the input transistors from seeing a large differential voltage. This structure was chosen to protect the input transistors against many (but not all) ESD and Overvoltage conditions, while also minimizing the effects of additional input bias currents ( $I_{Bias}$ ) resulting from the leakage current of the ESD devices. Note that this leakage current is temperature-dependent and will dominate at higher temperatures (see [Figure 2-15](#)).



**FIGURE 4-5:** Simplified Analog Input ESD Structures.

The input ESD diodes clamp the inputs when they try to go more than one diode drop below  $V_{SS}$ . They also clamp any voltages well above  $V_{DD}$ ; their breakdown voltage is high enough to allow normal operation, but not low enough to protect against slow overvoltage (beyond  $V_{DD}$ ) events. Very fast ESD events (that meet the specification) are limited so that damage can largely be prevented. The internal ESD protection scheme is intended to protect the device during test, assembly and manufacturing process. Note that the internal protection is not intended to be used as clamping or limiting devices for sustained in-circuit operation. If such Overvoltage (i.e., exceeding the supply rails by more than 0.5V) and/or Overcurrent conditions (i.e., current flow at each input pin exceeding 5 mA) are expected as part of the application circuit, external protection devices may be needed.

Figure 4-6 shows one approach of protecting the inputs against Overvoltage conditions with external diodes. The device marked as  $D_{Ext}$  may be small-signal silicon diodes, or Schottky diodes, for lower clamping voltages, or diode connected FETs for low leakage. Depending on the application, the additional diode capacitance should be considered.

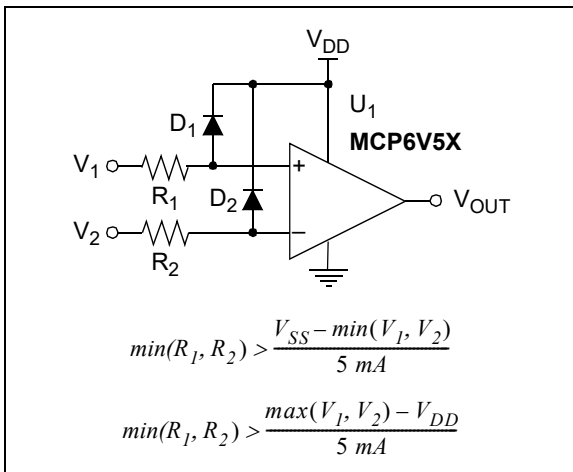


**FIGURE 4-6:** Protecting the Analog Inputs Against High Voltages.

A current limit resistor ( $R_{Limit}$ ) may be needed to prevent excessive current flow through the external diodes ( $D_{Ext}$ ). If the amplifier inputs will be subjected to Overvoltage conditions as part of the application, an additional resistor ( $R_{IN}$ ) in series with the vulnerable input pin (here  $V_{IN+}$ ) may be needed to limit the Fault current to a safe level (e.g., 2 mA).

#### 4.2.1.3 Input Current Limits

In order to prevent damage and/or improper operation of these amplifiers, the circuit must limit the currents into the input pins (see [Section 1.1 “Absolute Maximum Ratings†”](#)). This requirement is independent of the voltage limits discussed previously. [Figure 4-7](#) shows one approach to protecting these inputs. The  $R_1$  and  $R_2$  resistors limit the possible current in or out of the input pins (and into  $D_1$  and  $D_2$ ).



**FIGURE 4-7:** Protecting the Analog Inputs Against High Currents.

It is also possible to connect the diodes to the left of the  $R_1$  and  $R_2$  resistors. In this case, the currents through the  $D_1$  and  $D_2$  diodes need to be limited by some other mechanism (see [Figure 4-6](#)). The resistors then serve as inrush current limiters; the DC current into the input pins ( $V_{IN+}$  and  $V_{IN-}$ ) should be very small.

A significant amount of current can flow out of the inputs (through the ESD diodes) when the Common-Mode Voltage ( $V_{CM}$ ) is below ground ( $V_{SS}$ ). See [Figure 2-16](#) for further details.

#### 4.2.2 INTEGRATED EMI FILTER

The MCP6V5X op amps have an integrated low-pass filter in their inputs for the dedicated purpose of reducing any Electromagnetic or RF Interference (EMI, RFI). The on-chip filter is designed as a second-order RC low-pass, which sets a bandwidth limit of approximately 115 MHz and attenuates the high-frequency interference. Performance results of the MCP6V51/2/4 devices' EMI Rejection Ratio (EMIRR) under various conditions can be seen in [Figure 2-31](#).

#### 4.2.3 RAIL-TO-RAIL OUTPUT

The output voltage range of the MCP6V51/2/4 zero-drift op amps is typically  $V_{DD} - 100 \text{ mV}$  and  $V_{SS} + 50 \text{ mV}$  when  $R_L = 10 \text{ k}\Omega$  is connected to  $V_{DD}/2$  and  $V_{DD} = 45\text{V}$ . Refer to [Figure 2-18](#), [Figure 2-19](#) and [Figure 2-20](#) for more information.

#### 4.2.4 THERMAL SHUTDOWN

Under certain operating conditions, the MCP6V5X amplifier can be subjected to a rise of its die temperature above the specified maximum junction temperature of  $+150^\circ\text{C}$ . To control possible overheating and damage, the MCP6V5X amplifier has internal thermal shutdown circuitry. Especially when operating with the maximum supply voltage of 45V, observe that the ambient temperature and/or the amplifier's output current are such that the junction temperature remains below the specified limit. To estimate the Junction Temperature ( $T_J$ ), consider these factors: the total Power Dissipation of the device ( $P_D$ ) and the Ambient Temperature at the device package ( $T_A$ ), and use [Equation 4-1](#) below.

#### EQUATION 4-1:

$$T_J = P_D \times \theta_{JA} + T_A$$

Where:

$\theta_{JA}$  = The thermal resistance between the die and the ambient environment, as shown in [Temperature Specifications](#)

# MCP6V51/2/4

To derive the power dissipation of the device, add the terms for the devices' quiescent power and the load power, as shown in Equation 4-2:

## EQUATION 4-2:

$$P_D = (V_{DD} - V_{SS}) \times I_Q + I_{OUT} \times (V_{DD} - V_{OUT})$$

This assumes that the device is sourcing the load current (i.e., current flowing from the  $V_{DD}$  supply into the load). Use the term  $(I_{OUT} \times (V_{OUT} - V_{SS}))$  when the device is sinking current. Note that this simple example assumes a constant (DC) signal current flow.

The thermal shutdown circuitry activates as soon as the junction temperature reaches approximately  $+175^\circ\text{C}$ , causing the amplifier's output stage to be tri-stated (high-impedance), effectively disabling any output current flow. The amplifier will remain in this disabled state until the junction temperature has cooled down to approximately  $+160^\circ\text{C}$ . At this point, the thermal shutdown circuitry will enable the output stage of the MCP6V5X amplifier and the device will resume normal operation.

If a Fault condition persists, for example, the amplifier's output ( $V_{OUT}$ ) is shorted causing excessive output current, the thermal shutdown circuitry may be triggered again and the previously described cycle repeats. This may continue until the Fault condition is removed.

It should be noted that the thermal shutdown feature of the MCP6V5X does not ensure that the device will remain undamaged when operated under stress conditions, during which the device is placed into the Shutdown mode.

## 4.3 Application Tips

### 4.3.1 INPUT OFFSET VOLTAGE OVER TEMPERATURE

The **DC Electrical Specifications** table gives both the linear and quadratic temperature coefficients ( $TC_1$  and  $TC_2$ ) of the input offset voltage. The input offset voltage, at any temperature in the specified range, can be calculated as follows:

## EQUATION 4-3:

$$V_{OS}(T_A) = V_{OS} + TC_1 \Delta T + TC_2 \Delta T^2$$

Where:

$$\Delta T = T_A - 25^\circ\text{C}$$

$$V_{OS}(T_A) = \text{Input offset voltage at } T_A$$

$$V_{OS} = \text{Input offset voltage at } +25^\circ\text{C}$$

$$TC_1 = \text{Linear temperature coefficient}$$

$$TC_2 = \text{Quadratic temperature coefficient}$$

### 4.3.2 DC GAIN PLOTS

Figure 2-8, Figure 2-9 and Figure 2-10 are histograms of the reciprocals (in units of  $\mu\text{V/V}$ ) of CMRR, PSRR and  $A_{OL}$ , respectively. They represent the change in Input Offset Voltage ( $V_{OS}$ ) with a change in Common-Mode Input Voltage ( $V_{CM}$ ), Power Supply Voltage ( $V_{DD}$ ) and Output Voltage ( $V_{OUT}$ ).

The  $1/A_{OL}$  histogram is centered near  $0 \mu\text{V/V}$  because the measurements are dominated by the op amp's input noise. The negative values shown represent noise and tester limitations, *not* unstable behavior. Production tests make multiple  $V_{OS}$  measurements, which validates an op amp's stability; an unstable part would show greater  $V_{OS}$  variability or the output would stick at one of the supply rails.

### 4.3.3 OFFSET AT POWER-UP

When these parts power up, the Input Offset ( $V_{OS}$ ) starts at its uncorrected value (usually less than  $\pm 5 \text{ mV}$ ). Circuits with high DC gain may cause the output to reach one of the two rails. In this case, the time to a valid output is delayed by an Output Overdrive Time ( $t_{ODR}$ ), in addition to the Start-up Time ( $t_{STR}$ ).

To avoid this extended start-up time, reducing the gain is one method. Adding a capacitor across the Feedback Resistor ( $R_F$ ) is another method.

### 4.3.4 SOURCE RESISTANCES

The input bias currents have two significant components: switching glitches that dominate at room temperature and below, and input ESD diode leakage currents that dominate at  $+85^\circ\text{C}$  and above.

Make the resistances seen by the inputs small and equal. This minimizes the output offset voltage caused by the input bias currents.

The inputs should see a resistance in the order of  $10\Omega$  to  $1 \text{ k}\Omega$  at high frequencies (i.e., above  $1 \text{ MHz}$ ). This helps minimize the impact of switching glitches, which are very fast, on overall performance. In some cases, it may be necessary to add resistors in series with the inputs to achieve this improvement in performance.

Small input resistances may be needed for high gains. Without them, parasitic capacitances might cause positive feedback and instability.

### 4.3.5 SOURCE CAPACITANCE

The capacitances seen by the two inputs should be small. Large input capacitances and source resistances, together with high gain, can lead to instability.

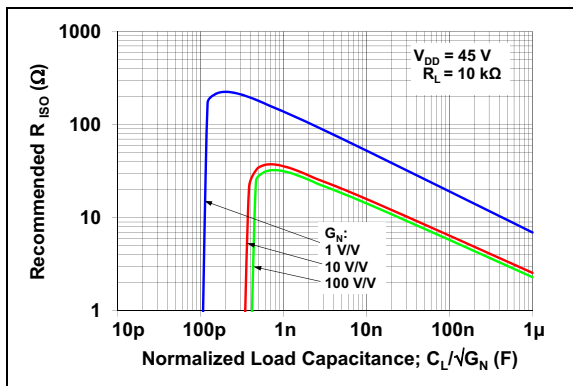
## 4.3.6 CAPACITIVE LOADS

Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the feedback loop's phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in the step response. These zero-drift op amps have a different output impedance compared to standard linear op amps, due to their unique topology.

When driving a capacitive load with these op amps, a Series Resistor at the output ( $R_{ISO}$  in Figure 4-9) improves the feedback loop's phase margin (stability) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitive load.

Figure 4-8 gives recommended  $R_{ISO}$  values for different capacitive loads and gains. The x-axis is the Load Capacitance ( $C_L$ ). The y-axis is the Resistance ( $R_{ISO}$ ).

$G_N$  is the circuit's Noise Gain. For noninverting gains,  $G_N$  and the Signal Gain are equal. For inverting gains,  $G_N$  is  $1+|\text{Signal Gain}|$  (e.g.,  $-1 \text{ V/V}$  gives  $G_N = +2 \text{ V/V}$ ).



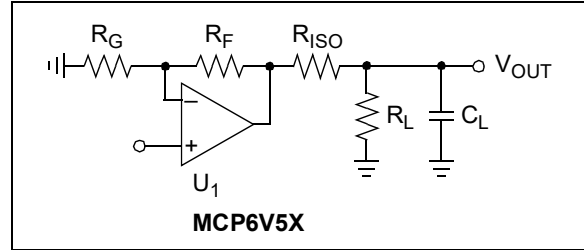
**FIGURE 4-8:** Recommended  $R_{ISO}$  Values for Capacitive Loads.

After selecting  $R_{ISO}$  for your circuit, double check the resulting frequency response peaking and step response overshoot. Modify the  $R_{ISO}$  value until the response is reasonable. Bench evaluation is helpful.

## 4.3.7 STABILIZING OUTPUT LOADS

This family of zero-drift op amps has an output impedance (Figure 2-28 and Figure 2-29) that has a double zero when the gain is low. This can cause a large phase shift in feedback networks that have low-impedance near the part's crossover frequency. This phase shift can cause stability problems.

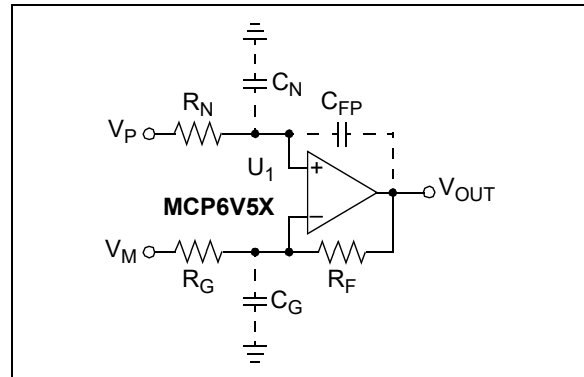
Figure 4-9 shows that the load on the output is  $(R_L + R_{ISO}) || (R_F + R_G)$ , where  $R_{ISO}$  is before the load. This load needs to be large enough to maintain stability; it is recommended to design for a total load of  $10 \text{ k}\Omega$ , or higher.



**FIGURE 4-9:** Output Resistor,  $R_{ISO}$ , Stabilizes Capacitive Loads.

## 4.3.8 GAIN PEAKING

Figure 4-10 shows an op amp circuit that represents noninverting amplifiers ( $V_M$  is a DC voltage and  $V_P$  is the input) or inverting amplifiers ( $V_P$  is a DC voltage and  $V_M$  is the input). The  $C_N$  and  $C_G$  capacitances represent the total capacitance at the input pins; they include the op amp's Common-Mode Input Capacitance ( $C_{CM}$ ), board parasitic capacitance and any capacitor placed in parallel. The  $C_{FP}$  capacitance represents the parasitic capacitance coupling between the output and the noninverting input pins.



**FIGURE 4-10:** Amplifier with Parasitic Capacitance.

$C_G$  acts in parallel with  $R_G$  (except for a gain of  $+1 \text{ V/V}$ ), which causes an increase in gain at high frequencies.  $C_G$  also reduces the phase margin of the feedback loop, which becomes less stable. This effect can be reduced by either reducing  $C_G$  or  $R_F || R_G$ .

$C_N$  and  $R_N$  form a low-pass filter that affects the signal at  $V_P$ . This filter has a single real pole at  $1/(2\pi R_N C_N)$ .

The largest value of  $R_F$  that should be used depends on the noise gain (see  $G_N$  in Section 4.3.6 "Capacitive Loads"),  $C_G$  and the open-loop gain's phase shift. An approximate limit for  $R_F$  is shown in Equation 4-4.

### EQUATION 4-4:

$$R_F \leq 10 \text{ k}\Omega \times \frac{3.5 \text{ pF}}{C_G} \times G_N^2$$

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Some applications may modify these values to reduce either output loading or gain peaking (step response overshoot).

At high gains,  $R_N$  needs to be small in order to prevent positive feedback and oscillations. Large  $C_N$  values can also help.

## 4.3.9 REDUCING UNDESIRED NOISE AND SIGNALS

Reduce undesired noise and signals with:

- Low Bandwidth Signal Filters:
  - Minimize random analog noise
  - Reduce interfering signals
- Good PCB Layout Techniques:
  - Minimize crosstalk
  - Minimize parasitic capacitances and inductances that interact with fast switching edges
- Good Power Supply Design:
  - Isolation from other parts
  - Filtering of interference on supply line(s)

## 4.3.10 SUPPLY BYPASSING AND FILTERING

With this operational amplifier, the power supply pins (only  $V_{DD}$  for single supply) should have a low-ESR ceramic bypass capacitor (i.e., 0.01  $\mu\text{F}$  to 0.1  $\mu\text{F}$ ) within 2 mm of the pins for good high-frequency decoupling.

It is recommended to place a bulk capacitor (i.e., 1  $\mu\text{F}$  or larger) within 100 mm of the device to provide large, slow currents. This bulk capacitor can be shared with other low-noise analog parts.

In some cases, high-frequency power supply noise (e.g., Switched-Mode Power Supplies) may cause undue intermodulation distortion with a DC offset shift; this noise needs to be filtered. Adding a small resistor or ferrite bead into the supply connection can be helpful.

## 4.3.11 PCB DESIGN FOR DC PRECISION

In order to achieve DC precision on the order of  $\pm 1 \mu\text{V}$ , many physical errors need to be minimized. The design of the Printed Circuit Board (PCB), the wiring and the thermal environment have a strong impact on the precision achieved. A poor PCB design can easily be more than 100 times worse than the MCP6V51/2/4 op amps' specifications.

### 4.3.11.1 PCB Layout

Any time two dissimilar metals are joined together, a temperature-dependent voltage appears across the junction (the Seebeck or thermojunction effect). This effect is used in thermocouples to measure temperature. The following are examples of thermojunctions on a PCB:

- Components (resistors, op amps, ...) soldered to a copper pad
- Wires mechanically attached to the PCB
- Jumpers
- Solder joints
- PCB vias

Typical thermojunctions have temperature-to-voltage conversion coefficients of 1 to 100  $\mu\text{V}/^\circ\text{C}$  (sometimes higher).

Microchip's Application Note – AN1258, "Op Amp Precision Design: PCB Layout Techniques" (DS01258) contains in-depth information on PCB layout techniques that minimize thermojunction effects. It also discusses other effects, such as crosstalk, impedances, mechanical stresses and humidity.

### 4.3.11.2 Crosstalk

DC crosstalk causes offsets that appear as a larger input offset voltage. Common causes include:

- Common-Mode noise (remote sensors)
- Ground loops (current return paths)
- Power supply coupling

Interference from the mains (usually 50 Hz or 60 Hz) and other AC sources can also affect the DC performance. Nonlinear distortion can convert these signals to multiple tones, including a DC shift in voltage. When the signal is sampled by an ADC, these AC signals can also be aliased to DC, causing an apparent shift in offset.

To reduce interference:

- Keep traces and wires as short as possible
- Use shielding
- Use ground plane (at least a star ground)
- Place the input signal source near the DUT
- Use good PCB layout techniques
- Use a separate power supply filter (bypass capacitors) for these zero-drift op amps

### 4.3.11.3 Miscellaneous Effects

Keep the resistances seen by the input pins as small, and as near to equal as possible, to minimize bias current related offsets.

Make the (trace) capacitances seen by the input pins small and equal. This is helpful in minimizing switching glitch induced offset voltages.

Bending a coax cable with a radius that is too small causes a small voltage drop to appear on the center conductor (the triboelectric effect). Make sure the bending radius is large enough to keep the conductors and insulation in full contact.

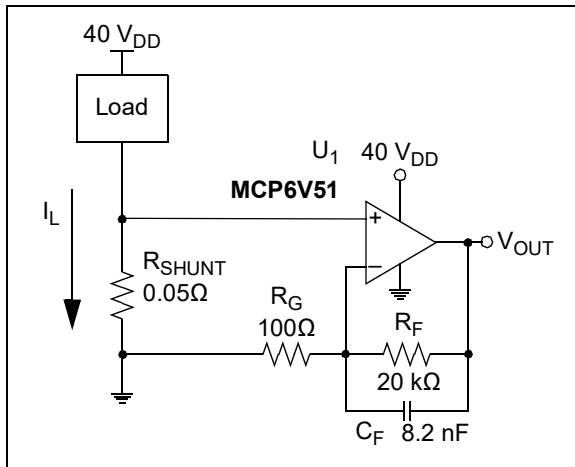
Mechanical stresses can make some capacitor types (such as some ceramics) to output small voltages. Use more appropriate capacitor types in the signal path and minimize mechanical stresses and vibration.

Humidity can cause electrochemical potential voltages to appear in a circuit. Proper PCB cleaning helps, as does the use of encapsulants.

## 4.4 Typical Applications

### 4.4.1 LOW-SIDE CURRENT SENSE

The Common-Mode input range of the MCP6V51/2/4 typically extends to 0.3V below ground ( $V_{SS}$ ), which makes this amplifier a good choice for low-side current sense application, especially where operation on higher supply voltages is required. One such example is shown in Figure 4-11. Here, the Load Current ( $I_L$ ) ranges from 0A to 1.5A, which results in a voltage drop across the shunt resistor of 0 to 75 mV. The gain on the MCP6V51/2/4 is set to 201 V/V, which gives an output voltage range of about 0V to +15V.



**FIGURE 4-11:** Low-Side Current Sense for 1.5A Maximum Load Current.

This circuit example can be adapted to a wide range of similar applications:

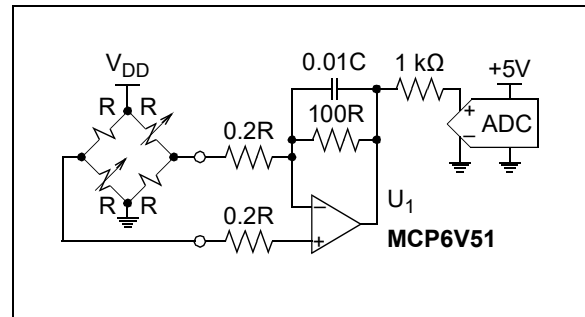
- For  $V_{DD}$  voltages from 4.5V up to 45V
- Adjusting the shunt resistor and/or gain for higher or lower load currents.

Because the MCP6V51/2/4 has a very low offset drift and virtually no 1/f noise, very small shunt resistor values can be selected, which helps in mediating the heating and size problems that may arise in such applications.

### 4.4.2 WHEATSTONE BRIDGE

Many sensors are configured as Wheatstone bridges. Strain gauges and pressure sensors are two common examples. These signals can be small and the Common-Mode noise large. Amplifier designs with high differential gain are desirable.

Figure 4-12 shows how to interface to a Wheatstone bridge with a minimum of components. Because the circuit is not symmetric, the ADC input is single-ended and there is a minimum of filtering; the CMRR is good enough for moderate Common-Mode noise.



**FIGURE 4-12:** Simple Design.

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Figure 4-13 shows a higher performance circuit for a Wheatstone bridge signal conditioning design. This example offers a symmetric, high-impedance load to the bridge with superior CMRR performance. It maintains this high CMRR by driving the signal differentially into the ADC.

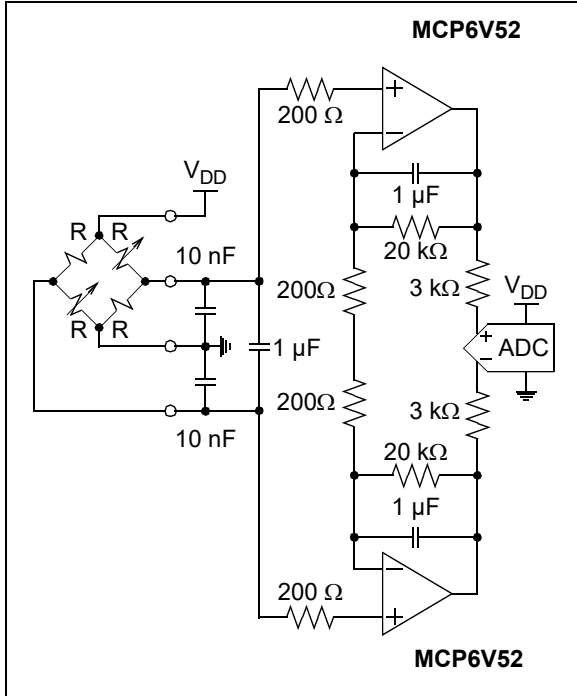


FIGURE 4-13: Higher Performance Design.

## 4.4.3 RTD SENSOR

The ratiometric circuit in Figure 4-14 conditions a two-wire RTD for applications with a limited temperature range.  $U_1$  acts as a difference amplifier, with a low-frequency pole. The sensor's Wiring Resistance ( $R_W$ ) is corrected in firmware. Failure (open) of the RTD is detected by an out-of-range voltage.

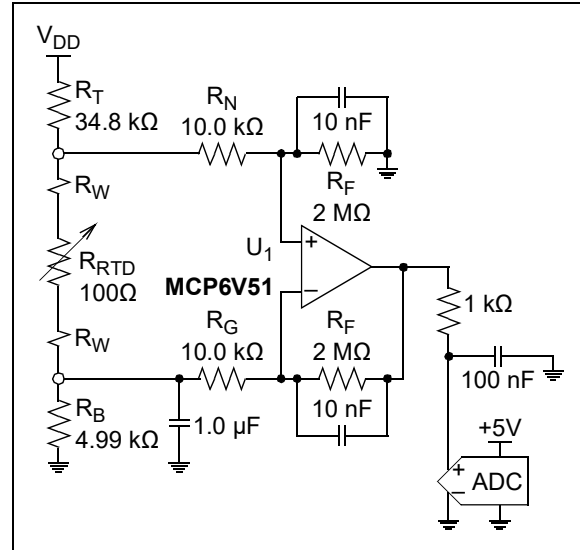


FIGURE 4-14: RTD Sensor.

## 5.0 DESIGN AIDS

Microchip provides the basic design aids needed for the MCP6V51/2/4 op amp.

### 5.1 Microchip Advanced Part Selector (MAPS)

MAPS is a software tool that helps efficiently identify Microchip devices that fit a particular design requirement. Available at no cost from the Microchip website at [www.microchip.com/maps](http://www.microchip.com/maps), MAPS is an overall selection tool for Microchip's product portfolio that includes Analog, Memory, MCUs and DSCs. Using this tool, a customer can define a filter to sort features for a parametric search of devices and export side-by-side technical comparison reports. Helpful links are also provided for data sheets, purchase and sampling of Microchip parts.

### 5.2 Analog Demonstration and Evaluation Boards

Microchip offers a broad spectrum of Analog Demonstration and Evaluation Boards that are designed to help customers achieve faster time to market. For a complete listing of these boards and their corresponding user's guides and technical information, visit the Microchip website at [www.microchip.com/analog\\_tools](http://www.microchip.com/analog_tools).

Some boards that are especially useful are:

- MCP6V01 Thermocouple Auto-Zeroed Reference Design (P/N MCP6V01RD-TCPL)
- MCP6XXX Amplifier Evaluation Board 1 (P/N DS51667)
- MCP6XXX Amplifier Evaluation Board 2 (P/N DS51668)
- MCP6XXX Amplifier Evaluation Board 3 (P/N DS51673)
- MCP6XXX Amplifier Evaluation Board 4 (P/N DS51681)
- Active Filter Demo Board Kit (P/N DS51614)
- 8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board (P/N SOIC8EV)
- 14-Pin SOIC/TSSOP/DIP Evaluation Board (P/N SOIC14EV)

## 5.3 Application Notes

The following Microchip Application Notes are available on the Microchip website at [www.microchip.com/appnotes](http://www.microchip.com/appnotes) and are recommended as supplemental reference resources.

- ADN003, "Select the Right Operational Amplifier for your Filtering Circuits" (DS21821)
- AN722, "Operational Amplifier Topologies and DC Specifications" (DS00722)
- AN723, "Operational Amplifier AC Specifications and Applications" (DS00723)
- AN884, "Driving Capacitive Loads With Op Amps" (DS00884)
- AN990, "Analog Sensor Conditioning Circuits - An Overview" (DS00990)
- AN1177, "Op Amp Precision Design: DC Errors" (DS01177)
- AN1228, "Op Amp Precision Design: Random Noise" (DS01228)
- AN1258, "Op Amp Precision Design: PCB Layout Techniques" (DS01258)

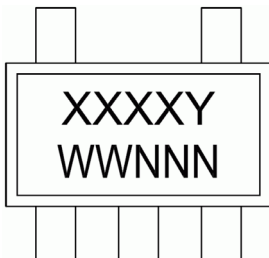


# MCP6V51/2/4

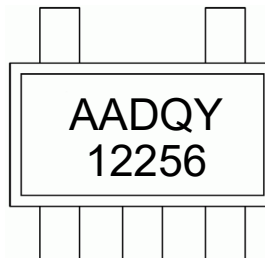
## 6.0 PACKAGING INFORMATION

### 6.1 Package Marking Information

5-Lead SOT-23 (MCP6V51)



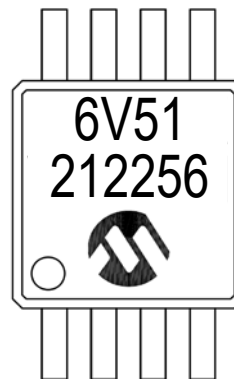
Example



8-Lead MSOP (MCP6V51, MCP6V52)



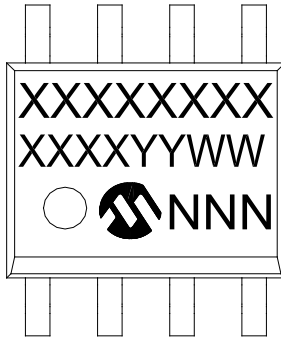
Example



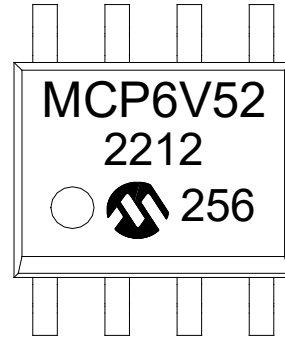
<b>Legend:</b>	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

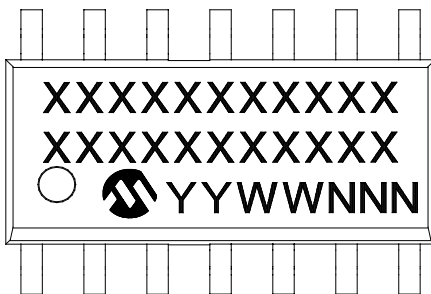
8-Lead SOIC (MCP6V52)



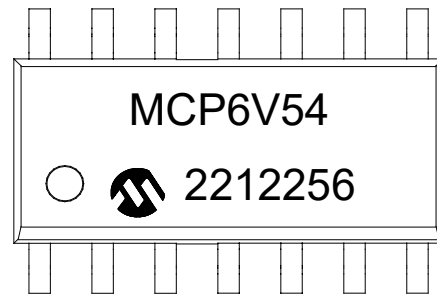
Example



14-Lead SOIC (MCP6V54)



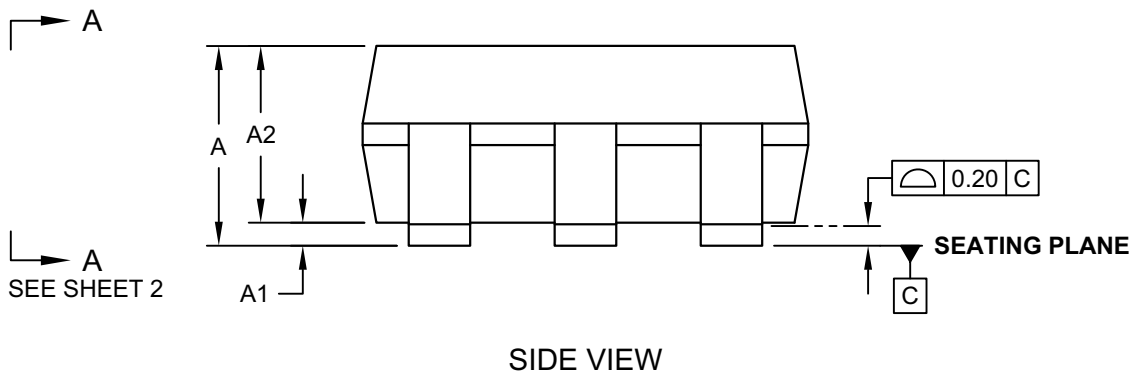
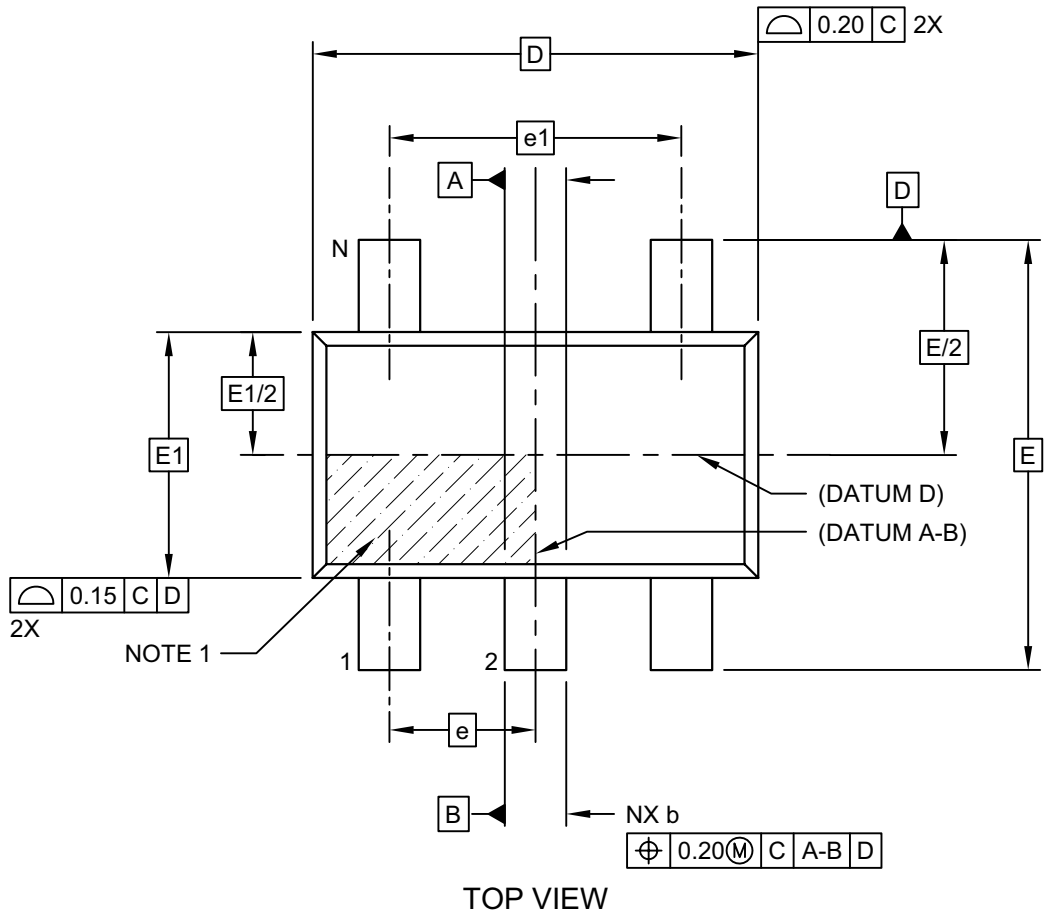
Example



# MCP6V51/2/4

## 5-Lead Plastic Small Outline Transistor (OT) [SOT23]

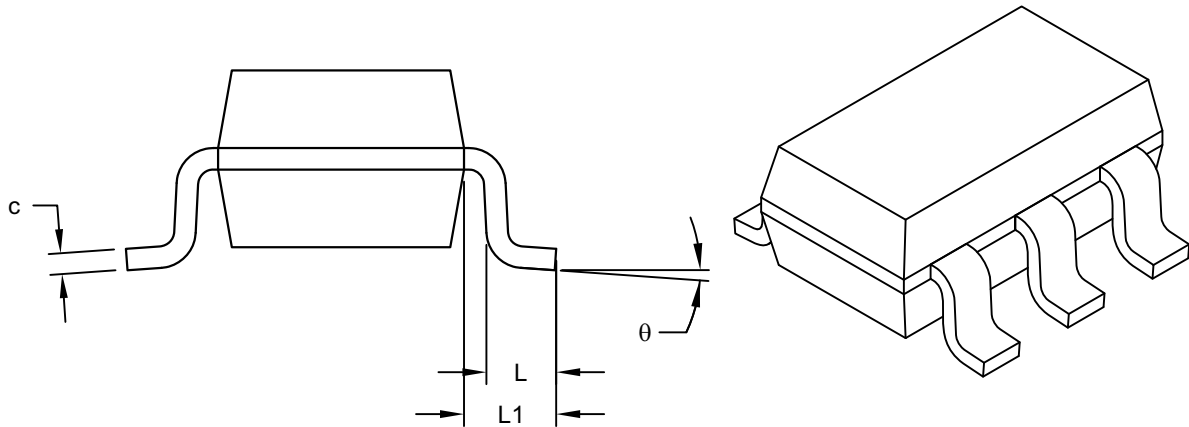
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-091-OT Rev F Sheet 1 of 2

## 5-Lead Plastic Small Outline Transistor (OT) [SOT23]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



VIEW A-A  
SHEET 1

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	5		
Pitch	e	0.95 BSC		
Outside lead pitch	e1	1.90 BSC		
Overall Height	A	0.90	-	1.45
Molded Package Thickness	A2	0.89	-	1.30
Standoff	A1	-	-	0.15
Overall Width	E	2.80 BSC		
Molded Package Width	E1	1.60 BSC		
Overall Length	D	2.90 BSC		
Foot Length	L	0.30	-	0.60
Footprint	L1	0.60 REF		
Foot Angle	φ	0°	-	10°
Lead Thickness	c	0.08	-	0.26
Lead Width	b	0.20	-	0.51

**Notes:**

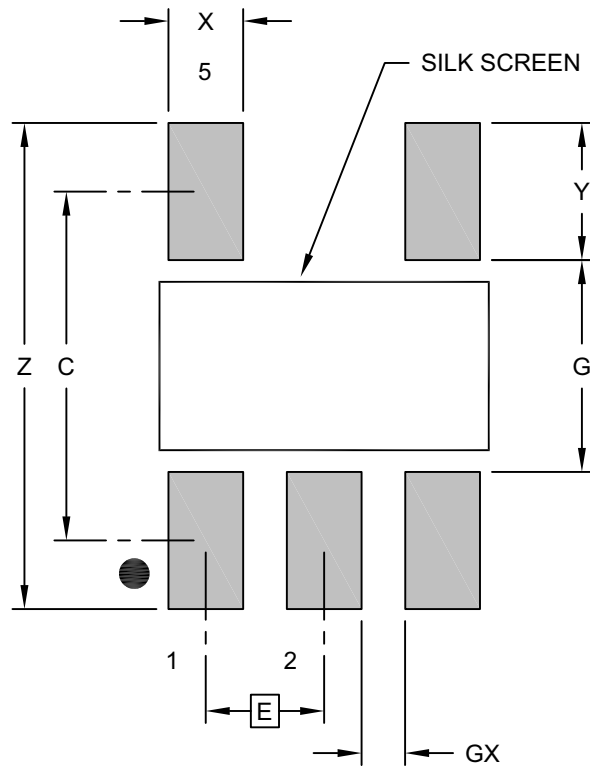
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
- Dimensioning and tolerancing per ASME Y14.5M  
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.  
 REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-091-OT Rev F Sheet 2 of 2

# MCP6V51/2/4

## 5-Lead Plastic Small Outline Transistor (OT) [SOT23]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.95 BSC		
Contact Pad Spacing	C		2.80	
Contact Pad Width (X5)	X			0.60
Contact Pad Length (X5)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

**Notes:**

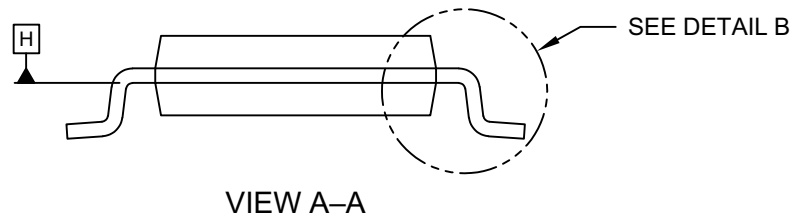
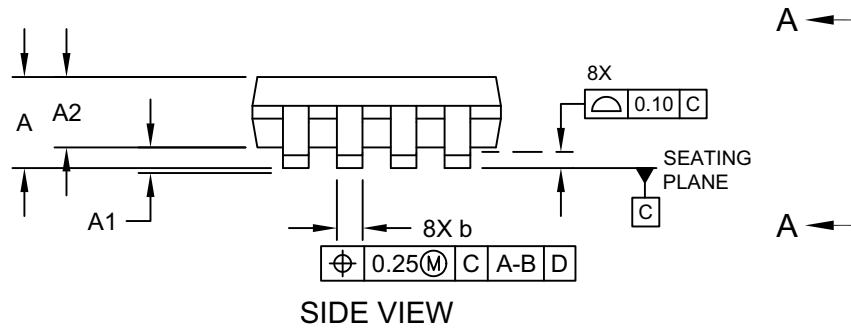
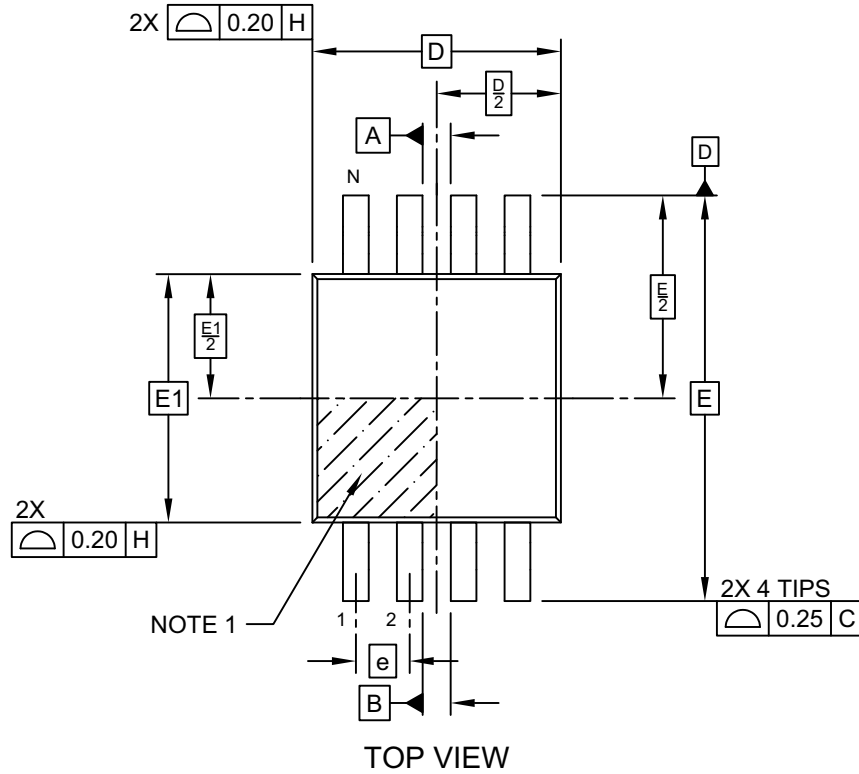
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2091-OT Rev F

## 8-Lead Plastic Micro Small Outline Package (MS) - 3x3 mm Body [MSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

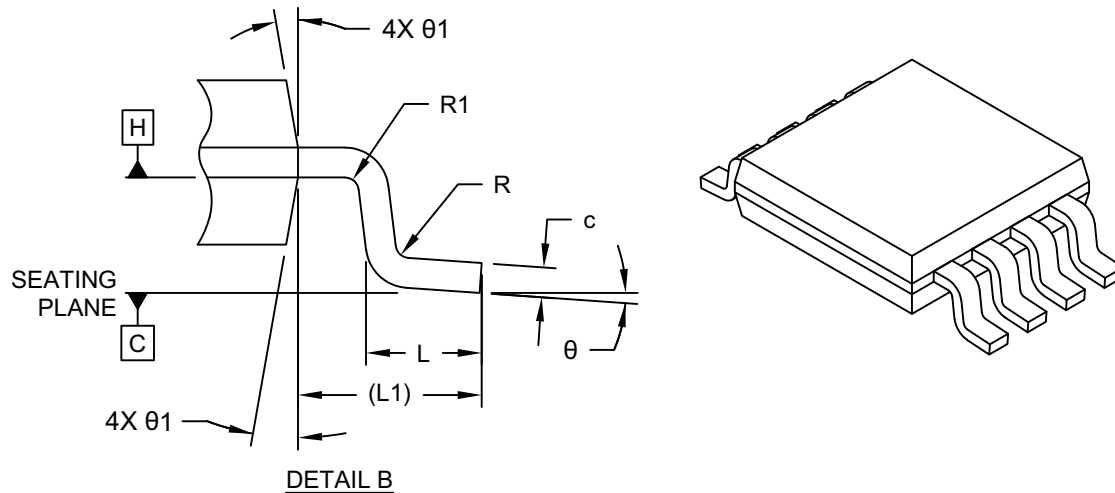


Microchip Technology Drawing C04-111-MS Rev D Sheet 1 of 2

# MCP6V51/2/4

## 8-Lead Plastic Micro Small Outline Package (MS) - 3x3 mm Body [MSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



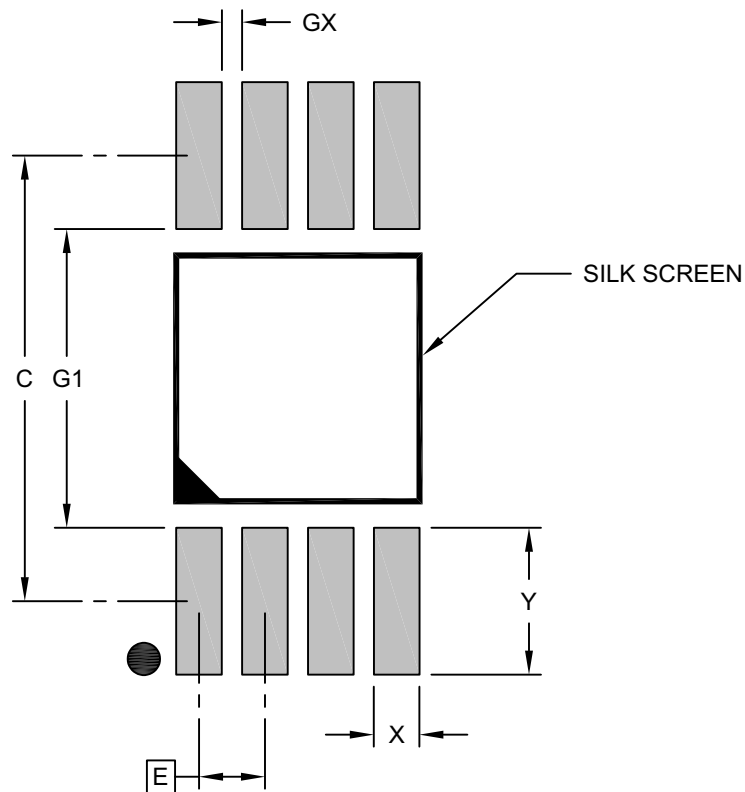
Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Terminals	N	8		
Pitch	e	0.65 BSC		
Overall Height	A	–	–	1.10
Standoff	A1	0.00	–	0.15
Molded Package Thickness	A2	0.75	0.85	0.95
Overall Length	D	3.00 BSC		
Overall Width	E	4.90 BSC		
Molded Package Width	E1	3.00 BSC		
Terminal Width	b	0.22	–	0.40
Terminal Thickness	c	0.08	–	0.23
Terminal Length	L	0.40	0.60	0.80
Footprint	L1	0.95 REF		
Lead Bend Radius	R	0.07	–	–
Lead Bend Radius	R1	0.07	–	–
Foot Angle	θ	0°	–	8°
Mold Draft Angle	θ1	5°	–	15°

**Notes:**

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
- Dimensioning and tolerancing per ASME Y14.5M  
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.  
 REF: Reference Dimension, usually without tolerance, for information purposes only.

## 8-Lead Plastic Micro Small Outline Package (MS) - 3x3 mm Body [MSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



### RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		4.40	
Contact Pad Width (X8)	X			0.45
Contact Pad Length (X8)	Y			1.45
Contact Pad to Contact Pad (X4)	G1	2.95		
Contact Pad to Contact Pad (X6)	GX	0.20		

**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

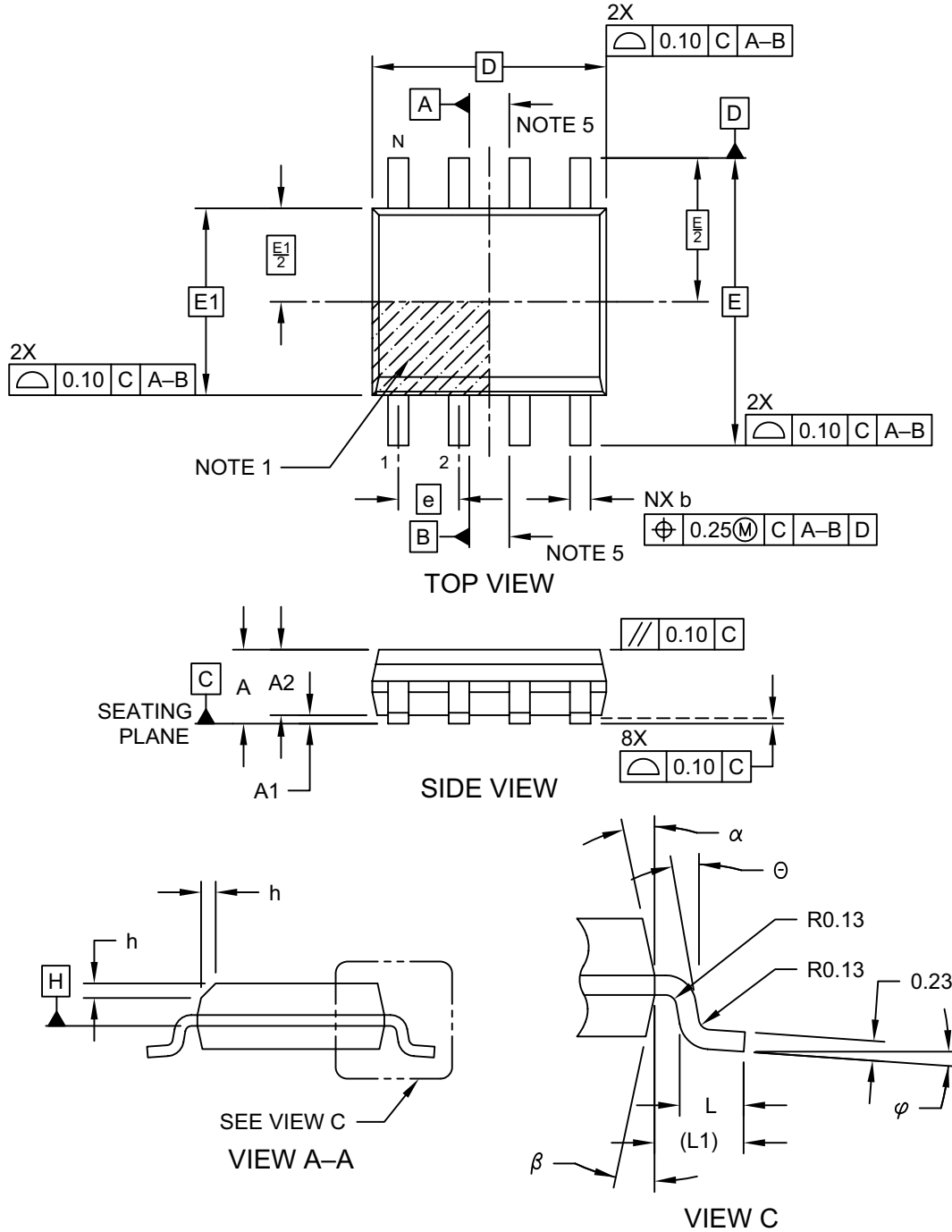
Microchip Technology Drawing C04-2111-MS Rev D



# MCP6V51/2/4

## 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

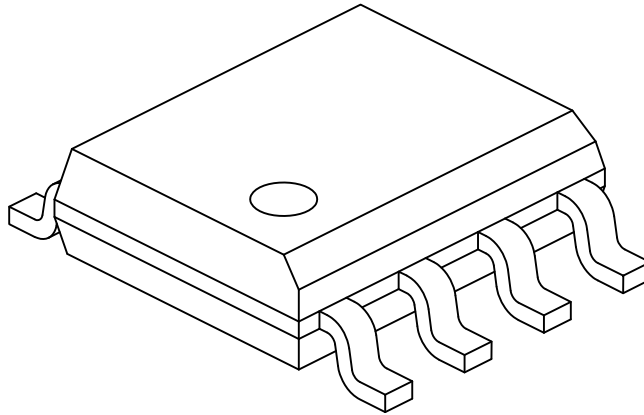
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing No. C04-057-SN Rev F Sheet 1 of 2

## 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1	1.04 REF		
Foot Angle	$\varphi$	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	$\alpha$	5°	-	15°
Mold Draft Angle Bottom	$\beta$	5°	-	15°

**Notes:**

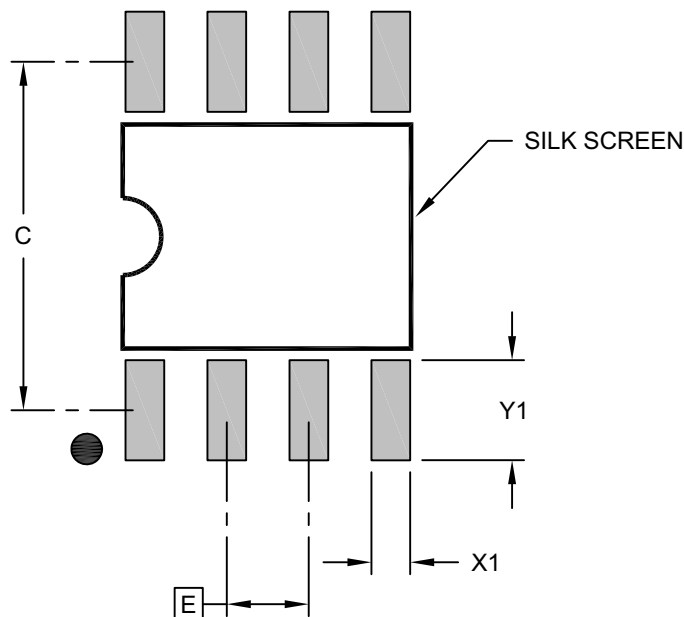
- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
- Dimensioning and tolerancing per ASME Y14.5M
  - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
  - REF: Reference Dimension, usually without tolerance, for information purposes only.
- Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SN Rev F Sheet 2 of 2

# MCP6V51/2/4

## 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



### RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

**Notes:**

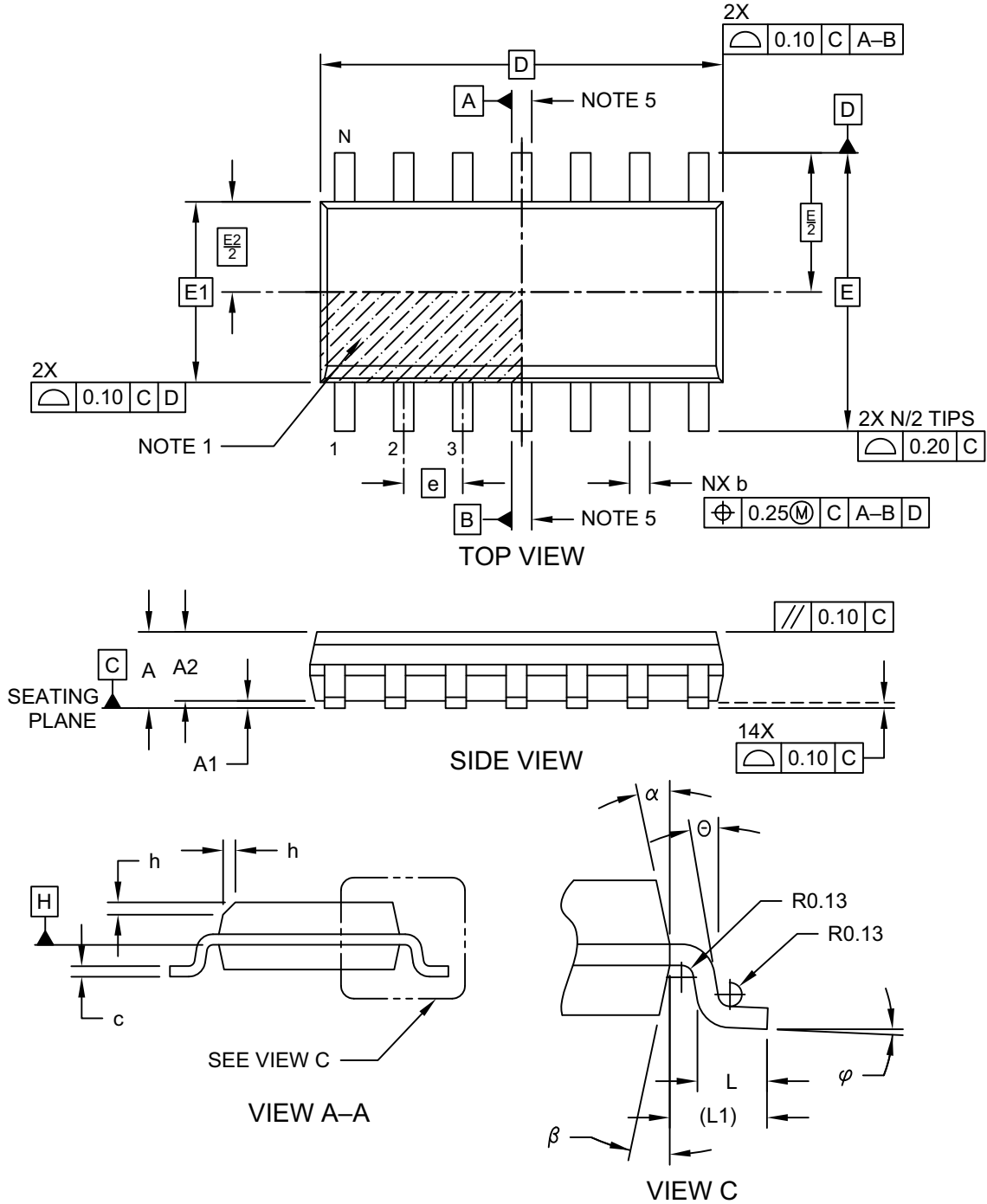
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-SN Rev F

## 14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

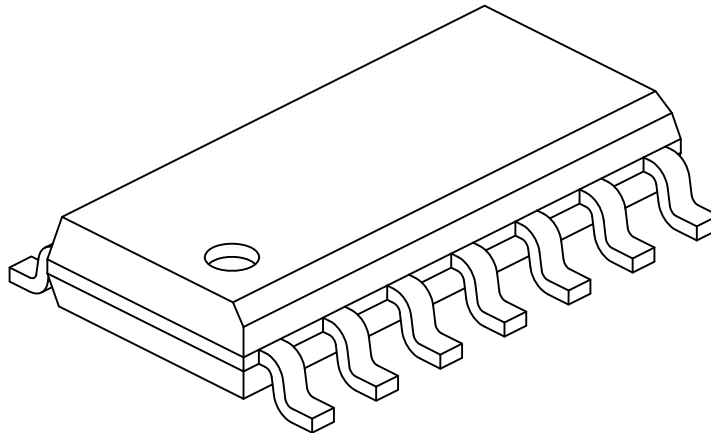


Microchip Technology Drawing No. C04-065-SL Rev D Sheet 1 of 2

# MCP6V51/2/4

## 14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	14		
Pitch	e	1.27 BSC		
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	8.65 BSC		
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1	1.04 REF		
Lead Angle	∅	0°	-	-
Foot Angle	∅	0°	-	8°
Lead Thickness	c	0.10	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

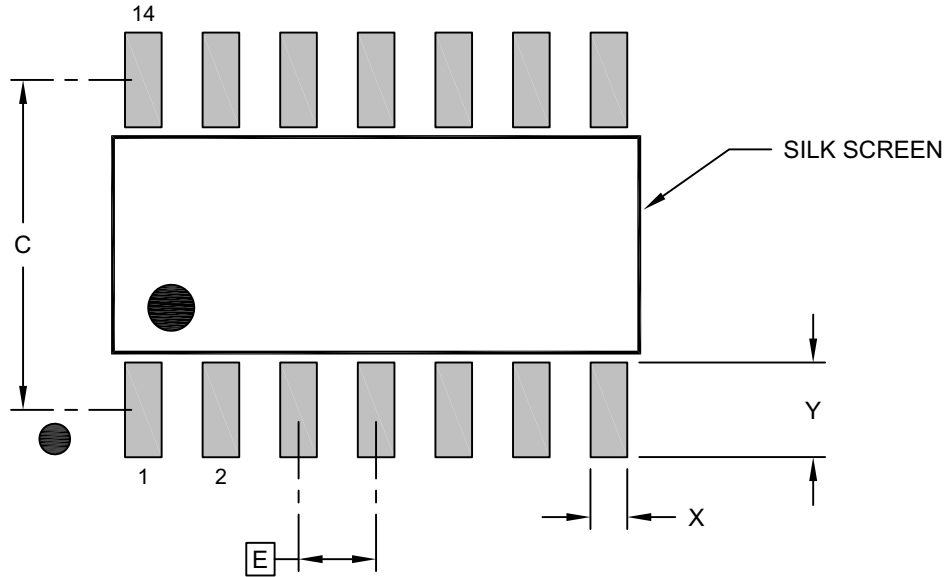
**Notes:**

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic
- Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.  
REF: Reference Dimension, usually without tolerance, for information purposes only.
- Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-065-SL Rev D Sheet 2 of 2

## 14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



### RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X14)	X			0.60
Contact Pad Length (X14)	Y			1.55

**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065-SL Rev D

# MCP6V51/2/4

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NOTES:

## **APPENDIX A: REVISION HISTORY**

### **Revision B (May 2022)**

- Added MCP6V52 and MCP6V54 devices.

### **Revision A (December 2018)**

- Initial release of this document



# MCP6V51

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NOTES:

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>[X]<sup>(1)</sup></u>	<u>X</u>	<u>/XX</u>
Device	Tape and Reel Option	Temperature Range	Package
<p><b>Device:</b> MCP6V5X: 45V, 2 MHz Zero-Drift Op Amp with EMI Filtering</p>			
<p><b>Tape and Reel Option:</b> Blank = Standard packaging (tube or tray) T = Tape and Reel<sup>(1)</sup></p>			
<p><b>Temperature Range:</b> E = -40°C to +125°C (Extended)</p>			
<p><b>Package:</b> OT = 5-Lead Plastic Small Outline Transistor (SOT-23) MS = 8-Lead Plastic Micro Small Outline Package, 3x3 mm Body (MSOP) SN = 8-Lead Plastic Small Outline, Narrow, 3.90 mm Body (SOIC) SL = 14-Lead Plastic Small Outline, Narrow, 3.90 mm Body (SOIC)</p>			
			<p><b>Examples:</b></p> <p>a) MCP6V51T-E/OT: 5-Lead SOT-23 package, Tape and Reel</p> <p>b) MCP6V51-E/MS: 8-Lead MSOP package</p> <p>c) MCP6V51T-E/MS: 8-Lead MSOP package, Tape and Reel</p> <p>d) MCP6V52-E/MS: 8-Lead MSOP package</p> <p>e) MCP6V52T-E/MS: 8-Lead MSOP package, Tape and Reel</p> <p>f) MCP6V52-E/SN: 8-Lead SOIC package</p> <p>g) MCP6V52T-E/SN: 8-Lead SOIC package, Tape and Reel</p> <p>h) MCP6V54-E/SL: 14-Lead SOIC package</p> <p>i) MCP6V54T-E/SL: 14-Lead SOIC package, Tape and Reel</p>
			<p><b>Note 1:</b> Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.</p>

# MCP6V5X

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NOTES:

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