UM11504

KITFS26SKTEVM evaluation board

Rev. 1.0 — 19 February 2021 User manual

Figure 1. KITFS26SKTEVM

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1 Introduction

This document is the user guide for the KITFS26SKTEVM programming board. This document is intended for the engineers involved in the evaluation, design, implementation, and validation of FS26 Fail-safe system basis chip with multiple SMPS and LDO.

The scope of this document is to provide the user with information to evaluate the FS26 Fail-safe system basis chip with multiple SMPS and LDO. This document covers connecting the hardware, installing the software and tools, configuring the environment and using the kit.

The board contains a socket for LQFP48 package in order to allow functional testing and programming of different samples.

2 Finding kit resources and information on the NXP web site

NXP Semiconductors provides online resources for this evaluation board and its supported device(s) on http://www.nxp.com.

The information page for KITFS26SKTEVM evaluation board is at http://www.nxp.com/KITFS26SKTEVM. The information page provides overview information, documentation, software and tools, parametrics, ordering information and a **Getting Started** tab. The **Getting Started** tab provides quick-reference information applicable to using the KITFS26SKTEVM evaluation board, including the downloadable assets referenced in this document.

2.1 Collaborate in the NXP community

The NXP community is for sharing ideas and tips, ask and answer technical questions, and receive input on just about any embedded design topic.

The NXP community is at http://community.nxp.com.

3 Getting ready

Working with the KITFS26SKTEVM requires the kit contents, additional hardware and a Windows PC workstation with installed software.

3.1 Kit contents

- Assembled and tested evaluation board and preprogrammed FRDM-KL25Z microcontroller board in an anti-static bag
- 3.0 ft USB-STD A to USB-B-mini cable
- Two connectors, terminal block plug, 2 pos., str. 3.81 mm
- Three connectors, terminal block plug, 3 pos., str. 3.81 mm
- Jumpers mounted on board
- Quick start guide

3.2 Additional hardware

In addition to the kit contents, the following hardware is necessary or beneficial when working with this kit.

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- Power supply with a range of 8.0 V to 40 V and a current limit set initially to 1.0 A

3.3 Windows PC workstation

This evaluation board requires a Windows PC workstation. Meeting these minimum specifications should produce great results when working with this evaluation board.

- USB-enabled computer with Windows 7 or Windows 10

3.4 Software

Installing software is necessary to work with this evaluation board.

- NXP GUI installation package

4 Getting to know the hardware

4.1 Kit overview

The KITFS26SKTEVM provides flexibility to play with all the features of the device and make measurements on the main part of the application. The KL25Z Freedom connected to the board, combined with the FS26 NXP GUI software allows to fully configure and control FS26 SBC. The LQFP48 Socket on board allows to test or to program different samples.

An FS26 SBC sample must be inserted in the socket to enable OTP programming, emulation or evaluation. The performance on this board is limited and KITFS26SKTEVM must be used for further evaluation.

4.1.1 KITFS26SKTEVM features

- VBAT power supply connectors (Jack and Phoenix)
- LQFP48 burn in open top Socket
- VPRE output 3.2 V to 6.35 V
- VBOOST in Independent mode or in Front end topology to support battery cranking profiles
- VCORE output 0.8 V to 3.3 V
- LDO1 and LDO2, from 3.3 V or 5.0 V, up to 400 mA
- VTRK1 and VTRK2, from 3.3 V or 5.0 V, up to 125 mA
- VREF 1% accuracy regulator for external ADC reference
- FS0B, FS1b external safety pins
- USB to SPI protocol for easy connection to software GUI.
- LEDs that indicate signal or regulator status
- Manual or Automated OTP fuse programming.
- Advance system monitoring via AMUX or external ADC.
- Analog variable resistor to test external VMON

4.2 Kit featured components

Figure 2 identifies the location of some of the main KIT features.

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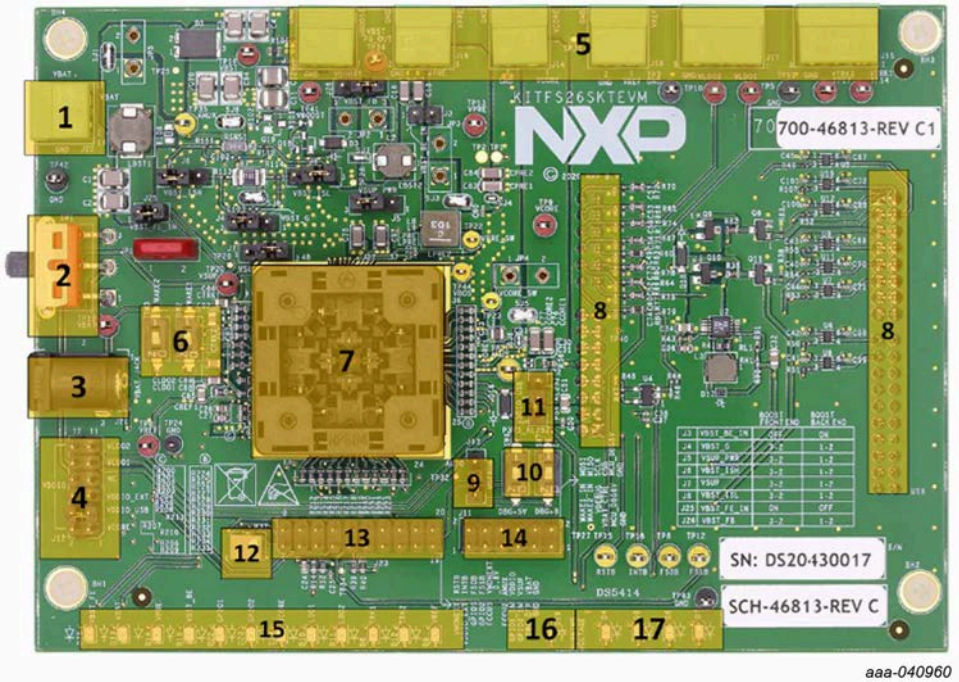

1. VBAT Phoenix connector
2. VBAT 3 position switch
3. VBAT Jack connector
4. VDDIO Selection
5. Regulators Outputs
6. WAKE1 and WAKE2 inputs switches
7. LQFP48 socket
8. KL25Z Freedom headers (Bottom)
9. VDEBUG pin source selection (switch or MCU)
10. VDEBUG pin voltage level switches
11. VDDIO USB voltage level selection
12. VMONEXT variable resistor
13. Signal connector
14. Program connector
15. Regulators output LED indicators
16. Program Burning voltage LED indicator
17. Safety outputs LED indicators

Figure 2. Evaluation board featured component locations

4.2.1 LQFP48 open top socket

This KIT is equipped with an LQFP48 open socket. This socket enables FS26 family OTP emulation and OTP programming on several samples with easy insertion or replacement. Socket part number is NP584-048-113 Yamaichi (maximum current per pin 1 A).

In order to insert or change a device you must push the top of the socket and keep it pressed, then carefully insert the IC with aligned pins. Pin 1 is on the top left of the socket.

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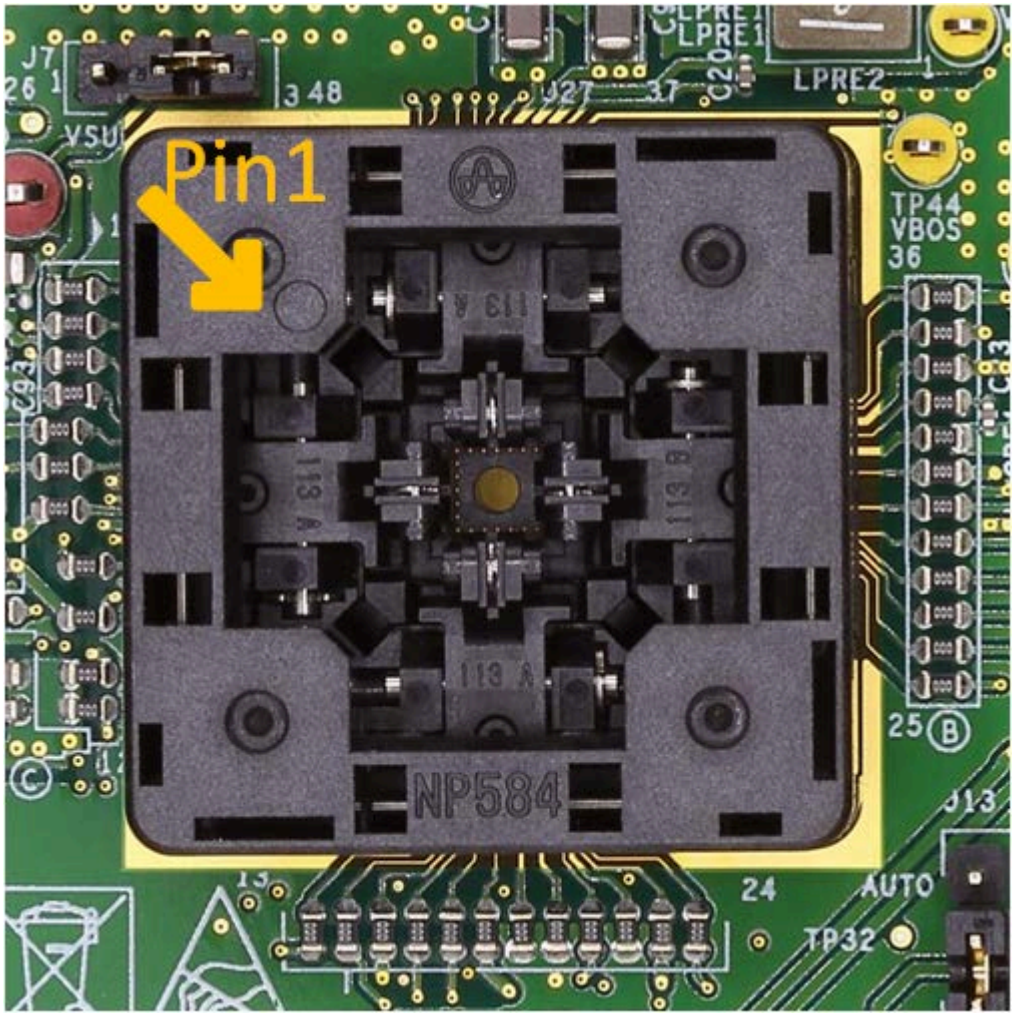

Figure 3. IC insertion on socket

4.2.2 VBAT connectors

There are two ways of supplying the board: either by a Phoenix Connector (J2) or a Jack connector (J2). The selection of the supplying connector is done thanks to a three-position switch (SW1). Figure 4 shows related schematic. Nominal VBAT voltage is 12 V and can support up to 40 V.

Table 1. VBAT Phoenix connector (J20)

Schematic label	Signal name	Description
J20-1	VBAT	Battery voltage supply input
J20-2	GND	Ground

Table 2. VBAT three position connector (SW1)

Schematic label	Signal name	Description
SW1 pin 2-3	VBAT Phoenix	Board supplied by Phoenix connector

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Table 2. VBAT three position connector (SW1)*...continued*

Schematic label	Signal name	Description
SW1 pin 2 (Middle position)	VBAT	Board not supplied
SW1 pin 2-1	VBAT jack	Board supplied by jack connector

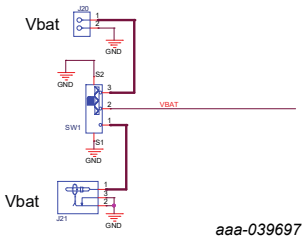

Figure 4. VBAT connectors schematic

4.2.3 Power topology configuration

There are two power topologies available depending on the application and OTP configuration. The device can be supplied directly by the battery after diode and pi filter; on the other side, the boost regulator can be connected in Front end topology to support cold cranking profiles.

It is possible to evaluate both power topologies with this board since external boost components for each topology are soldered separately as shown in Figure 5.

A set of jumper configurations allows you to select between the two options. See Figure 6 and Table 3. Default jumper configuration is boost in front end topology.

In front end topology boost is connected to the battery after reverse diode; the output of the boost supplies the device during cold cranking profiles. Otherwise, boost stops switching, and it is bypassed. See reference [1] for more information.

In back end topology or independent boost, the device is supplied by the battery, and the boost is supplied by the buck regulator VPRE.

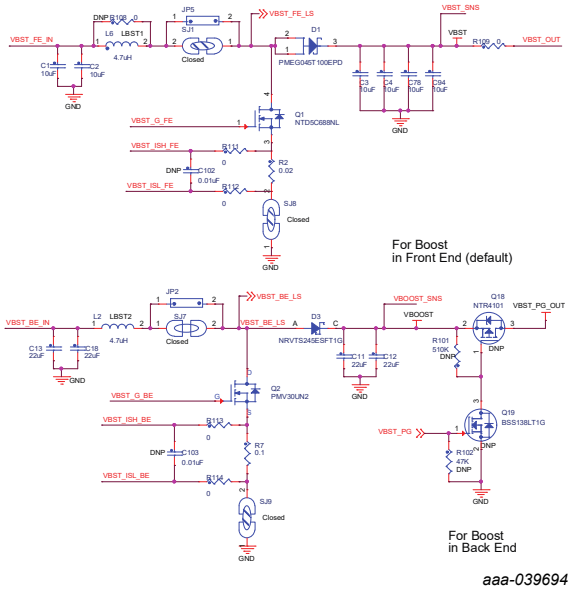

Figure 5. Schematic of boost external components for front end and back end topologies

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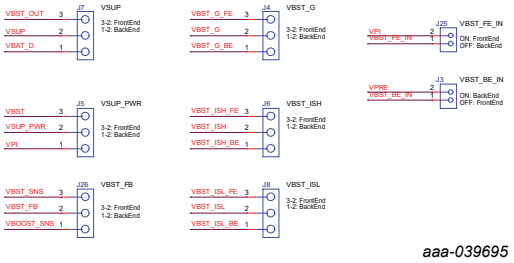

Figure 6. Boost configuration jumper section in EVB schematic

Table 3. Jumper configuration for front end and back end power topologies

Schematic label	Signal Name	BOOST Front end (Default positions)	BOOST Back end
J25	VBST_FE_IN	ON	OFF
J3	VBST_BE_IN	OFF	ON
J7	VSUP	3-2	1-2
J5	VSUP_PWR	3-2	1-2
J4	VBST_G	3-2	1-2
J6	VBST_ISH	3-2	1-2
J8	VBST_ISL	3-2	1-2
J26	VBST_FB	3-2	1-2

Figure 7 shows a simplified diagram of jumper configuration to associated device pins.

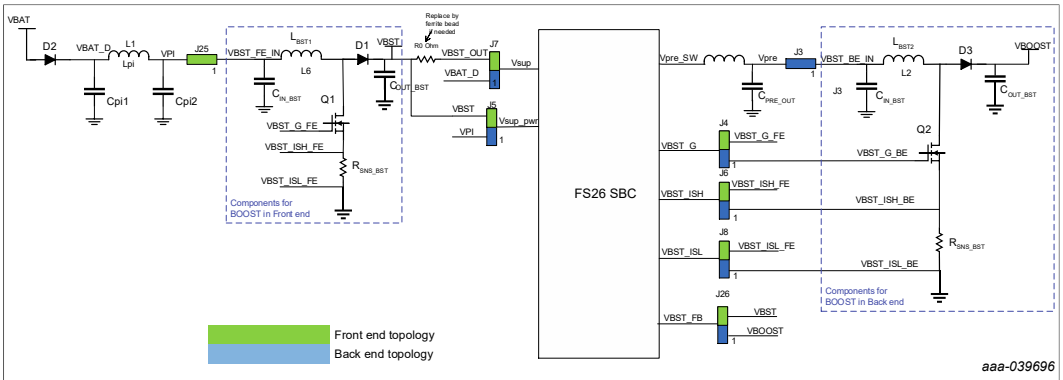

Figure 7. Simplified diagram of jumper configuration for front end and back end topologies

When testing the FS26 SBC with a front end configuration at very low battery level and loading product at its maximum rating, make sure that the power supply is capable of providing at least 4 A.

4.2.4 Output power supply connectors

Output regulators are accessible through test points or Phoenix connectors in order to make measurement or plug loads. Male connectors are included on this kit to plug or unplug wires easily. All output regulators are located at the top edge of the board as shown in Figure 2.

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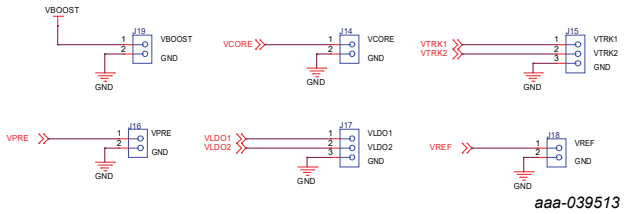

Figure 8. Power output Phoenix connectors

Table 4. VBOOST connector (J19)

Schematic label	Signal name	Description
J19-1	VBOOST	VBOOST power supply output
J19-2	GND	Ground

Table 5. VPRE connector (J16)

Schematic label	Signal name	Description
J16-1	VPRE	VPRE power supply output
J16-2	GND	Ground

Table 6. VCORE connector (J14)

Schematic label	Signal name	Description
J16-1	VCORE	VCORE power supply output
J16-2	GND	Ground

Table 7. VLDO1/VLDO2 connector (J17)

Schematic label	Signal name	Description
J17-1	LDO1	LDO1 power supply output
J17-2	LDO2	LDO2 power supply output
J17-3	GND	Ground

Table 8. VTRK1/VTRK2 connector (J15)

Schematic label	Signal name	Description
J15-1	VTRK1	VTRK2 power supply output
J15-2	VTRK2	VTRK1 power supply output
J15-3	GND	Ground

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Table 9. VREF connector (J18)

Schematic label	Signal name	Description
J18-1	VREF	VREF reference output
J18-2	GND	Ground

4.2.5 Signal and program connectors

Signal and program connectors allow access to most of the device signals in order to program the device externally or to perform debug and diagnosis.

Table 10. Signal connector (J23)

Schematic label	Signal name	Description
J23_1	VMONEXT	External monitoring, resistor bridge side
J23_2	RSTB	RSTB IC safety output
J23_3	VDDIO_EXT	Optional external supply for VDDIO, make sure that there is a jumper between J12 5-6 pins
J23_4	INTB	INTB interruption output
J23_5	GPIO1	GPIO1 IC side, for signal access; disconnect R87 before use as an output
J23_6	FS0B	FS0B IC safety output
J23_7	GPIO2	GPIO2 IC side, for signal access; disconnect R87 before use as an output
J23_8	FS1B	FS1B IC safety output
J23_9	FCCU1	FCCU1
J23_10	VMONEXT_0.8V	VMONEXT IC side, for access or disconnect R39 to apply 0.8 V externally
J23_11	FCCU2	FCCU2
J23_12	AMUX	AMUX pin read
J23_13	GPIO1_IN	GPIO1 input side
J23_14	VDDIO	VDDIO IC side access
J23_15	GPIO2_IN	GPIO2 input side
J23_16	VSUP	VSUP pin access
J23_17	DBG_OTP	DBG_OTP power supply(8V) access
J23_18	VBAT	VBAT access
J23_19	GND	GND
J23_20	GND	GND

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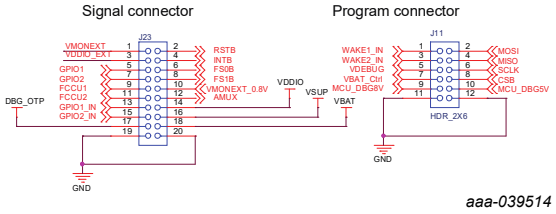

Figure 9. Signal and debug headers connectors

Table 11. Program connector (J11)

Schematic label	Signal name	Description
J11_1	WAKE1_IN	WAKE1 input access
J11_2	MOSI	MOSI signal access
J11_3	MISO	MOSI signal access
J11_4	WAKE2_IN	WAKE2 input access
J11_5	VDEBUG	VDEBUG pin
J11_6	SCLK	SCLK signal access
J11_7	VBAT_Ctrl	VBAT_Ctrl KL25Z output access; to control VBAT power by MCU, JP1 must be OFF
J11_8	CSB	CSB signal access
J11_9	MCU_DBG8V	MCU_DBG8V KL25Z output access
J11_10	MCU_DBG5V	MCU_DBG5V KL25Z output access
J11_11	GND	GND
J11_12	GND	GND

4.2.6 Indicators

On this board there are LEDs to display VBAT regulators, safety outputs, and GPIO status. For VBAT, regulators and GPIOs there are GREEN LEDs indicating that the output is powered on. The power supply of these indicators is usually VPRE, and it is controlled by a low voltage MOSFET by the corresponding signal or regulator.

These regulators can be turned off manually at any time with the switch SW4 in order to avoid undesired losses and obtain more accurate current consumption measurements.

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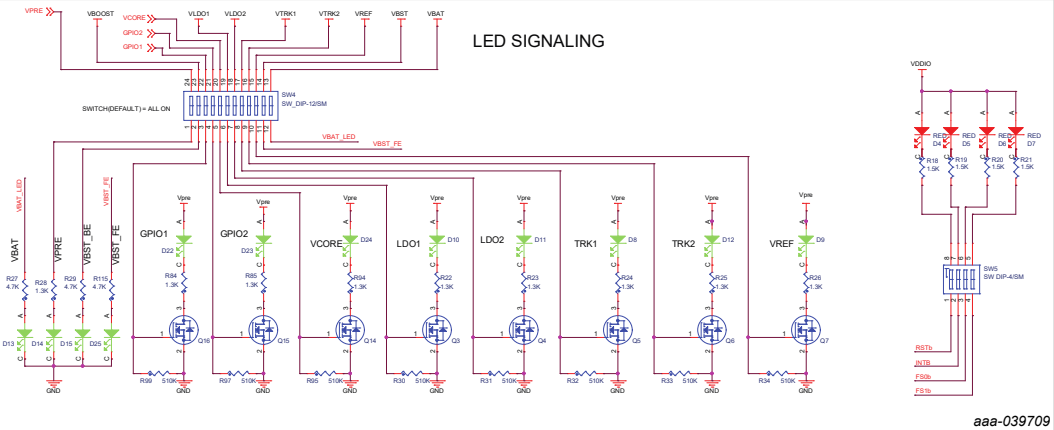

Figure 10. Power and Regulators LED indicators

The color of the Safety outputs LED indicators is RED. When the safety output is asserted, LED indicators are turned on and off when the safety output is released. LEDs can be disabled as well using switch SW5.

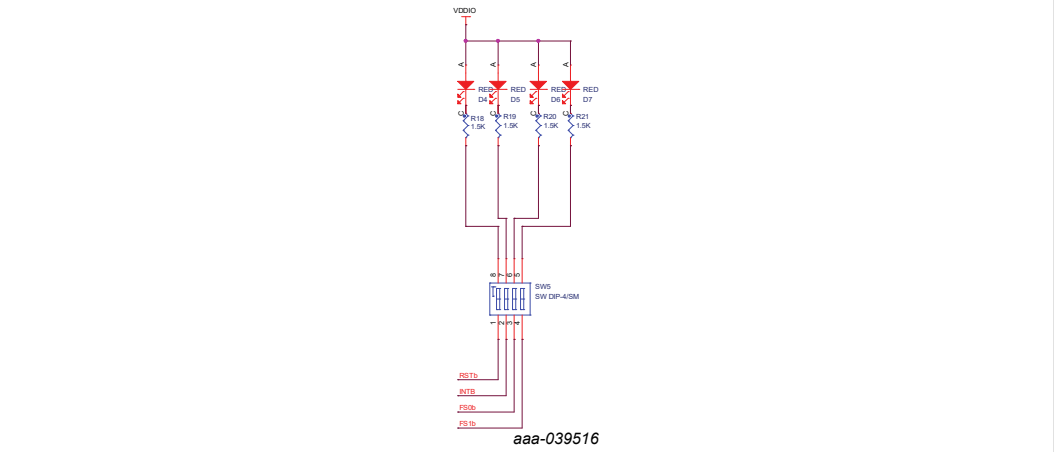

Figure 11. Safety outputs LED indicators

4.2.7 Test points

The KITFS26SKTEVM evaluation board has several test points for easy access and measurements. The test points are color coded, and can be different part numbers or without a part number, as shown in Figure 12.

- Orange: Test loop access to device signals such as safety outputs, analog pins and regulator switch nodes.
- Red: Test loop access for power supplies
- Black: Test loop access to GND
- Blue: Not a part; through hole small test points on board close to the signal

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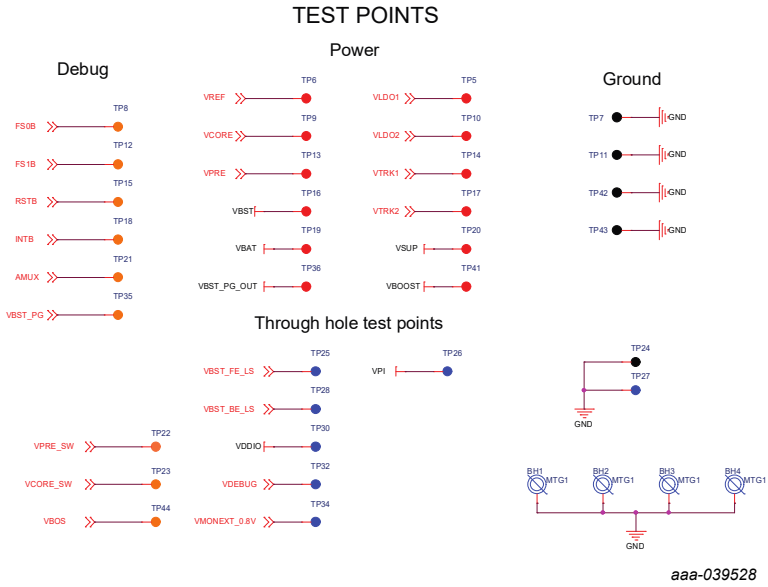

Figure 12. KITFS26SKTEVM test points

4.2.8 VDDIO selection

VDDIO reference can be supplied by 3.3 V or 5 V depending on the system. The supply can be generated on board, from a voltage regulator, or from an external source.

J12 allows selection of the supply source, as shown in Table 12.

Table 12. VDDIO connector (J12)

Schematic label	Signal name	Description
J12_1-2	VCORE	VDDIO supply is VCORE
J12_3-4(Default)	VDDIO_USB	VDDIO supply is VDDIO_USB(J22_2)
J12_5-6	VDDIO_EXT	VDDIO supply is VDDIO_EXT (J23_3)
J12_7-8	NC	VDDIO Not connected
J12_9-10	VLDO1	VDDIO supply is VLDO1
J12_11-12	VLDO2	VDDIO supply is VLDO2

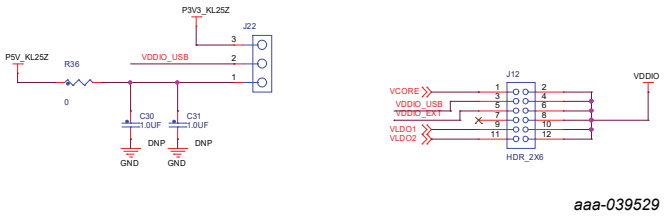

Figure 13. VDDIO source selector headers

4.2.9 Wake input switches

Wake inputs can be exercised by switches SW2 for WAKE1_IN and SW3 for WAKE2_IN. These interrupts are supplied by the battery to VBAT signal.

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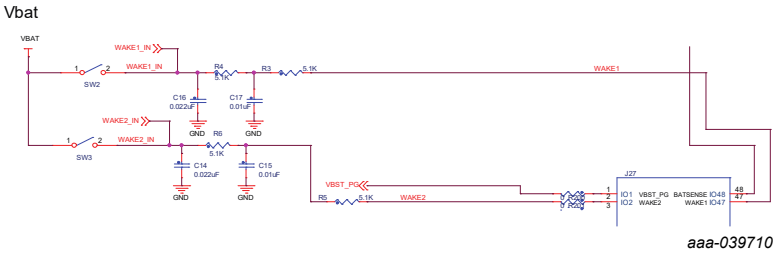

Figure 14. WAKE pins control switches

4.2.10 VDebug pin voltage control

VDEBUG pin allows FS26 SBC to enter the different operating modes to perform debug or programming by applying different voltage thresholds or sequences. These thresholds can be generated on board and debug pin can be controlled manually or fully automated by KL25Z.

The selection for manual (default) or automatic is done by J13.

Table 13. Debug control selector (J13)

Schematic label	Signal name	Description
J13_1-2	Manual (default)	Debug threshold are control by SW6 and SW7
J13_2-3	Automatic	Debug thresholds are controlled by KL25Z

Different voltage levels and sequences can be used to enter debug mode, emulate an OTP configuration, or burn an OTP configuration to the fuses. The threshold levels are:

- **VDEBUG < VDBG4TH (VDEBUG < 4.2 V):** Waive debug entry at power up or after low power modes exit.
- **VDEBUG > VDBG4TH (VDEBUG > 4.2 V):** Enter debug mode at power up or after low power modes exit.
- **VDEBUG VDBG65TH (VDEBUG > 6.9 V):** Burning level for OTP programming.

The power supply to generate the debug entry voltage threshold comes from KL25Z USB. This means that Freedom and USB must be plugged in. Burning voltage for OTP is generated by an on-board boost IC that is also powered by KL25Z Freedom.

For Manual mode use SW6 to allow connection to 5 V power supply, and SW7 to connect to 8 V power supply; when VDBG65TH is reached a blue LED (D19) turns on. Table 14 shows the possible output voltage level to apply to VDebug pin depending on SW6 and SW7 positions.

Table 14. SW6 and SW7 VDebug output configuration

SW6	SW7	VDebug (J13-2) voltage level
OFF	OFF	0 V
OFF	ON	7.8 V
ON	OFF	4.5 V
ON	ON	7.8 V

When automatic mode is selected on connector J13 and KL25Z is plugged in and used, 5 V and 8 V thresholds can be controlled on the NXP GUI by KL25Z signals. It is

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also possible to control VBAT by an MCU signal to generate automated sequences for program and emulations; these signals are:

- VBAT_Ctrl: Open or close VBAT power supply
- MCU_DBG5V: 5 V on VDebug pin
- MCU_DBG8V: 8 V on VDebug pin

Debug mode entry

To enter debug mode, follow the below sequence:

1. VBAT OFF (SW1)
2. VDebug (J13) > VDBG4TH
3. VBAT ON (SW1)
4. At this step debug mode is enabled and you can emulate an OTP configuration or access the SPI register map. You can read FS_STATES register to verify you are in debug mode.

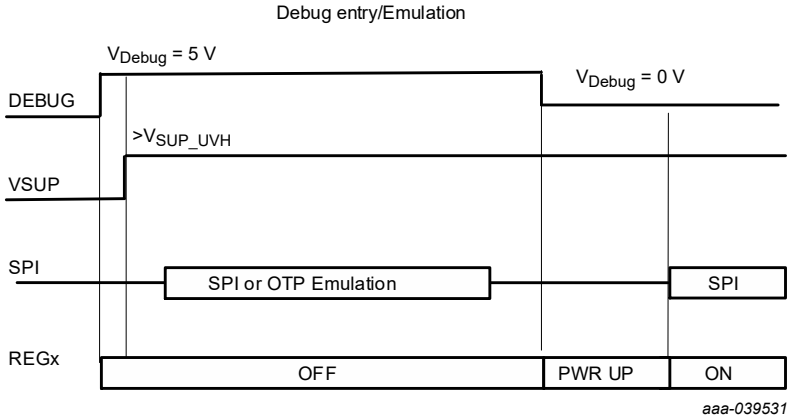

Figure 15. Debug entry voltage sequence

OTP programming

To burn an OTP configuration on the fuses permanently, the following sequence must be applied. More detailed instructions are explained in Section 8.5 "Program an OTP configuration".

1. VBAT OFF (SW1)
2. VDebug (J13) > VDBG4TH (SW6 ON).
3. VBAT ON (SW1)
4. At this step debug mode is enabled and you can emulate an OTP configuration or access the SPI register map. You can read FS_STATES register to verify you are in debug mode.
5. VDebug (J13) > VDBG65TH (SW7 ON). If the threshold is applied D19 blue LED turns on.
6. Load an OTP configuration file and wait until all commands are sent.
7. Put VDebug (J13) to 0 V (first SW7 and then SW6)
8. The device should power up with selected OTP configuration or you can restart the device power supply to load the burned OTP configuration from fuses.

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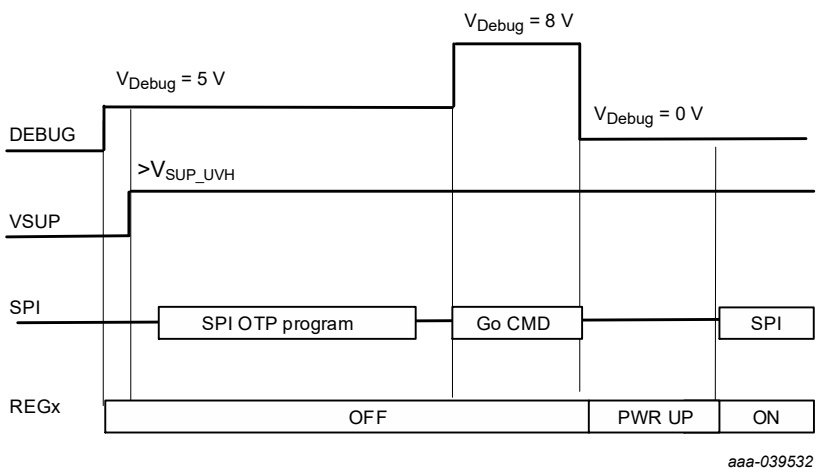

Figure 16. OTP programming voltage sequence

Figure 17 shows the VDebug voltage sources and its selection.

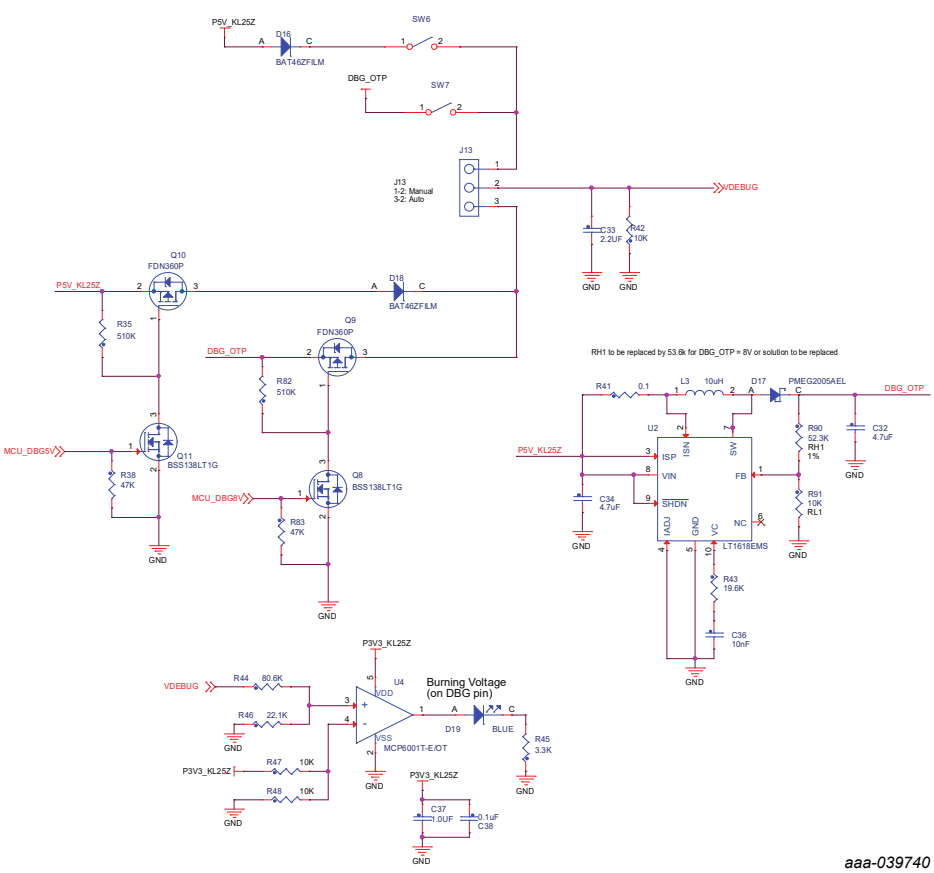

Figure 17. VDebug pin source selection schematic

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4.2.11 VMONEXT monitoring

FS26 VMONEXT monitoring pin can be accessed in different ways. VMONEXT value should always be 0.8 V if used. VMONEXT signal can be supplied by any source or regulator and VMONEXT_0.8V value can be adjusted by using a screwdriver on R37 potentiometer. Default bridge resistor is 22.2 kΩ.

To apply 0.8 V directly to VMONEXT_0.8V, remove R39 and apply 0.8 V to connector J10_1.

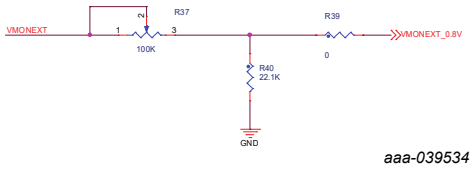

Figure 18. VMONEXT voltage resistor bridge schematic

4.2.12 GPIO1 and GPIO2

GPIO1 and GPIO2 FS26 pins are connected by default as outputs, and can be accessed by J10 connector.

- J10_5 for GPIO1
- J10_7 for GPIO2.

To exercise GPIO pins as inputs, R87 and R89 must be populated in order to apply voltage before RC filter. GPIO input supply can be applied through J10 header.

- GPIO1_IN can be access through J10_13, R87 must be populated.
- GPIO2_IN can be access through J10_15, R89 must be populated.

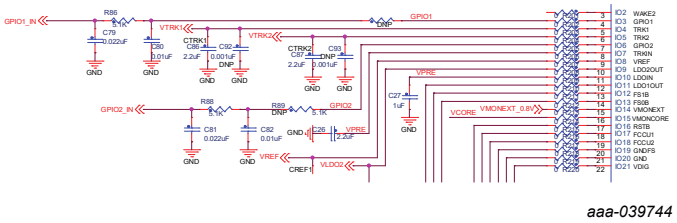

Figure 19. GPIO1 and GPIO2 schematics

Note: There are no external pull-ups or pull-downs for the GPIO. If the internal pull-ups or pull-downs are not enabled by OTP you can add external PU/PD through J10.

4.3 Default jumper configuration

KIT is provided with the below default jumper configuration. This configuration is suited for a Boost in front end topology.

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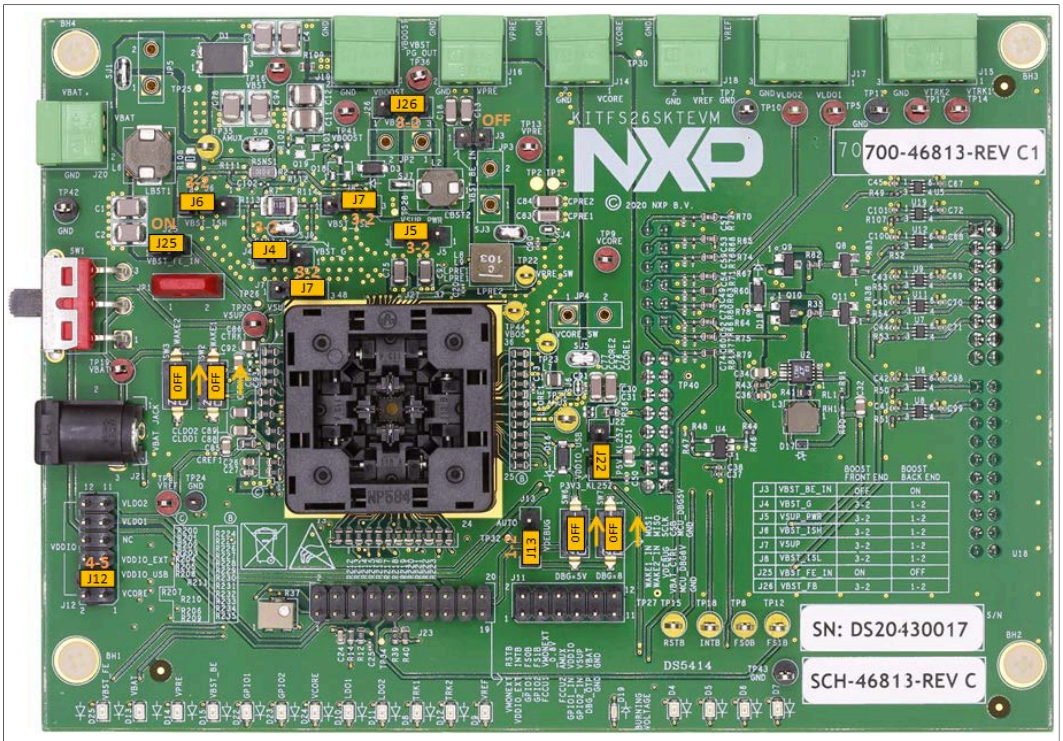

Figure 20. Default jumper configuration on KITFS26SKTEVM

4.4 Schematic, board layout and bill of materials

The schematic, board layout and bill of materials for the KITFS26SKTEVM evaluation board are available at http://www.nxp.com/KITFS26SKTEVM.

5 Installing and configuring software and tools

5.1 Flashing or updating the GUI firmware

The KITFS26SKTEVM is delivered with the GUI firmware flashed. If MCU firmware is flashed, ignore this section. If it is specified to update the firmware or it is malfunctioning, follow these instructions:

5.1.1 Flashing Freedom board firmware for Windows 7

Steps 1 and 2 are not required if BOOTLOADER is already loaded in the Freedom board and a start is required from Step 3.

1. Press the RST push button and connect the USB cable into the SDA port on the Freedom board.
   - A new “BOOTLOADER” device should appear on the left pane of the File explorer.
2. Drag and drop the file “MSD-DEBUG-FRDM-KL25Z_Pemicro_v118.SDA” into the BOOTLOADER drive.
   - ***Note:*** *Make sure to allow enough time for the firmware to be saved in the Boot loader.*

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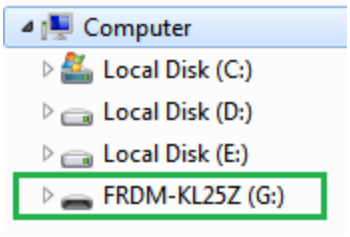
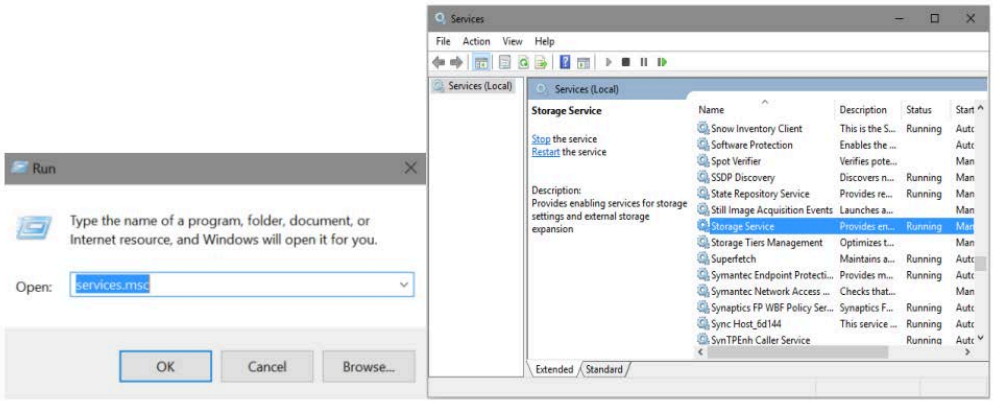
3. Disconnect and reconnect the USB cable into the SDA port.
   - This time WITHOUT pressing the RST push button, FRDM_KL25Z device should appear on the left pane of the File explorer as pictured below.



4. Locate the file “nxp-gui-fw-frdmkl25z-usb_hid-fs2630_vX.Y.bin” from the package and drag and drop the file into the FRDM_KL25Z device.
   - ***Note:*** *Make sure to allow enough time for the firmware to be saved.*
5. Freedom board Firmware is successfully loaded. Disconnect and reconnect the USB cable into the KL25Z USB port.

5.1.2 Flashing Freedom board firmware from Windows 10

1. Disable the storage services: Run the services, double click on the storage service from the list and press the stop button.



   Steps 2 and 3 are not required if BOOTLOADER is already loaded in the Freedom board and a start is required from Step 4.
2. Press the RST push button and connect the USB cable into the SDA port on the Freedom board.
   a. A new “BOOTLOADER” device should appear on the left pane of the File explorer.
3. Drag and drop the file “MSD-DEBUG-FRDM-KL25Z_Pemicro_v118.SDA” into the BOOTLOADER drive.
   a. ***Note:*** *Make sure to allow enough time for the firmware to be saved in the Boot loader.*

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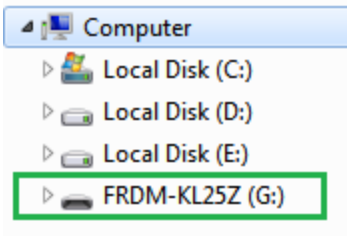
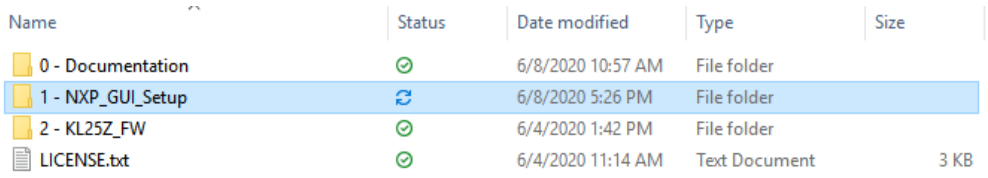
4. Disconnect and reconnect the USB cable into the SDA port.
   - This time WITHOUT pressing the RST push button, FRDM_KL25Z device should appear on the left pane of the File explorer as pictured below.



5. Locate the file “nxp-gui-fw-frdmkl25z-usb_hid-fs2630_vX.Y.bin” from the package and drag and drop the file into the FRDM_KL25Z device.
   - ***Note:*** *Make sure to allow enough time for the firmware to be saved.*
6. Freedom board Firmware is successfully loaded. Disconnect and reconnect the USB cable into the KL25Z USB port.

5.2 Installing GUI software package

To install the FS26 NXP GUI Download or obtain the NXP GUI package, unzip an open 1-NXP_GUI_Setup folder:



Then double click on the NXP_GUI_version-Setup.exe and follow the instructions.

Proceed with the following pop-up windows to install the application on Windows PC:

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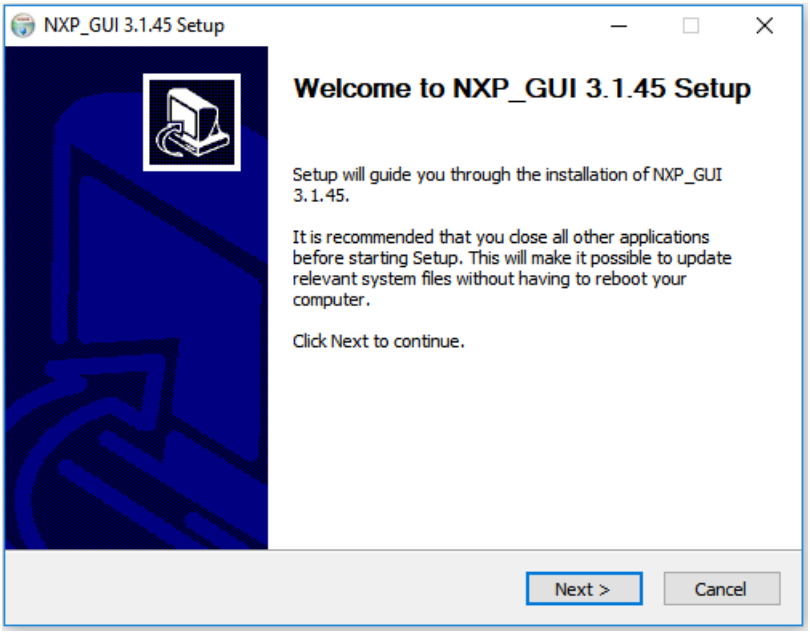

Figure 21. Application setup initial window

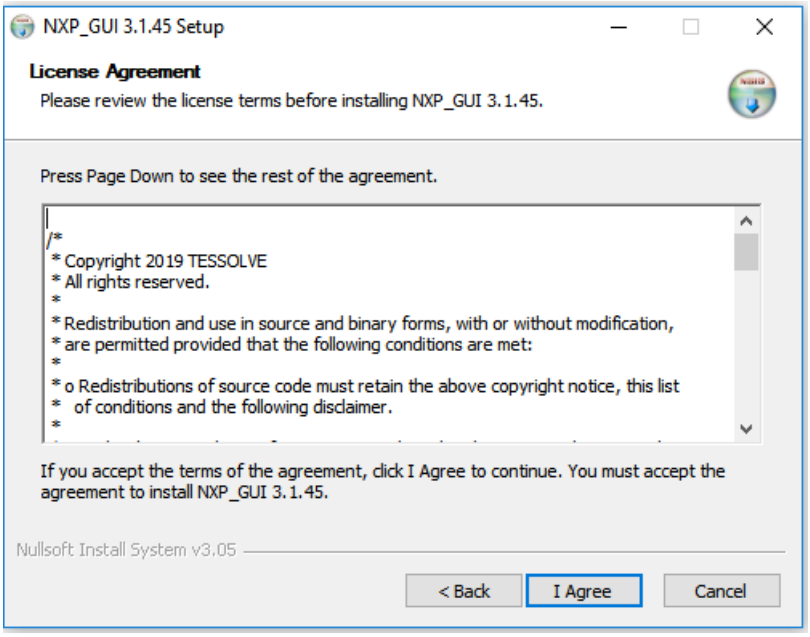

Figure 22. License agreement window

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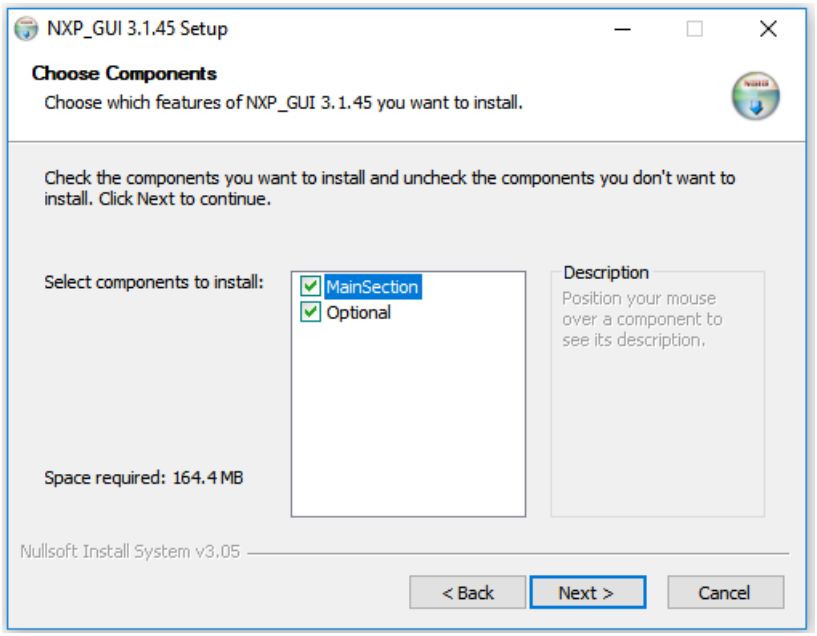

Figure 23. Select FS2630_GUI feature

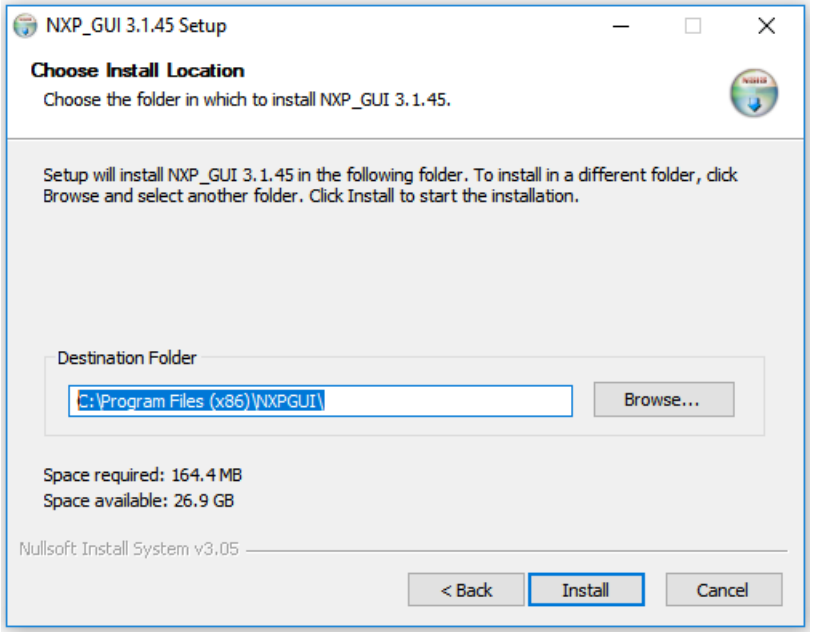

Figure 24. Choose the folder to install

Select the below options before completing the installation of the setup

- Run NXP_GUI
- Show Readme

Select **Finish** to complete the installation

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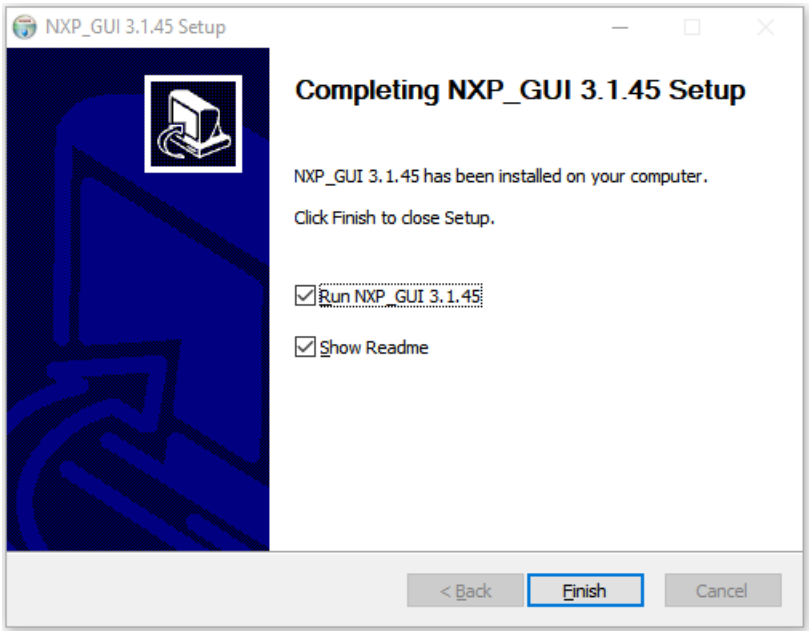

Figure 25. Run NXP_GUI

When installation is finished the application can be found in the windows search bar as “NXPGUI”. Click to launch

6 Configuring the hardware

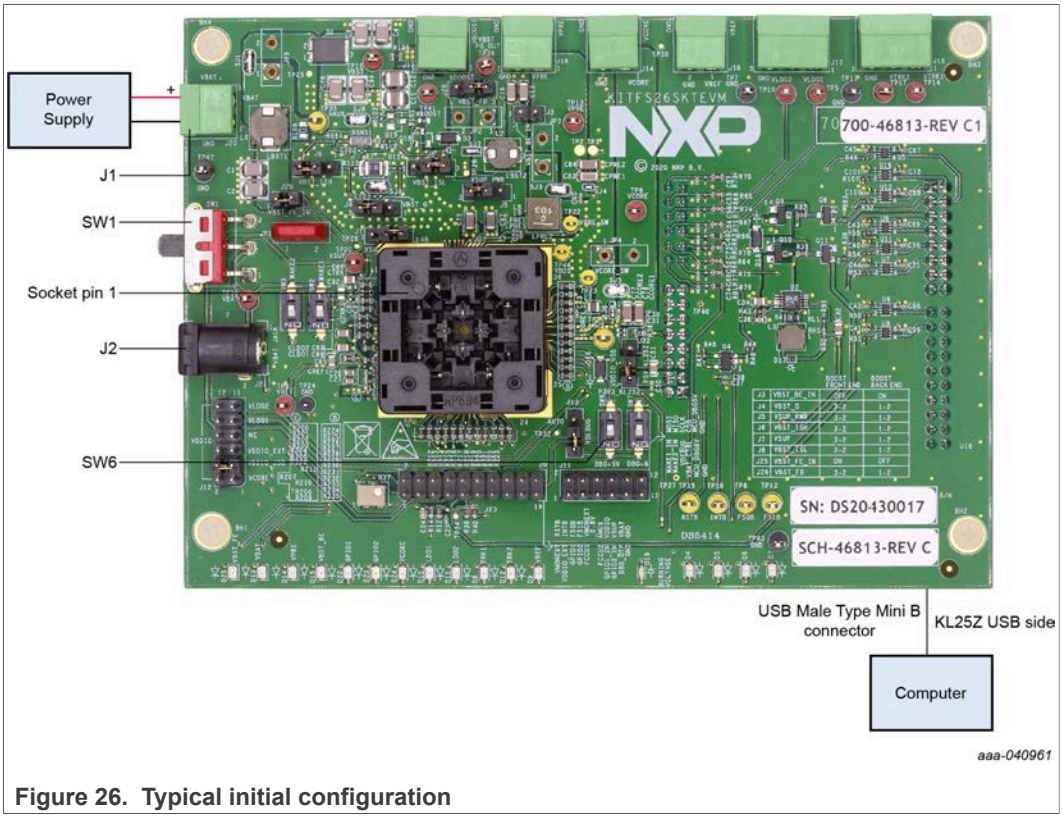

Figure 26. Typical initial configuration

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To configure the hardware and workstation, complete the following procedure:

1. With board disconnected, push and insert an FS26 device into the socket. Pin 1 is on the top left of the socket.
2. With SW1 in middle position, set DC power supply to 12 V and current limit to 1.0 A. Attach the DC power supply positive and negative output to KITFS26SKTEVM VBAT Phoenix connector (J1). Or connect 12 V power supply to VBAT Jack (J2).

Table 15. VBAT Phoenix connector (J1)

Schematic label	Signal name	Description
J1-1	VBAT	Battery voltage supply input
J1-2	GND	Ground

Table 16. VBAT three position connector (SW1)

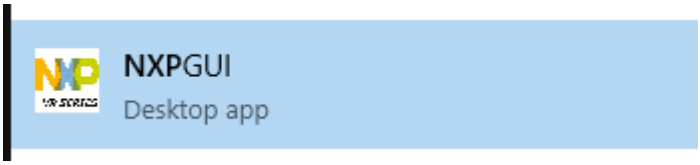
Schematic label	Signal name	Description
SW1 pin 2-3	VBAT Phoenix	Board supplied by Phoenix connector
SW1 pin 2 (middle position)	VBAT	Board not supplied
SW1 pin 2-1	VBAT jack	Board supplied by jack connector

3. Connect the Windows PC USB port to the KL25Z USB side of the freedom board included in KIT, using the provided USB 2.0 cable.
4. Turn On SW6 to apply 5.0 V to the VDebug pin.
5. Turn on the power supply
6. Close SW1

Note: *At this step, the product is in debug mode and all regulators are turned off. The user can then power up with OTP configuration or configure the mirror registers before power up. Power up is effective as soon as SW6 is turned off.*

7 FS26 NXP GUI

Once the KIT is ready and the NXP GUI is installed launch the KIT from the Windows search bar.



Launching FS26_GUI Application

Once the NXP GUI is open, the **Kit Selection** window is displayed. Check for the following settings and select **OK.**

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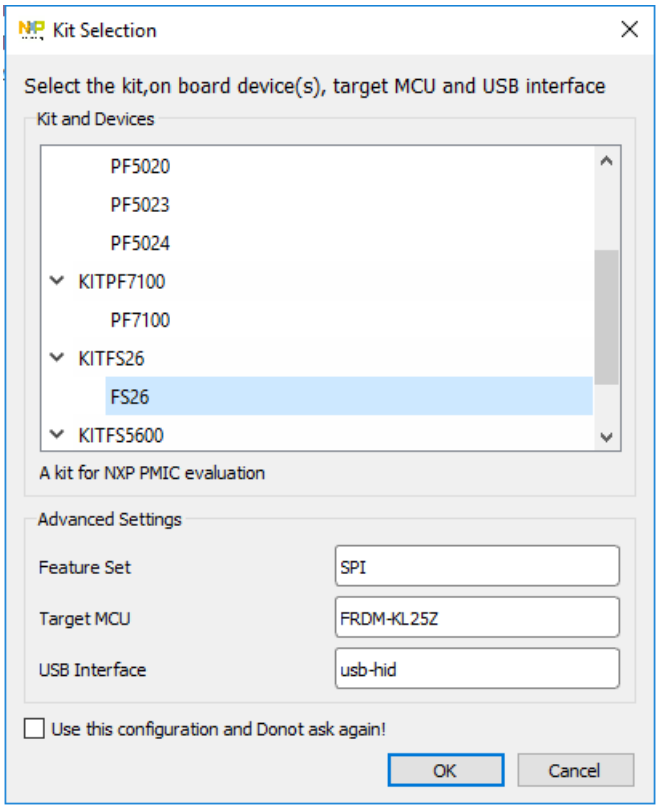
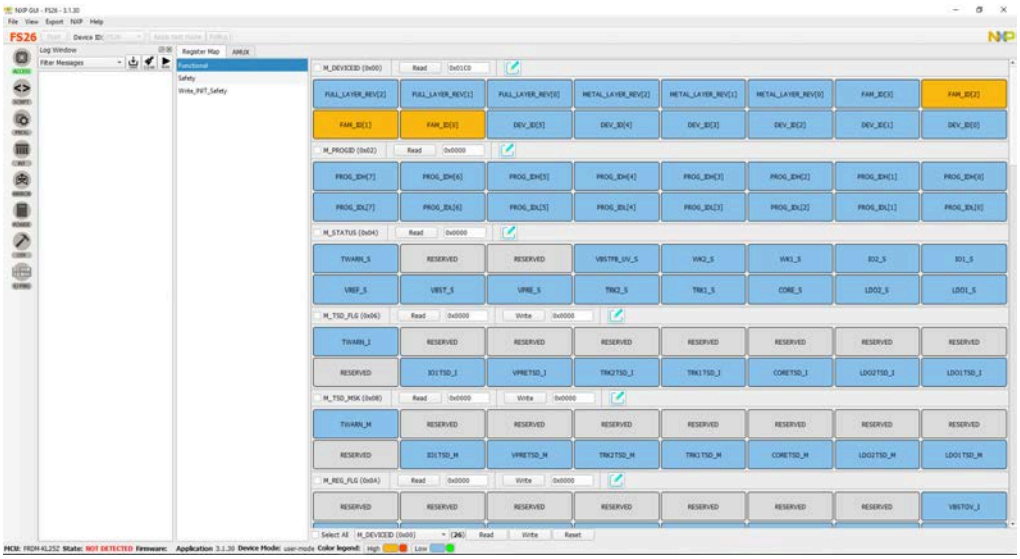


Figure 27. Kit Selection window

To avoid the Kit Selection window on every launch, check the box “Use this configuration and do not ask again”.

The below window opens.



7.1 Framework

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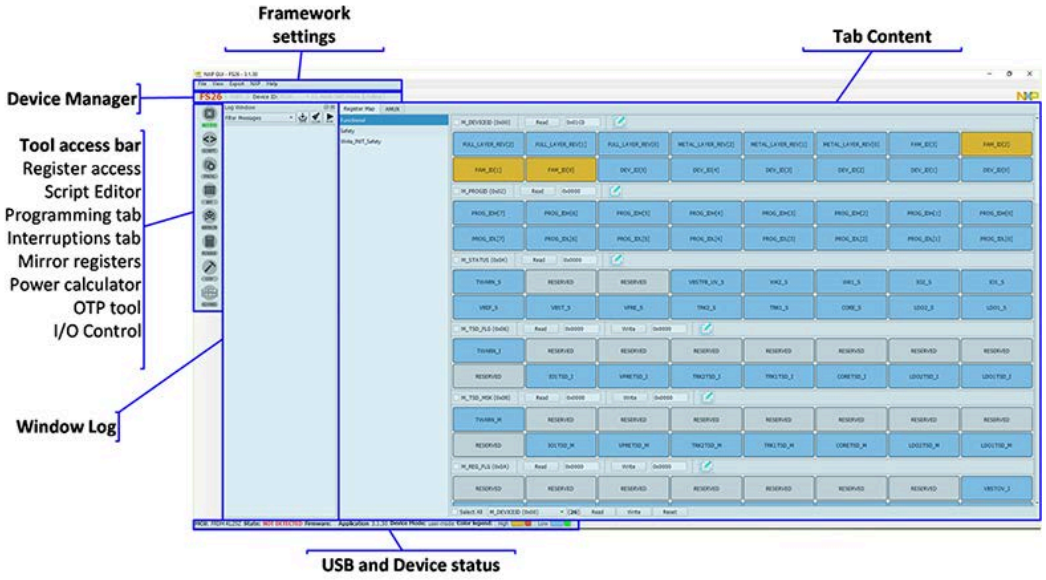

Device Manager: Start communication with device. Enter or exit test mode. Quick access to execute system scripts.

Framework settings: Import or export files, configure framework.

Window log: USB and Device communication events.

USB and Device status: Displays if USB or Device is connected or disconnected. Displays Firmware and GUI version. Display current state of FS state machine; click on display button to refresh.

Tool access bar: Quick access to the FS26 evaluation tools and features.

Tab content: Content of each tool or tab; there can be more tabs, boxes, or windows inside.

7.1.1 Framework settings

The NXP GUI Main Menu has five GUI Elements: File, View, Export, NXP, and Help

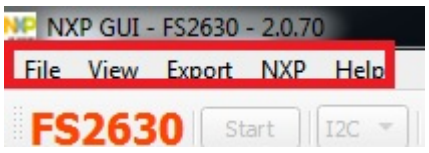

Figure 28. GUI elements

7.1.2 File

Load or save a configuration OR exit the application. Load and Save are only enabled when OTP tool tab is active.

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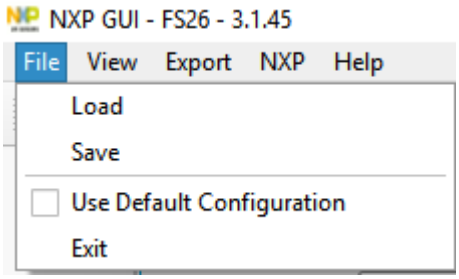

- **Load:** Loads an existing configuration file previously exported from OTP tool to continue to modify it on the OTP tool. This file has a .cfg extension. It is usually named as: FS26_ProgIDASILlevel_CONFIG.cfg. Example: FS26_A0D_CONFIG.cfg.
- **Save:** Saves the current configuration of the OTP tool as a .cfg file.
- **Use default configuration:** Load default values into the OTP tool.
- **Exit:** Exits NXP GUI application

7.1.3 View

This main menu has options that are related to GUI display options and menu, and contains the following subitems:

1. Display
2. Show
3. Naming Conventions

- **Display:** It consists of Connection Tool Bar (enabled by default) option. To show or hide, go to **View>>Display** and select **Connection Tool Bar**

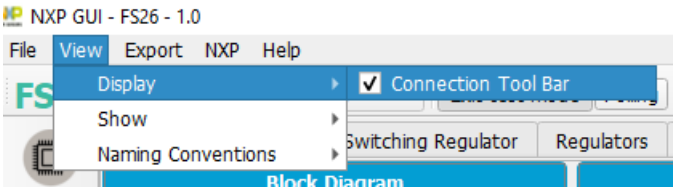

Figure 29. Display options

- **Show:** This option can be used to access various sections of the GUI as shown below

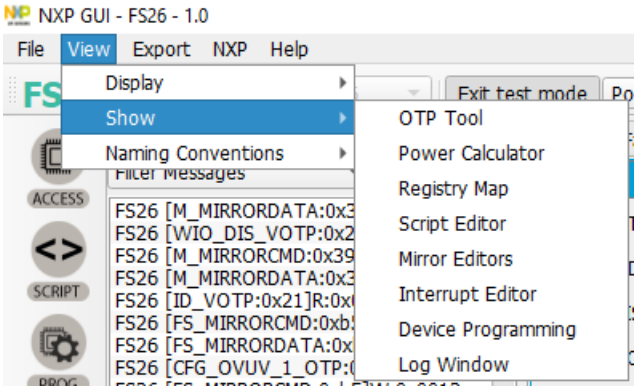

Figure 30. Show options

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- **Naming Conventions:** Select Friendly or Register name display for OTP tool. Option enabled only when OTP tool is active.

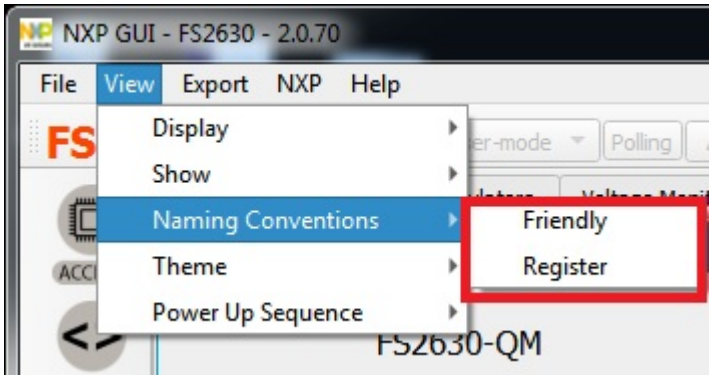

Figure 31. Naming conventions options

Friendly: Go to View >>Naming Conventions >>Friendly. This mode helps to view the registers names as user friendly names throughout the OTP Tool.

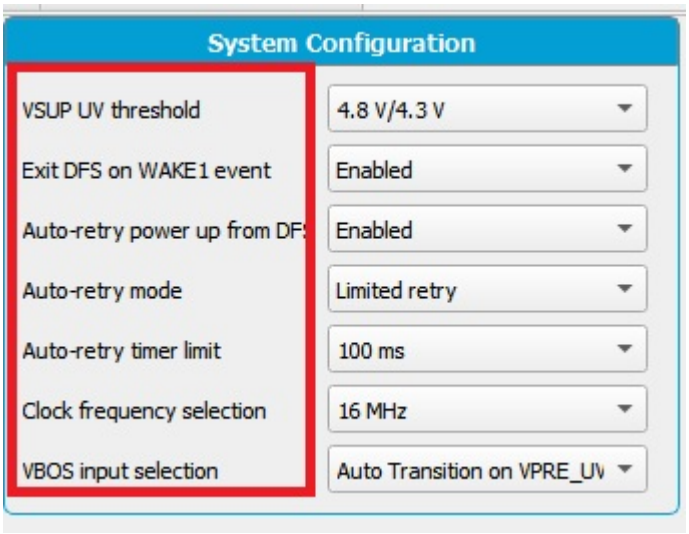

Figure 32. Friendly mode

Register: Go to View >>Naming Conventions >>Register**.** This mode helps to view the register names as Register's Technical names throughout the OTP Tool. Example: VSUP UV threshold -> VSUP_UVTH_OTP

7.1.4 Export

This option allows user to export the current OTP from the OTP tool into different script formats.

- OTP: Exports OTP configuration into OTP script file for programming.
- TBB: Exports OTP configuration into a TBB script file for emulation
- I-HEX: Exports to Intel Hex script file
- S-HEX: Exports to Simple Hex script file

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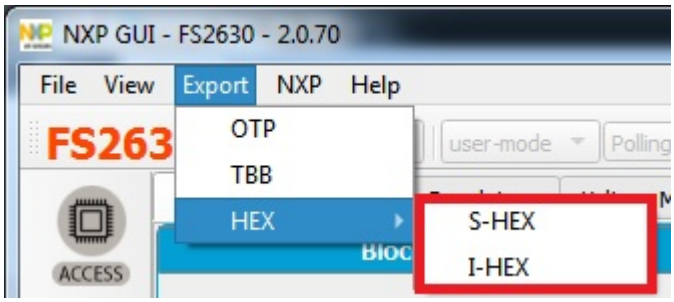


Figure 33. Export options

This option will be enabled only in OTP Tool and will remain disabled in other sections of the GUI.

7.2 Device manager

The device manager allows start/stop of communication with device as well as enter/exit of the test mode; it also allows quick access to execute useful system scripts.

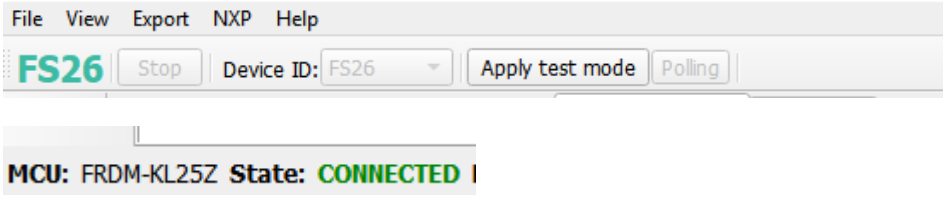
Figure 34. Device manager

7.2.1 Device connection

If USB is detected from USB and device status bar, USB status changes from **NOT DETECTED** to **DISCONNECTED.** Start button is enabled.

Click on start button to start communication with FS26 device.

When connected successfully, FS26 color changes to green and other buttons are enabled. USB status changes to **CONNECTED**.



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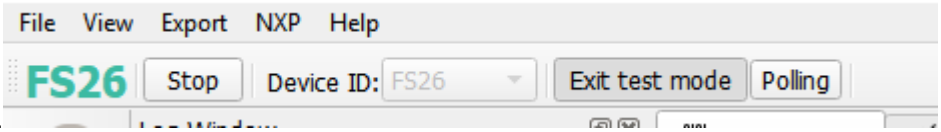
Apply test mode to send MAIN and Failsafe Test mode entry keys.
If test mode is entered correctly, button will change to “Exit test mode”.



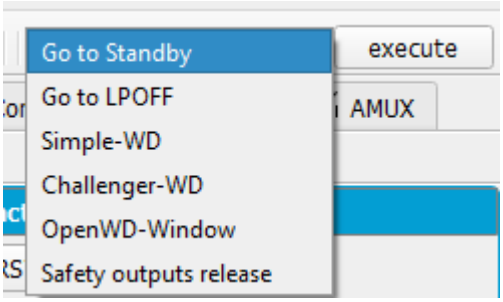
When test mode is entered, tabs requiring test mode are enabled, such as Mirrors tabs and device programming.

Click on polling to do a continuous check of test mode entry.

If the Device versioning bits are already programmed with an existing part number, the NXP GUI decodes and displays the assigned Device ID. The below example displays FS2633D.

7.2.2 Script shortcuts

To find a section with system script shortcuts, select the script and click on execute to the device. Notice that it does not warrant the entry or acknowledge of the device. Device must be in INIT FS state in most cases.



7.3 Access

7.3.1 Register map

The register access tab allows read/write to the FS26 Main and Failsafe register maps and is divided in the following sections:

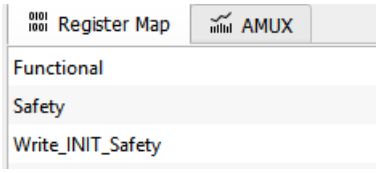


Figure 35. Register access tab

- **Functional:** MAIN functional SPI registers (Diagnostics, configuration and controls)
- **Safety:** Safety SPI registers (Diagnostics and configuration)

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- **Write_INIT_Safety**: Safety registers that can be configured during INIT FS state (ex. WD configuration, WD window).

Figure 36. Main register maps

There are three types of registers: read only (only read button), write only (only write button) or read/write (read and write buttons).

7.3.1.1 Register read only

To read the values of a register, click on **READ** button; the value is read from the device and displayed on label near **READ** button, and is displayed on the log window.

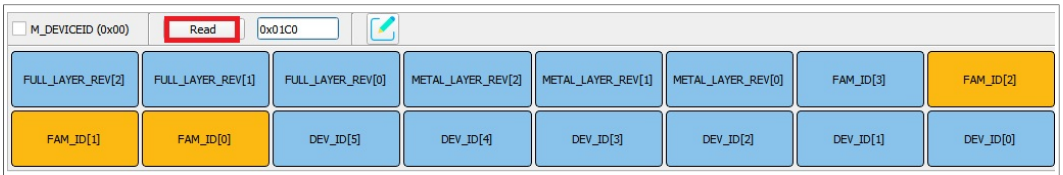

Figure 37. Read only register

To view the values of all the bits from a register after read operation, click on **Edit button.** Bits are read with their corresponding values displayed as a pop-up window.

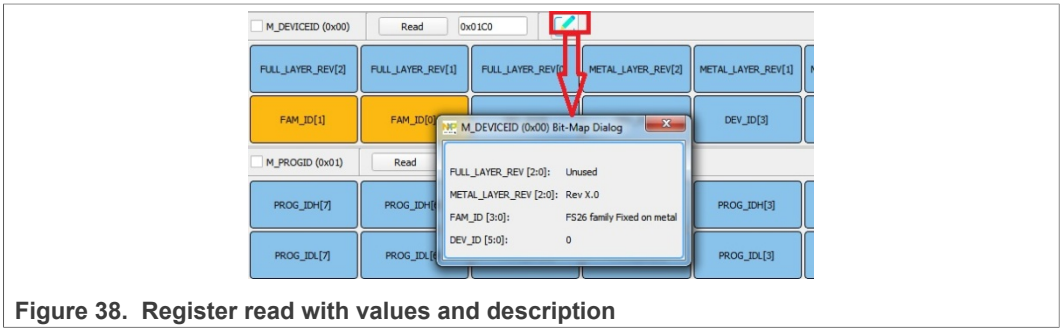

Figure 38. Register read with values and description

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7.3.1.2 Register write only

To write the bit values individually, click on the desired bit and corresponding bit button changes color. The value is updated on the log window. Click on WRITE button to write on the register.

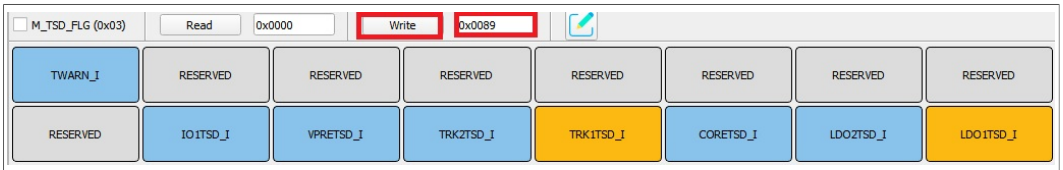

Figure 39. Write only registers

To write the values through text box near WRITE button, input the appropriate write value then click on **WRITE** button to write to the register.

Figure 40. Write only register with input data box

The value can be written as well by selecting the edit option near **WRITE** button; the bits and corresponding values are displayed as a pop window. Select the options of all write bits, close the input dialog box and select the **WRITE** button.

Selected input combinations are written to the register.

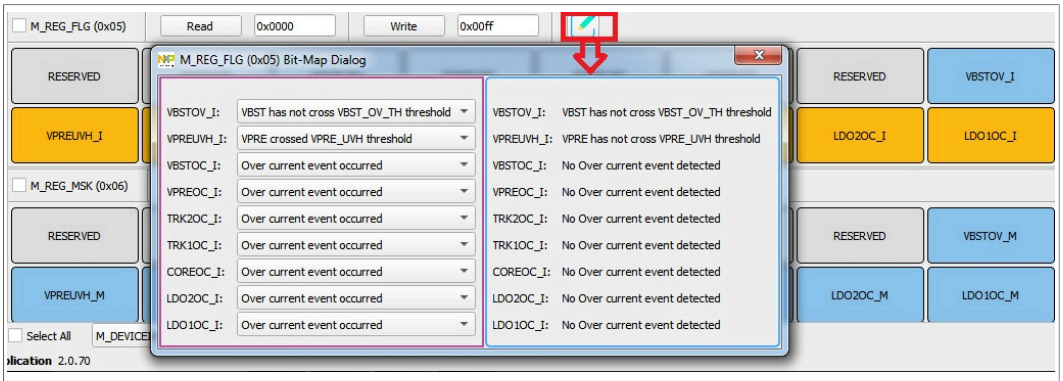

Figure 41. Dialog box write button

7.3.1.3 Register read/write

To read or write the bit values individually, click on each bit button; the value is read from the bit or written to the bit based on its properties and displayed on the log window and in the label near **READ** and textbox near **WRITE** button correspondingly. The bit button color changes accordingly.

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7.3.1.4 Global read/write

The global read/write and reset option is located at the left bottom section of the register tab.

The **SELECT ALL** option selects all the registers on the tab.

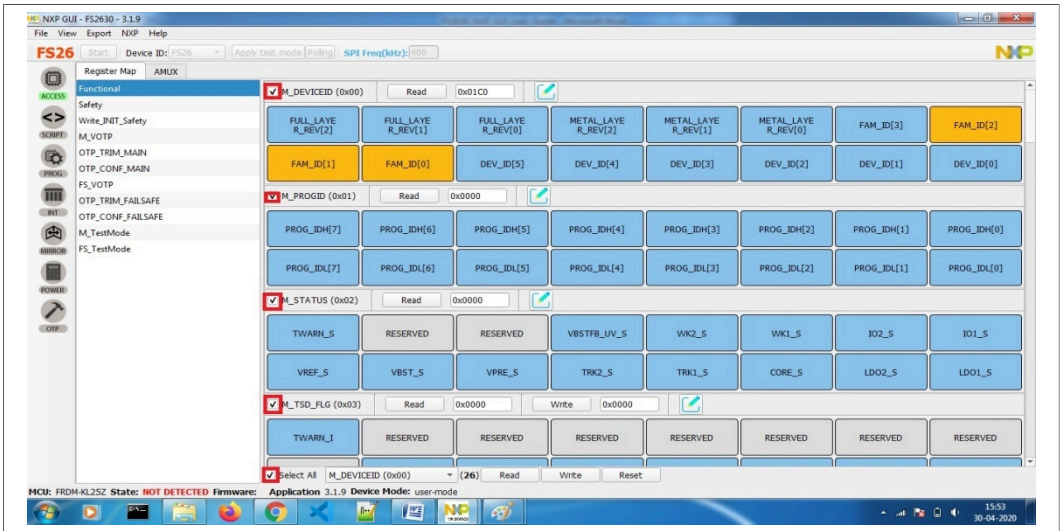

Figure 42. Global read/write

WRITE: Writes data to all selected registers at once

READ: Reads data back from the selected register at once

RESET: Resets all input textboxes to 0x00. Write bits are set to 0 and change register bit buttons to default setting.

7.3.2 INIT FS tab

Configure reaction of safety outputs for VMON, FCCU, ERRMON, and configure Fault Monitor. It is required to be in INIT FS to configure registers. Click on read all button to get current configuration, then modify it.

Click on the combo box controls to select configuration, then click on write button.

Click on Read or Read all button to get configuration; read values appear to the right of controls.

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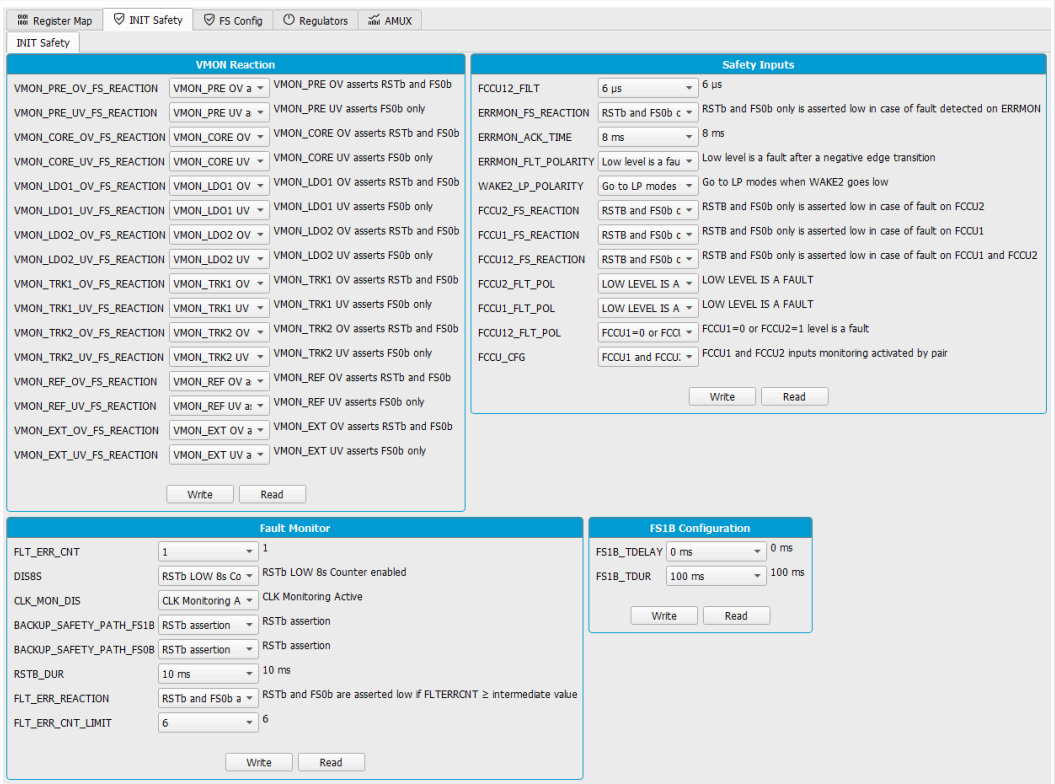

Figure 43. INIT FS tab

To get current state, click on FS_STATES display from USB and Device status bar on the bottom.

7.3.3 FS config tab

This tab helps to configure safety features such as Watchdog and fault error counter.

Click on Read all button to get current configuration.

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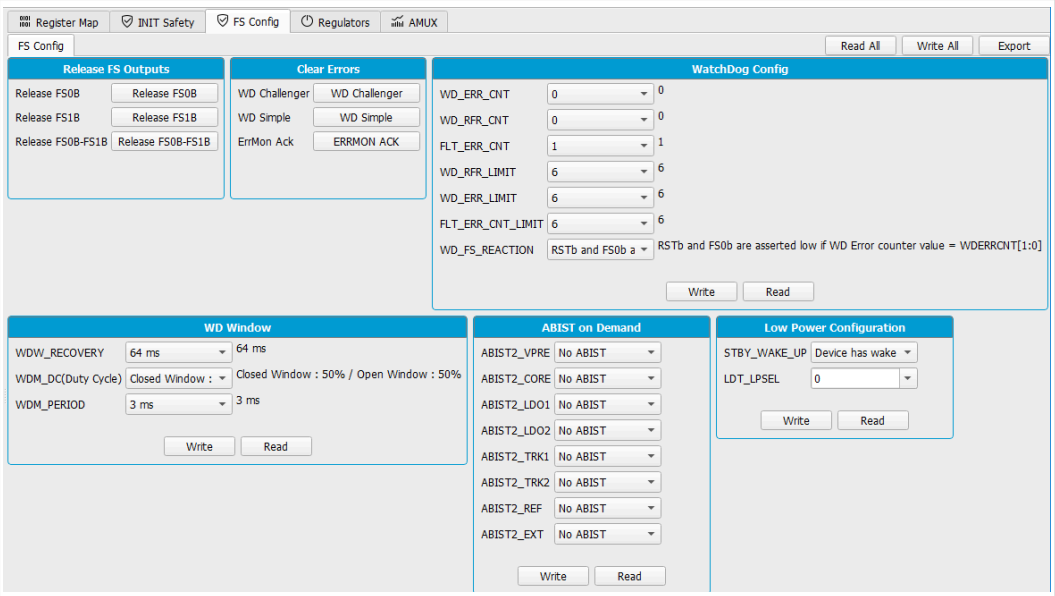

Figure 44. FS config tab

7.3.4 Regulators control

Enable or disable FS26 regulators. Check Enable or Disable box then click on write button. These registers do not provide regulator status; it writes ‘1’ to apply the command then restart to 0. Write ‘0’ has no effect. VPRE can be only enabled or disabled in test mode.

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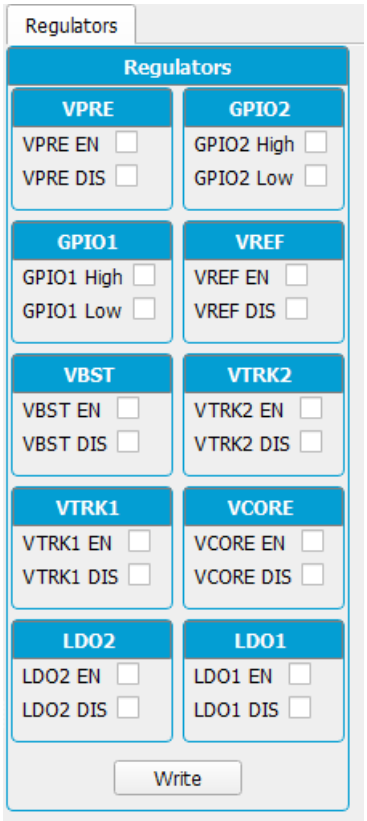

Figure 45. Regulators control

7.3.5 AMUX

This Menu can be accessed from Tool Bar >REG ACCESS or View >>Show>> Register Map >>AMUX Registers.

This tab allows selection of AMUX pin channel and gets its current value by using KL25Z AMUX ADC pin. The voltage or temperature graph can do a single read or dynamically display various channels.

The displayed values apply to the divider and temperature formulas.

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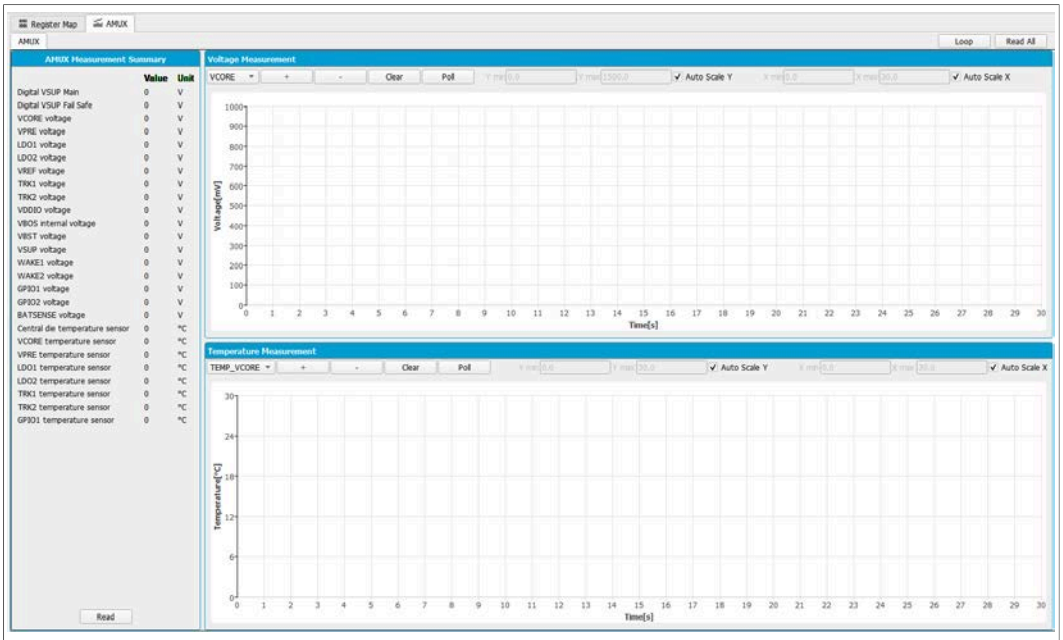

Figure 46. AMUX

To do a single read of all channels click on Read button.

To use the dynamic graph, select the channel then click on “+” button to add to the graph and then start polling with **Poll** button.

Click again on Poll button to stop measurements.

7.4 Script editor

The script editor allows you to create or send existing sequences to the device. You can read/write individually to a register, to an I/O or to an analog pin. You can emulate an OTP configuration as well with this tab.

This Menu can be accessed from Tool Bar >>SCRIPT or View >>Show>> Script Editor.

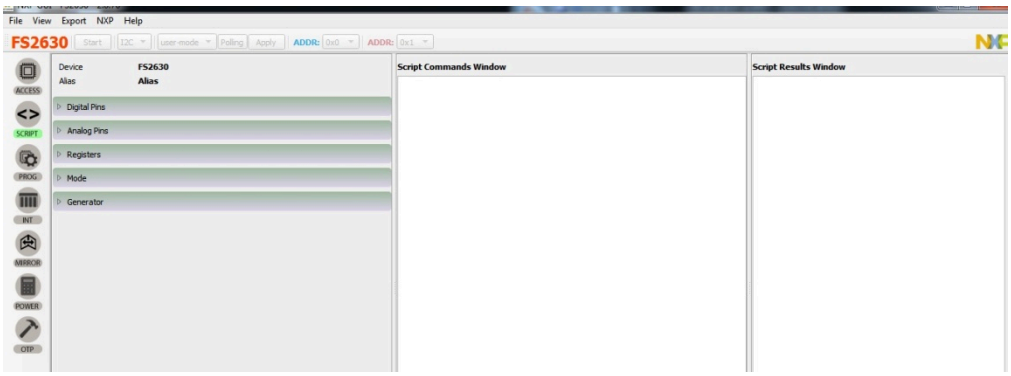

Figure 47. Script editor window

The script can be written by selecting and configuring the pins and registers that are available on the script commands section, or by loading a previously exported .txt file.

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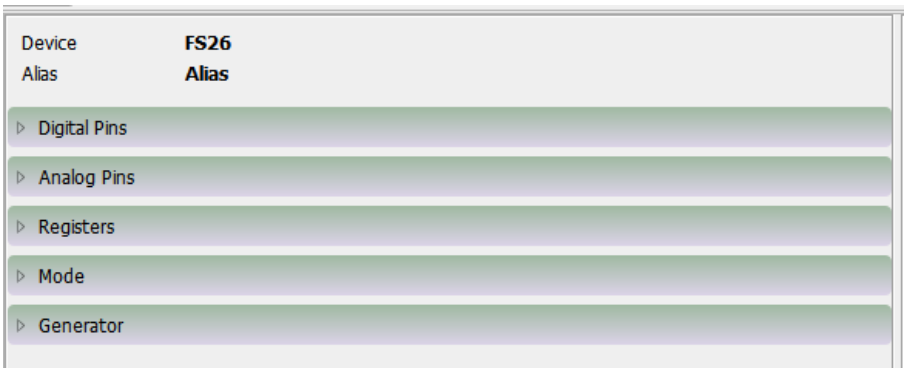
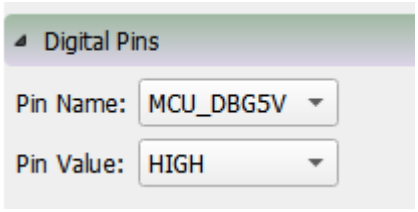
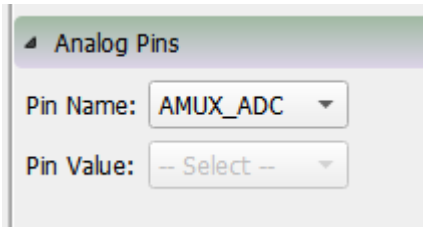


Click on one type of command to access more options, until the command to build the sequence is found.

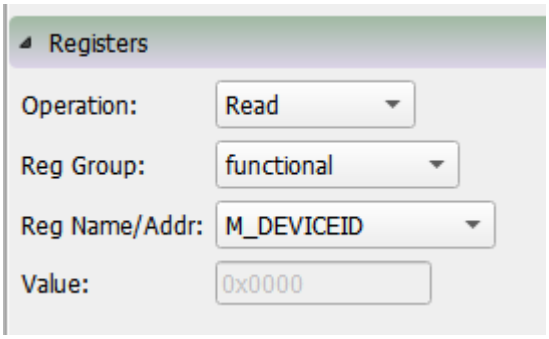
- Digital pins: Select the pin name, then pin value (High or Low). Command is automatically added to the script.



- Analog pins: Select the pin name then write the pin value. If the pin is read only, pin value will not be enabled and it will be added to script editor automatically.



- Registers: Select the Operation (Read/Write).
  - Read: Select the register group then the register name. Register is added to script editor automatically.



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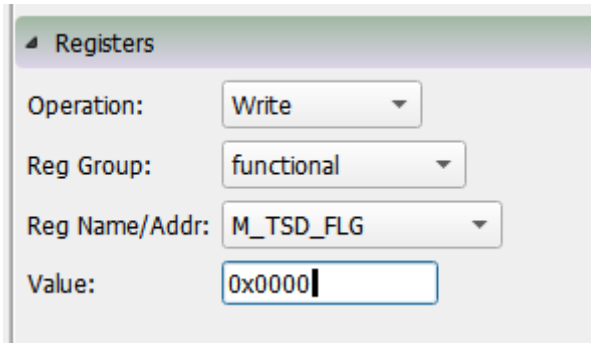
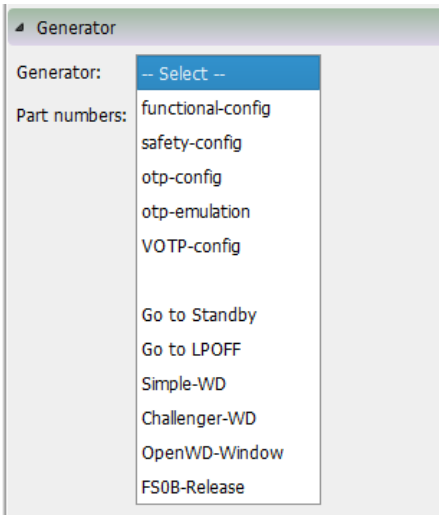
- Write: Select the register group then the register name. Write value and click on enter key. Value must be written in HEX. Push Enter key to add to the editor.



- Mode: Write command to exit or enter different device modes.
  - Test mode: Send Main and Failsafe test mode entry keys
  - User mode: Exit test mode if device is in test mode.
- Generator: Select an existing script to add to the script editor. Please consider that some options may require to be in a specific mode or state.



The script operations can be found in the bottom of the script editor window. This section is responsible for:

- Execution of script.
- Script management : Create, Open, Save, Run
- Logging feature : Load, Save, Clear

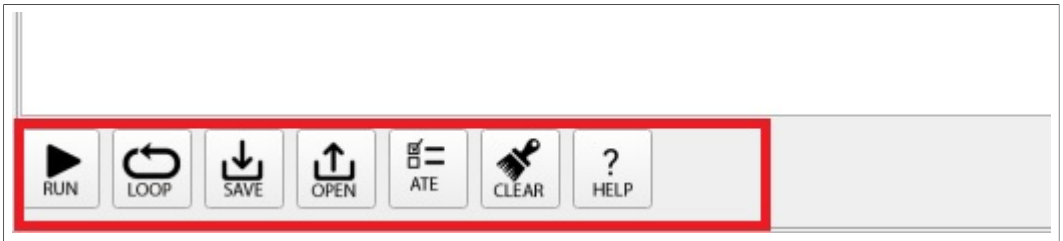


Figure 48. Script editor options

Run: Runs the script once

Loop: Runs the script continuously in loop

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Save: Saves the script that is present in the script command window in text file

Open: Opens a saved script from the desired location

ATE: Saves the script in ATE format

Clear: Clears the script command window

Script Editor Help Window: This section describes the commands available in Script editor and their formats. This Menu can be accessed from Menu >> SCRIPT >> Help or View >>**Show**>> Script Editor >> Help

7.5 OTP mirror registers

To enable this tab, test mode must be applied. This tab is divided in Main and Failsafe OTP registers.

Each bit group box can be read or written, or the whole page can be read. OTP configuration can be imported or exported from this tab.

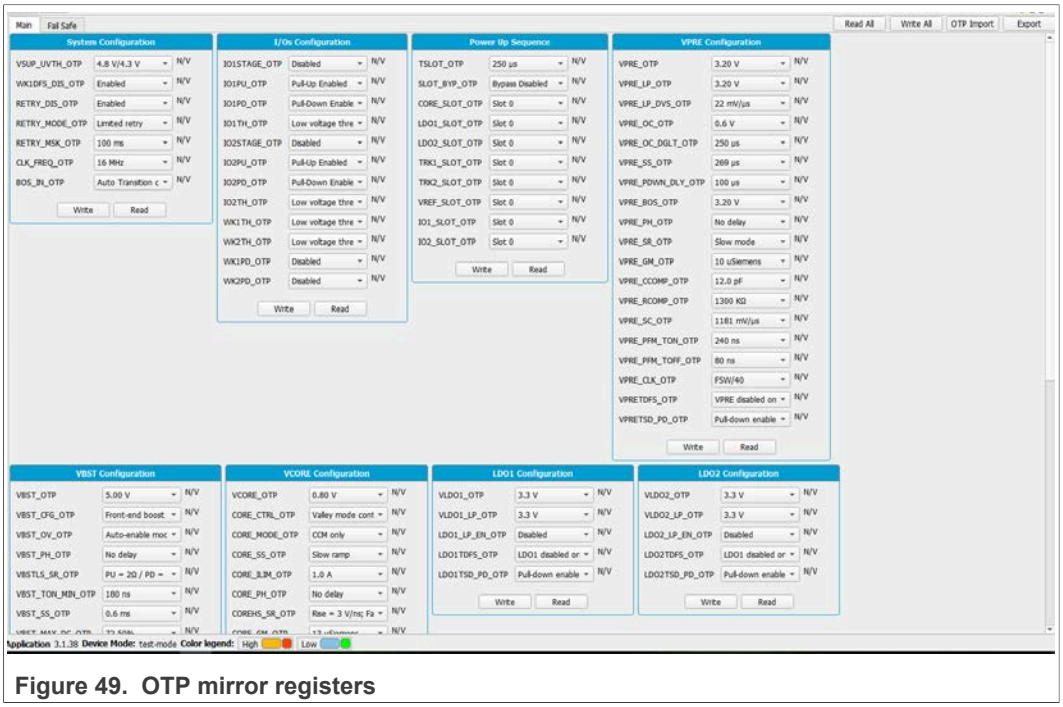

Figure 49. OTP mirror registers

7.5.1 Read/write operation

To read a bit group, click on the read button from a box. Read values are displayed to the right of each register.

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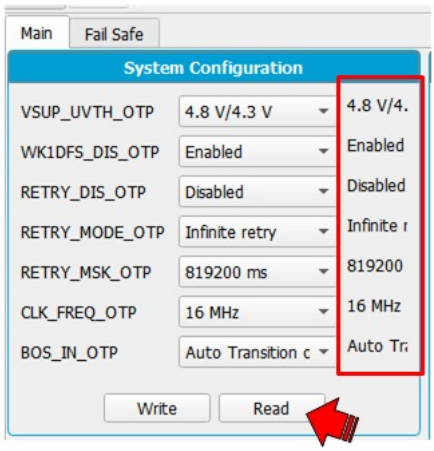

Figure 50. Read bit group

To write to a bit group, modify the controls of each register, then click on write button.

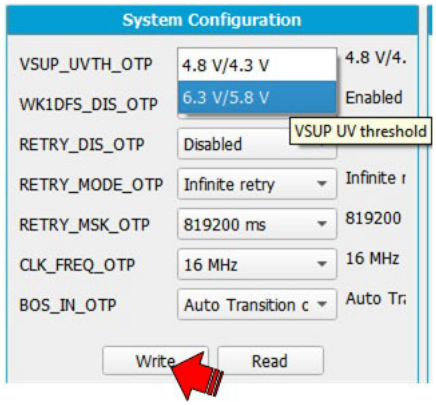

Figure 51. Write bit group

7.5.2 Read/write all and write all operation

Read all will read all the bits of each block from all mirror registers.

Read values will appear at the right of each register as well on the window log.

Figure 52. Read all

To write all OTP bit groups configuration click on Write all button.

7.5.3 Mirror registers export option

This operation generates and saves as text file in local device which can be imported later into this tab. Figure 53 shows the generate .txt configuration file.

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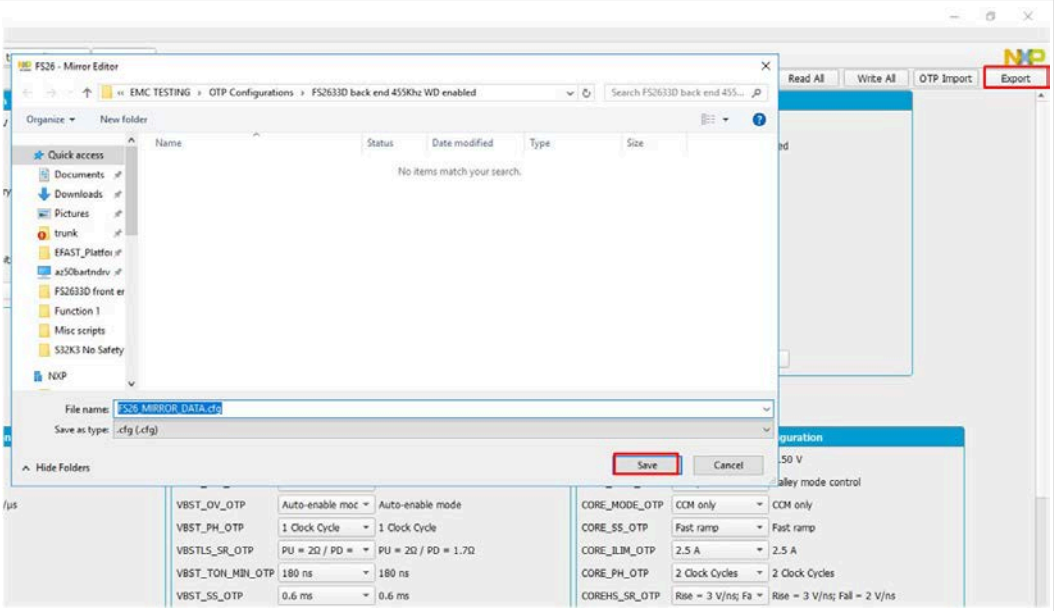

Figure 53. Export Option for reference

7.5.4 OTP import to mirror registers

This option is used to import the configuration file previously saved. Click on OTP import button and select the the.txt configuration file previously saved from this tab.

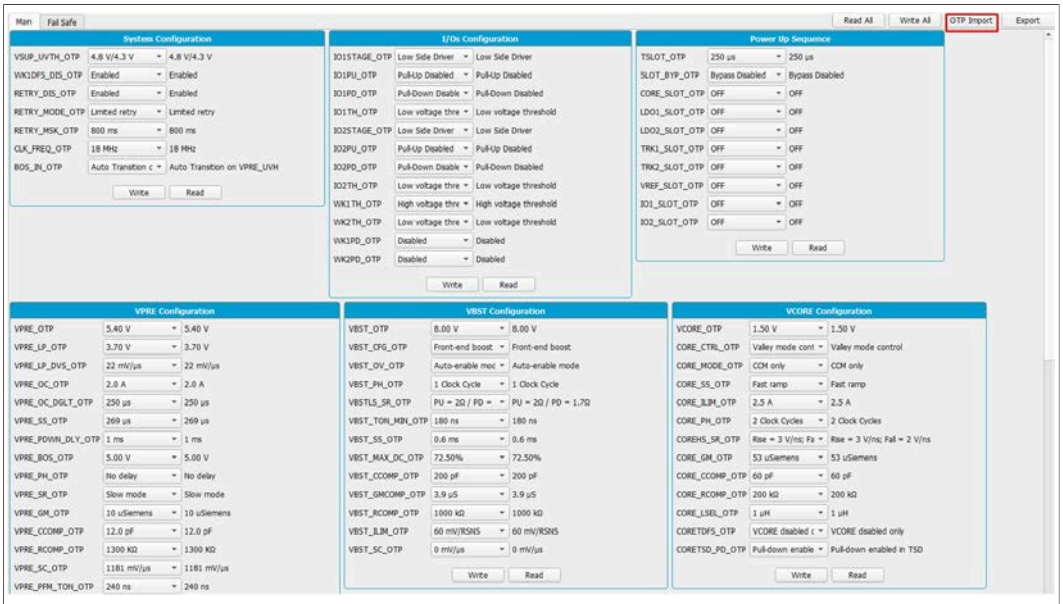

Figure 54. OTP Import for reference

7.6 Device programming

This section is used to burn permanently an OTP configuration on the OTP fuses. To enable this window device must be in test mode.

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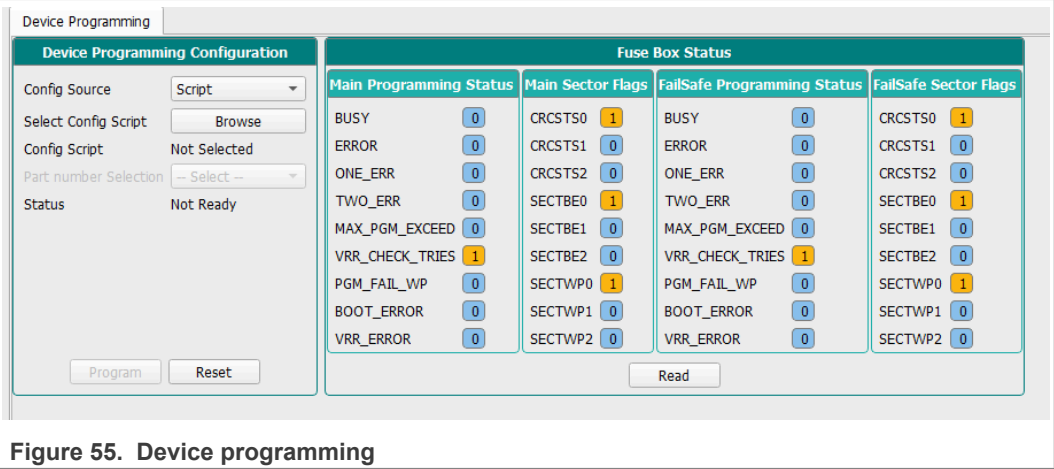

Figure 55. Device programming

To program an OTP configuration Vdebug pin must be higher than VDBG65TH. To apply this voltage, turn on SW7 (Apply 8 V to Vdebug).

Click on Browse to select an OTP script file, then click on program button to run the script. If Vdebug not set to 8 V a pop-up appears asking to turn on SW7, or it turns on automatically if jumper J13 is on Automatic mode J13 3-2.

If the required conditions are met (sectors available), the programming starts. Otherwise the execution is cancelled. To verify sectors are available click on read button from Fuse Box Status.

OTP is programmed into SECTBE2 of Main and Failsafe. SECTBE1 and SECTBE0 are reserved for NXP users only.

Blue or ‘0’: Available

Yellow or ‘1’: Not available

When programming is complete, a pop-up appears to request to turn off SW7 and SW6 (Put Vdebug to 0 V).

If the device was programmed correctly the power-up sequence starts. Fuse box status can be read to verify if sectors are burned. In some conditions a power up could be required.

7.7 INT tab

This tab allows access to monitor the regulators and safety events. To access the Interrupt Editor window, Menu >> INT **OR** View >>Show>> Interrupt Editor

It is separated in two tabs: interrupt tab and safety diagnostic tab.

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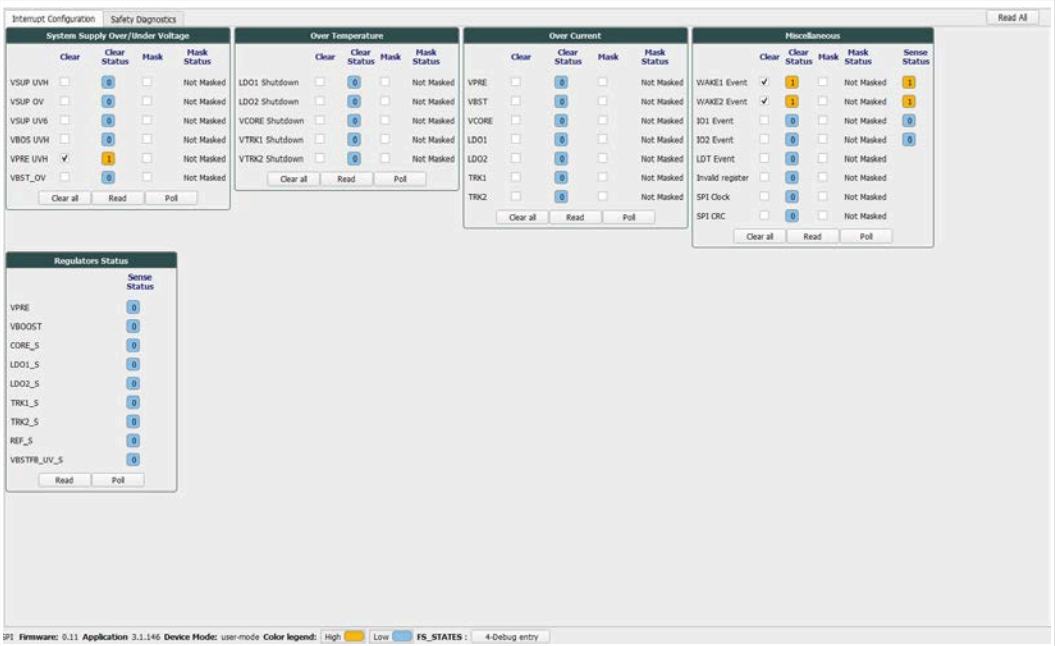

Figure 56. Interrupt Configuration tab

The below legend and functions apply to both tabs:

- **Blue** means Low or not activated.
- **Yellow** means High or activated.
- To **clear** flags, click on each check box from clear column or click on clear all button.
- To **mask** the interruption, check the box of each interruption from mask column.
- Click on **Read** button of each box to read the current status or on **Read all** button to update the whole tab.
- Use **Poll** button to read each box periodically.

Sense status can be read only.

7.7.1 Interruptions

This tab allows the user to monitor the regulators, Wake inputs, I/O and communication events or status. It allows read, write and poll over/under voltage, over temperature and over current of device. You can read, clear or mask an interruption.

If an event occurs flag changes to red. When regulators are red or ‘1’ they are turned ON.

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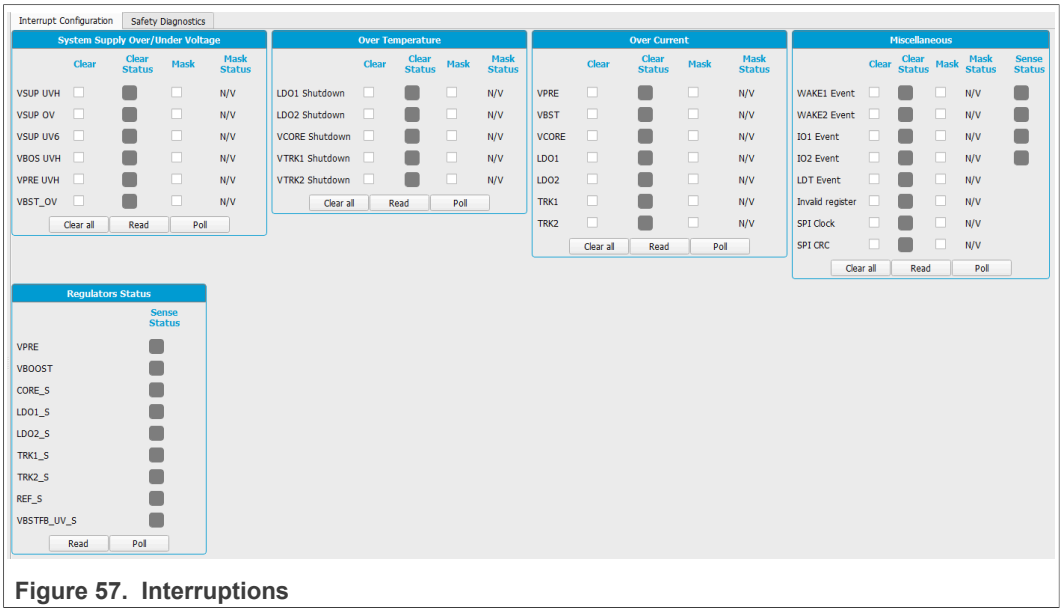

Figure 57. Interruptions

7.7.2 Safety diagnostics

Safety diagnostics tab allows the monitoring of safety events such as VMON status, bad WD, SPI communication errors, FCCU pins, safety outputs, ABIST1 and ABIST2 status.

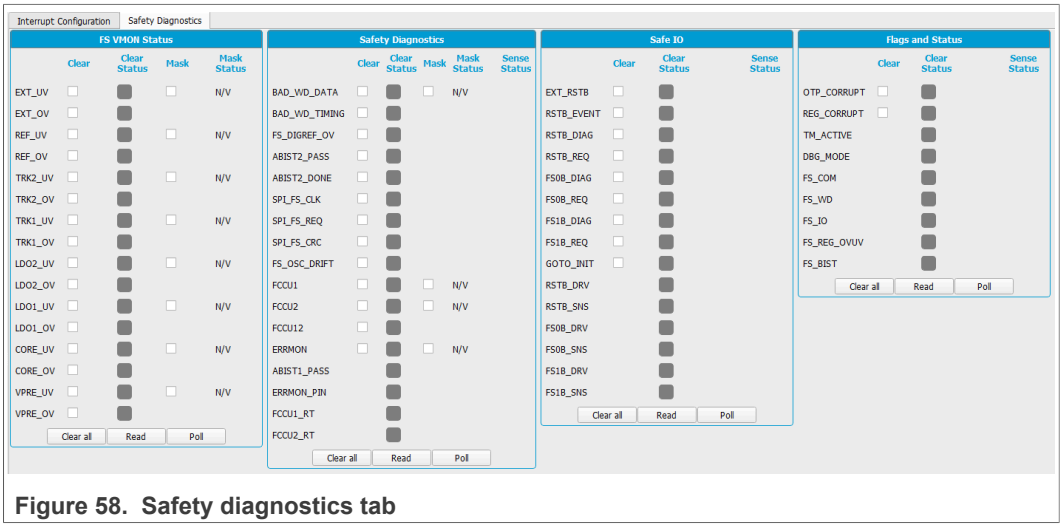

Figure 58. Safety diagnostics tab

ABIST1_PASS Yellow means that it is done and PASS, since we can read ‘1’ from its register. 0 or blue after execution means fail.

7.8 OTP tool

This tool allows user to configure OTP registers, to save configurations and to generate scripts in different file formats which can be burnt (OTP script) or emulated (TBB script) into the FS26 SBC.

To access the FS26 OTP tool, launch NXP GUI Application and Navigate to the **OTP** Tool **OR** Access OTP Tool from Menu: View >> Show/Hide >>OTP Tool

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It is possible to save a configuration to visualize or to modify it later. Click on save config to export or File then Save. To import Click on Import button or from File then Load.

7.8.1 OTP tool application menu

All blocks in the OTP tool have default values configured on launch. It consists of the following configuration sections:

- System configuration
- Switching regulators
- Regulators
- Voltage monitoring
- System safety configuration

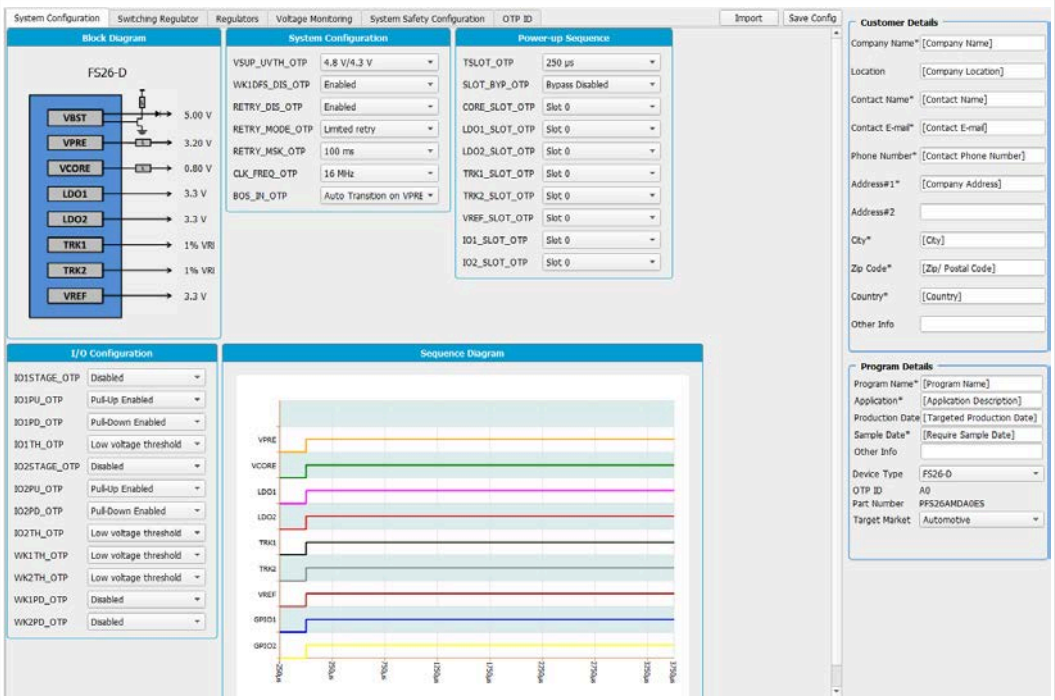

Figure 59. OTP tool configuration tabs for FS26

7.8.2 OTP configuration sections

7.8.2.1 System config

This block consists of the parameter (bits) settings that are related to the System configuration registers of FS26. It displays block diagram with the selected regulators output values from Regulators section. It contains the Power up sequence configuration which is displayed in the sequence diagram. You can configure the I/O and Wake inputs as well.

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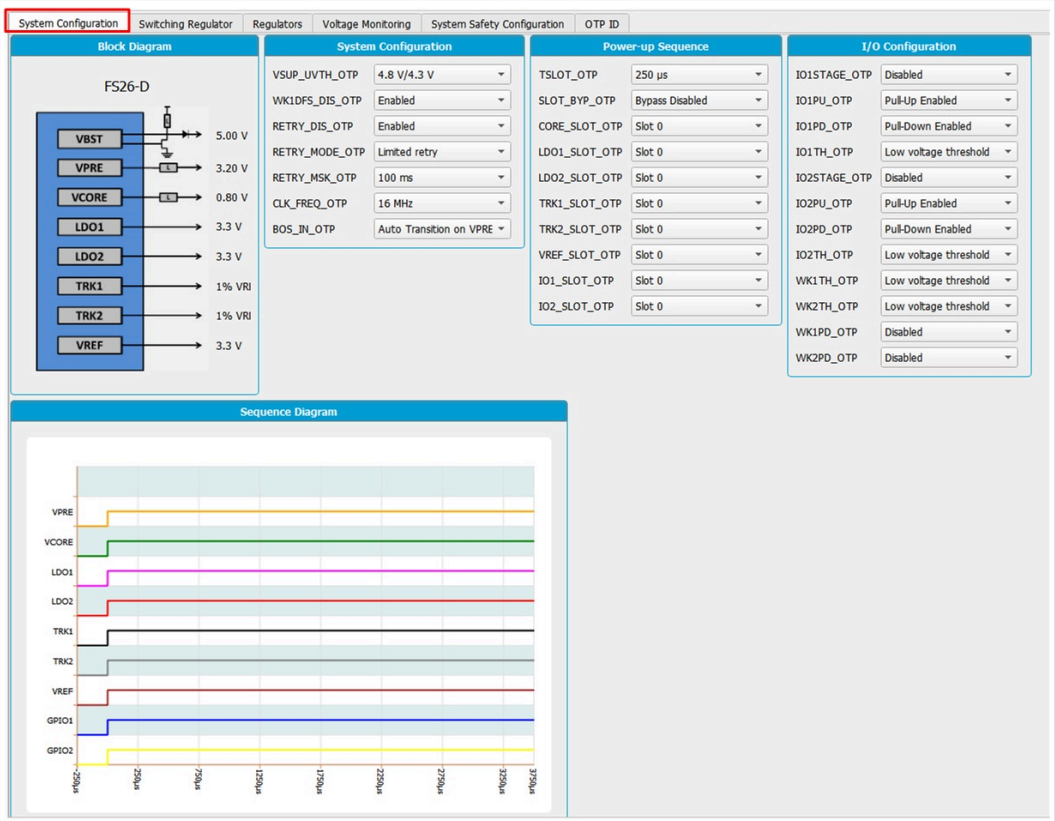

Figure 60. System configuration tab

7.8.2.2 Regulators

The FS26 regulators are separated in two tabs, Switching regulator and Regulators (LDOs).

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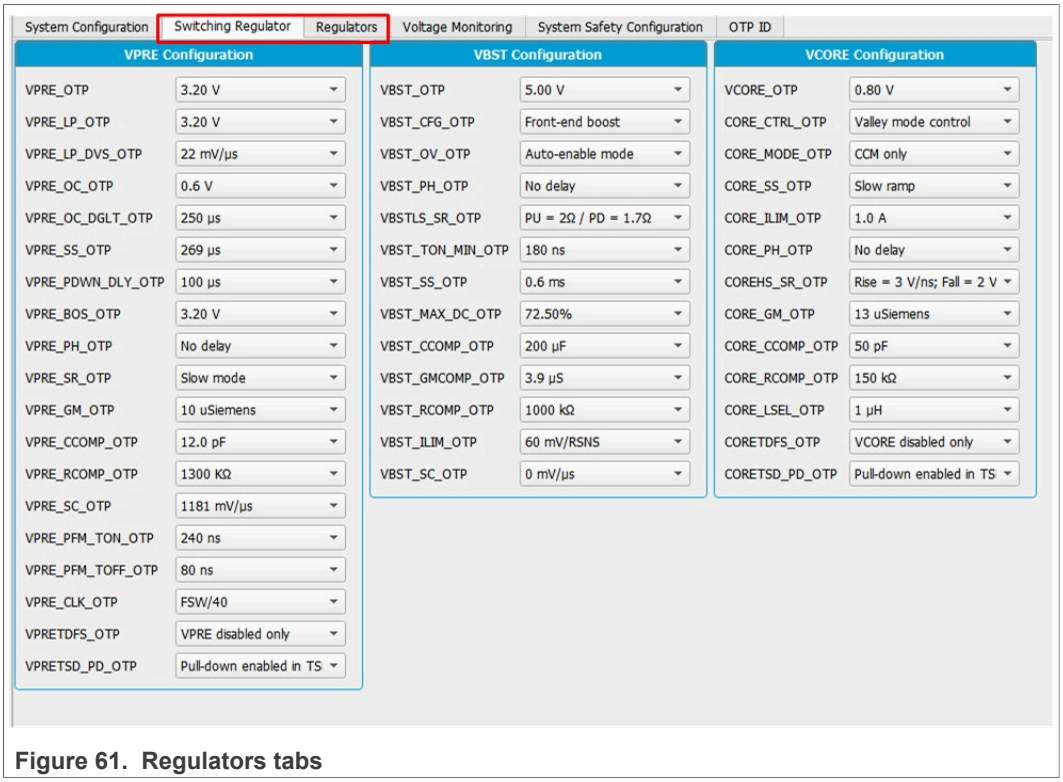
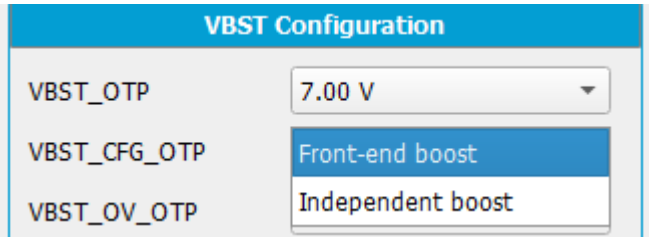


Figure 61. Regulators tabs

In the switching regulators you can configure VPRE, VBST and VCORE output values and its internal parameters. You can select the Power topology by configuring the VBST_CFG_OTP bit group.



In the Regulators tab, you will find: VLDO1, VLDO2, VTRK1, VTRK2, VREF output values and its TSD behavior.

7.8.2.3 System safety configuration

This tab allows user to configure ABIST1 for each regulator, configure system reaction in case of Fault or enable and disable Watchdog timer.

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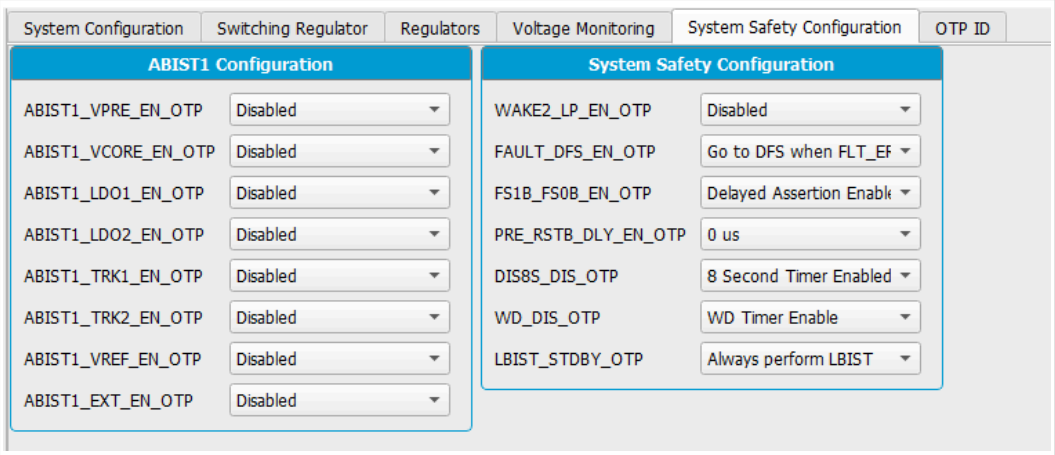

Figure 62. System safety configuration

7.8.2.4 Voltage monitoring

This tab allows user to configure FS26 voltage monitoring and consists of the following:

- VMONPRE Configuration
- VMONLDO1 Configuration
- VMONCORE Configuration
- VMONLDO2 Configuration
- VMONEXT Configuration
- VMONREF Configuration

Make sure that each VMON is assigned with the same voltage output value configured on regulators tab, then select its fault OV/UV threshold and filtering time.

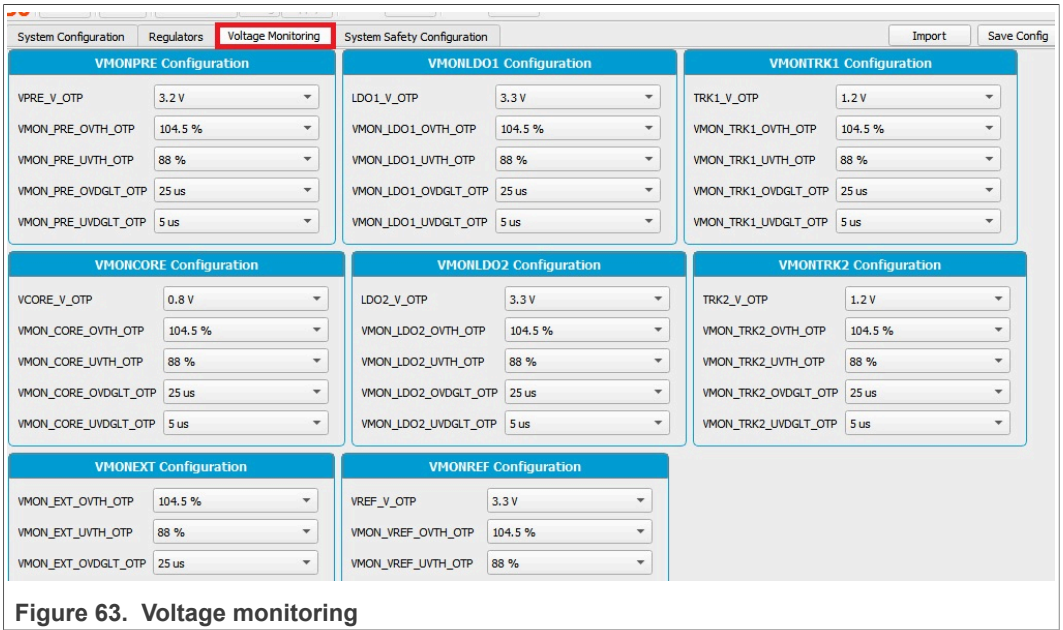

Figure 63. Voltage monitoring

7.8.2.5 OTP ID

Displays OTP ID. Only NXP users can create a new OTP ID.

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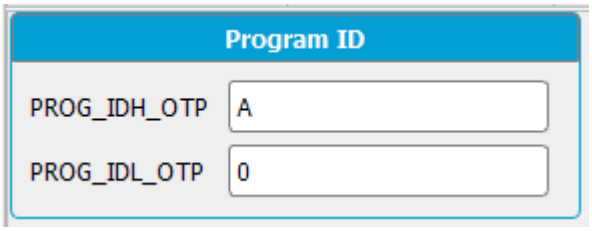

7.9 I/O pins tab

This section can control some I/Os connected to the KL26Z plugged freedom. It can read the device safety outputs externally or to control different voltage sources in order to apply sequences to apply debug mode without moving any switches.

The input pins are the pins that can be read from the MCU, they are input pins from MCU point of view. This section contains the safety outputs FS0B, FS1B and RSTB. You can read it once with Read button. Or you can select at which frequency you want to the read the pins, select the duration then start polling with Poll button.

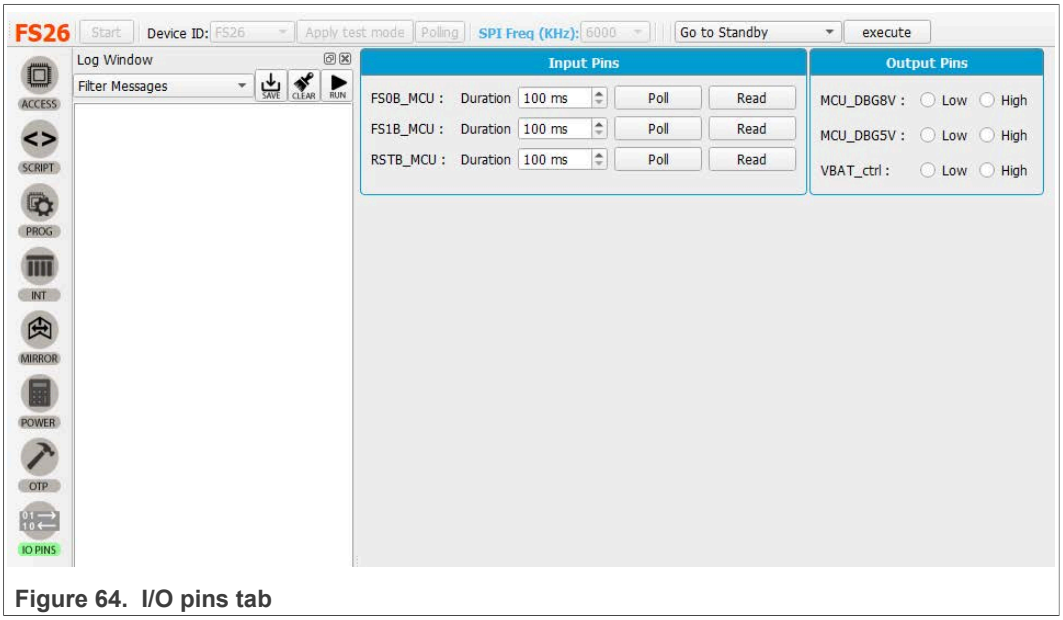

Figure 64. I/O pins tab

The output pins are thresholds that can be controlled with MCU. These pins are described in Section 4.2.10 "VDebug pin voltage control".

- VBAT_Ctrl: Open or close VBAT power supply
- MCU_DBG5V: 5 V on VDebug pin
- MCU_DBG8V: 8 V on VDebug pin

They can be used instead of the Manual switches SW6 and SW7. In order to use MCU_DBG5V and MCU_DBG8V for debug pin control, J13 must be on ‘’Auto mode’’ J13 position 3-2. Select high or low to control the pins, default is low.

To use VBAT_Ctrl the red jumper JP1 next to the VBAT switch must be OFF. Once you remove JP1 you can start using VBAT_Ctrl instead of SW1 to turn on or off power supply.

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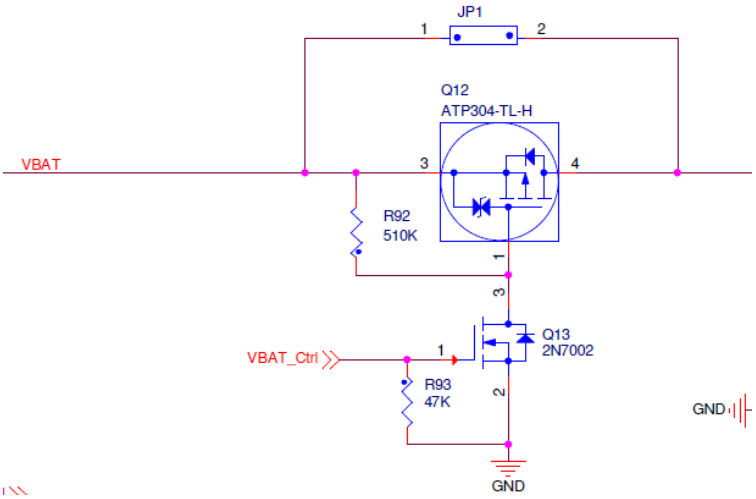

These pins are also accessible from script editor; you could use those pins to create script sequences.

8 Using FS26 NXP GUI

Once you have installed the NXP GUI (Section 5.2 "Installing GUI software package") you can follow these instructions for a quick power up, debug, programming or enter the different operating modes of the FS26 SBC.

8.1 Power up

If your FS26 device already contains an OTP configuration, you only need to connect a power supply to the VBAT Phoenix connector or the VBAT jack connector. See Section 4.2.2 "VBAT connectors".

It is recommended to set your power supply to an initial value of 12 V and current limited to 1 A.

Make sure your board has the right jumper configuration. Every KIT is delivered with a default jumper configuration as in Section 4.3 "Default jumper configuration". This configuration is enabled for a boost in front end topology. For back end see Section 4.2.3 "Power topology configuration".

Verify the KL25Z freedom is plugged, as well as the USB cable on KL25Z USB connector side. It is important that the USB cable is connected since in addition to enabling the communication with the NXP GUI, it provides voltages and references to some circuits on board as well as generates the VDDIO reference for the IC.

Since all the previous statements are valid or considered, you may use the switch SW1 to power on your board.

If your OTP configuration has many safety features enabled, your device may restart or turn off after a few seconds. Enter debug mode to waive some of those features.

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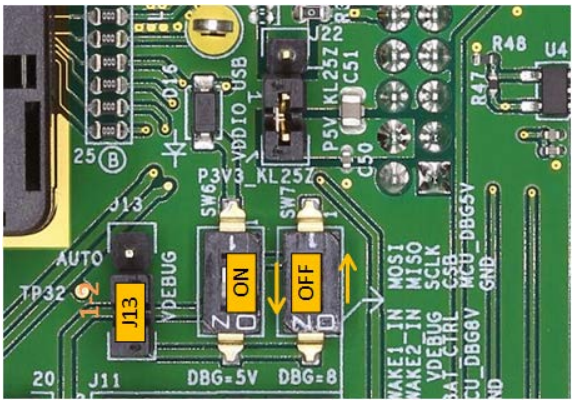
8.2 Debug mode entry

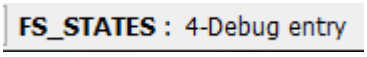
To modify any parameters or to communicate with the IC, you may enter the debug mode. To enter debug mode, you should consider the power and connection statements from Section 8.1 "Power up".

Once your KIT is ready, follow the next steps:

1. Make sure the device is powered off (SW1 middle position).
2. Turn ON SW6 to apply 5 V to the VDebug pin. Make sure the jumper of J13 has the right configuration; default is Manual. See Section 4.2.10 "VDebug pin voltage control" for more details.



3. Power on VBAT, and the device will enter debug mode. This allows access to the register map, to emulate, or to program an OTP configuration on the NXP GUI.
4. To verify you are in debug mode, you can use NXP GUI Register map window to Read FS_STATES (0x17) or you can click on FS_STATES display from USB and Device status bar.



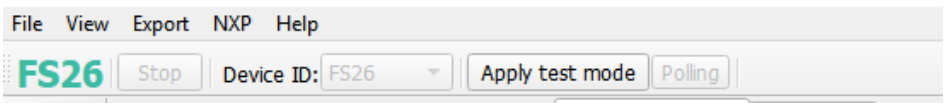
It is possible to start power up sequence and stay in debug mode. In order to start power up sequence, turn SW6 off to put VDebug pin to 0 V.

8.3 Test mode entry

To enter the test mode, the chip needs to be in the Debug mode. Then test mode can be accessed by writing the appropriate key sequences.

You can access test mode from NXP GUI device manager or write the keys to the script editor

From Device Manager: Click on “Apply test mode” button to send the Main and Failsafe test mode entry keys.



From Script Editor:

Copy and paste the keys in the script editor:

// Main Test mode entry

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SET_REG:FS26:M_TestMode:M_TM_ENTRY:0x0000

SET_REG:FS26:M_TestMode:M_TM_ENTRY:0xD5A7

SET_REG:FS26:M_TestMode:M_TM_ENTRY:0xB8EE

SET_REG:FS26:M_TestMode:M_TM_ENTRY:0x0F37

//Fail Safe Test mode entry

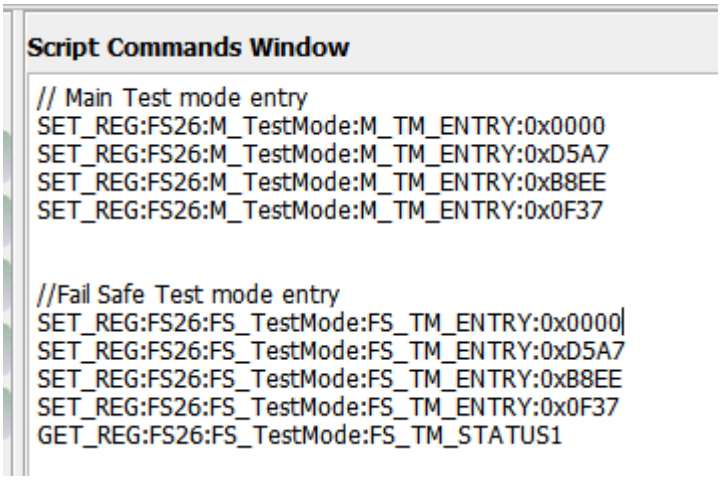
SET_REG:FS26:FS_TestMode:FS_TM_ENTRY:0x0000

SET_REG:FS26:FS_TestMode:FS_TM_ENTRY:0xD5A7

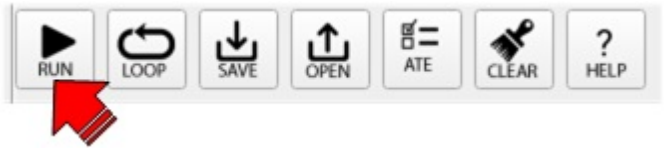
SET_REG:FS26:FS_TestMode:FS_TM_ENTRY:0xB8EE

SET_REG:FS26:FS_TestMode:FS_TM_ENTRY:0x0F37

GET_REG:FS26:FS_TestMode:FS_TM_STATUS1



Then click on Run Script.



8.4 Emulate an OTP configuration

Before starting, make sure that the power conditions from Section 8.1 "Power up" are valid.

If you're not in debug mode:

1. Make sure the device is Powered off (SW1 middle position).

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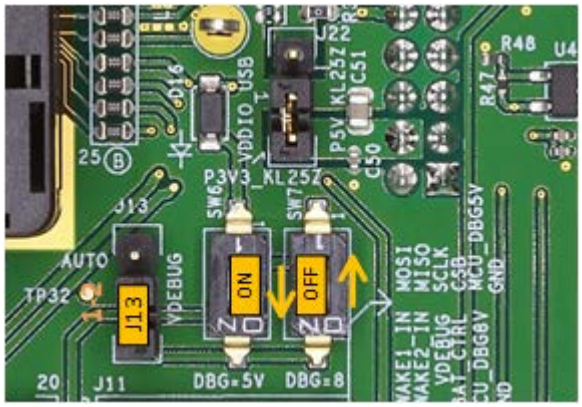
2. Then turn ON SW6 to apply ~4.5 V to the VDebug pin. Make sure jumper J13 has the right configuration, default is Manual. See Section 4.2.2 "VBAT connectors" for more details.



3. Power on VBAT(SW1), and the device will be in debug mode.

If already in debug entry:

1. Open the NXP GUI, connect the device, and open the script editor.
2. Load a provided or created OTP configuration script (TBB) to load into the mirror registers.

3. Then click on the Run Script button.

A TBB script typically contains Test mode entry keys, if it doesn't have it. See Section 8.3 "Test mode entry" to enter Test mode.

After running the script, you can read the mirror registers to verify the loaded OTP configuration in the OTP Mirrors tab. Turn the VDebug (SW6) switch to 0 V to start the power up sequence.

8.5 Program an OTP configuration

This section is intended to burn an OTP configuration permanently into the fuses. You can program device sectors only one time. Make sure sectors are available.

You can program an OTP configuration from Device Programming tab. See Section 7.6 "Device programming" OR from the script editor.

1. If not in debug mode, see Section 8.2 "Debug mode entry".

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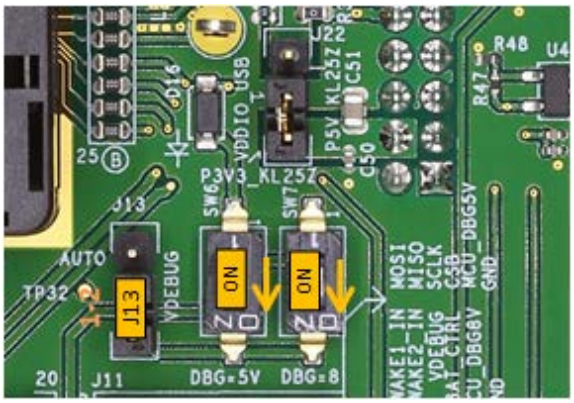
2. Turn on the SW7 to apply ~8 V to the VDebug pin in order to reach the OTP burning threshold VDBG65TH. If this voltage is turn on, a blue LED will turn on (D19).



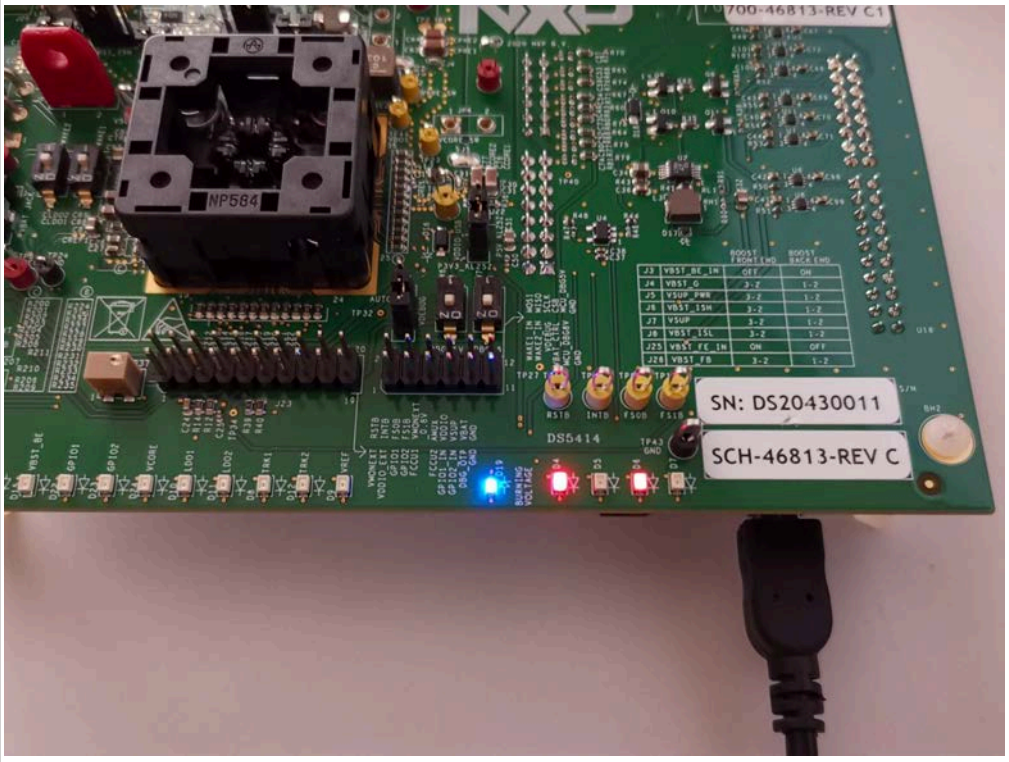


Figure 65. Burning voltage LED indicator (D19)

3. Open the NXP GUI, connect the device, and go to the script editor.
4. Load a provided or created OTP configuration script to load on the mirror registers. Then click on Run button to run the script.

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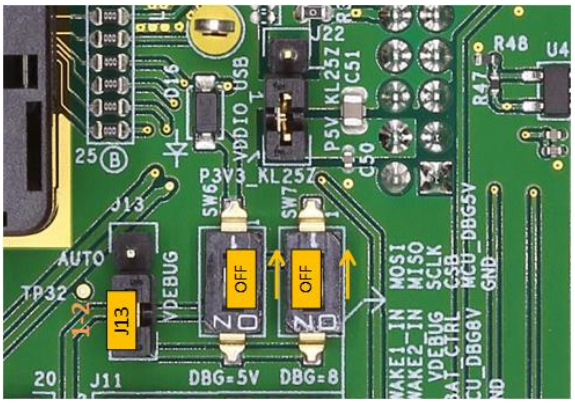
5. Once the script has been sent, turn off SW7 then SW6.



6. Device should power up with the burned OTP configuration or perform a POR on VBAT to verify the fused OTP configuration.

8.6 Go to INIT FS in debug mode

From Power up:

1. Put Debug pin to 5 V (SW6 On) to access debug entry.
2. Device Power up (SW1)
3. If the device does not have an OTP configuration Emulate or program an OTP configuration. See Section 8.4 "Emulate an OTP configuration" for Emulation or Section 8.5 "Program an OTP configuration" for programming.
4. Put off SW6 to continue the state machine and access INIT FS. You can verify current state from USB and device status bar; click on display to refresh.

FS_STATES : 9-INIT_FS

8.7 Go to Normal mode

To enter Normal mode from GUI, you must be in debug mode and in INIT FS state. If simple Watchdog, you can use a script to release safety outputs FS0B and FS1B. If Watchdog challenger, sequence must be sent manually.

1. Once in INIT FS, verify ABIST1 is pass from Safety diagnostics tab
2. Configure or verify Watchdog type from Mirrors tab.
3. Use a script to release safety outputs; use script A for watchdog simple or script B for watchdog challenger. Script to release safety outputs is available in device manager

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scripts section, orr from script editor > Generator > Safety outputs release script and run.

a. **Sequence to enter normal mode with a Watchdog simple:**

```
//INIT FS and simple WD enabled required
//Open WD window
SET_REG:FS26:Safety:FS_WDW_DURATION:0x008B
SET_REG:FS26:Safety:FS_NOT_WDW_DURATION:0xF144
//Send 1 good wd refresh to close INIT window
SET_REG:FS26:Safety:FS_WD_ANSWER:0x5AB2
//clean fault error counter
SET_REG:FS26:Safety:FS_WD_ANSWER:0x5AB2
SET_REG:FS26:Safety:FS_WD_ANSWER:0x5AB2
SET_REG:FS26:Safety:FS_WD_ANSWER:0x5AB2
SET_REG:FS26:Safety:FS_WD_ANSWER:0x5AB2
SET_REG:FS26:Safety:FS_WD_ANSWER:0x5AB2
SET_REG:FS26:Safety:FS_WD_ANSWER:0x5AB2
//Exit dbg mode
SET_REG:FS26:Safety:FS_STATES:0x4000
//release FS0B and FS1B
SET_REG:FS26:Safety:FS_RELEASE_FS0B_FS1B:0xB2A5
```

b. **Sequence to enter normal mode with a Watchdog Challenger:**

```
//INIT FS and WD Challenger required
//Open WD window
SET_REG:FS26:Safety:FS_WDW_DURATION:0x008B
SET_REG:FS26:Safety:FS_NOT_WDW_DURATION:0xF144
//Send 1 ZD refresh to close INIT window
SET_REG:FS26:Safety:FS_WD_ANSWER:0xa54d
//clean fault error counter
SET_REG:FS26:Safety:FS_WD_ANSWER:0x4a9a
SET_REG:FS26:Safety:FS_WD_ANSWER:0x9535
SET_REG:FS26:Safety:FS_WD_ANSWER:0x2a6a
SET_REG:FS26:Safety:FS_WD_ANSWER:0x54d4
SET_REG:FS26:Safety:FS_WD_ANSWER:0xa9a9
SET_REG:FS26:Safety:FS_WD_ANSWER:0x5353
//Exit dbg mode
SET_REG:FS26:Safety:FS_STATES:0x4000
//release FS0B and FS1B
SET_REG:FS26:Safety:FS_RELEASE_FS0B_FS1B:0xA565
```

Release safety outputs without script

To release safety outputs step by step, continue with these instructions:

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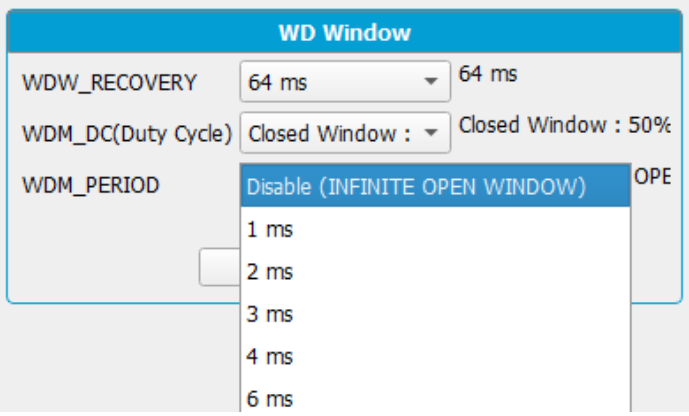
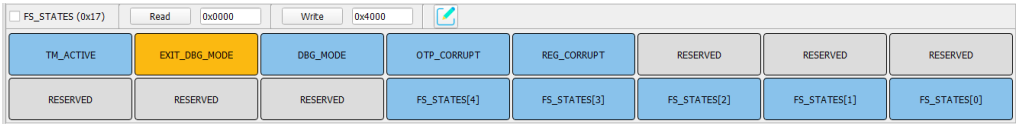
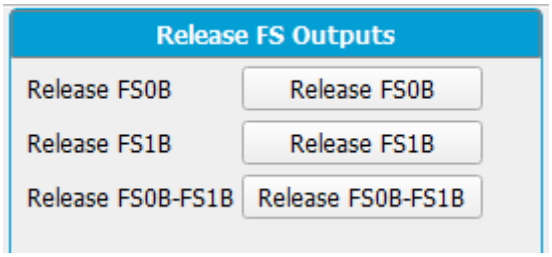
1. Configure WD window. Since it is not possible to send a WD refresh periodically, open WD Window. From FS config tab, go to WD window box, select INFINITE window and click on write button.



   Or from device manager select Open WD Window script and click on execute.
2. Send one good WD refresh to move on the state machine. From FS Config tab, click on WD challenger or WD simple one time.
   Or execute it from script editor or device manager.
3. Send the number selected good WD refresh to clean the Fault error counter. Example: Default number is 6. Click 6 times on WD Challenger or WD simple buttons. You can verify the Fault error count is now 0 (FLT_ERR_CNT) in FS config tab.
4. Exit debug mode. Write 1 to exit debug mode bit in FS_STATES. Go to register map, then to safety tab.



5. Send “FS0b release” or “FS0b and FS1b release” command to move to normal mode. You can find these buttons in FS config tab.



6. After these steps, device should move to Normal mode. To verify current state, click on FS states display from USB and Device status bar.

8.8 Low power modes

Once in INIT FS or Normal mode, select a way to exit the low power modes. Write 1 to the event or events that can wake the product from the low power modes.

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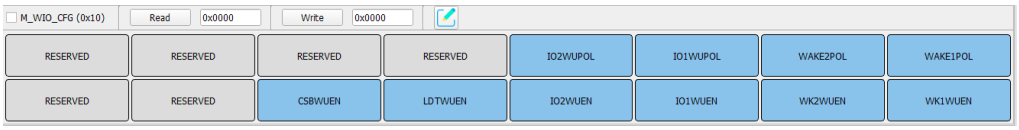
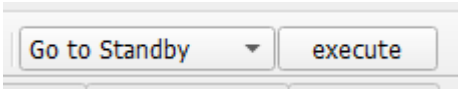


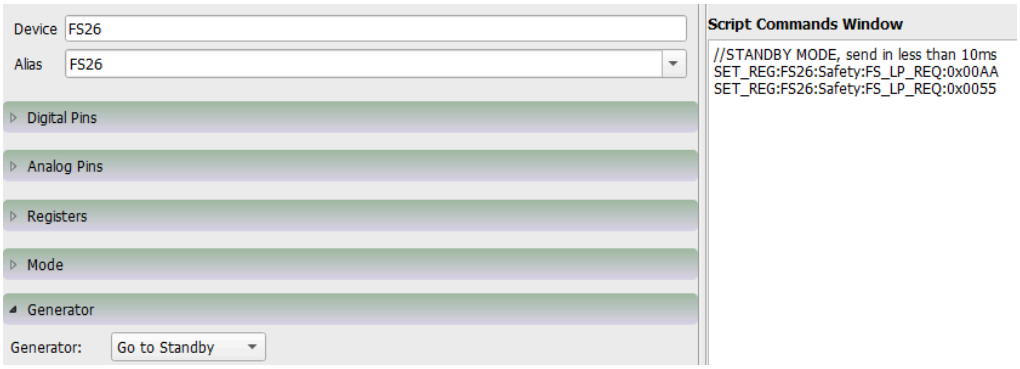
8.8.1 Go to Standby

Execute Go to Standby script from Device Manager.

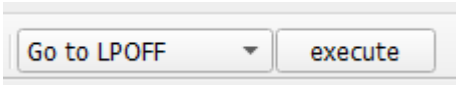


Or from Script editor > Generator, select Go to Standby script and run it.

Device should go to standby mode. Only VPRE stays turn ON and LDOs as configured.

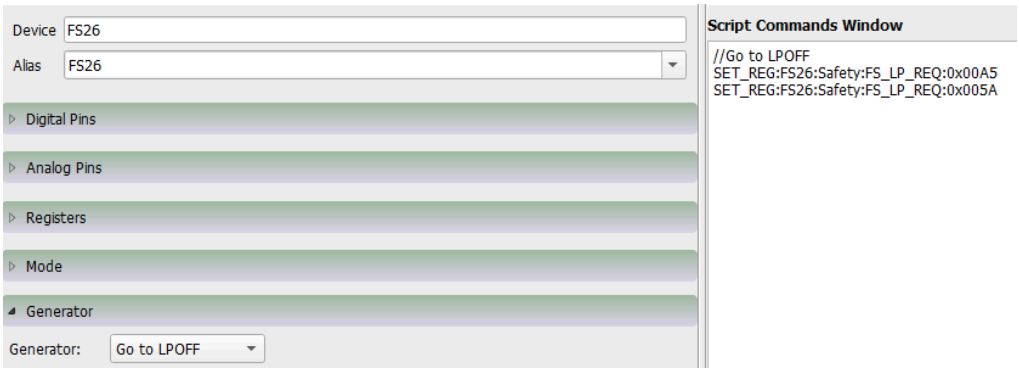


8.8.2 Go to LPOFF



Once in INIT FS or Normal mode, execute Go to LPOFF script from Device Manager. Or from Script editor > Generator, select Go to LPOFF script and run it.

Device should go to LPOFF mode. Only VPRE stays ON.



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9 References

[1] **FS26 datasheet** — Safety System Basis Chip with Low Power for ASIL D FS26 Datasheet-Product Preview-REV 1.3 — Dec 2020.pdf

Revision history

Rev	Date	Description
v.1.0	20210218	Initial version

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Date of release: 19 February 2021
Document identifier: UM11504