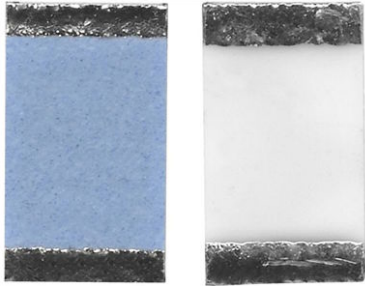


## High Precision Wraparound - $\pm 2$ ppm/°C TCR Thin Film Chip Resistors



### ADDITIONAL RESOURCES



For low noise and precision applications, superior stability, low temperature coefficient of resistance, and low voltage coefficient, Vishay Sfernice's proven precision thin film wraparound resistors exceed requirements of MIL-PRF-55342G characteristics typical  $\pm 2$  ppm/°C (-55 °C; +155 °C).

### FEATURES

- Load life stability 0.05 % typical at 2000 h at 70 °C under Pn
- Low temperature coefficient:  **$\pm 2$  ppm/°C** (-55 °C; +155 °C)
- Very low noise < -35 dB and voltage coefficient < 0.01 ppm/V
- Wide resistance range: 100  $\Omega$  to 3.6 M $\Omega$  depending on size
- Tolerances to  **$\pm 0.01$  %**
- Termination: thin film technology
- Sulfur resistant (per ASTM B809-95 humid vapor test)
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**  
**GREEN**  
(5-2008)

### STANDARD ELECTRICAL SPECIFICATIONS

MODEL	SIZE	RESISTANCE RANGE ( $\Omega$ )	RATED POWER W Pn (1)	RATED POWER W Pd (1)	LIMITING ELEMENT VOLTAGE V	TOLERANCE $\pm$ %
P2TC0402	0402	100 to 88K	0.063	0.040	50	0.01, 0.02, 0.05, 0.1, 0.25, 0.5, 1, 2, 5
P2TC0603	0603	100 to 160K	0.125	0.100	75	0.01, 0.02, 0.05, 0.1, 0.25, 0.5, 1, 2, 5
P2TC0805	0805	100 to 360K	0.200	0.125	150	0.01, 0.02, 0.05, 0.1, 0.25, 0.5, 1, 2, 5
P2TC1206	1206	100 to 1.3M	0.330	0.250	200	0.01, 0.02, 0.05, 0.1, 0.25, 0.5, 1, 2, 5
P2TC2010	2010	100 to 3.6M	1	0.500	300	0.01, 0.02, 0.05, 0.1, 0.25, 0.5, 1, 2, 5

#### Notes

- (1) Pn = nominal power : Pd = derated power intended to improve stability  
 (2) For ohmic range versus tolerance and TCR see detailed table on next page

### CLIMATIC SPECIFICATIONS

Operating temperature range	-55 °C; +155 °C
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#### Note

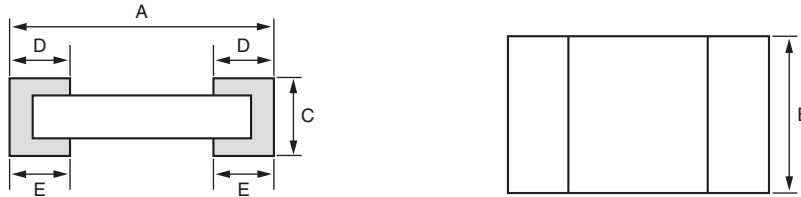
- For temperature up to 230 °C, see PHT datasheet ([www.vishay.com/doc?53050](http://www.vishay.com/doc?53050))

### PERFORMANCE VS. HUMID SULFUR VAPOR

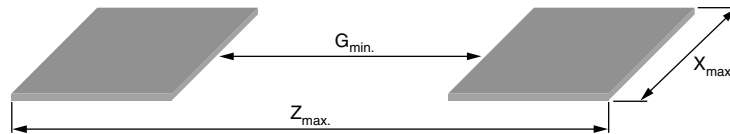
Test conditions	50 °C $\pm$ 2 °C, 85 % $\pm$ 4 % RH, exposure time 500 h
Test results	Resistance drift < (0.05 % R + 0.05 $\Omega$ ), no corrosion products observed

### MECHANICAL SPECIFICATIONS

Substrate	Alumina
Technology	Thin film
Film	<b>Nickel chromium</b> with mineral passivation
Protection	Epoxy + silicone
Terminations	<b>N type:</b> SnAg over nickel barrier for solder reflow <b>G type:</b> gold over nickel barrier for other applications

**DIMENSIONS** in millimeters (inches)


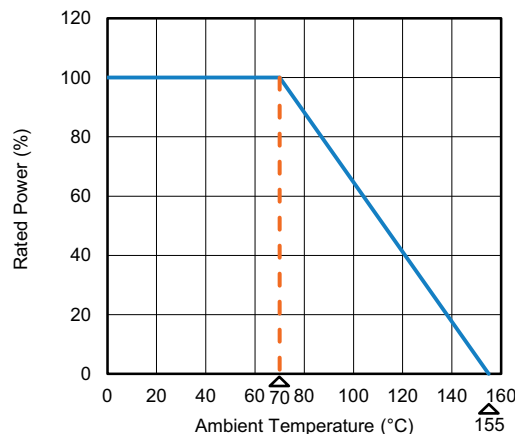
CASE SIZE	A		C	D/E	
	MAX. TOL. +0.152 (+0.006)	MAX. TOL. +0.127 (+0.005)		NOMINAL	TOLERANCE
	MIN. TOL. -0.152 (-0.006)	MIN. TOL. -0.127 (-0.005)			
	NOMINAL	NOMINAL			
0402	1.00 (0.039)	0.60 (0.024)	0.5 (0.02) ± 0.127 (0.005)	0.25 (0.010)	0.1 (0.004)
0603	1.52 (0.060)	0.85 (0.033)		0.38 (0.015)	0.13 (0.005)
0805	1.91 (0.075)	1.27 (0.050)		0.40 (0.016)	
1206	3.06 (0.120)	1.60 (0.063)		0.48 (0.019)	
2010	5.08 (0.200)	2.54 (0.100)			

**SUGGESTED LAND PATTERN** (to IPC-7351A)


CHIP SIZE	DIMENSIONS in millimeters (inches)		
	Z <sub>max.</sub>	G <sub>min.</sub>	X <sub>max.</sub>
0402	1.55 (0.061)	0.15 (0.006)	0.73 (0.029)
0603	2.37 (0.093)	0.35 (0.014)	0.98 (0.039)
0805	2.76 (0.109)	0.74 (0.029)	1.40 (0.055)
1206	3.91 (0.154)	1.85 (0.073)	1.73 (0.068)
2010	5.93 (0.233)	3.71 (0.146)	2.67 (0.105)

**TEMPERATURE COEFFICIENT**

TYPICAL TCR (ppm/°C)	TYPICAL TCR AND MAX. SPREAD (ppm/°C)
± 2	± 2 ± 2

**POWER DERATING CURVE**


BEST TOLERANCE AND TCR VS. OHMIC VALUE		
STYLE	RANGE ( $\Omega$ )	TOLERANCE ( $\pm$ %)
0402	100 to < 250	0.02; 0.05; 0.1; 0.25; 0.5; 1; 2; 5
	250 to 88K	0.01; 0.02; 0.05; 0.1; 0.25; 0.5; 1; 2; 5
0603	100 to < 250	0.02; 0.05; 0.1; 0.25; 0.5; 1; 2; 5
	250 to 160K	0.01; 0.02; 0.05; 0.1; 0.25; 0.5; 1; 2; 5
0805	100 to < 250	0.02; 0.05; 0.1; 0.25; 0.5; 1; 2; 5
	250 to 360K	0.01; 0.02; 0.05; 0.1; 0.25; 0.5; 1; 2; 5
1206	100 to < 250	0.02; 0.05; 0.1; 0.25; 0.5; 1; 2; 5
	250 to 1M3	0.01; 0.02; 0.05; 0.1; 0.25; 0.5; 1; 2; 5
2010	100 to < 250	0.02; 0.05; 0.1; 0.25; 0.5; 1; 2; 5
	250 to 3M6	0.01; 0.02; 0.05; 0.1; 0.25; 0.5; 1; 2; 5

### POPULAR OPTIONS

For any option it is recommended to consult Vishay Sfernice for availability first.

#### Option: Enlarged Terminations

For stringent and special power dissipation requirements, the thermal resistance between the resistive layer and the solder joint can be reduced using enlarged terminations chip resistors which are soldered on large and thick copper pads acting as heatsink (see application note: 53048 Power Dissipation in High Precision Vishay Sfernice Chip Resistors and Arrays (P Thin Film, PRA Arrays, CHP Thick Film) [www.vishay.com/doc?53048](http://www.vishay.com/doc?53048)).

Option to order 0063: (applies to size 1206 / 2010).

DIMENSIONS (Option 0063) in millimeters							
CASE SIZE	A	B	E	D	F		
	MAX. TOL. +0.152 MIN. TOL. -0.152	MAX. TOL. +0.127 MIN. TOL. -0.127	MAX. TOL. +0.13 MIN. TOL. -0.13	MAX. TOL. +0.13 MIN. TOL. -0.13			
	NOMINAL	NOMINAL	NOMINAL	NOMINAL	NOMINAL	MIN.	MAX.
1206	3.06	1.60	0.40	1.215	0.63	0.50	0.76
2010	5.08	2.54	0.48	2.215			

SUGGESTED LAND PATTERN (Option 0063)			
CHIP SIZE	DIMENSIONS (in millimeters)		
	Z <sub>max.</sub>	G <sub>min.</sub>	X <sub>max.</sub>
	1206	3.91	1.73
2010	5.93	0.50	2.67



**Option: Marking**

Option to order 0013:

Marking of ohmic value and tolerance:

Sizes 0805: 3 digits marking (according to EIA-96)

Sizes 1206 and 2010: 4 digits marking (same codification than in the ordering procedure)

Tolerance indicated by a color dot.

Option to order 0014:

Marking of ohmic value:

Sizes 0805: 3 digits marking (according to EIA-96)

Sizes 1206 and 2010: 4 digits marking (same codification than in the ordering procedure)

No standard marking available for smaller sizes.

A price adder will apply to the unit price of the parts for options 0013 and 0014.

**PACKAGING**

ESD packaging available: waffle-pack, and plastic tape and reel (low conductivity).

SIZE	MOQ	NUMBER OF PIECES PER PACKAGE			TAPE WIDTH	
		WAFFLE PACK 2" x 2"	TAPE AND REEL			
			MIN.	MAX.		
0402	100	340	100	5000	8 mm	
0603		100				
0805						4000
1206						
2010						60

**PACKAGING RULES**

**Waffle Pack**

Can be filled up to maximum quantity indicated in the table here above, taking into account the minimum order quantity. When quantity ordered exceeds maximum quantity of a single waffle pack, the waffle packs are stacked up on the top of each other and closed by one single cover.

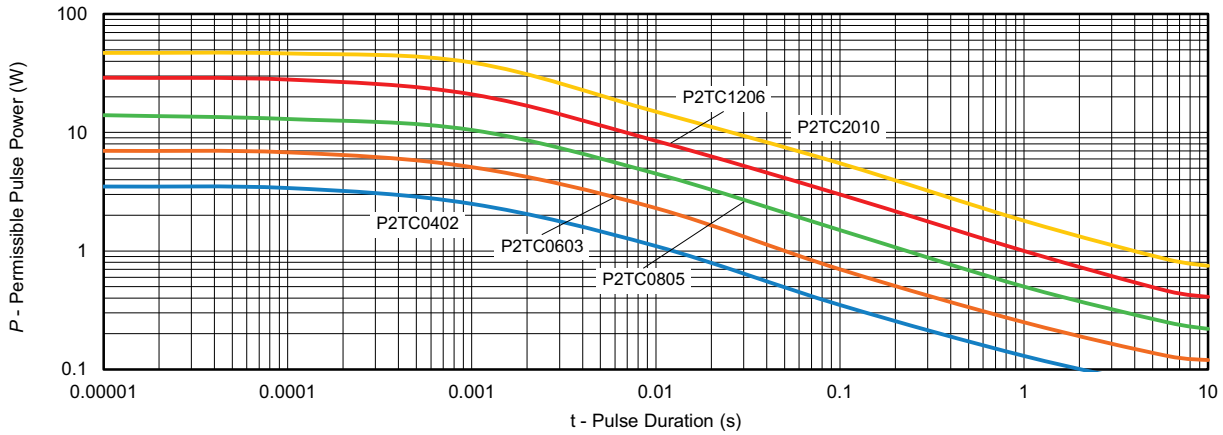
**To get “not stacked up” waffle pack in case of ordered quantity > maximum number of pieces per package: Please consult Vishay Sfernice for specific ordering code.**

**Tape and Reel**

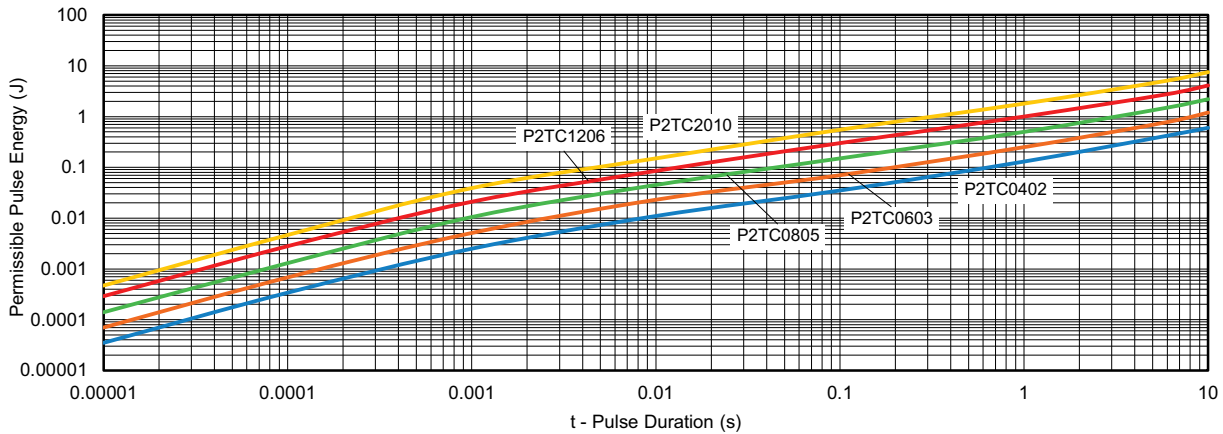
See Part Numbering information to get the quantity desired by tape.

PERFORMANCE			
TESTS	CONDITIONS	MIL OR CECC REQUIREMENTS	TYPICAL PERFORMANCES
Thermal shock	MIL-PRF-55342G MIL-STD-202 F-Method 107 F	± 0.05 %	± 0.02 %
Short time overload	MIL-PRF-55342G PARA 3.10.4.7.5	± 0.05 %	± 0.01 %
Low temperature operation	MIL-PRF-55342G PARA 3.9 and 4.7.4	± 0.05 %	± 0.01 %
Resistance to solder heat	MIL-PRF-55342G PARA 3.12, 4.7.7, 4.7.1.2	± 0.05 %	± 0.03 %
Moisture resistance	MIL-PRF-55342G PARA 3.13 and 4.7.8 MIL-STD-202 F-Method 106 E	± 0.10 %	± 0.01 %
	CECC 56 days / 40 °C / 93 % RH	± 0.10 %	± 0.01 %
High temperature	MIL-PRF-55342G PARA 3.11 and 4.7.6	± 0.05 %	± 0.05 %
Load life	MIL-PRF-55342G 8000 h Pn at 70 °C MIL-STD-202 F-Method 108 A	± 0.5 %	± 0.1 % <sup>(2)</sup>

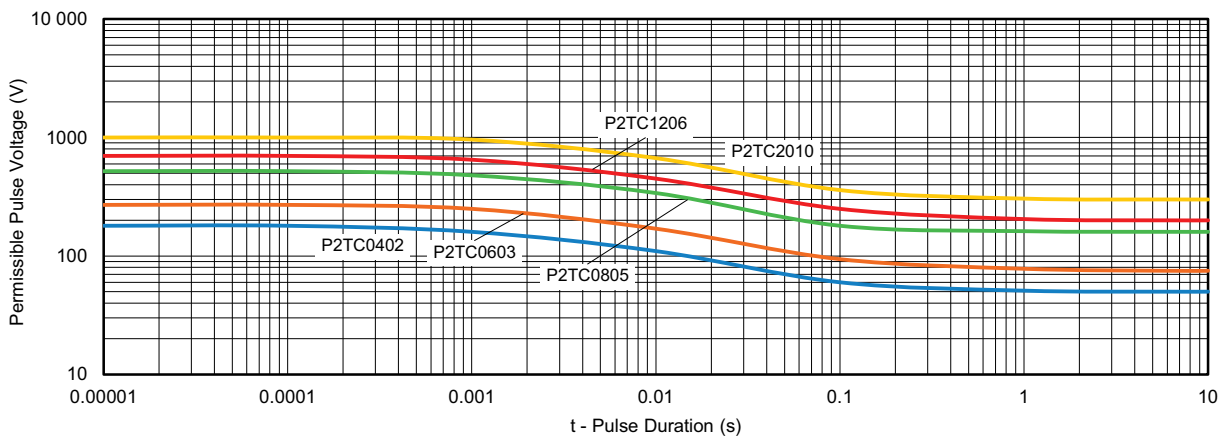
Maximum permissible pulse load  $P_i$  max. for single pulse <sup>(1)</sup>



Energy for single pulse <sup>(1)</sup>



Maximum permissible pulse voltage  $U_i$  max. for single pulse <sup>(1)</sup>

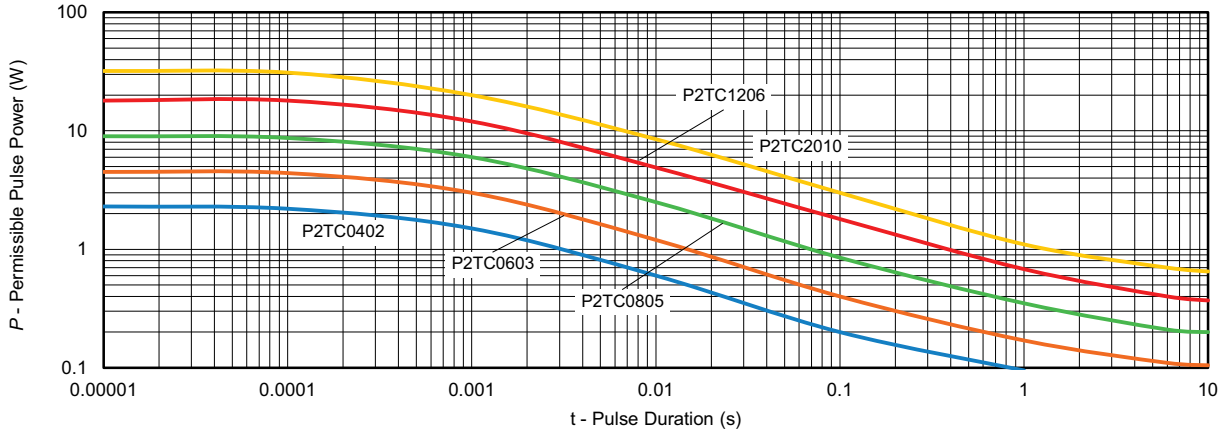


**Note**

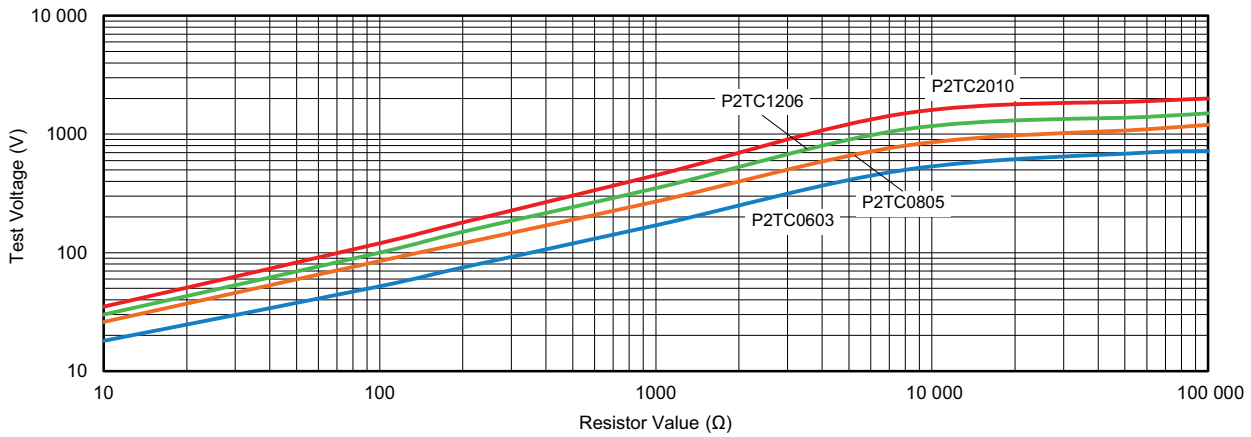
<sup>(1)</sup> One should apply the datas mentioned on the 3 curves together to get the right performances



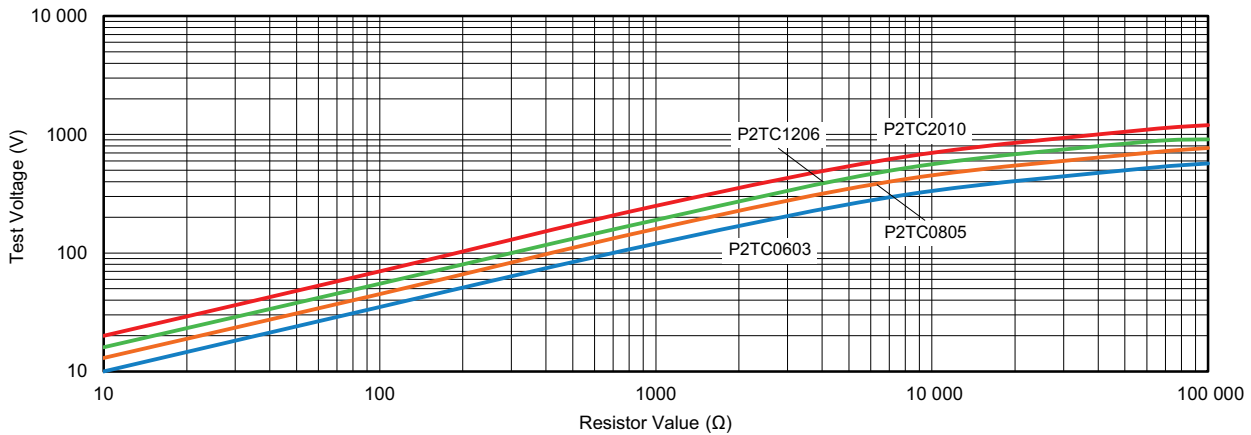
Maximum permissible pulse load  $P_i$  max.



1.2/50  $\mu$ s lightning surge



10/700  $\mu$ s lightning surge





GLOBAL PART NUMBER INFORMATION																	
New Global Part Numbering: P2TC1206D1003BNT99																	
P	2	T	C	1	2	0	6	D	1	0	0	3	B	N	T	9	9
GLOBAL MODEL	SIZE	TCR	VALUE		TOLERANCE		TERMINATION		PACKAGING		OPTION						
P2TC	0402 0603 0805 1206 2010	D = ± 2 ppm	The first three digits are significant figures and the last digit specifies the number of zeros to follow, R designates decimal point  Examples: 1000 = 100 Ω 3901 = 3900 Ω 1004 = 1 MΩ		L = ± 0.01 % P = ± 0.02 % W = ± 0.05 % B = ± 0.1 % C = ± 0.25 % D = ± 0.5 % F = ± 1 % G = ± 2 % J = ± 5 %		N: SnAg over nickel barrier G: gold over nickel barrier		For more information see "Codification of packaging" table		For more information see "Codification of packaging" table  Leave blank if no option						

CODIFICATION OF OPTIONS ON TWO DIGITS	
OPTION	OPTION 2 DIGITS
..	..
0099	99
0100	0A
0101	0A
0102	0C
0103	0D
0104	0E
0105	0F
..	..
0124	0Y
0125	0Z
0126	1A
0127	1B
0128	1C
..	..
0320	8M
0321	8N
0322	8O
0323	8P
0324	8Q
0325	8R
..	..

CODIFICATION OF SIZES	
CODE 18	CODE 40
9	0402
C	0603
D	0805
H	1206
J	2010

CODIFICATION OF PACKAGING	
CODE 18	PACKAGING
<b>WAFFLE PACK</b>	
W	100 min., 1 mult.
WA	100 min., 100 mult. (available only in size 1206)
<b>PLASTIC TAPE (in standard for all sizes)</b>	
T	100 min., 1 mult.
TA	100 min., 100 mult.
TB	250 min., 250 mult.
TC	500 min., 500 mult.
TD	1000 min., 1000 mult.
TE	2500 min., 2500 mult.
TF	Full tape (quantity depending on size of chips)



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