

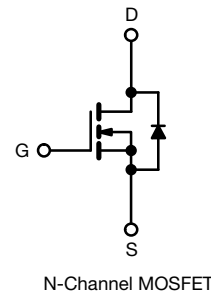
Automotive N-Channel 60 V (D-S) 175 °C MOSFET

PowerPAK® SO-8L

FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

 AUTOMOTIVE
GRADE

RoHS
COMPLIANT
HALOGEN
FREE


PRODUCT SUMMARY	
V _{DS} (V)	60
R _{DS(on)} (Ω) at V _{GS} = 10 V	0.0029
I _D (A)	293
Configuration	Single
Package	PowerPAK SO-8L

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V _{DS}	60	V
Gate-source voltage		V _{GS}	± 20	
Continuous drain current	T _C = 25 °C ^a	I _D	293	A
	T _C = 125 °C		169	
Continuous source current (diode conduction) ^a		I _S	454	
Pulsed drain current ^b		I _{DM}	335	
Single pulse avalanche current	L = 0.1 mH	I _{AS}	52	
Single pulse avalanche energy		E _{AS}	135	
Maximum power dissipation	T _C = 25 °C	P _D	500	W
	T _C = 125 °C		166	
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) ^d			260	

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-ambient	PCB mount ^c	R _{thJA}	42	°C/W
Junction-to-case (drain)		R _{thJC}	0.30	

Notes

- Package limited
- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
- When mounted on 1" square PCB (FR4 material)
- See solder profile (www.vishay.com/doc?73257). The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection



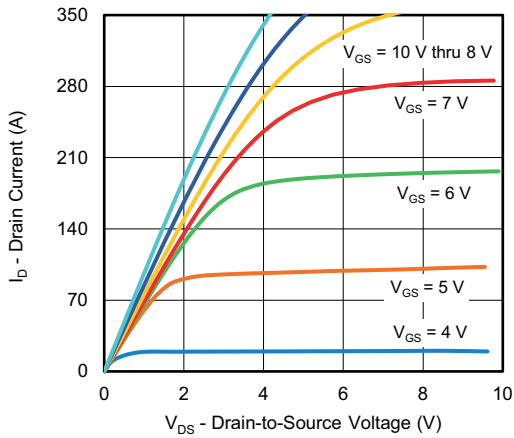
SPECIFICATIONS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0, I_D = 250\text{ }\mu\text{A}$	60	-	-	V
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.5	3.0	3.5	
Gate-source leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{GS} = 0\text{ V}$ $V_{DS} = 60\text{ V}$	-	-	1	μA
		$V_{GS} = 0\text{ V}$ $V_{DS} = 60\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	50	
		$V_{GS} = 0\text{ V}$ $V_{DS} = 60\text{ V}, T_J = 175\text{ }^\circ\text{C}$	-	-	250	
On-state drain current ^a	$I_{D(on)}$	$V_{GS} = 10\text{ V}$ $V_{DS} \geq 5\text{ V}$	30	-	-	A
Drain-source on-state resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$ $I_D = 15\text{ A}$	-	0.00235	0.0029	Ω
		$V_{GS} = 10\text{ V}$ $I_D = 15\text{ A}, T_J = 125\text{ }^\circ\text{C}$	-	-	0.0049	
		$V_{GS} = 10\text{ V}$ $I_D = 15\text{ A}, T_J = 175\text{ }^\circ\text{C}$	-	-	0.0060	
Forward transconductance ^b	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 10\text{ A}$	-	23	-	S
Dynamic ^b						
Input capacitance	C_{iss}	$V_{GS} = 0\text{ V}$ $V_{DS} = 25\text{ V}, f = 1\text{ MHz}$	-	4365	6111	pF
Output capacitance	C_{oss}		-	1828	2560	
Reverse transfer capacitance	C_{rss}		-	53	75	
Total gate charge ^c	Q_g	$V_{GS} = 10\text{ V}$ $V_{DS} = 30\text{ V}, I_D = 40\text{ A}$	-	54	81	nC
Gate-source charge ^c	Q_{gs}		-	21	-	
Gate-drain charge ^c	Q_{gd}		-	4	-	
Gate resistance	R_g	$f = 1\text{ MHz}$	0.6	1.3	2.0	Ω
Turn-on delay time ^c	$t_{d(on)}$	$V_{DD} = 30\text{ V}, R_L = 0.75\text{ }\Omega$ $I_D \cong 40\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$	-	17	26	ns
Rise time ^c	t_r		-	5	9	
Turn-off delay time ^c	$t_{d(off)}$		-	29	44	
Fall time ^c	t_f		-	4	8	
Source-Drain Diode Ratings and Characteristics ^b						
Pulsed current ^a	I_{SM}		-	-	335	A
Forward voltage	V_{SD}	$I_F = 15\text{ A}, V_{GS} = 0\text{ V}$	-	-	1.1	V
Body diode reverse recovery time	t_{rr}	$I_F = 8\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	-	50	100	ns
Body diode reverse recovery charge	Q_{rr}		-	52	104	nC
Reverse recovery fall time	t_a		-	22	-	ns
Reverse recovery rise time	t_b		-	29	-	
Body diode peak reverse recovery current	$I_{RM(REC)}$			-	1.8	-

Notes

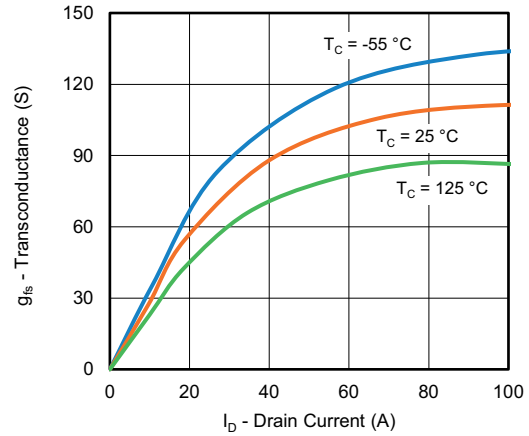
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
- b. Guaranteed by design, not subject to production testing
- c. Independent of operating temperature

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

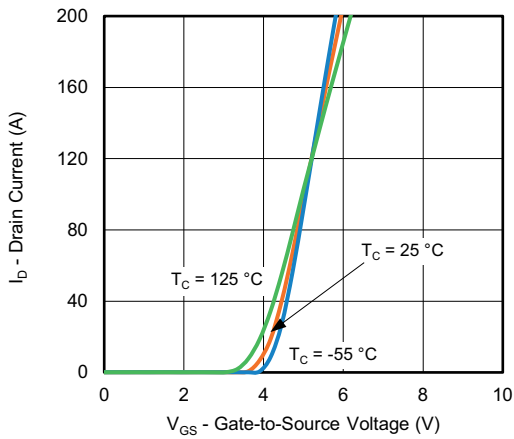
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



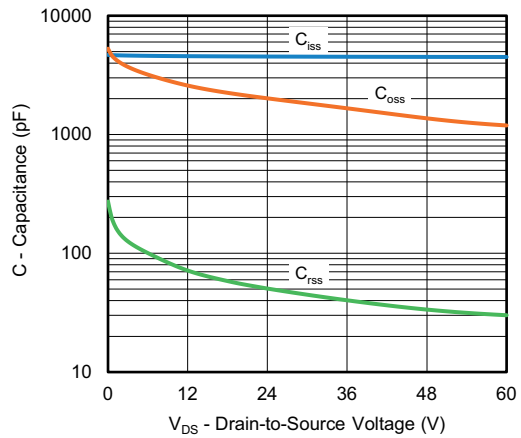
Output Characteristics



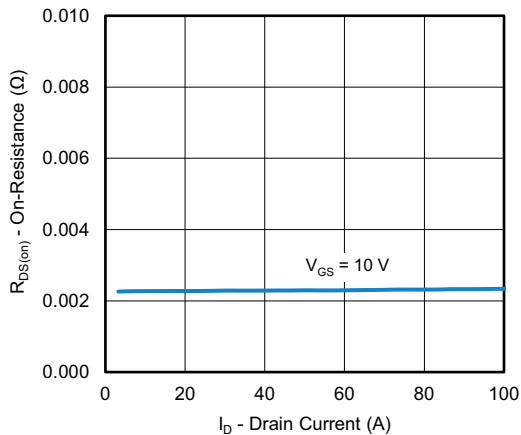
Transconductance



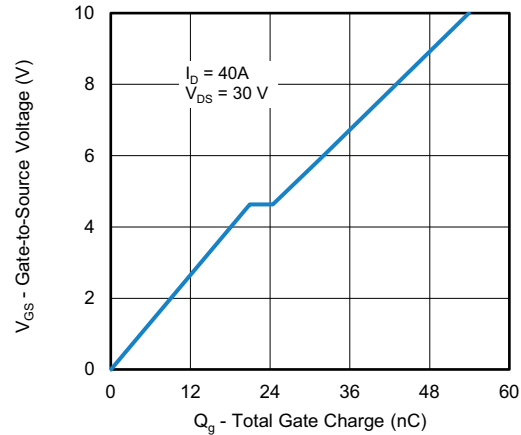
Transfer Characteristics



Capacitance

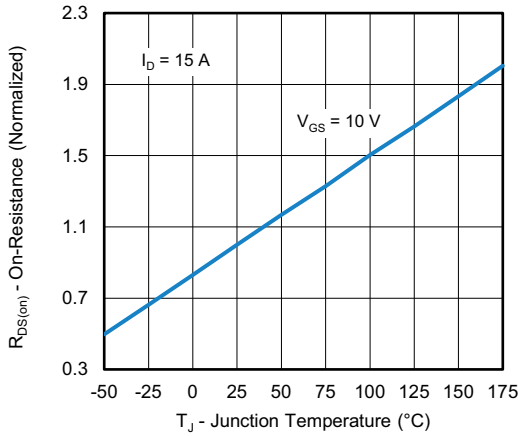


On-Resistance vs. Drain Current

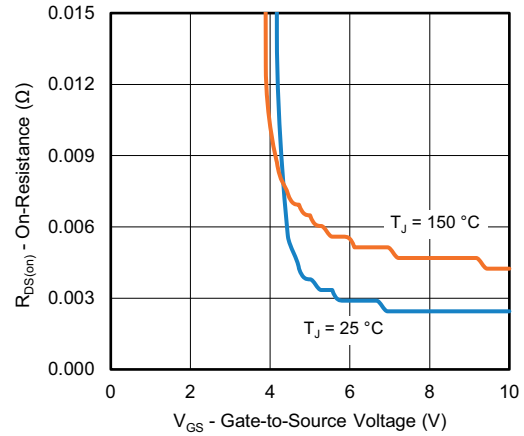


Gate Charge

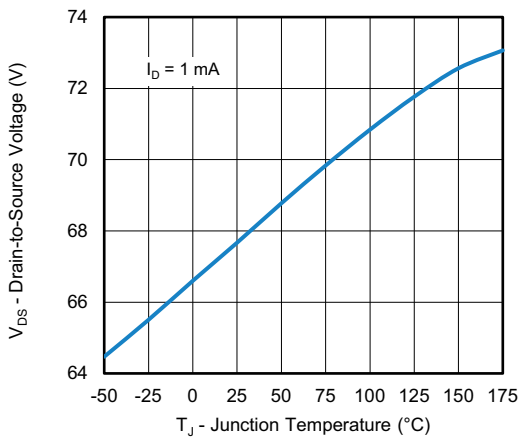
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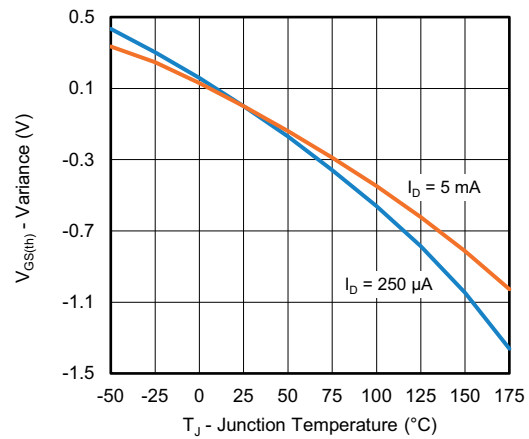
On-Resistance vs. Junction Temperature



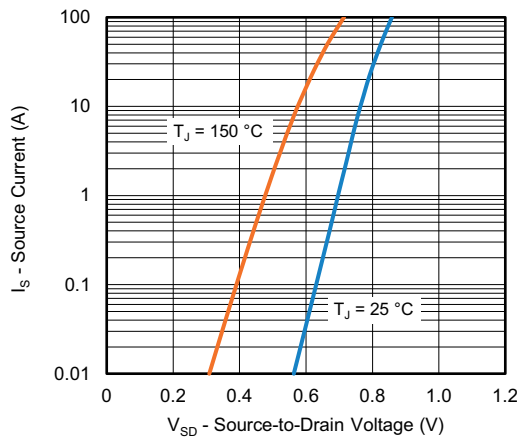
On-Resistance vs. Gate-to Source Voltage



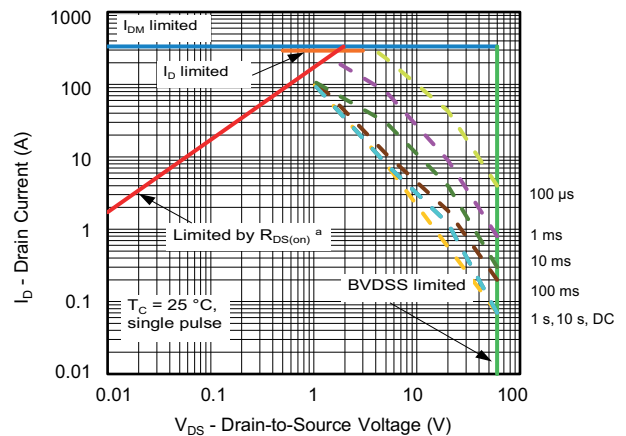
Drain Source Breakdown vs. Junction Temperature



Threshold Voltage



Source Drain Diode Forward Voltage



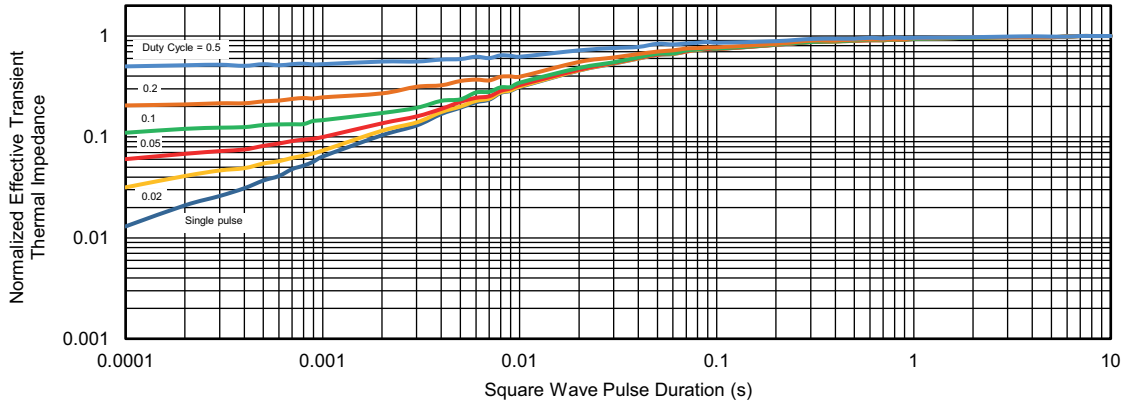
Safe Operating Area

Note

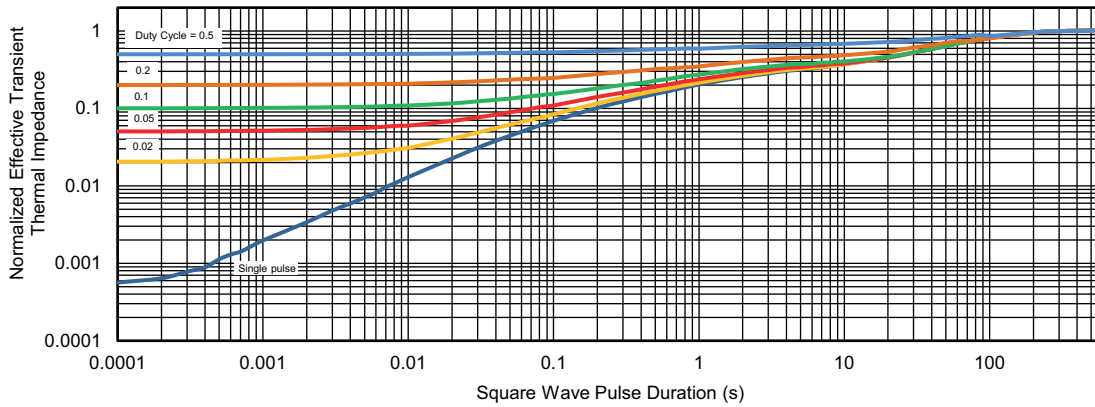
a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case



Normalized Thermal Transient Impedance, Junction-to-Ambient

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