



PESD2V0Y1BSF

Extremely low capacitance bidirectional ESD protection diode

4 April 2018

Product data sheet

1. General description

Extremely low capacitance bidirectional ElectroStatic Discharge (ESD) protection diode, part of the TrEOS protection family. This device is housed in a DSN0603-2 (SOD962) leadless ultra small Surface-Mounted Device (SMD) package designed to protect one signal line from the damage caused by ESD and other transients.

2. Features and benefits

- Bidirectional ESD protection of one line
- Extremely low trigger-voltage V_{t1} of 4.3 V TLP
- Extremely low diode capacitance $C_d = 0.69$ pF
- Extremely low clamping voltage to protect sensitive I/Os
- Extremely low-inductance protection path to ground
- ESD protection up to ± 20 kV according to IEC 61000-4-2
- Ultra small SMD package

3. Applications

- USB 3.2 and Universal Flash Storage (UFS) data lines
- Cellular handsets and accessories
- Portable electronics
- Communication systems
- Computers and peripherals

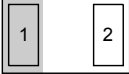
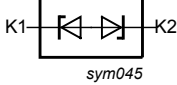
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage		-	-	2	V
C_d	diode capacitance	$f = 1$ MHz; $V_R = 1$ V; $T_{amb} = 25$ °C	-	0.69	-	pF

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K1	cathode (diode 1)	 <p>Transparent top view DSN0603-2 (SOD962)</p>	 <p>sym045</p>
2	K2	cathode (diode 2)		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD2V0Y1BSF	DSN0603-2	silicon, leadless ultra small package; 2 terminals; 0.4 mm pitch; 0.6 x 0.3 x 0.3 mm body	SOD962

7. Marking

Table 4. Marking codes

Type number	Marking code
PESD2V0Y1BSF	C6

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{RWM}	reverse standoff voltage			-	2	V
I_{PPM}	rated peak pulse current	$t_p = 8/20 \mu s$	[1] [2]	-	6	A
T_{amb}	ambient temperature			-40	125	°C
T_{stg}	storage temperature			-65	150	°C
ESD maximum ratings						
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2; contact discharge	[3]	-20	20	kV
		IEC 61000-4-2; air discharge	[3]	-20	20	kV

[1] Device stressed with 8/20 μs exponential decay waveform according to IEC 61000-4-5.

[2] In positive and negative direction.

[3] Device stressed with ten non-repetitive ESD pulses.

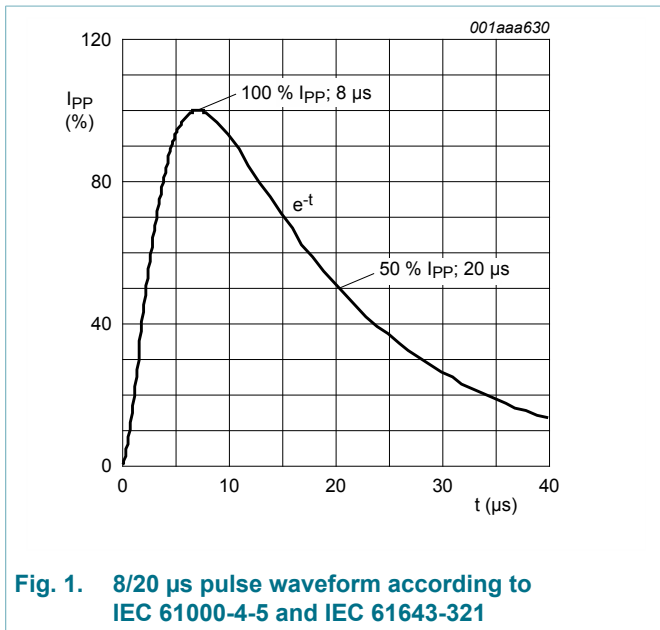


Fig. 1. 8/20 μs pulse waveform according to IEC 61000-4-5 and IEC 61643-321

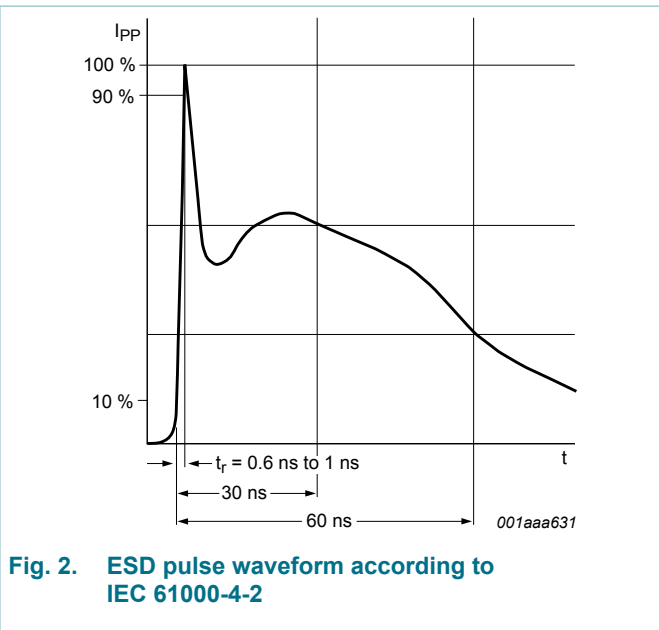


Fig. 2. ESD pulse waveform according to IEC 61000-4-2

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
V _{BR}	breakdown voltage	I _R = 1 mA; T _{amb} = 25 °C	[1]	-	3.3	3.6	V
I _{RM}	reverse leakage current	V _{RWM} = 2 V; T _{amb} = 25 °C	[1]	-	1	50	nA
C _d	diode capacitance	f = 1 MHz; V _R = 1 V; T _{amb} = 25 °C	-	0.69	-	pF	
V _{CL}	clamping voltage	I _{PPM} = 6 A; T _{amb} = 25 °C	[2]	-	3	-	V
R _{dyn}	dynamic resistance	I _R = 10 A; T _{amb} = 25 °C	[3]	-	0.2	-	Ω
		I _R = -10 A; T _{amb} = 25 °C	[3]	-	0.2	-	Ω

[1] Guaranteed by design.

[2] Device stressed with 8/20 μs exponential decay waveform according to IEC 61000-4-5.

[3] Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008.

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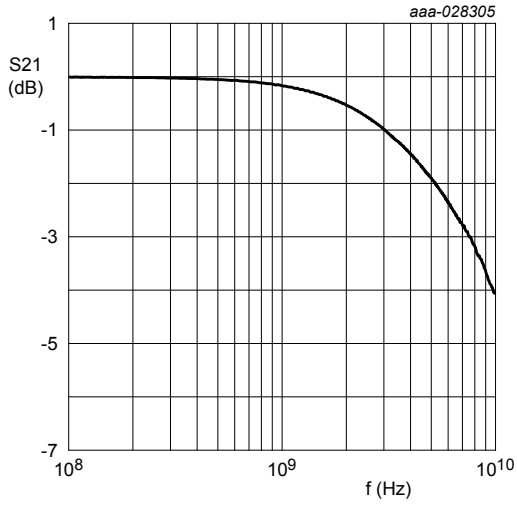
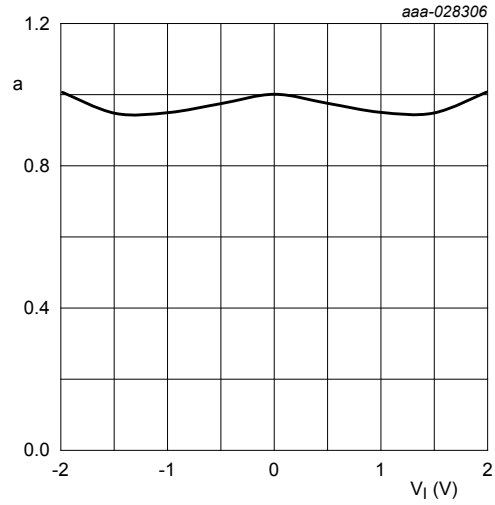


Fig. 3. Insertion loss; typical values



$$a = \frac{C_d}{C_d(V_{RWM} = 0 \text{ V})}$$

Fig. 4. Relative capacitance as a function of input voltage; typical values

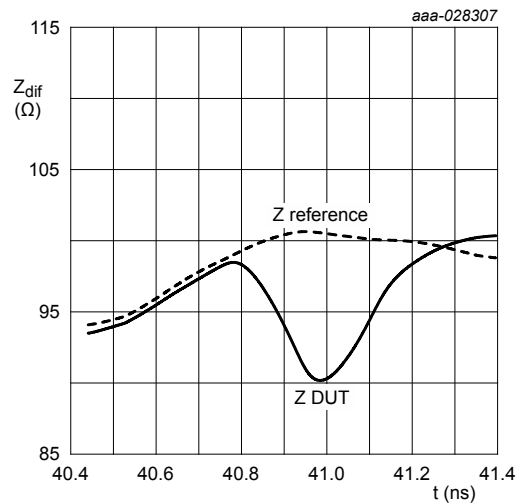
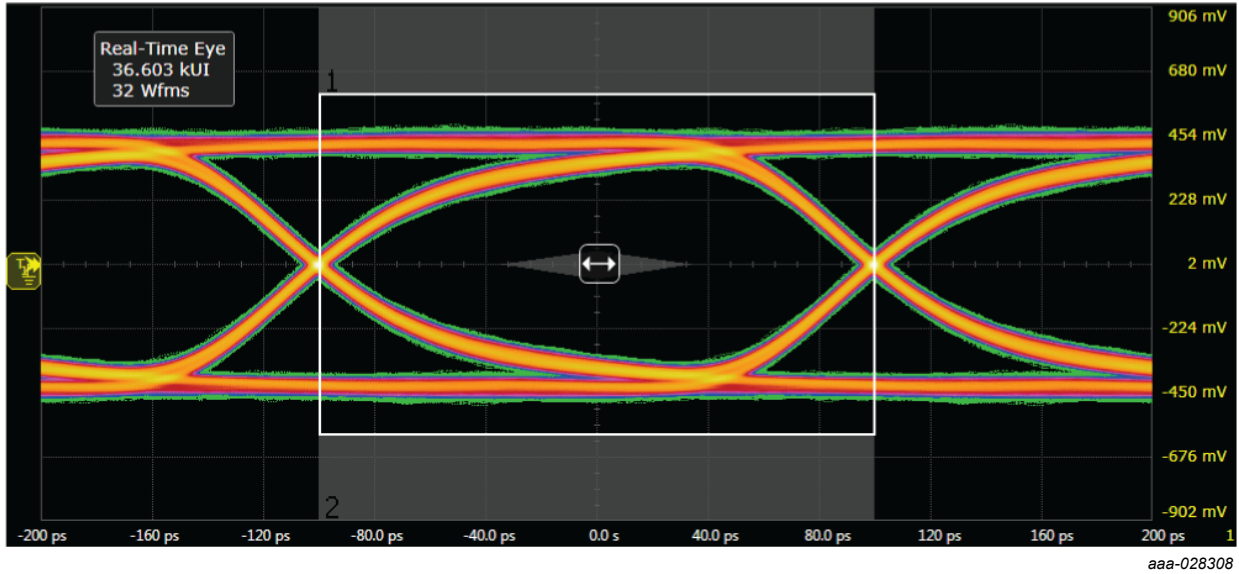
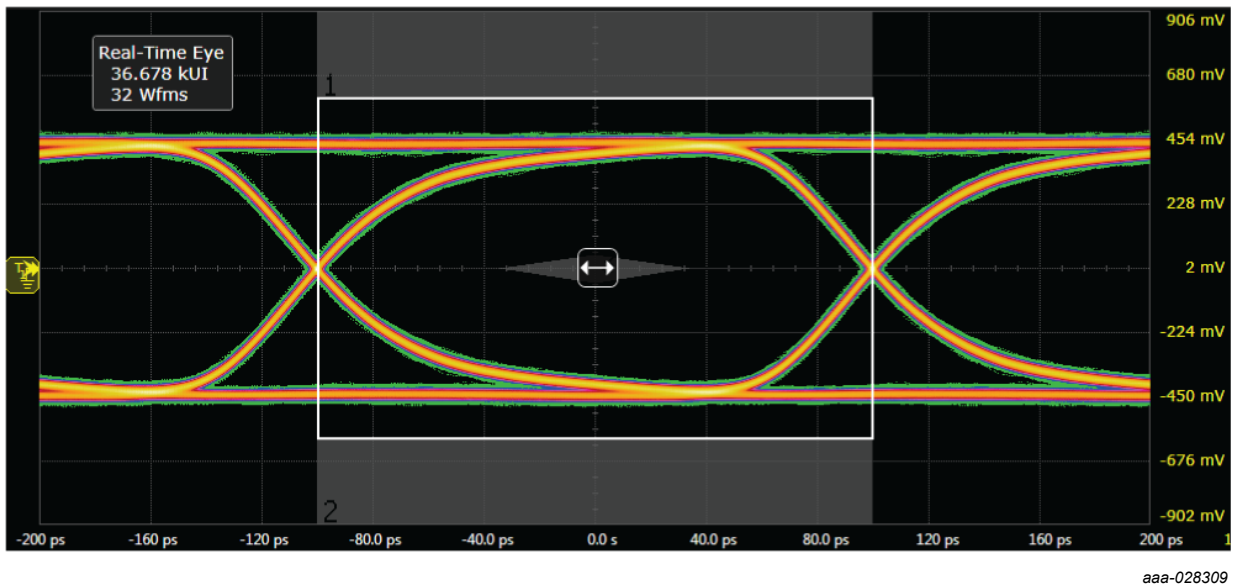


Fig. 5. Differential Time Domain Reflectometer (TDR) plot; typical values



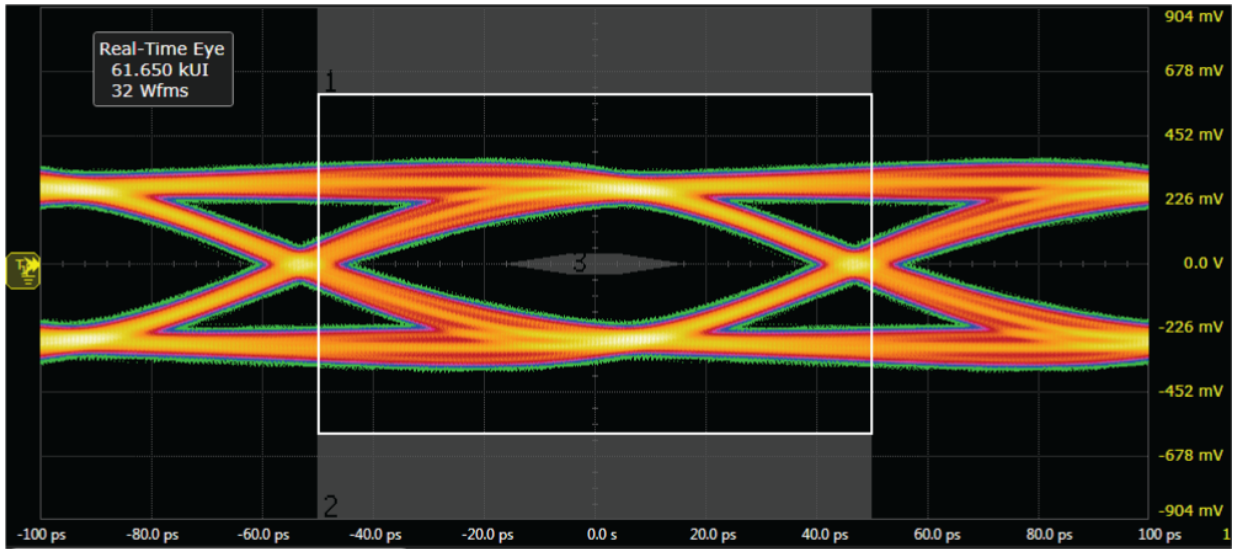
Data rate: 5 Gbit/s

Fig. 6. USB 3.2 eye diagram, PCB with device; typical values



Data rate: 5 Gbit/s

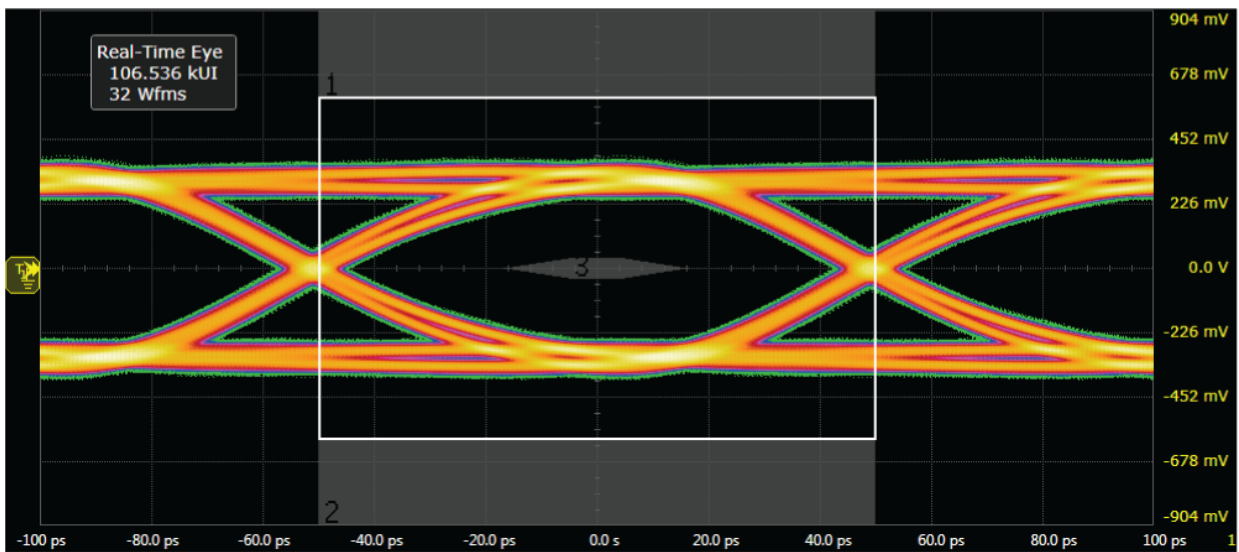
Fig. 7. USB 3.2 eye diagram, PCB without device; typical values



aaa-028310

Data rate: 10 Gbit/s

Fig. 8. USB 3.2 eye diagram, PCB with device; typical values



aaa-028311

Data rate: 10 Gbit/s

Fig. 9. USB 3.2 eye diagram, PCB without device; typical values

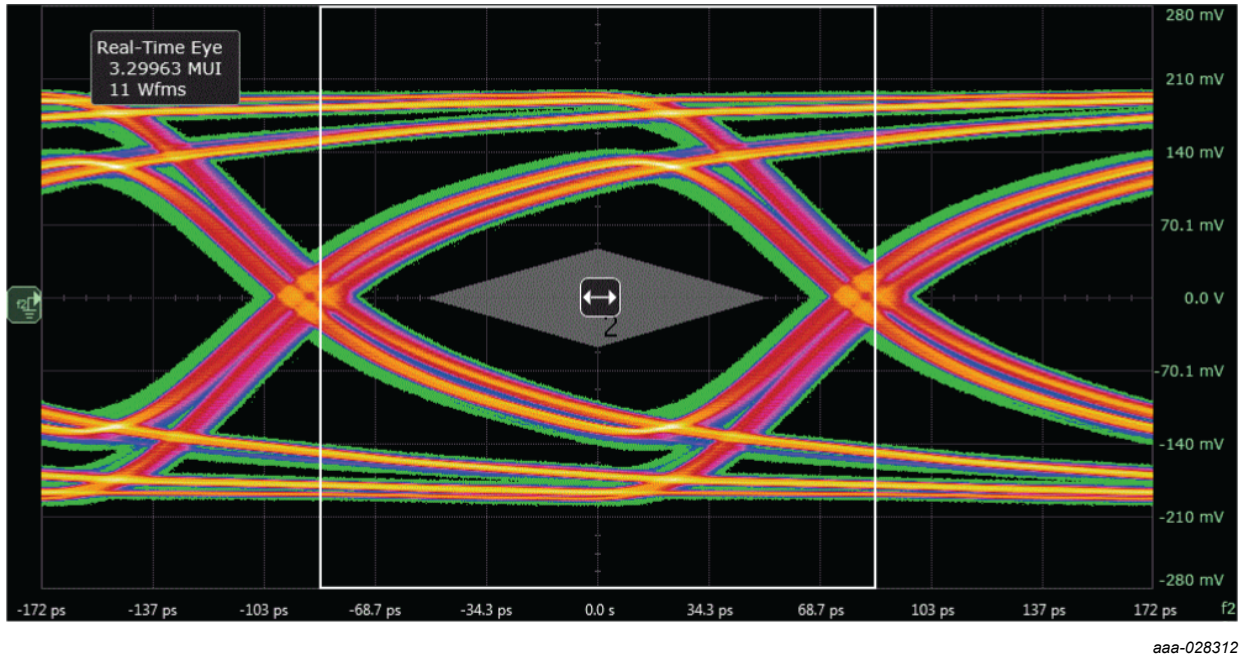


Fig. 10. Universal Flash Storage (UFS) eye diagram, PCB with device; typical values

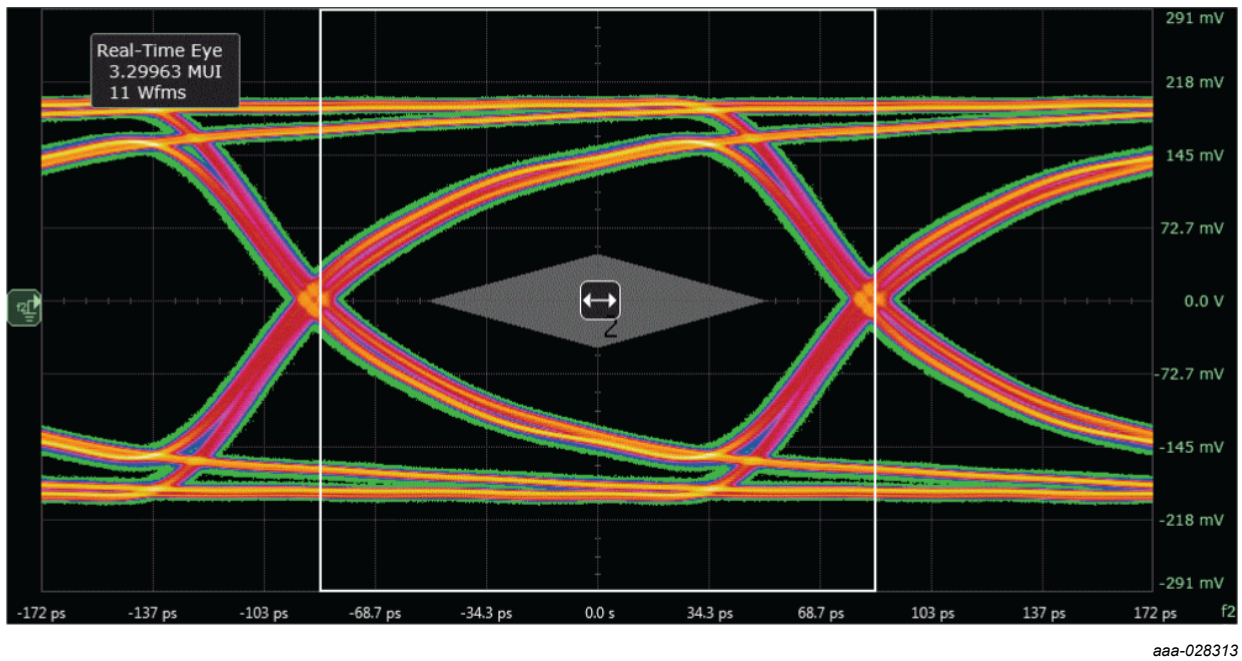
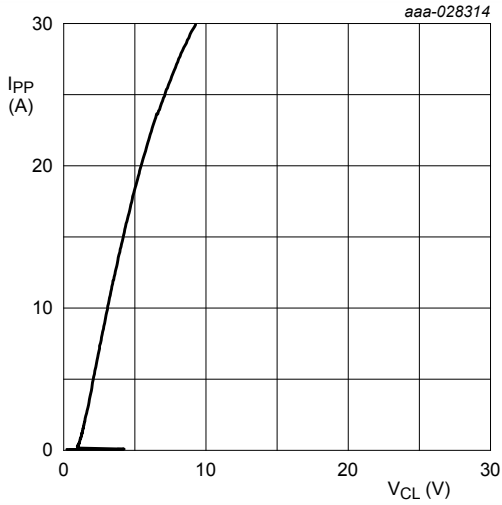
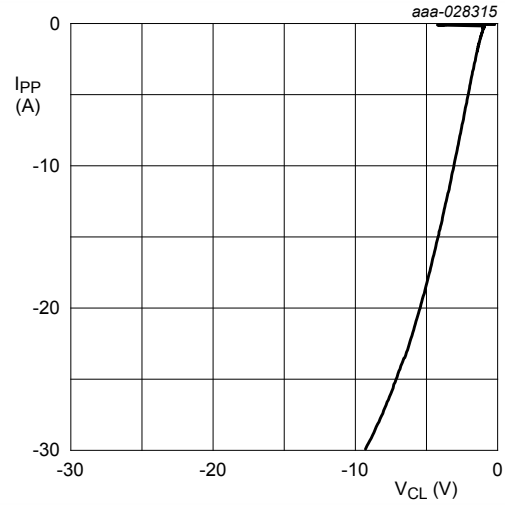


Fig. 11. Universal Flash Storage (UFS) eye diagram, PCB without device; typical values



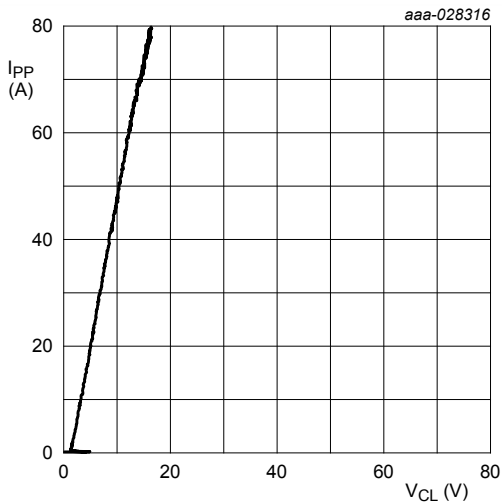
$t_r = 1 \text{ ns}$
 $t_p = 100 \text{ ns}$; Transmission Line Pulse (TLP)

Fig. 12. Dynamic resistance with positive clamping; typical values



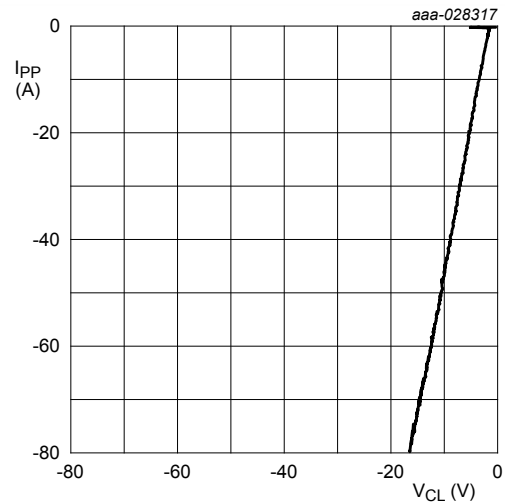
$t_r = 1 \text{ ns}$
 $t_p = 100 \text{ ns}$; Transmission Line Pulse (TLP)

Fig. 13. Dynamic resistance with negative clamping; typical values



$t_r = 600 \text{ ps}$
 $t_p = 5 \text{ ns}$; Transmission Line Pulse (TLP)

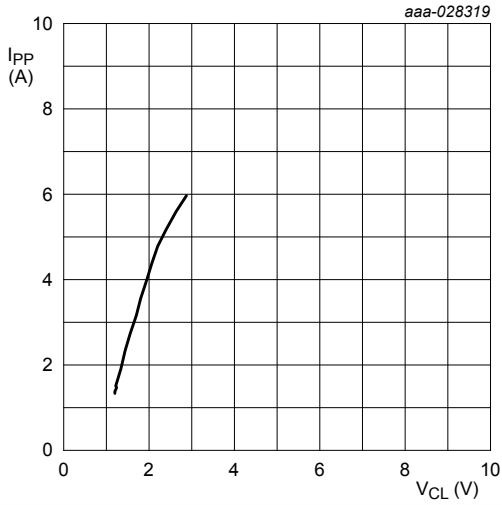
Fig. 14. Dynamic resistance with positive clamping; typical values



$t_r = 600 \text{ ps}$
 $t_p = 5 \text{ ns}$; Transmission Line Pulse (TLP)

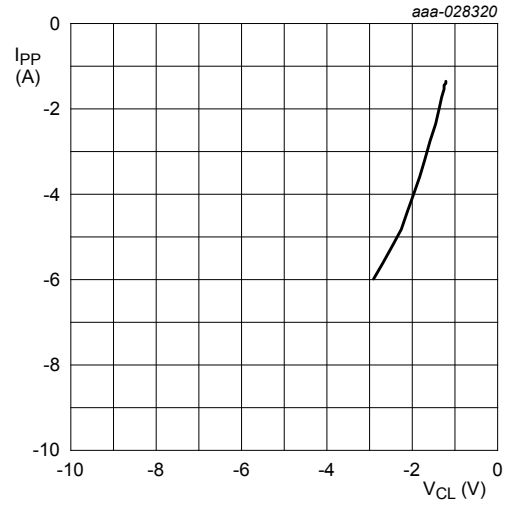
Fig. 15. Dynamic resistance with negative clamping; typical values

Extremely low capacitance bidirectional ESD protection diode



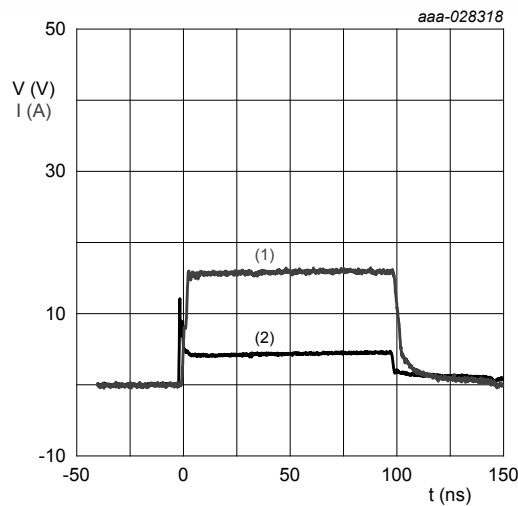
IEC 61000-4-5; $t_p = 8/20 \mu s$; positive pulse

Fig. 16. Dynamic resistance with positive clamping; typical values



IEC 61000-4-5; $t_p = 8/20 \mu s$; negative pulse

Fig. 17. Dynamic resistance with negative clamping; typical values



$t_r = 1 \text{ ns}$
 (1) TLP current
 (2) TLP voltage

Fig. 18. TLP voltage and current over time, typical values

10. Application information

The device is designed for the protection of one bidirectional data line from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are both positive and negative with respect to ground.

The device uses an advanced clamping structure showing a negative dynamic resistance. This snap-back behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in snap-back state after exceeding breakdown voltage (due to an ESD pulse for instance).

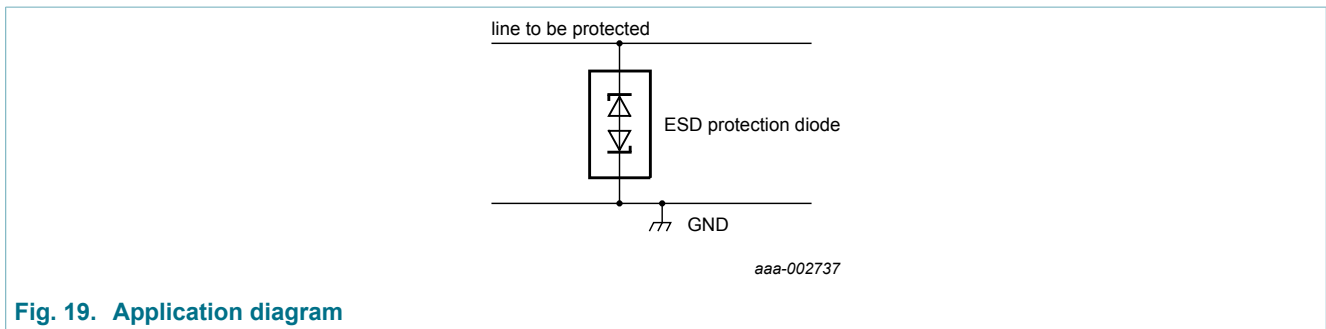


Fig. 19. Application diagram

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

11. Package outline

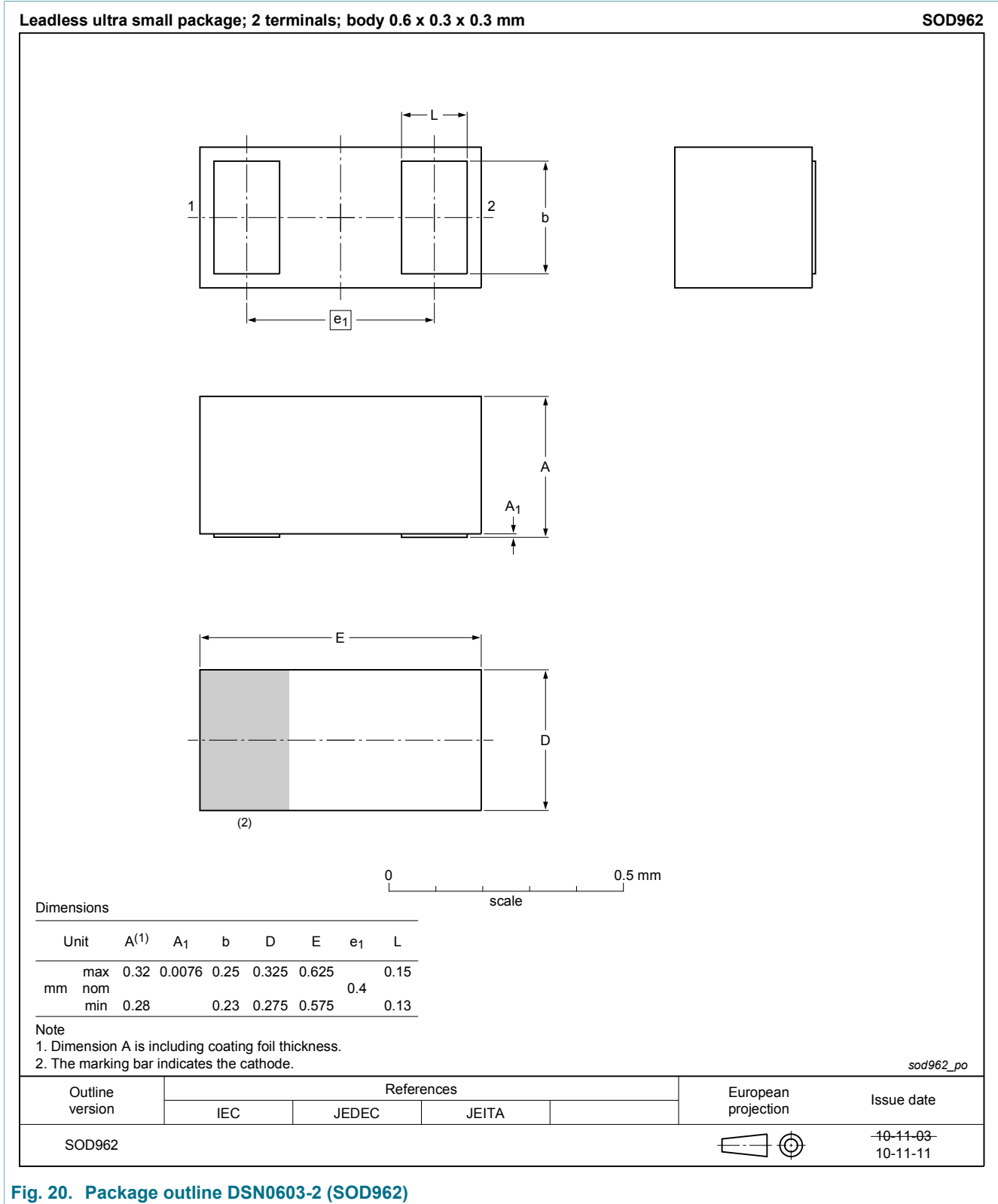
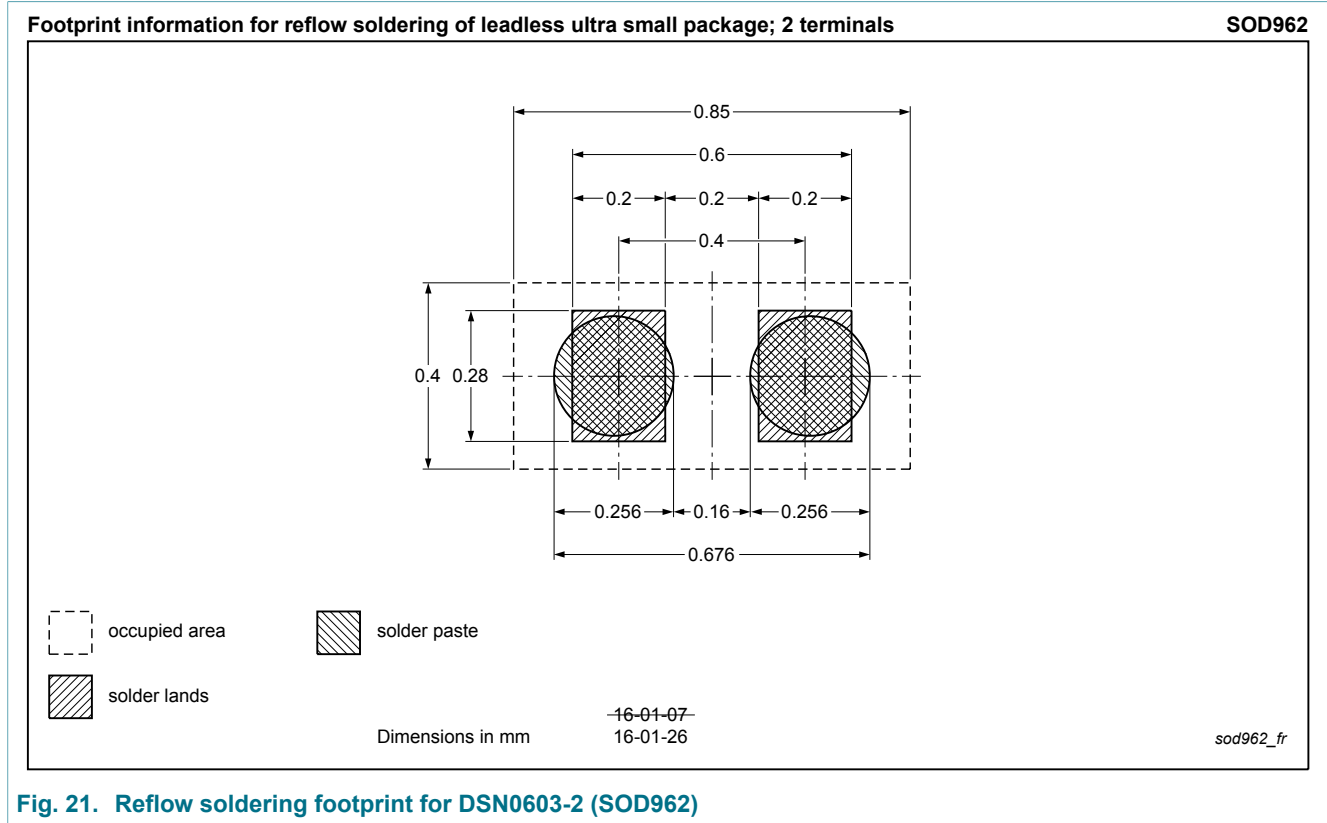


Fig. 20. Package outline DSN0603-2 (SOD962)

12. Soldering



13. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD2V0Y1BSF v.1	20180404	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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15. Contents

1. General description.....	1
2. Features and benefits.....	1
3. Applications.....	1
4. Quick reference data.....	1
5. Pinning information.....	2
6. Ordering information.....	2
7. Marking.....	2
8. Limiting values.....	2
9. Characteristics.....	3
10. Application information.....	10
11. Package outline.....	11
12. Soldering.....	12
13. Revision history.....	13
14. Legal information.....	14

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