Product Change Notification / SYST-05HSKF759

Date:

06-Nov-2020

Product Category:

8-bit Microcontrollers

PCN Type:

Silicon Die Revision

Notification Subject:

ERRATA - PIC18F06/16Q41 Silicon Errata and Data Sheet

Affected CPNs:

SYST-05HSKF759_Affected_CPN_11062020.pdf
SYST-05HSKF759_Affected_CPN_11062020.csv

Notification Text:

SYST-05HSKF759

Microchip has released a new Product Documents for the PIC18F06/16Q41 Silicon Errata and Data Sheet of devices. If you are using one of these devices please read the document located at PIC18F06/16Q41 Silicon Errata and Data Sheet.

Notification Status: Final

Description of Change: Added Silicon Revision A5.

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Estimated First Ship Date: 20 Dec 2020

NOTE: Please be advised that after the estimated first ship date customers may receive pre and post change parts.

Markings to Distinguish Revised from Unrevised Devices: Traceability Code

Attachments:

PIC18F06/16Q41 Silicon Errata and Data Sheet

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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PIC18F06/16Q41 Silicon Errata and Data Sheet Clarifications

The PIC18F06/16Q41 devices you have received conform functionally to the current device data sheet (DS40002214**C**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the table below.

The errata described in this document will be addressed in future revisions of the PIC18F06/16Q41 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Table 1. Silicon Device Identification

Part Number	Device ID	Revision ID	
		A4	A5
PIC18F06Q41	0x7580	0xA004	0xA005
PIC18F16Q41	0x7560	0xA004	0xA005

Important: Refer to the **Device/Revision ID** section in the current **"PIC18-Q41 Family Programming Specification"** (DS40002143) for more detailed information on Device Identification and Revision IDs for a specific device.

Table 2. Silicon Issue Summary

Module	Feature	Item No.	Issue Summary	Affected Revisions	
				A4	A5
Analog-to-Digital Converter with Computation	ADCC	1.1.1	ADC cannot operate in certain low-power conditions	X	
Oscillator	XT mode	1.2.1	Maximum clock frequency limited to 2 MHz for XT mode	X	
	Fail-Safe Clock Monitor	1.2.2	Enabling the FOSC Fail-Safe Clock Monitor alongside the Primary or Secondary Oscillator Clock Monitor causes issues in Sleep	X	
	EC mode	1.2.3	Maximum clock frequency for EC mode is 32 MHz for V_{DD} < 2.0V	X	
I^2C	I^2C	1.3.1	I2CxADR0/1/2/3 registers have incorrect Reset value	X	
Operational Amplifier	OPA	1.4.1	Charge Pump On Control (CPON) bit is reserved	X	
	OPA	1.4.2	Internal resistor ladder does not disconnect in Unity Gain mode	X	
Program Flash Memory	PFM	1.5.1	Endurance of PFM cell is lower than specified	X	X

Note: Only those issues indicated in the last column apply to the current silicon revision.

Table of Contents

1. Silicon Errata Issues

Notice: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the bold font in the following tables apply to the current silicon revision.

1.1 Module: Analog-to-Digital Converter with Computation (ADCC)

1.1.1 ADC Cannot Operate in Certain Low-Power Conditions

The ADC will not function when all of the following conditions exist: When the MCU system clock is sourced from LFINTOSC or SOSC and when both the BOR and FVR features are disabled.

Work around

- Method 1: Use a system clock other than LFINTOSC or SOSC.
- Method 2: Enable the BOR feature.
- Method 3: Enable the FVR feature.

Affected Silicon Revisions

A4	A5
X	

1.2 Module: Oscillator

1.2.1 Maximum Clock Frequency Limited to 2 MHz for XT Mode

The maximum clock frequency for the intermediate gain setting that supports quartz crystal and ceramic resonator operation (XT mode) is being reduced from 4 MHz to 2 MHz.

Work around

For crystal or resonator frequencies above 2 MHz, use HS mode.

Affected Silicon Revisions

A4	A5
X	

1.2.2 Enabling the FOSC Fail-Safe Clock Monitor Alongside the Primary or Secondary Oscillator Clock Monitor Causes Issues with Sleep

When the FOSC Fail-Safe Clock Monitor is enabled (FCMEN Configuration bit = 1) and either the Primary or Secondary Fail-Safe Clock Monitor is also enabled (FCMENS and/or FCMENP = 1), putting the device to Sleep will cause a Fail-Safe condition to trigger. This has the effect of erroneously triggering Fail-Safe interrupts when there has not been a clock interruption. This can also cause the Watchdog Timer to not properly wake up the part from Sleep.

Work around

If proper functionality in Sleep is required, do not enable the Primary or Secondary Fail-Safe Clock Monitor while the FOSC Fail-Safe Clock Monitor is enabled. If Primary or Secondary Clock Monitoring in Sleep is desired, disable the FOSC Fail-Safe Clock Monitor before the device goes to Sleep.

Affected Silicon Revisions

A4	A5
X	

1.2.3 Maximum Clock Frequency for EC Mode Is 32 MHz for V_{DD} < 2.0V

When configured in External Clock High-Power (ECH) mode and operating at V_{DD} < 2.0V, the maximum input clock frequency is 32 MHz.

Work around

To obtain a system clock frequency of 64 MHz in ECH mode at V_{DD} < 2.0V, use a 16 MHz external clock in conjunction with the 4x Phase-Locked Loop (PLL) circuit (i.e., either RSTOSC Configuration bits = 0b010 or OSCCON1bits.NOSC = 0b010).

Affected Silicon Revisions

A4	A5
X	

1.3 Module: I^2C

1.3.1 I2CxADR0/1/2/3 Registers Have Incorrect Reset Value

The I2CxADR0/2 registers reset to 0xFF when the I2CxMD is enabled instead of 0x00. The I2CxADR1/3 registers reset to 0xFE when the I2CxMD is enabled instead of 0x00.

Work around

None.

Affected Silicon Revisions

A4	A5
X	

1.4 Module: Operational Amplifier

1.4.1 Charge Pump On Control (CPON) Bit Is Reserved

When not operating the OPAMP near the rails, the Charge Pump On Control (CPON) bit can be used to disable the charge pump in order to save on current consumption. This feature is currently not available, and the charge pump is always enabled whenever the OPAMP module is in operation.

Work around
None.

Affected Silicon Revisions

A4	A5
X	

1.4.2 Internal Resistor Ladder Does Not Disconnect in Unity Gain Mode

When using the OPA module in a unity gain configuration, the internal resistor ladder will not automatically disconnect from the operational amplifier, which may adversely affect the gain of the circuit. This applies when the peripheral has been configured to operate in Unity Gain mode in software by setting the UG bit, or in hardware using the hardware controlled override feature.

Work around
Disconnect the internal resistor ladder from the operational amplifier by writing to the Inverting Input Channel Selection (NCH) bits. All signals can be disconnected from the operational amplifier by writing `0b000` to the NCH bits.

Affected Silicon Revisions

A4	A5
X	

1.5 Module: PFM - Program Flash Memory

1.5.1 Endurance of PFM Cell Is Lower than Specified

The Flash memory cell endurance specification (Parameter MEM30) is lower than specified in the device data sheet. The PFM cell endurance is 1K cycles instead of 10K cycles.

Work around
None.

Affected Silicon Revisions

A4	A5
X	X

2. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40002214**C**):

Note:

Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

2.1 None

There are no known data sheet clarifications as of this publication date.

3. Appendix A: Revision History

Doc Rev.	Date	Comments
C	11/2020	Adding silicon revision A5.
B	08/2020	Adding silicon erratum item 1.5.1.
A	06/2020	Initial document release.

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Affected Catalog Part Numbers (CPN)

PIC18F06Q41-E/SL
PIC18F06Q41-E/ST
PIC18F06Q41-I/SL
PIC18F06Q41-I/ST
PIC18F06Q41T-I/SL
PIC18F06Q41T-I/ST
PIC18F16Q41-E/P
PIC18F16Q41-E/REB
PIC18F16Q41-E/SO
PIC18F16Q41-E/SS
PIC18F16Q41-I/P
PIC18F16Q41-I/REB
PIC18F16Q41-I/SO
PIC18F16Q41-I/SS
PIC18F16Q41T-I/SO
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