User's Manual

HIP2210EVAL1Z

User's Manual: Evaluation Board

Industrial Analog and Power

Renesas Electronics Corporation
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HIP2210EVAL1Z

Evaluation Board

The HIP2210EVAL1Z evaluation board is designed to provide a quick and comprehensive method for evaluating the HIP2210 100V 3A source, 4A sink high frequency half-bridge driver for driving the gates of two N-channel MOSFETs in a half-bridge configuration. Two N-channel MOSFETs (with dual footprint supporting multiple packages such as TO220 and DPAK) and an inductor-capacitor LC filter are included on the evaluation board to allow for the evaluation of a half-bridge driven load such as a synchronous buck switching regulator.

The HIP2210 half-bridge driver is offered in a 10 Ld DFN package (with enhanced thermal EPAD). The HIP2210EVAL1Z evaluation board operates from a supply voltage of 6V to 18V DC with the capability of driving both the high-side and low-side MOSFETs in a 100V half-bridge configuration ICs.

Key Features

- 3A source and 4A sink NMOS gate drivers
- Internal level shifter and bootstrap diode for gate driver on high-side NFET
- Up to 100V high-side bootstrap reference
- 6V to 18V bias supply operation
- Fast 15ns typical propagation delay and 2ns typical propagation delay match supports up to 1MHz operation

Specifications

This board is optimized for the following operating conditions:

- V_{DD} supply: 12V nominal
- V_{BRIDGE} supply input: 0V to 60V
- PWM switching frequency: 100kHz
- Peak gate drive current: 3A source and 4A sink

Ordering Information

Part Number	Description
HIP2210EVAL1Z	HIP2210 10 Ld DFN evaluation board

Related Literature

For a full list of related documents, visit our website:

- HIP2210, HIP2211 device pages

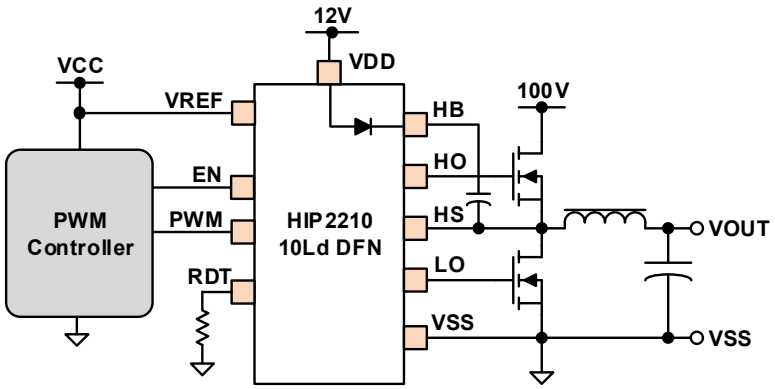

Figure 1. HIP2210 Typical Application Block Diagram

1. Functional Description

The HIP2210EVAL1Z is designed to provide a comprehensive and versatile platform for you to evaluate the functionality and prototype an application of the HIP2210 N-channel MOSFET half-bridge drivers. This evaluation board includes the MOSFETs (with dual footprint supporting for TO220 and DPAK) and an inductor-capacitor output filter for evaluating an open-loop type synchronous buck DC/DC converter where the output voltage is controlled through the duty cycle of the signals into the PWM pin.

1.1 Operating Range

The HIP2210EVAL1Z evaluation board is designed for 60V half-bridge applications with 12V supply to bias the VDD of the HIP2210 IC. While the HIP2210 voltage ratings for the bootstrap reference and VDD supply are much higher, you should monitor the transient voltages at the switching nodes for applications exceeding 60V on the half-bridge or 12V on the driver bias to ensure they do not violate the absolute maximum ratings of the HIP2210 driver.

The inductance and capacitance value of the output LC filter is chosen for a 100kHz switching operation. You can replace these components with different values if a different switching frequency is required.

1.2 Recommended Equipment

- A power supply that can deliver 12V or higher with at least 2A source current capability
- A power supply that can deliver 5V or higher
- A power supply that can deliver 60V or higher to bias the half bridge
- A square wave or pulse generator with 0V to 5V logic levels output and 100kHz capability
- Minimum 4-channel oscilloscope to monitor LI, HI, LO, HO, and HS signals
- Optional: A DC electronic load to draw current out of the LC filter output

1.3 Quick Start Guide

1. The programmable dead time of the HO and LO signal is set to around 35ns with a 10kΩ resistor from the RDT pin to GND. To change the dead time, replace the resistor at R_2 with the value corresponding to the required dead time.
2. Ensure that the enable switch (SW_1) is set to the off position.
3. Connect a 6V to 18V supply to the VDD terminals {J2 (+) and J3 (-)}.
4. Connect a 5V supply to VREF terminal {TP3}.
5. Connect a power supply capable of 60V or higher and 10A to the V_BRIDGE terminals {J18(+) and J17(-)}.
6. Connect a 0V to 5V 100kHz square wave signal to the PWM BNC connector J13.
   Note: The magnitude of the square wave signal needs to match VREF.
7. Turn on the VDD supply to 12V. Turn on the VREF supply to 5V.
8. Turn on the 0V to 5V 100kHz square wave signal.
9. Turn on the bridge voltage supply V_BRIDGE to the required voltage (such as 48V).
10. Toggle the enable switch (SW_1) to the on position.
11. Verify the HO and LO outputs are switching. LO switches between GND and VDD (12V in this case) phase inverted from the PWM. HO switches between GND and VHB+V_BRIDGE in phase with PWM.

2. PCB Layout Guidelines

For best thermal performance, connect the driver EPAD to a low thermal impedance ground plane. Use as many vias as possible to connect the top layer PCB thermal land to the ground planes on other PCB layers. For best electrical performance, connect the VSS and AGND pins through the EPAD to maintain a low impedance connection between the two pins.

When adjustable dead time is used, connect the resistor to the RDT pin and GND plane close to the IC to minimize ground noise from disrupting the timing performance.

Place the VDD decoupling capacitors and bootstrap capacitors close to the VDD-VSS and HB-HS pins, respectively. Use decoupling capacitors to reduce the influence of parasitic inductors. To be effective, these capacitors must also have the shortest possible lead lengths. If vias are used, connect several paralleled vias to reduce the inductance.

In addition:

- Keep power loops as short as possible by paralleling the source and return traces.
- Adding resistance might be necessary to dampen resonating parasitic circuits. In PCB designs with long leads on the LO and HO outputs, add series gate resistors on the bridge FETs to dampen the oscillations.
- Large power components (such as power FETs, electrolytic capacitors, and power resistors) have internal parasitic inductance, which cannot be eliminated. This must be accounted for in the PCB layout and circuit design.
- If you simulate your circuits, consider including parasitic components.

2.1 HIP2210EVAL1Z Evaluation Board

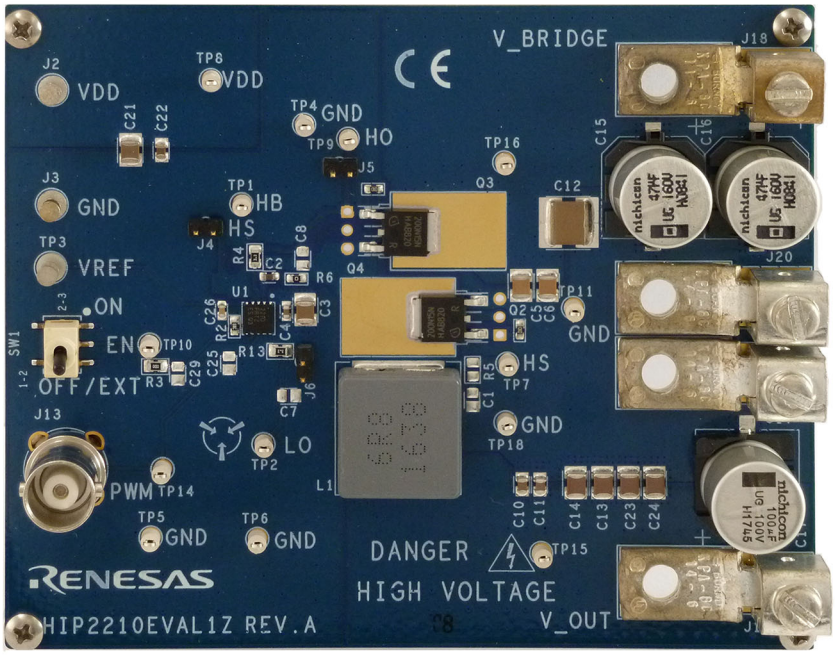

Figure 2. HIP2210EVAL1Z Evaluation Board (Top)

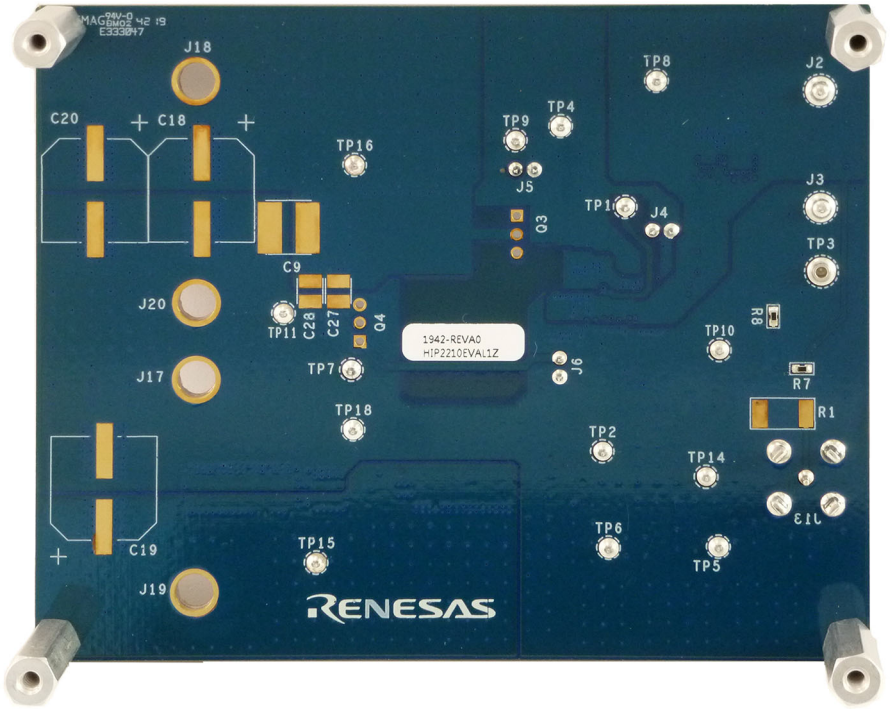

Figure 3. HIP2210EVAL1Z Evaluation Board (Bottom)

2.2 HIP2210EVAL1Z Circuit Schematic

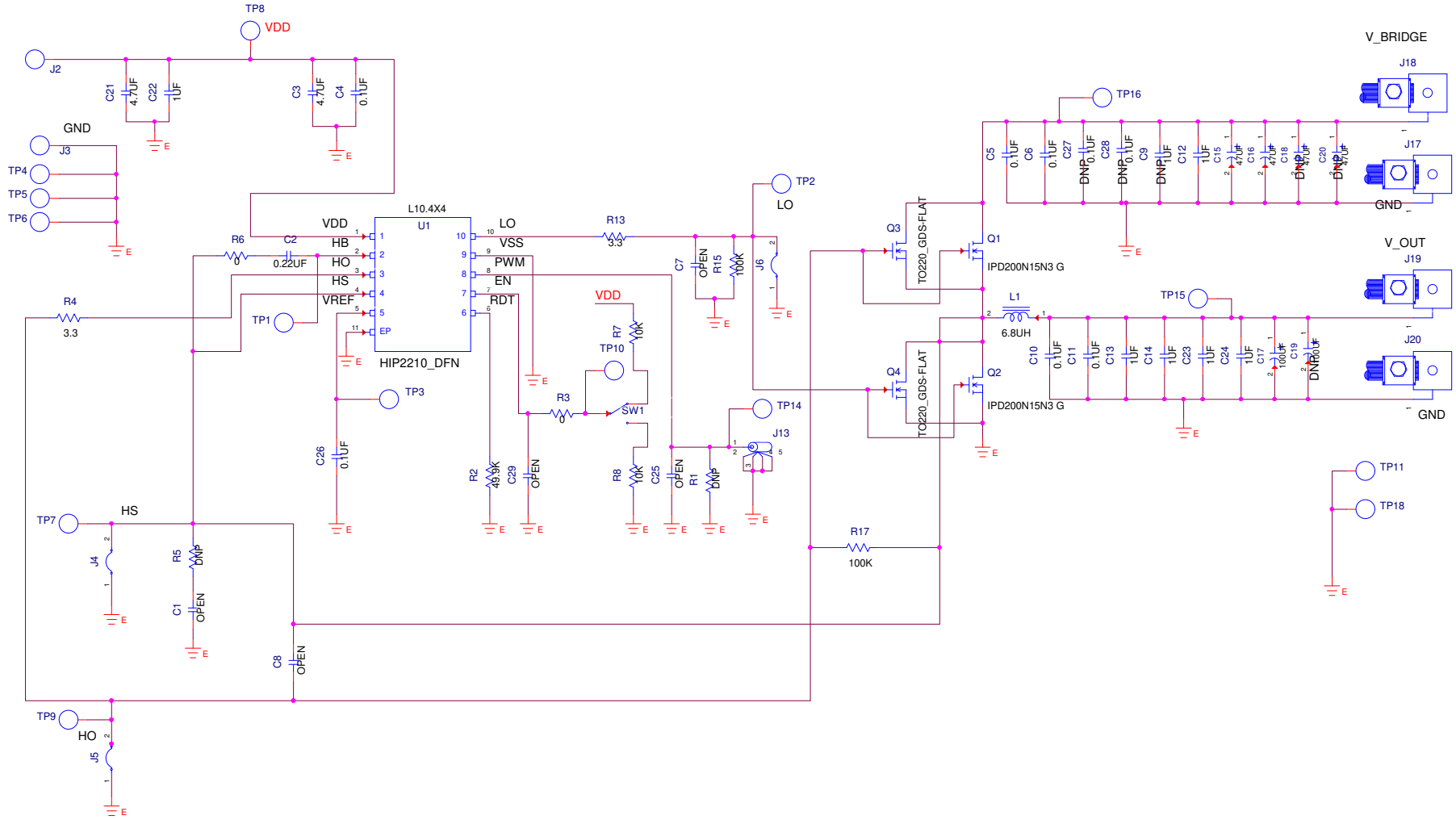

Figure 4. HIP2210EVAL1Z Schematic

2.3 Bill of Materials

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
1		PWB-PCB, HIP2210EVAL1Z, REVA, ROHS	IMAGINEERING INC	HIP2210EVAL1ZREVAPCB
2	C5, C6	CAP, SMD, 1210, 0.1µF, 200V, 20%, X7R, ROHS	KEMET	C1210C104K2RAC
1	C12	CAP, SMD, 2225, 1.0µF, 200V, 10%, X7R, ROHS	KEMET	C2225C105K2RAC7800
1	C26	CAP, SMD, 0603, 0.1µF, 16V, 10%, X7R, ROHS	MURATA	GCM188R71C104KA37D
1	C4	CAP, SMD, 0603, 0.1µF, 50V, 10%, X7R, ROHS	AVX	06035C104KAT2A
1	C2	CAP, SMD, 0603, 0.22µF, 50V, 10%, X7R, ROHS	MURATA	GCM188R71H224KA64D (AEC-Q200)
2	C10, C11	CAP, SMD, 0805, 0.1µF, 100V, 10%, X7R, ROHS	TDK	C2012X7R2A104K
1	C22	CAP, SMD, 0805, 1.0µF, 50V, 10%, X7R, ROHS	MURATA	GRM21BR71H105KA12L
4	C13, C14, C23, C24	CAP, SMD, 1210, 1.0µF, 100V, 10%, X7R, ROHS	VENKEL	C1210X7R101-105KNE
2	C3, C21	CAP, SMD, 1210, 4.7µF, 50V, 10%, X7R, ROHS	MURATA	GRM32ER71H475KA88L
3	J2, J3, TP3	CONN-TURRET, TERMINAL POST, TH, ROHS	KEYSTONE	1514-2
1	J13	CONN-BNC, RECEPTACLE, TH, 4 POST, 50Ω, SILVERCONTACT, ROHS	AMPHENOL	31-5329-51RFX
14	TP1, TP2, TP4-TP11, TP14, TP15, TP16, TP18	CONN-MINI TEST POINT, VERTICAL, WHITE, ROHS	KEYSTONE	5002
3	J4, J5, J6	CONN-HEADER, 1x2, RETENTIVE, 2.54mm, 0.230x 0.120, ROHS	BERG/FCI	69190-202HLF
1	L1	COIL-INDUCTOR, AEC-Q200, SMD, 16.9mm, 6.8µH, 20%, 19A, ROHS	BOURNS	SRP1770TA-6R8M
1	U1	IC-100V 4A HALF BRIDGE DRIVER, 10P, TDFN, 4x4, ROHS	RENESAS ELECTRONICS AMERICA	HIP2210FRTZ
2	Q1, Q2	TRANSIST-MOS, N-CHANNEL, SMD, 3P, TO-252-3, 150V, 50A, ROHS	INFINEON TECHNOLOGY	IPD200N15N3GATMA1
1	R6	RES, SMD, 0603, 0Ω, 1/10W, TF, ROHS	VENKEL	CR0603-10W-000T
2	R7, R8	RES, SMD, 0603, 10k, 1/10W, 1%, TF, ROHS	VENKEL	CR0603-10W-1002FT
2	R15, R17	RES, SMD, 0603, 100k, 1/10W, 1%, TF, ROHS	VENKEL	CR0603-10W-1003FT
1	R2	RES, SMD, 0603, 49.9k, 1/10W, 1%, TF, ROHS	VENKEL	CR0603-10W-4992FT
2	R4, R13	RES, SMD, 0805, 3.3Ω, 1/8W, 1%, TF, ROHS	PANASONIC	ERJ-6RQF3R3V
1	R3	RES, SMD, 0805, 0Ω, 1/8W, TF, ROHS	YAGEO	RC0805JR-070RL

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
1	SW1	SWITCH-TOGGLE, SMD, 6PIN, SPDT, 2POS, ON-NONE-ON, ROHS	ITT INDUSTRIES/C&K DIVISION	GT11MSCBE
4	Four corners	SCREW, 4-40x1/4in, PHILLIPS, PANHEAD, STAINLESS, ROHS	BUILDING FASTENERS	PMSSS 440 0025 PH
4	Four corners	STANDOFF, 4-40x3/4in, F/F, HEX, ALUMINUM, 0.25 OD, ROHS	KEYSTONE	2204
4	J17, J18, J19, J20	HDWARE, MTG, CABLE TERMINAL, 6-14AWG, LUG&SCREW, ROHS	BERG/FCI	KPA8CTP
1	C17	CAP, SMD, 12.5x16, 100µF, 100V, 20%, ALUM.ELEC., ROHS	NICHICON	UUG2A101MNQ1MS
2	C15, C16	CAP, SMD, 13.6mm, 47µF, 160V, 20%, ALUM.ELEC., ROHS	NICHICON	UUG2C470MNL1MS

2.4 Board Layout

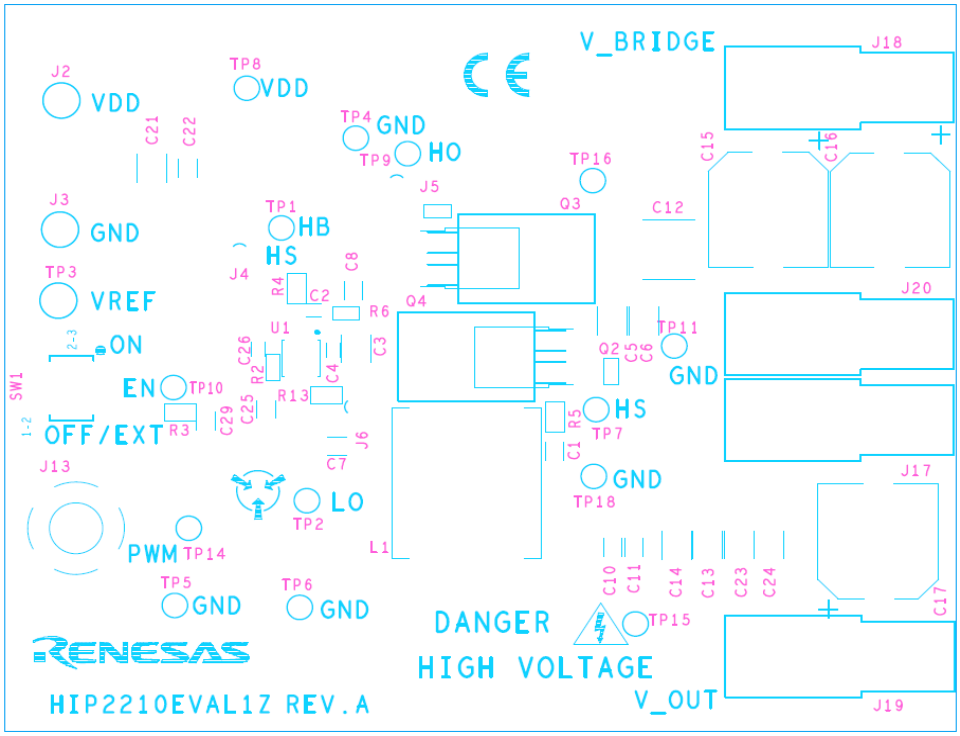

Figure 5. Silkscreen Top Layer

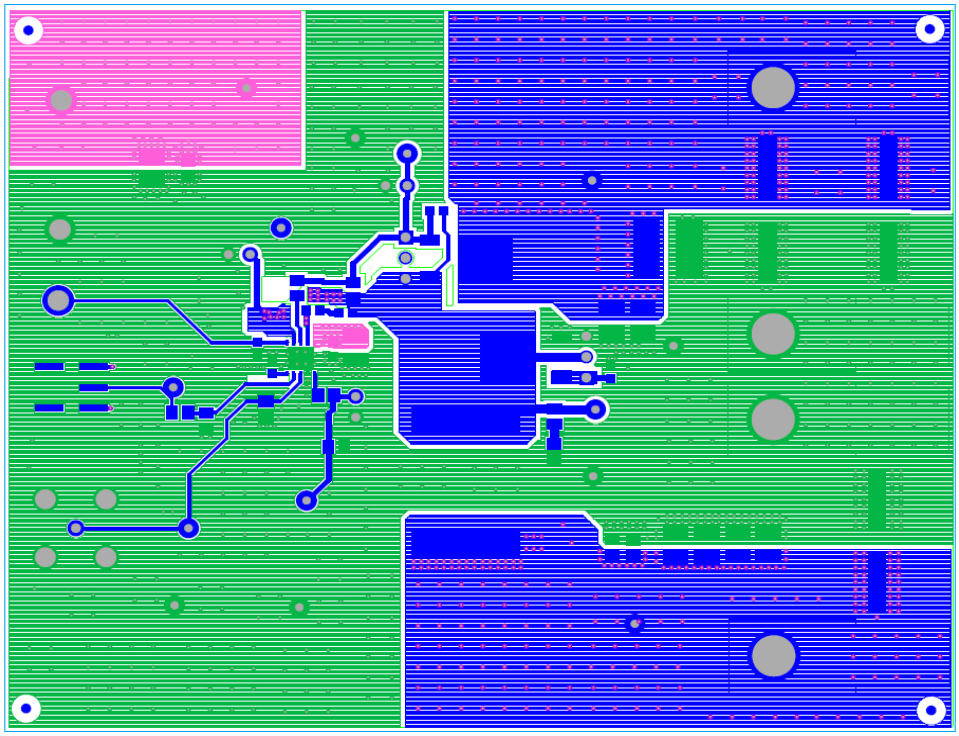

Figure 6. Layer 1

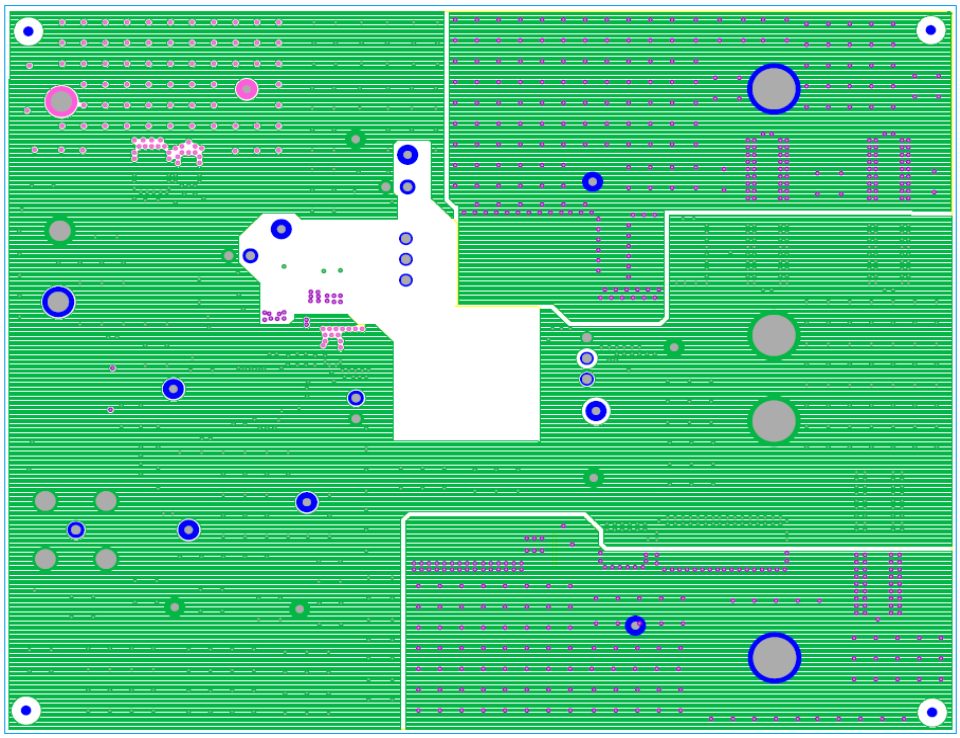

Figure 7. Layer 2

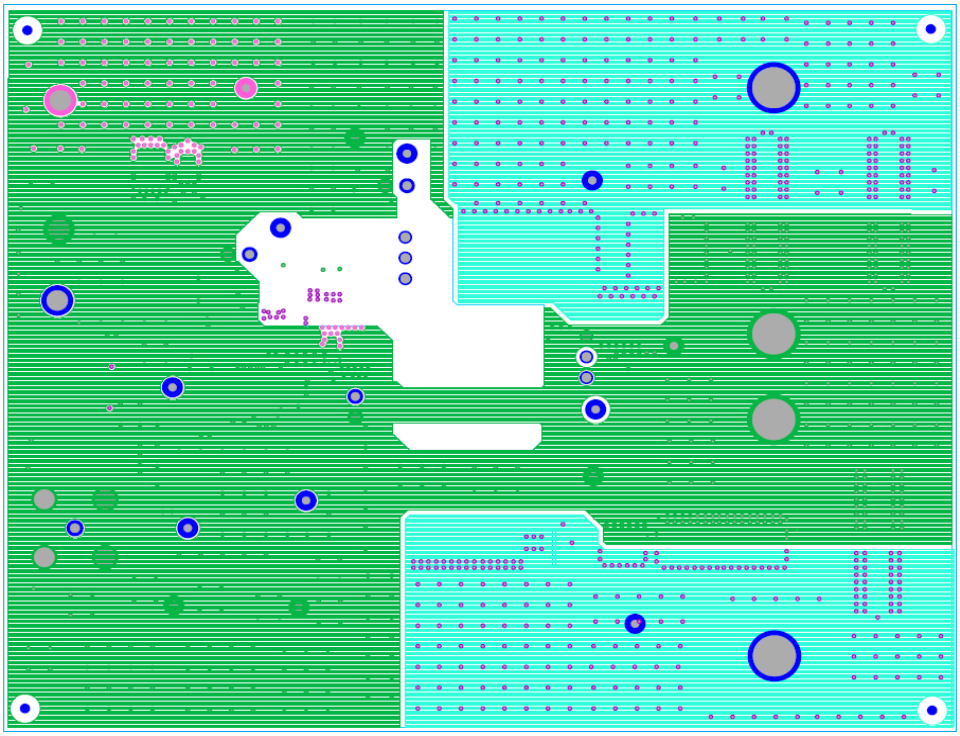

Figure 8. Layer 3

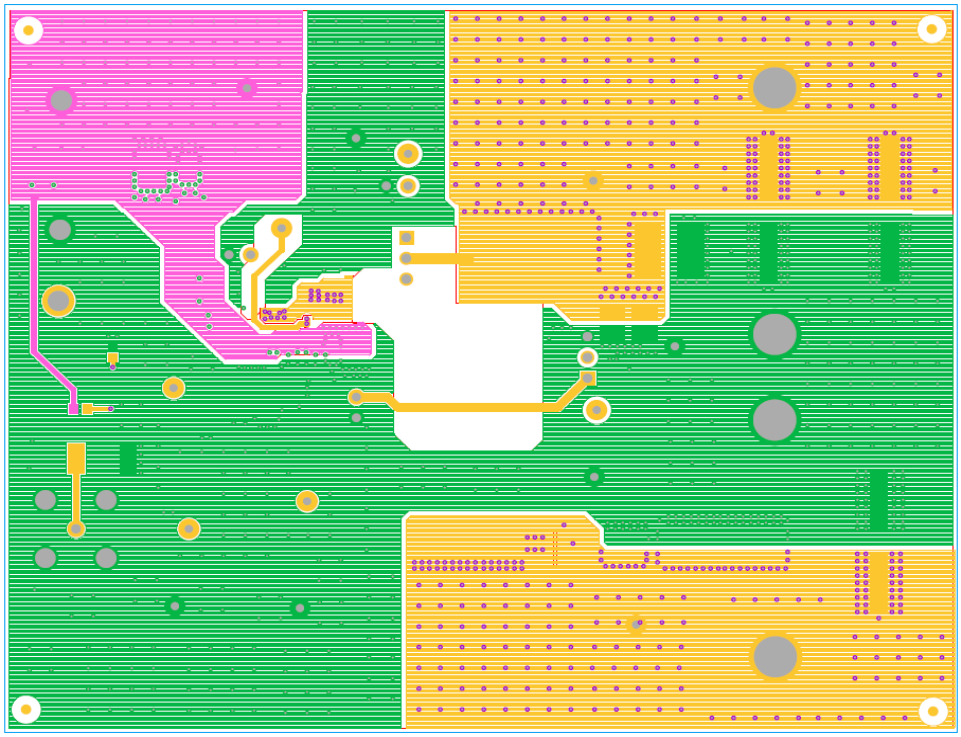

Figure 9. Layer 4

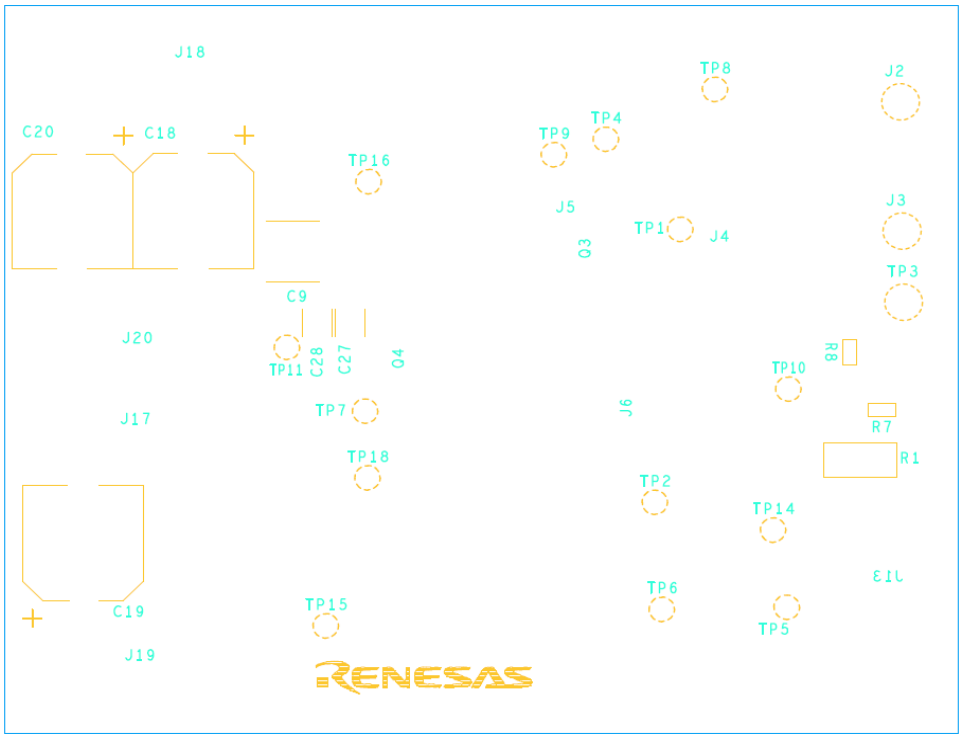

Figure 10. Silkscreen Bottom Layer

3. Typical Performance Curves

Unless noted: V_{DD} = 12V, V_{BRIDGE} = 48V, PWM = 100kHz square wave, 0V to 5V, 35% duty cycle, T_A = +25°C

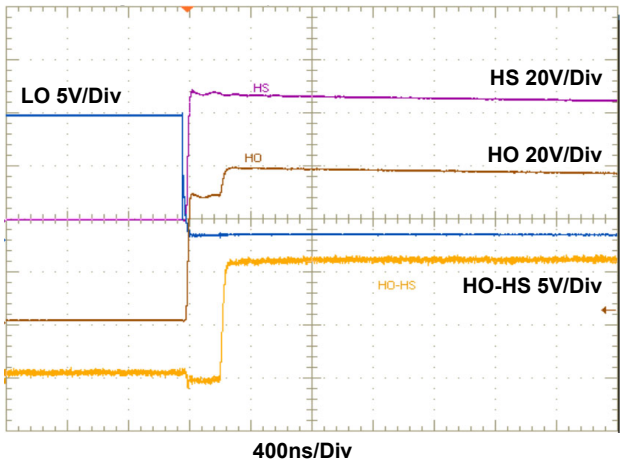

Figure 11. Dead Time LO Falling to HO Rising

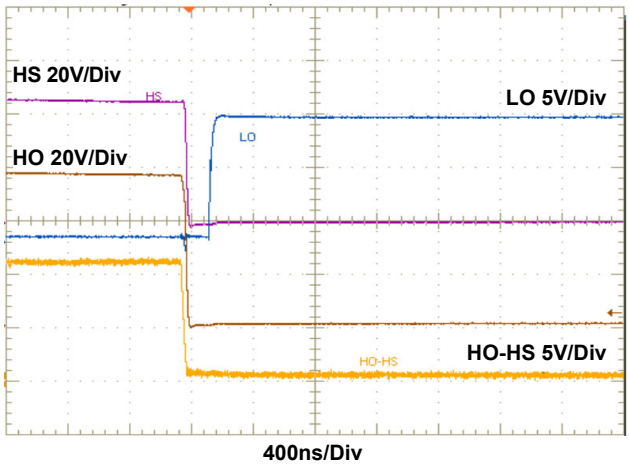

Figure 12. Dead Time HO Falling to LO Rising

4. Revision History

Rev.	Date	Description
1.00	Feb.11.20	Initial release

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