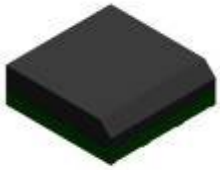
EVERLIGHT

Surface - Mount
I²C Digital Ambient Light Sensor

ALS-PDIC17-81B/TR8

Features



- Close to human eye spectral response.
- CMOS IC Technology.
- 20bits effective resolution.
- High dynamic sensing range from 0Lux to 10,500Klux.
- High resolution 0.04Lux/count. (ITIME=1275ms.)
- 50Hz/60Hz flicker rejection.
- Standard I²C protocol interface.
- Convert light intensity to digital data.
- Supply voltage 2.4V ~ 3.6V.
- Low-power consumption.
- Low shutdown current 1uA.
- Package size : 2.0mm x 2.0mm x 0.6mm.
- RoHS complaint & Pb Free.

Description

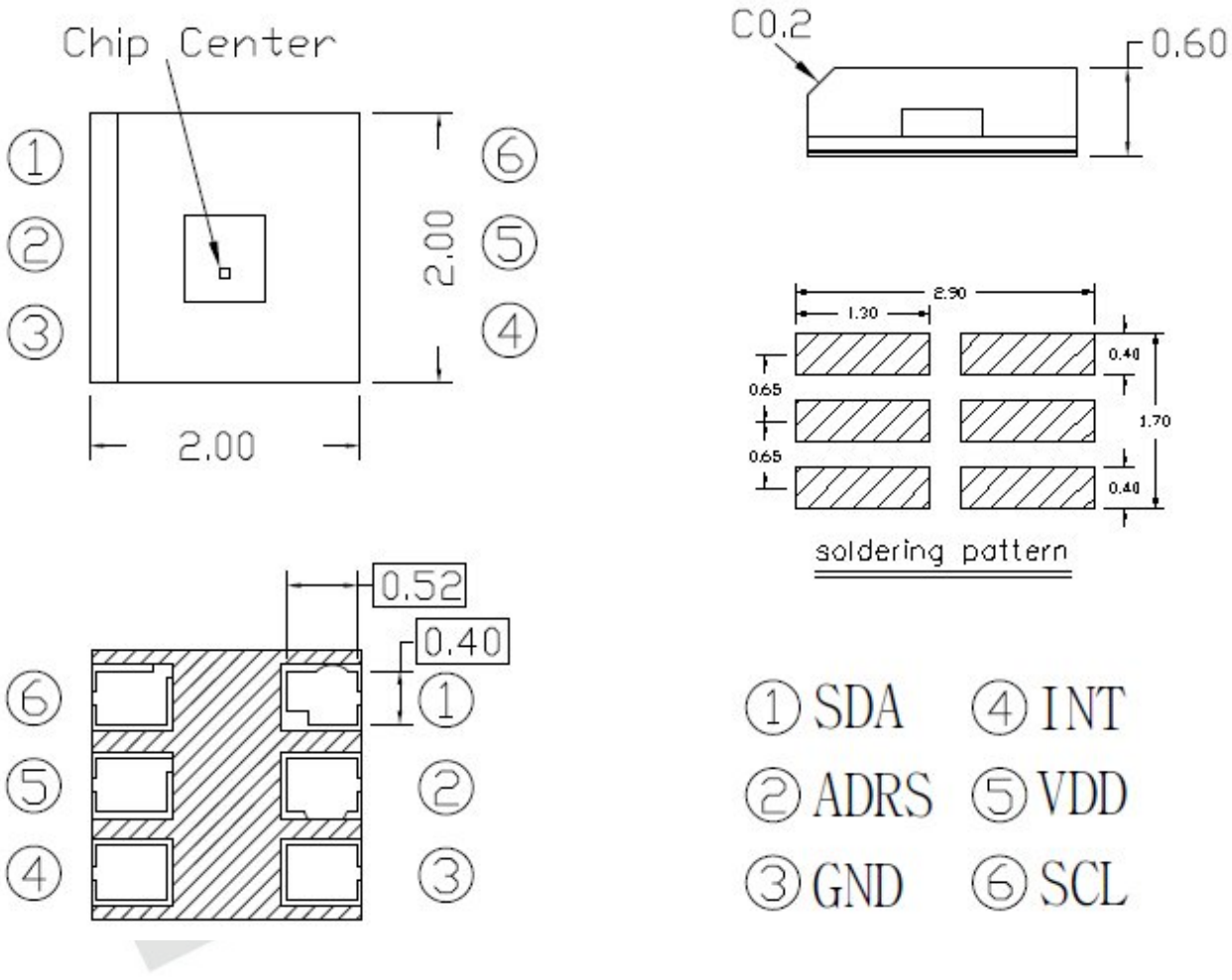
The ALS-PDIC17-81B is an advance digital output ambient light sensor (ALS) with I²C protocol interface that is compatible SMBus. The ALS-PDIC17-81B consists of a light shielded photodiode and an opened photodiode to improve the dark noise and provide an effective 20 bit dynamic range on a CMOS integrated circuit.

The ALS-PDIC17-81B has been coated IR-filter on package and best spectral response to be close to human eye of visible wavelength, software shutdown mode is provided which reduces power consumption to be less than 1uA and operation voltages from 2.4V to 3.6V, and the maximum detecting range is to 10,500KLux.

Applications

- Detection of ambient light for backlight dimming control of Digital LCD TV, tablet PC, Notebook PC,
  LCD Monitor, Navigation system and display-equipment.
- Automatic residential and commercial light management
- Automatic contrast enhancement for electronic signboard

Package Dimensions



Unit: mm
Tolerances: ±0.1mm

Pin Description

PIN NO	SYMBOL	FUNCTION
1	SDA	I²C Serial Data Line
2	ADRS	Address Select
3	GND	Ground
4	INT	Interrupt; Logic output
5	VDD	Power Supply
6	SCL	I²C Serial Clock Line

Absolute Maximum Ratings (Ta=25℃)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Storage temperature	T_{STG}	-40	85	°C
Operating temperature	T_{OPR}	-40	85	°C
Supply voltage	V_{DD}	0	4.0	V
Digital output voltage	V_O	-0.5	4.0	V
Digital output current	I_O	-1	20	mA
ESD tolerance, Human Body Model	HBM	8	-	KV

Block Diagram

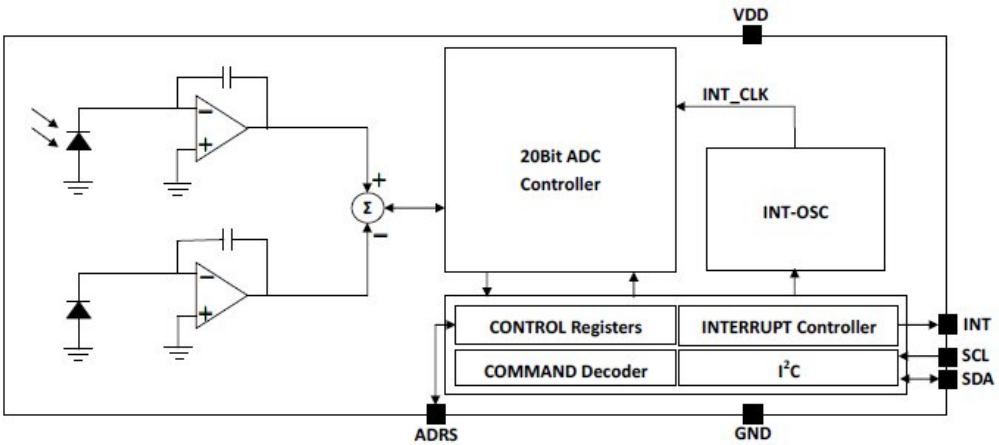


Figure 1 ALS-PDIC17-81B Functional Block Diagram

Electrical and Optical Characteristics (Ta=25℃, V_{DD}=3.3V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Power supply voltage	V_{DD}		2.4	-	3.6	V
I^2C Bus pin voltage	V_{Bus}		2.4	-	3.6	V
Supply Current	I_{DD1}	Normal mode	-	200	250	uA
	I_{DD2}	Fast mode	-	600	750	uA
Shutdown Current	I_{DDQ}	Power down		1	3	uA
I^2C output low voltage	V_{OL}	8mA sink current	0	-	0.4	V
High level input voltage	V_{IH}		V_{DD}*0.7	-	-	V
Low level input voltage	V_{IL}		-	-	V_{DD} *0.3	V
ADC integration/conversion time	t_{INT}	20-bit ADC data	-	100	1275	ms
Detection		Full scale	-	-	1048576	count
		ITIME= 100ms	-	526000	-	Lux
Peak sensitivity wavelength	λ_p		-	580	-	nm
Response in dark environment	R_{DARK}	Ev= 0Lux, ITIME= 100mS	-	-	1	counts
Response to incandescent lamp	R_{ICD}	Ev= 100Lux ITIME= 100mS	-	220	-	counts
Response to fluorescent lamp	R_{FRST1}	Ev= 100Lux ITIME= 100mS	120	180	240	counts
Response to fluorescent lamp	R_{FRST2}	Ev= 1000Lux ITIME= 100mS	1200	1800	2400	counts

Notice:

1. Fluorescent light (Color Temperature= 6500K) is used as light source. However, white LED is substituted in mass production.
2. Illuminance by CIE standard illuminant-A / 2856K, incandescent lamp.

Revision : 1
Release Date:2013-03-24 02:25:10.0
LifecyclePhase: 正式發行 Approved
Expired Period: Forever

I²C Characteristics

The following table and figure show the timing condition of SDA and SCL bus lines for fast mode I²C bus devices. NOTE1

(V_{DD}=5.0V±10%, GND=0V, T_{OPR}=-40~85°C)

PARAMETER	SYMBOL	MIN	MAX	UNIT
SCL clock frequency	f_{SCL}	0	400	KHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	$t_{HD;STA}$	0.6	-	us
Low period of SCL clock	t_{LOW}	1.3	-	us
High period of SCL clock	t_{HIGH}	0.6	-	us
Set-up time for a repeated START condition	$t_{SU;STA}$	0.6	-	us
Data hold time	$t_{HD;DAT}$	0	0.9	us
Data set-up time	$t_{SU;DAT}$	100	-	ns
Clock/data rise time	t_R	0	300	ns
Clock/data fall time	t_F	0	300	ns
Set-up time for STOP condition	$t_{SU;STO}$	0.6	-	us
Bus free time between STOP and START condition	t_{BUF}	1.3	-	us

NOTE1: All timing is shown with respect to 30% V_{DD} and 70% V_{DD}

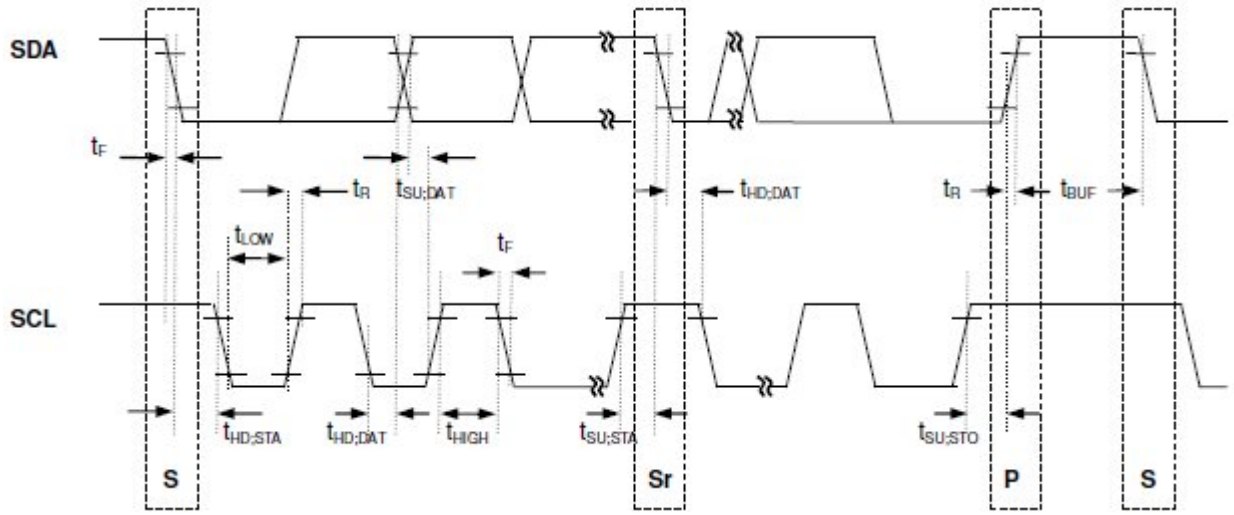


Figure 2 I²C Timing Diagram

Typical Electrical and Optical Characteristics Curves

Fig 3 Light Output vs. Illuminance

(Typ.)

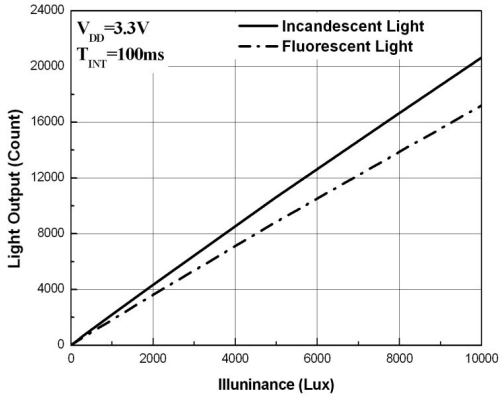


Fig 4 Current Consumption vs. Illuminance

(Typ.)

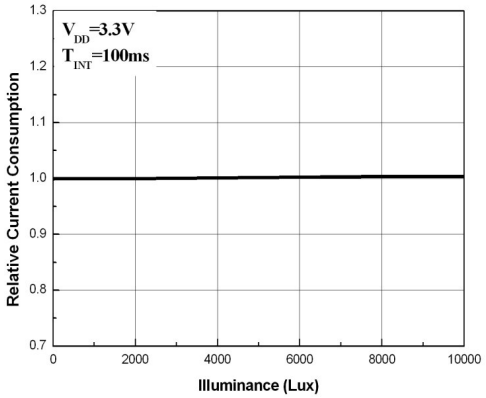


Fig 5 Current Consumption vs. Supply Voltage

(Typ.)

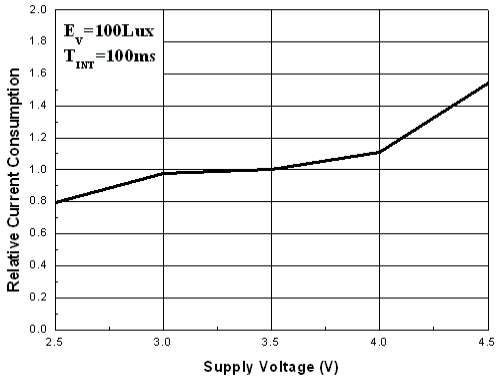


Fig 6 Light Output vs. Supply Voltage

(Typ.)

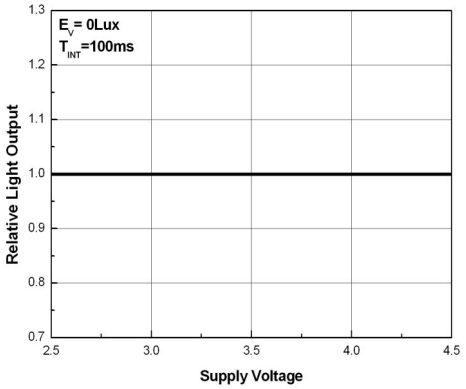


Fig 7 Light Output vs. Supply Voltage

(Typ.)

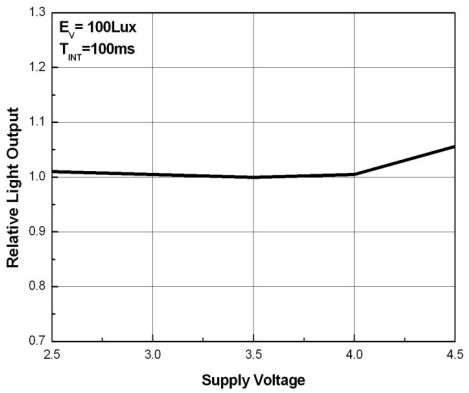


Fig 8 Current Consumption vs. Temperature

(Typ.)

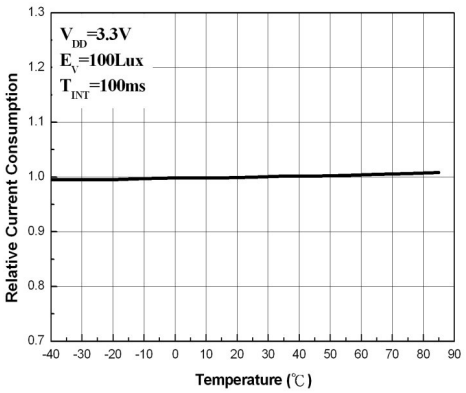


Fig 9 Light Output vs. Temperature

(Typ.)

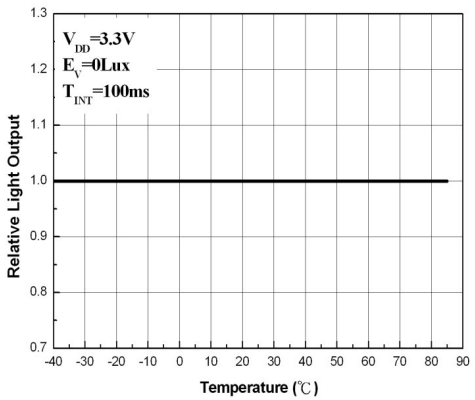


Fig 10 Light Output vs. Temperature

(Typ.)

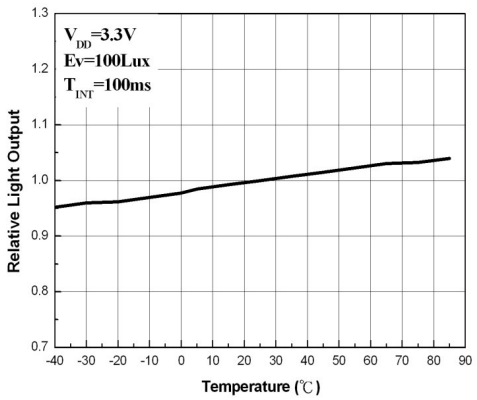


Fig 11 Spectrum

(Typ.)

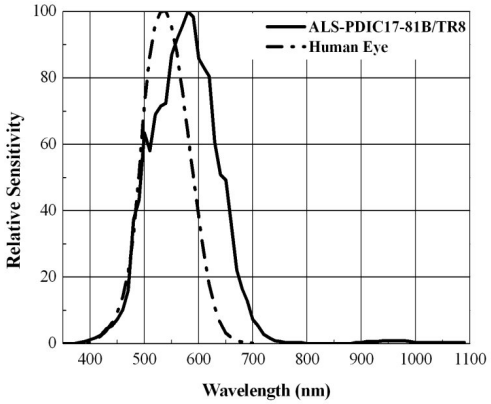
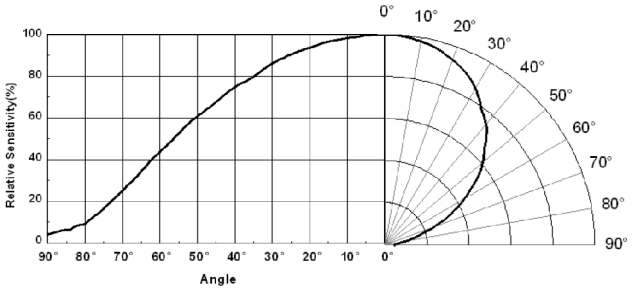


Fig 12 Relative Sensitivity vs. Angle

(Typ.)



Communication Protocol

1. I²C Protocol

1-1 Overview

The I²C is one of industrial standard serial communication protocols and which uses 2 bus lines Serial Data Line (SDA) and Serial Clock Line (SCL) to exchange data. Because both SDA and SCL lines are open-drain output, each line needs pull-up resistor. The features are as shown below,

- Compatible with I²C bus standard
- Up to 400KHz data transfer
- Support two 7-bits slave address
- Slave operation only

1-2 I²C Bit Transfer

The data on the SDA line must be stable during HIGH period of the clock (SCL). The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. The exceptions are START(S), repeated START(Sr) and STOP(P) condition where data line changes when clock line is high.

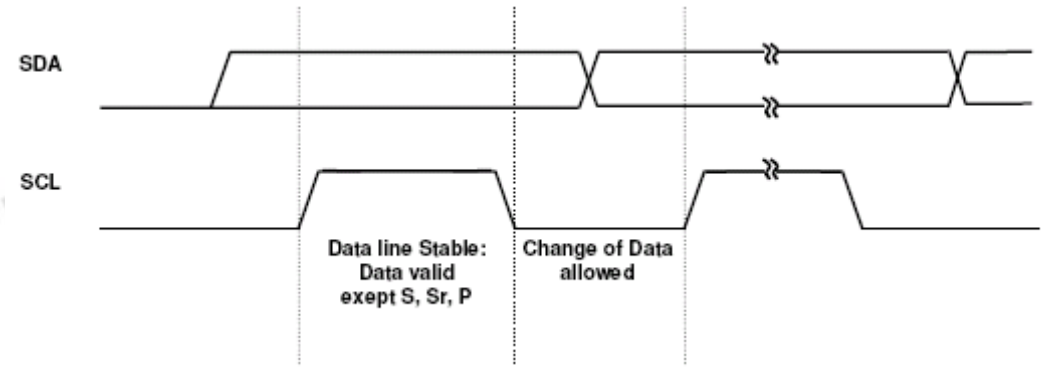


Figure 13 Bit Transfer on the I²C-Bus

1-3 Start/ Repeated Start/ Stop

One master can issue a START(S) condition to notice other devices connected to the SCL, SDA lines that is will use the bus. A STOP(P) condition is generated by the master to release the bus lines, so that other devices can use it.

A high to low transition on the SDA line while SCL is high defines a START (S) condition.

A Low to high transition on the SDA line while SCL is high defines a STOP (P) condition.

START and STOP conditions are always generated by a master. The bus is considered to be busy after START condition. The bus is considered to be free again after STOP condition, ie, the bus is busy between START and STOP condition. If a repeated START condition (Sr) is generated instead of STOP condition, the bus stays busy. So, the START and repeated START condition are functionally identical.

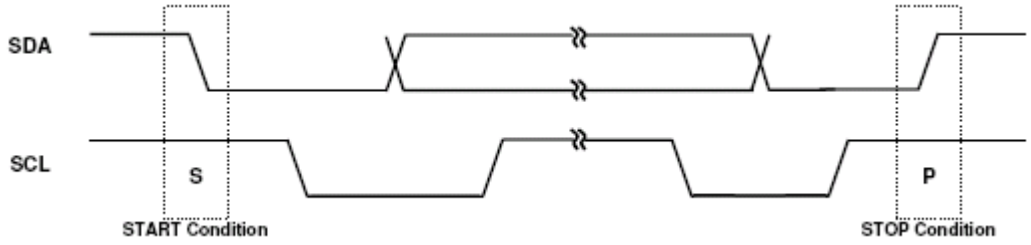


Figure 14 START and STOP Condition

1-4 Data Transfer

Every byte put on the SDA line must be 8-bits long. The number of bytes that can be transmitted per transfer is unlimited. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first. If a slave can't receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL LOW to force the master into a wait state. Data transfer then continues when the slave is ready for another byte of data and releases clock line SCL.

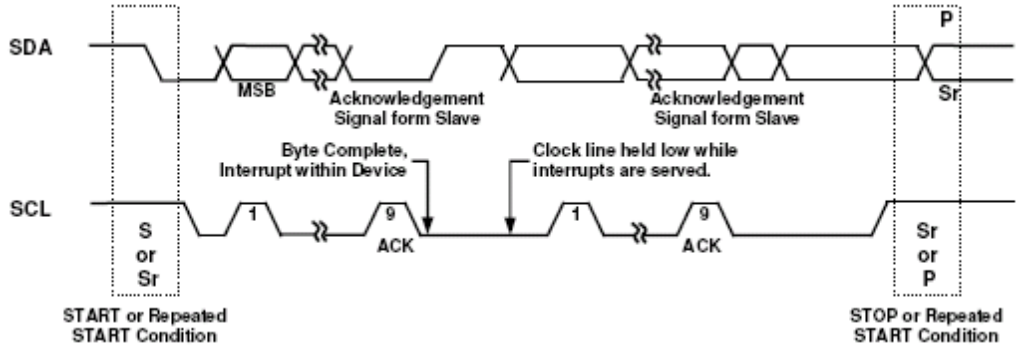


Figure 15 STOP or Repeated START Condition

1-5 Acknowledge

Acknowledge related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse. When a slave is addressed by a master (Address Packet), and if it's unable to receive or transmit because it's performing some real time function, the data line must be left HIGH by the slave else, when a slave addressed by a master is unable to receive more data bits, the slave receiver must release the SDA line (Data Packet). The master can then generate either a STOP condition to abort the transfer or a repeated START condition to start a new transfer.

If a master receiver is involved in a transfer, it must signal the end of data to the slave transmitter by not generating an acknowledge on the last byte that was clocked out of the slave. The slave transmitter must release the data line to allow the master to generate a STOP or repeated START condition.

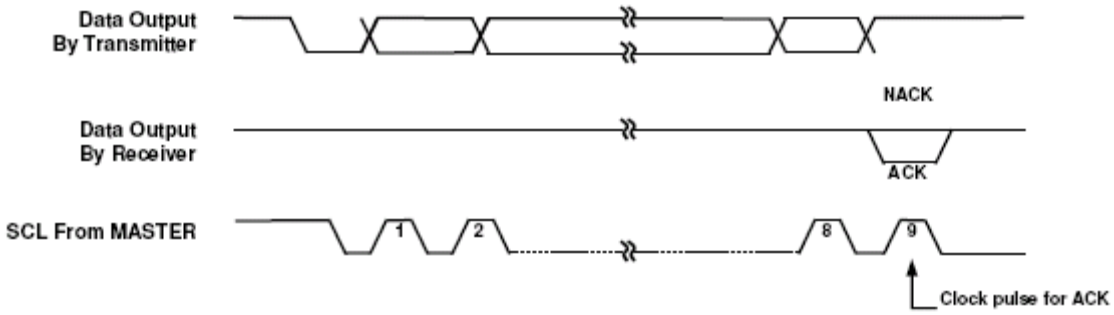


Figure 16 Acknowledge on the I²C Bus

1-6 Operation

The I²C is byte-oriented serial protocol and data transfer between master and this slave device is initiated by a start condition(S) from master. After start condition, the master sends 7-bits slave address and 1-bit read-write control bit. We call these 8-bits data address packet.

The next bytes followed by address packet are all data packet unless another start condition is detected before a stop condition. When a byte sent from master right after address packet with the most significant bit (MSB) equal to "1" will be interpreted as a COMMAND byte. The lower 5-bits of the COMMAND bytes from the register select address, which is used to select the destination for the subsequent bytes transferred.

The ALS-PDIC17-81B's I²C interface slave address is configured as "10101000" or "01010110" according to the input condition of ADRS pin.

Although I²C is byte-oriented and has no limit for number of data byte, we use "4" kinds of transfer protocol based on I²C standard. This is because there is no CPU in this device and consequently all controls like preparing data to be transmitted or handling data to be received are all treated by hardware. The 4 kinds of transfers are (1) Byte write Protocol (2) Byte Read Protocol (3) Multi Byte Write Protocol (4) Multi Byte Read Protocol.

The multi byte protocols are needed to select register address to be accessed. Note that multi byte protocol must have a COMMAND byte or the data byte to be transferred has no meaning.

1-6-1 Byte Write Protocol

The master transmits a start condition(S), slave address and Write bit. If the high 7-bits of address packet equal to the device's slave address, the ALS-PDIC17-81B acknowledges by pulling down the SDA line at the 9th SCL clock period. After address packet and acknowledge bit, the master transmits data to be written and sends a stop condition regardless of the acknowledged for the data.

The destination address for the data byte is "00_H" if no multi byte transfer is performed before or "predetermined address" by previously performed multi byte transfer. This applies to Byte Read Protocol also.

Cautions: When Byte Write Protocol is used, the MSB of data packet should be "0" or it will interpreted as a COMMAND byte and communication will not succeed.

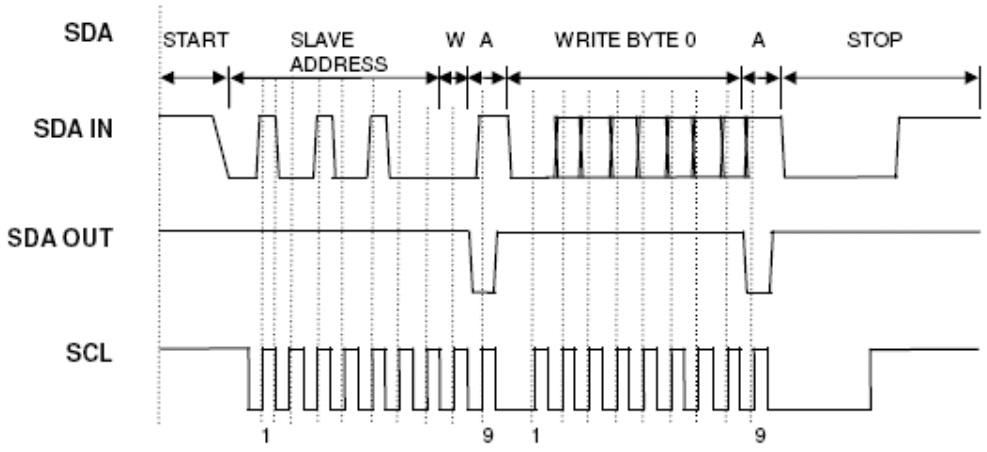


Figure 17 Byte Write Protocol

1-6-2 Byte Read Protocol

The master transmits a start condition(S), slave address and Read bit. If the high 7-bits of address packet equal to the device's slave address, the ALS-PDIC17-81B acknowledges by pulling down the SDA line at the 9th SCL clock period. After address packet and acknowledge bit, the ALS-PDIC17-81B transmits data and the master does not acknowledges by releasing the SDA line to send a stop condition and finish the transfer.

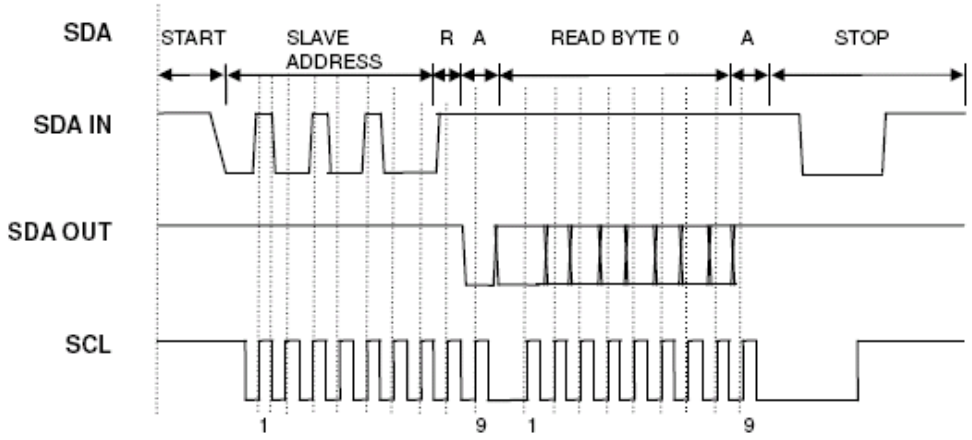


Figure 18 Byte Read Protocol

1-6-3 Multi Byte Write Protocol

The master transmits a start condition(S), slave address and Read bit. If the high 7-bits of address packet equal to the device's slave address, the ALS-PDIC17-81B acknowledges by pulling down the SDA line at the 9th SCL clock period. After address packet and acknowledge bit, the master transmits a data with MSB "1" to notify COMMAND byte. At 9th SCL clock, the base address for subsequent data transmit is defined. The master transmits a number of data to be written and the slave always acknowledges for every data received. To finish transfer the master sends a stop condition regardless of the acknowledgement.

The destination addresses for incoming data byte increments automatically by one data packet. For example, if master transmits 5 data bytes including a COMMAND byte and the base address (=command address) is configured as 03H, the internal address ids defined as 03_H for 1st data byte, 04_H for 2nd data byte, 05_H for 3rd data byte and 06_H for 4th data byte. This applies to Multi Byte Read Protocol also.

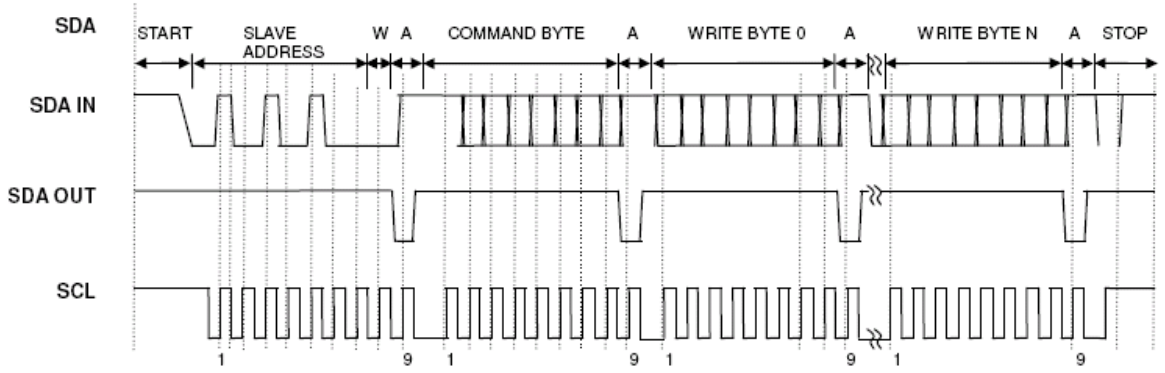


Figure 19 Multi Byte Write Protocol

1-6-4 Multi Byte Read Protocol

The master transmits a start condition(S), slave address and Read bit. If the high 7-bits of address packet equal to the device's slave address, the ALS-PDIC17-81B acknowledges by pulling down the SDA line at the 9th SCL clock period. After address packet and acknowledge bit, the master transmits a data with MSB "1" to notify COMMAND byte. At 9th SCL clock, the base address for subsequent data transmit is defined. To initiate read operations, the master sends repeated start condition and slave address with Read bit. After this address packet, the master reads data bytes until it does not acknowledge. Note that to send a stop condition after receiving last data byte, the master must generate a NACK (not acknowledging) on the last data byte received.

Note that transfer direction changes in this protocol.

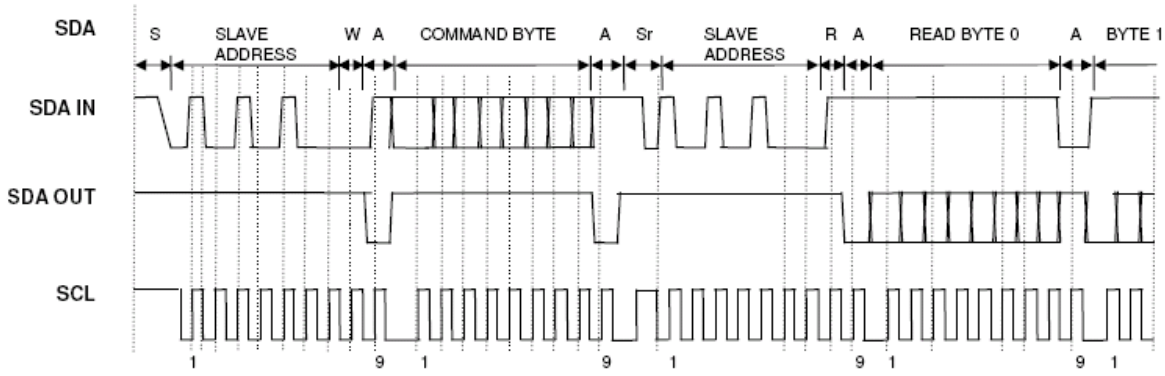


Figure 20 Multi Byte Read Protocol

2. Registers

2-1 Overview

The ALS-PDIC17-81B contains an eight bit registers accessed via the I²C bus, controlled and monitored by 13 registers. These registers provide a variety of control functions and can be read to determine results of the ADC conversion.

2-2 Register Description

ADRS	REG NAME	DIR	DESCRIPTION	RESET VALUE
–	COMMAND	W	Command Register	–
00_H	CONTROL	R/W	Control Register	00_H
01_H	INTR	R/W	Interrupt Control Register	00_H
02_H	ITIME	R/W	Integration Time Register	FF_H
03_H	THDL1	R/W	[7:0] 0~7 bit Thresholds Low Register	00_H
04_H	THDL2	R/W	[7:0] 8~15 bit Thresholds Low Register	00_H
05_H	THDL3	R/W	[3:0] 16~19 bit Thresholds Low Register	00_H
06_H	THDH1	R/W	[7:0] 0~7 bit Thresholds High Register	00_H
07_H	THDH2	R/W	[7:0] 8~15 bit Thresholds High Register	00_H
08_H	THDH3	R/W	[3:0] 16~19 bit Thresholds High Register	00_H
14_H	DATA1	R	[7:0] 0~7 bit Data Register	00_H
15_H	DATA2	R	[7:0] 8~15 bit Data Register	00_H
16_H	DATA3	R	[3:0] 16~19 bit Data Register	00_H

2-3 Salve Address

ALS-PDIC17-81B provides the address selective function for the system design convenience. The address can be defined by ADRS pin via high, low voltage and floating. In following table, it describes the salve address selection method and the cooperation with the command setting.

ADRS PIN	ID Address	COMMAND ADDRESS	OPERATION
PULL LOW	0xA8	0xA8	Write command
		0xA9	Read command
PULL HIGH	0x56	0x56	Write command
		0x57	Read command
FLOATING	0x34	0x34	Write command
		0x35	Read command

2-4 Function Description

ADRS	REG NAME	BIT								RESET VALUE
		7	6	5	4	3	2	1	0	
–	COMMAND	CMD	0	0	ADRS4	ADRS3	ADRS2	ADRS1	ADRS0	–
00_H	CONTROL	0	0	ADCIF	VALID	0	0	ADCEN	POWER	00_H
01_H	INTR	INTCLR	ONESHOT	0	0	PERSIST3	PERSIST2	PERSIST1	PERSIST1	00_H
02_H	ITIME	ITIME7	ITIME6	ITIME5	ITIME4	ITIME3	ITIME2	ITIME1	ITIME0	FF_H
03_H	THDL1	THDL7	THDL6	THDL5	THDL4	THDL3	THDL2	THDL1	THDL0	00_H
04_H	THDL2	THDL15	THDL14	THDL13	THDL12	THDL11	THDL10	THDL9	THDL8	00_H
05_H	THDL3	0	0	0	0	THDL19	THDL18	THDL17	THDL16	00_H
06_H	THDH1	THDH7	THDH6	THDH5	THDH4	THDH3	THDH2	THDH1	THDH0	00_H
07_H	THDH2	THDH15	THDH14	THDH13	THDH12	THDH11	THDH10	THDH9	THDH8	00_H
08_H	THDH3	0	0	0	0	THDH19	THDH18	THDH17	THDH16	00_H
14_H	DATA1	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	00_H
15_H	DATA2	DATA15	DATA14	DATA13	DATA12	DATA11	DATA10	DATA9	DATA8	00_H
16_H	DATA3	0	0	0	0	DATA19	DATA18	DATA17	DATA16	00_H

Revision : 1
Release Date:2013-03-24 02:25:10.0
LifecyclePhase: 正式發行 Approved
Expired Period: Forever

2-4-1 Command Register

7	6	5	4	3	2	1	0
CMD	0	0	ADRS4	ADRS3	ADRS2	ADRS1	ADRS0

Reset Value: –

1. CMD: Select command register. A Master must write "1" to this bit when addressing COMMAND register. The right after data byte after address packet can be COMMAND byte. Subsequent bytes are just data bytes.

BIT 7	OPERATION
0	1 Byte transfer is initiated by master.
1	Transaction is command.

2-4-2 Control Register (00hex)

00_H

7	6	5	4	3	2	1	0
0	0	ADCIF	VALID	0	0	ADCEN	POWER

Reset Value: 00_H

1. ADCIF: ADC Interrupt Flag; Bit 5. Indicates that the device is asserting an interrupt, read only.

BIT 5	OPERATION
0	Interrupt is cleared or not triggered.
1	Interrupt is triggered.

2. VALID: ADC Valid; Bit 4. This is ADC channel has completed an integration cycle, read only.

BIT 4	OPERATION
0	Integration cycle is ongoing or ADC is disabled.
1	Integration cycle elapsed.

3. ADCEN: Shutdown; Bit 1. This is enable ADC channel to begin integration.

BIT 1	OPERATION
0	Disable Photo Diode and ADC.
1	Enable Photo Diode and ADC.

4. POWER; Bit 0. This is for proper operation the bit must be enable prior to the ADCEN bit.

BIT 0	OPERATION
0	Turns off.
1	Turns on.

Revision : 1
Release Date:2013-03-24 02:25:10.0
LifecyclePhase: 正式發行 Approved
Expired Period: Forever

2-4-3 Interrupt Control Register (01hex)

01_H

7	6	5	4	3	2	1	0
INTCLR	ONESHOT	0	0	PERSIST3	PERSIST2	PERSIST1	PERSIST0

Reset Value: 00_H

1. INTCLR: Clears Interrupt; Bit 7.

BIT 7	OPERATION
0	No operation.
1	Clear ADC interrupt pending, it's auto-cleared.

2. ONESHOT: Stop ADC integration on interrupt; Bit 6.

BIT 6	OPERATION
0	Continuous operation.
1	Once an interrupt is asserted, ADC integration will stop and also the ADCEN bit in CONTROL register is to be cleared. To resume operation 1st clear interrupt flag by setting INTCLR bit in this register, 2nd re-assert ADCEN.

3. PERSIST[3:0]: Interrupt persistence; These bit field control the rate of interrupt request to host chip

BITS [3:0]	OPERATION	BITS [3:0]	OPERATION
0000	Every cycle generates interrupt.	1000	8 integration time periods range.
0001	Any value outside of threshold range.	1001	9 integration time periods range.
0010	2 integration time periods range.	1010	10 integration time periods range.
0011	3 integration time periods range.	1011	11 integration time periods range.
0100	4 integration time periods range.	1100	12 integration time periods range.
0101	5 integration time periods range.	1101	13 integration time periods range.
0110	6 integration time periods range.	1110	14 integration time periods range.
0111	7 integration time periods range.	1111	15 integration time periods range.

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2-4-4 Integration Time Control Register (02hex)

02_H

7	6	5	4	3	2	1	0
ITIME7	ITIME6	ITIME5	ITIME4	ITIME3	ITIME2	ITIME1	ITIME0

Reset Value: FF_H

ITIME[7:0]: Specifics the integration time in 5.0ms intervals.

Integration time= 5ms x ITIME[7:0]

BITS [7:0]	REFRESH TIMING TABLE	BITS [7:0]	REFRESH TIMING TABLE
00_H	Invalid.	14_H	100ms.
01_H	5ms.	28_H	200ms.
02_H	10ms.	50_H	400ms.
04_H	20ms.	78_H	600ms.
$0A_H$	50ms.	FF_H	1275ms.

ITIME	MAX DETECT RANGE	LUX/COUNT
50ms	1052KLux	1.006
100ms	526KLux	0.503
200ms	263KLux	0.252
400ms	131KLux	0.126
600ms	87.6KLux	0.084
800ms	65.7KLux	0.063
1275ms	41.2KLux	0.04

Resolution & Max Detect Range Comparison Table

Revision : 1
Release Date:2013-03-24 02:25:10.0
LifecyclePhase: 正式發行 Approved
Expired Period: Forever

2-4-5 Interrupt Threshold Register (03, 04, 05, 06, 07 and 08hex)

03_H

7	6	5	4	3	2	1	0
THDL7	THDL6	THDL5	THDL4	THDL3	THDL2	THDL1	THDL0

Reset Value: 00_H

04_H

7	6	5	4	3	2	1	0
THDL15	THDL14	THDL13	THDL12	THDL11	THDL10	THDL9	THDL8

Reset Value: 00_H

05_H

7	6	5	4	3	2	1	0
0	0	0	0	THDL19	THDL18	THDL17	THDL16

Reset Value: 00_H

06_H

7	6	5	4	3	2	1	0
THDH7	THDH6	THDH5	THDH4	THDH3	THDH2	THDH1	THDH0

Reset Value: 00_H

07_H

7	6	5	4	3	2	1	0
THDH15	THDH14	THDH13	THDH12	THDH11	THDH10	THDH9	THDH8

Reset Value: 00_H

08_H

7	6	5	4	3	2	1	0
0	0	0	0	THDH19	THDH18	THDH17	THDH16

Reset Value: 00_H

An interrupt event (ADCIF) is governed by the high and low thresholds in register 03, 04, 05, 06, 07 and 08hex (THDL1, THDL2, THDL3, THDH1, THDH2 and THDH3). The store value to be used as the high and low trigger points for the DATA registers 14, 15 and 16hex crosses below or equal to the low or high threshold specified.

Note: These low and high threshold registers are 20bit wide.

2-4-6 ADC Data Register (14, 15 and 16Hex)

14_H

7	6	5	4	3	2	1	0
DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Reset Value: 00_H

15_H

7	6	5	4	3	2	1	0
DATA15	DATA14	DATA13	DATA12	DATA11	DATA10	DATA9	DATA8

Reset Value: 00_H

16_H

7	6	5	4	3	2	1	0
0	0	0	0	DATA19	DATA18	DATA17	DATA16

Reset Value: 00_H

The ADC included in ALS-PDIC17-81B has 20bit resolution and the integrated values appear on three register DATA1, DATA2 and DATA3 respectively. All ADC data registers are read only and default to 00_H on power up.

3. Application Information

3-1 Software

After applying V_{DD}, the device will initially in the power down mode. To operate the device, issue a command to access the CONTROL register followed by the data value 01_H to the CONTROL register to power up the device. The ITIME register should be configured for the preferred integration time, and then the ADCEN bit in CONTROL register should be set to 1 to enable ADC channel.

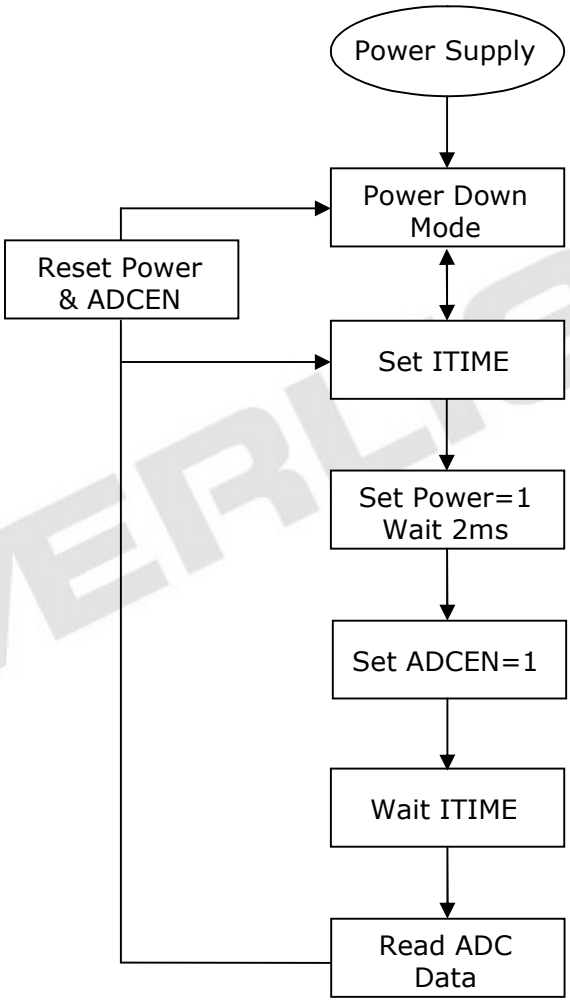


Figure 21 Operating Modes

The below explains matters to be attended to when customer develops a program for ALS-PDIC17-81B.

1. Operation Voltage 2.4 to 3.6V.

2. Set slave address (ADRS pin)
Pull Low: Write command: 0xA8, Read command: 0xA9.
Pull High: Write command: 0x56, Read command: 0x57.
Floating: Write command: 0x34, Read command: 0x35.

3. I²C speed is the standard, about 100kHz.
When writing I²C Multi bytes. (Single byte read and write rarely is used.)

Multi bytes Writing:
START(M)+SlaveAddress_W(0xA8,M)+ACK(S)+COMMAND(0x80,M)+ACK(S)+WRITE_BYTE0+ACK(S)…+STOP(M)
For example, When ADRS pin is low and want to write 0x33 in CONTROL (00_H) Register, it should follow the sequence.
START+0xA8+ACK+0x80+ACK+0x33+ACK+STOP

When reading I²C Multi bytes.
Multi bytes reading:
START(M)+SlaveAddress_W(0xA8,M)+ACK(S)+COMMAND(0x80,M)+ACK(S)+START+SlaveAddress_R(0xA9,M)+ACK(S)+READ_BYTE0(S)+ACK(M)…+NACK+STOP(M)
For example, when ADRS pin is low and want to read values of ADC Data (address 14H~16H) register, it should follow the below sequence.
START+0xA8+ACK+0x94+ACK+START+0xA9+ACK+DATA1+ACK+…+NACK+STOP

After sending I²C Read/Write command, delay time needs about 2ms for protocol transferring.

3-2 Application Circuit

ALS-PDIC17-81B is a Ambient Light Sensor (ALS) with I²C bus interface. The standard serial digital interface is easy to access. Adding a 0.1uF capacitor should be close to VDD pin for power supply noise rejection. The hardware design is shown in Figure 21. The pull up resister of two line serial bus "SCL" and "SDA" are recommended to be around 4.7Kohm, the pull up resistor for "INT" connected to Micro controller must be 100Kohm. The Pull up Voltage of "SCL", "SDA" and "INT" has to be the same as supply Voltage of ALS-PDIC17-81B.

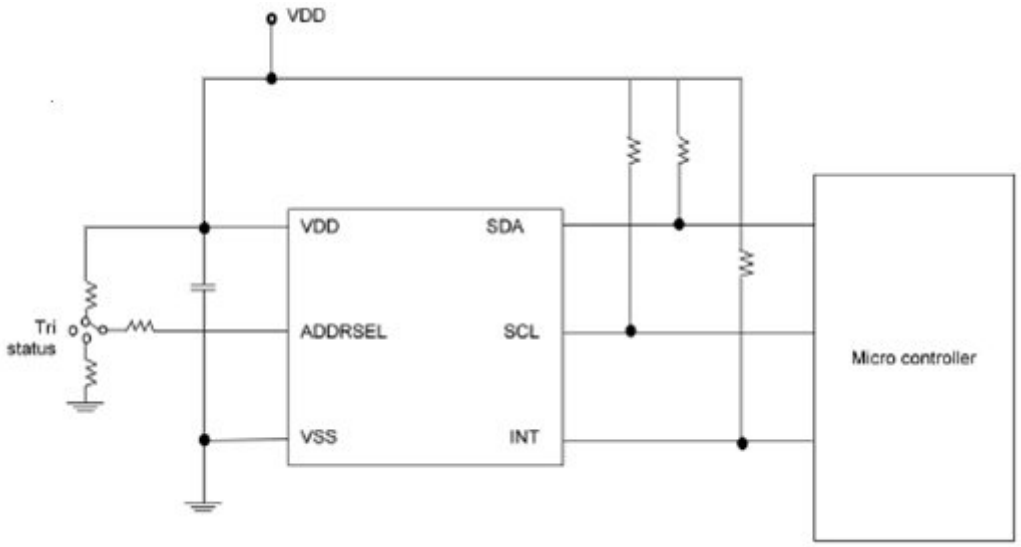
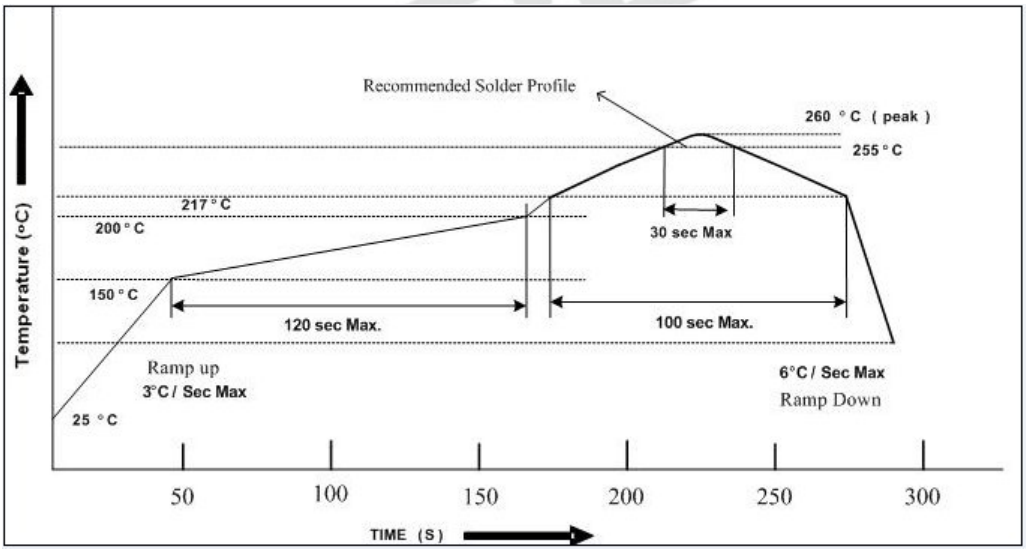


Figure 22 Application Circuit

Recommended method of storage

1. Do not open moisture proof bag before devices are ready to use.
2. Shelf life in sealed bag from the bag seal date:
   18 months at 10°C~30°C and < 90% RH.
3. After opening the package, the devices must be stored at 10°C~30°C and ≤ 60%RH, and used within 168 hours (floor life).
4. If the moisture absorbent material (desiccant material) has faded or unopened bag has exceeded the shelf life or devices (out of bag) have exceeded the floor life, baking treatment is required.
5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure or recommend the following conditions:
   192 hours at 40°C +5/−0°C and < 5 % RH (reeled/tubed/loose units) or
   96 hours at 60°C ± 5°C and < 5 % RH (reeled/tubed/loose units) or
   24 hours at 125°C ± 5°C, not suitable for reel or tubes.

Recommended Solder Profile



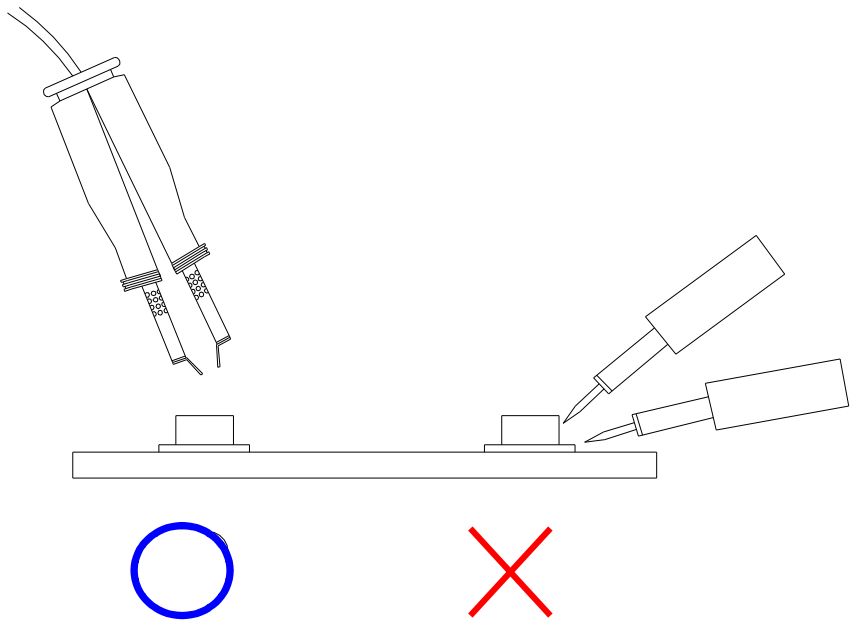
Notice:
1. Reflow soldering should not be done more than two times.
2. When soldering, do not put stress on the devices during heating.
3. After soldering, do not warp the circuit board.

Soldering Iron

Each terminal is to go to the tip of soldering iron temperature less than 350℃ for 3 seconds within once in less than the soldering iron capacity 25W. Leave two seconds and more intervals, and do soldering of each terminal. Be careful because the damage of the product is often started at the time of the hand solder.

Repairing

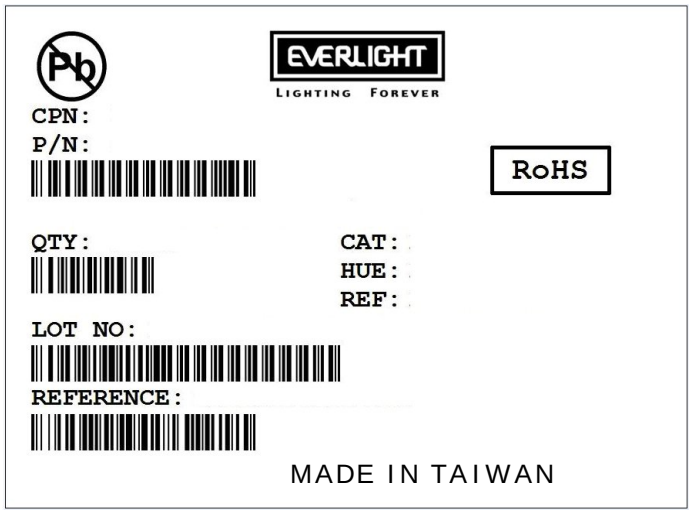
Repair should not be done after the device have been soldered. When repairing is unavoidable, a double-head soldering iron should be used (as below figure). It should be confirmed beforehand whether the characteristics of the device will or will not be damaged by repairing.



Packing Quantity Specification

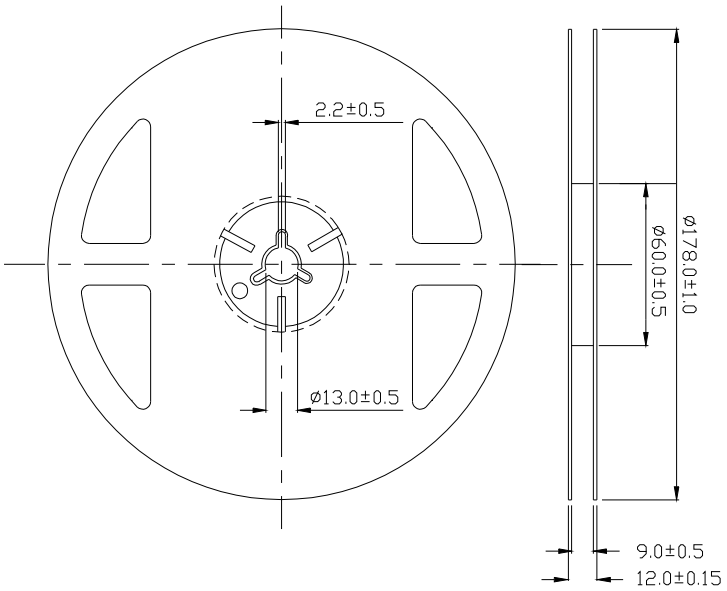
2000 PCS/ 1 Reel

Label Format



CPN: Customer's Production Number
P/N : Production Number
QTY: Packing Quantity
CAT: Ranks
HUE: Peak Wavelength
REF: Reference
LOT No: Lot Number
MADE IN TAIWAN: Production place

Reel Dimensions

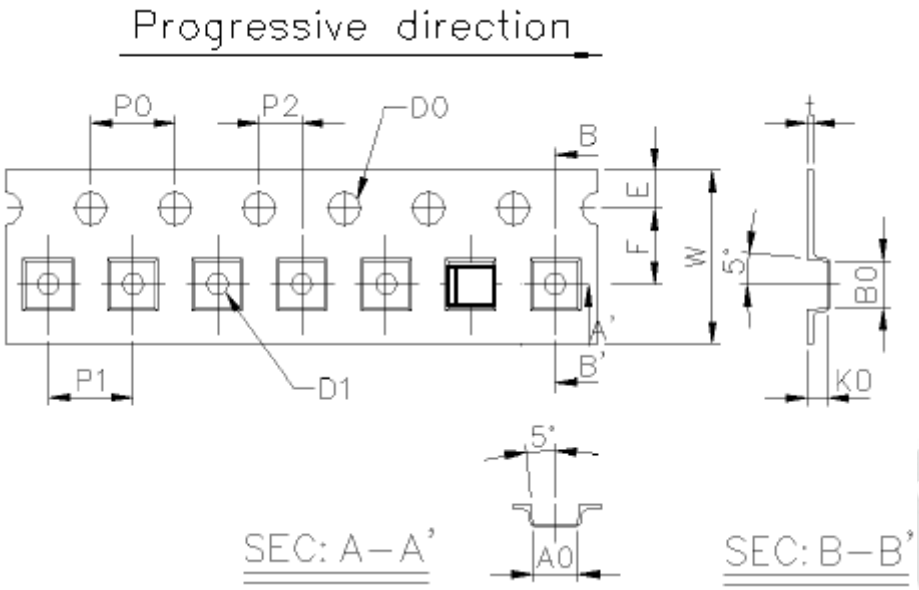


Unit: mm

Tolerance: ± 0.1mm

Revision : 1
LifecyclePhase: 正式發行 Approved
Release Date:2013-03-24 02:25:10.0
Expired Period: Forever

Tape Dimensions



Note:

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