PRODUCT/PROCESS CHANGE NOTIFICATION

PCN MMS-MMY/12/7312
Notification Date 06/05/2012

Improved design in CMOSF8H process for the M24256, 256 Kbit Serial I2C bus EEPROM / industrial range

Table 1. Change Implementation Schedule

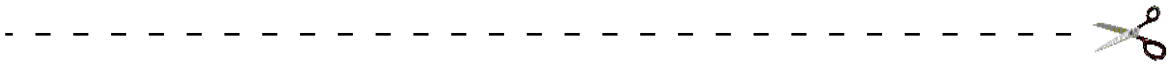
Forecasted implementation date for change	29-May-2012
Forecasted availabillity date of samples for customer	29-May-2012
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	29-May-2012
Estimated date of changed product first shipment	04-Sep-2012

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	M24256 products family
Type of change	Product design change
Reason for change	Line up to state of art of design
Description of the change	Improved design of the CMOSF8H Process Technology
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	Process ID is "8" for Improved F8H design
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN MMS-MMY/12/7312**
Please sign and return to STMicroelectronics Sales Office	**Notification Date 06/05/2012**

☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
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Malbranche, Jean-Luc	Division Q.A. Manager

PRODUCT / PROCESS CHANGE NOTIFICATION

Improved design in CMOSF8H process for the M24256, 256 Kbit Serial I2C bus EEPROM / industrial range

What is the change?

The **M24256, 256 Kbit Serial I²C bus EEPROM** product family currently produced using the CMOSF8H process technology at ST Rousset (France) 8 inch wafer diffusion plant will undergo through an **improved design** leading to a die size reduction (more compact layout).
The M24256 with the improved design is functionally compatible to the current CMOSF8H version, as per datasheet (rev. 25 – November 2011, here attached).

Concurrent to this change, the following production rationalization will follow:

- SO8N (Narrow, 150 mils) assembled on SHD line at ST Shenzhen will use 0.8 mil Copper wire (as introduced in PCN MMS-MMY/11/6929).
- MLP 2x3 (UFDFPN) will change from small exposed pad (package code “MB”) to large exposed pad (package code “MC”), PTN will be released in 2h/2012.
- WLCSP (Wafer Level Chip scale Package) M24256-BRCS6TP/A will be stopped and replaced by end 2012. PTN will be released in 2h/2012.

(See Appendix B for list of Commercial Part numbers)

Why?

The strategy of STMicroelectronics Memory Division is to support our customers on a long-term basis. In line with this commitment, the qualification of the improved design on the M24256 will increase the production capacity throughput and consequently improve the service to our customers.

When?

The production of the M24256 with the improved design will ramp up from June 2012 and shipments can start from August 2012 onward (or earlier upon customer approval).

How will the change be qualified?

The M24256 with the improved design will be qualified using the standard ST Microelectronics Corporate Procedures for Quality and Reliability.
The **Qualification Report QRMMY1124** is included inside this document.

What is the impact of the change?

- Form: marking change: refer to **Device marking** paragraph
- Fit: no change
- Function: no change

How can the change be seen?

- ***BOX LABEL MARKING***

On the BOX LABEL MARKING, the difference is visible inside the **Finished Good Part Number**: The **Mask revision** identifier is "**B**" for the CMOSF8H **improved design** version, this identifier being "A" for the current CMOSF8H version.

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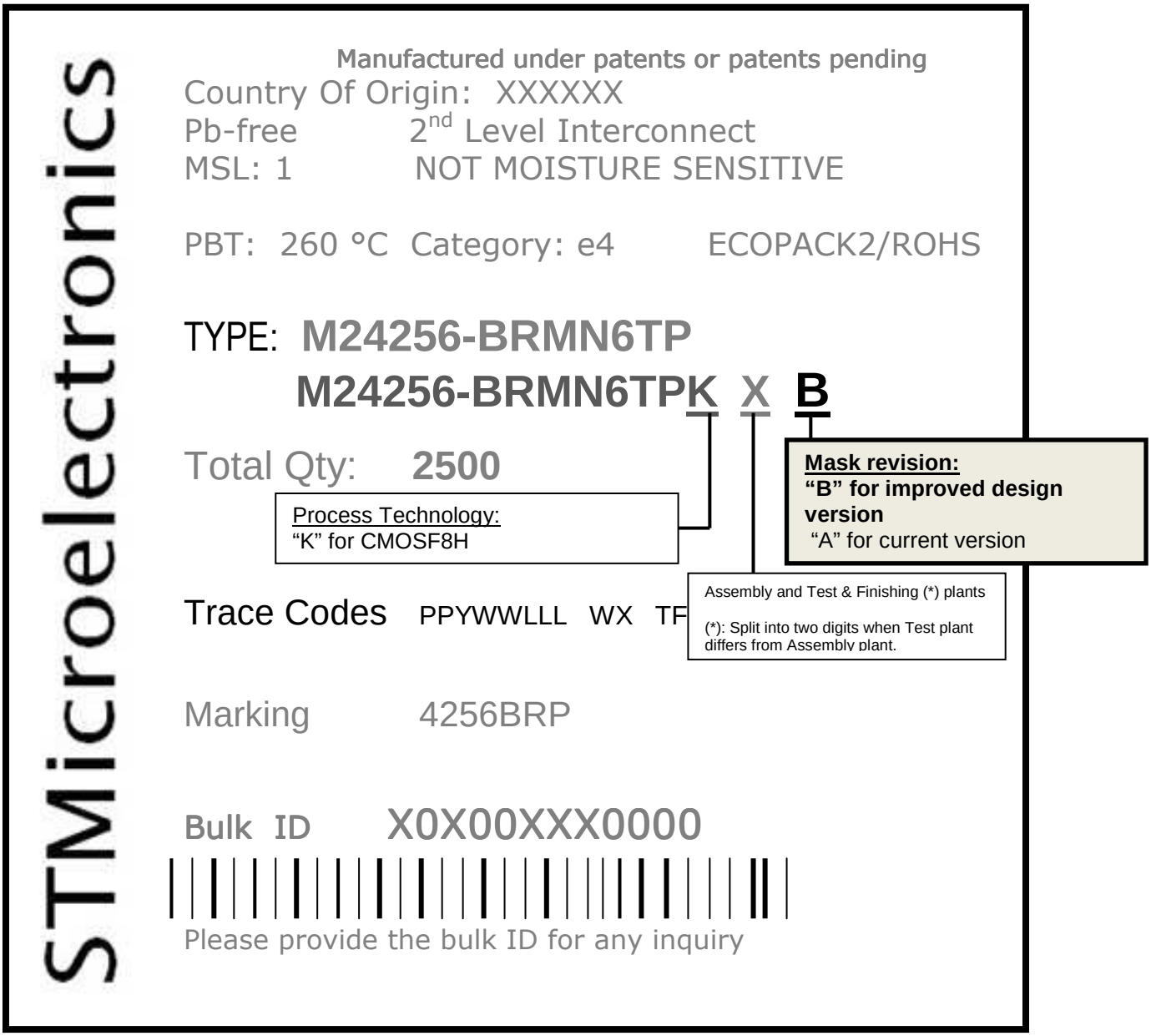
➔ *Example for M24256-BRMN6TP*



How can the change be seen?

- DEVICE MARKING

On the DEVICE MARKING of the **SO8N** package, the difference is visible inside the trace code (PYWWT) where the last digit "T" for **Process Technology identifier** is "**8**" for the **improved design** version, this identifier being "K" for the current CMOSF8H version.

	Improved Design CMOSF8H (Rev. B)	Current CMOSF8H (Rev. A)
SO8N Example: M24256-BRMN6TP	4256BRP PYWW**8**	4256BRP PYWW**K**

Legend:

P = Assembly plant
Y = Year of Assembly last digit
WW = Assembly Week
T = Process Technology code / Wafer Fab ID

For **TSSOP8**, the difference is visible inside the product name: **improved design** version is ending by "**8**", the current version being ended by "K".

	Improved Design CMOSF8H (Rev. B)	Current CMOSF8H (Rev. A)
TSSOP8 Example: M24256-BRDW6TP	456R**8** PYWW	456R**K** PYWW

Legend:

P = Assembly plant
Y = Year of Assembly last digit
WW = Assembly Week

For **MLP 2x3**, the difference is visible inside the product name: **improved design** version is ending by "**8**", the current version being ended by "K".

	Improved Design CMOSF8H (Rev. B)	Current CMOSF8H (Rev. A)
MLP 2x3 Example: M24256-BFMC6TG	456**8** PYWW	456**K** PYWW

Legend:

P = Assembly plant
Y = Year of Assembly last digit
WW = Assembly Week

Appendix A- Product Change Information

Product family / Commercial products:	M24256 products family
Customer(s):	All
Type of change:	Product design change
Reason for the change:	Line up to state of art of design
Description of the change:	Improved design of the CMOSF8H Process Technology.
Forecast date of the change: (Notification to customer)	Week 22 / 2012
Forecast date of Qualification samples availability for customer(s):	See details in next page
Forecast date for the internal STMicroelectronics change, Qualification Report availability:	The Qualification Report **QRMMY1124** is included inside this document
Marking to identify the changed product:	Process ID is “8” for Improved F8H design
Description of the qualification program:	Standard ST Microelectronics Corporate Procedures for Quality and Reliability
Product Line(s) and/or Part Number(s):	See Appendix B
Estimated date of first shipment:	Week 36 / 2012

Appendix B: Concerned Commercial Part Numbers:

- The following commercial part numbers will use the M24256 with the improved design:

Commercial Part Numbers	Package	Samples Availability
M24256-BRMN6P	SO8N	No samples in tube
M24256-BRMN6TP	SO8N	Available
M24256-BWMN6P (*)	SO8N	No samples in tube
M24256-BWMN6TP (*)	SO8N	Available
M24256-BFDW6TP	TSSOP8	Available
M24256-BWDW6TP (*)	TSSOP8	Available
M24256-BRDW6P	TSSOP8	No samples in tube
M24256-BRDW6TP	TSSOP8	Available
M24256-BFMC6TG	MLP 2x3	July 2012

(*) Following product line rationalization, we recommend customer to use **–R** version (1.8 V – 5.5 V) when –W (2.5 V – 5.5 V) is used.
For instance, **M24256-BRMN6TP should be preferred** to M24256-BWMN6TP.

- The following part numbers will not be kept in production, replacement part numbers are:

Current Commercial Part Numbers	Replacement Commercial Part Numbers	Package	Samples availability
M24256-D**R**DW6TP	M24256-D**F**DW6TP	TSSOP8	June 2012
M24256-BF**MB**6TG	M24256-BF**MC**6TG	MLP 2x3	July 2012
M24256-RCS6TP/K	To be defined	WLCSP	N/A

Appendix C: Qualification Report:

See following pages

QRMMY1124
Qualification report

Improved design / M24256-DF M24256-BR M24256-BW M24256BF using the CMOSF8H technology in the Rousset 8” Fab

Table 1. Product information

General information	
Commercial product	M24256-BRMN6P M24256-BRMN6TP M24256-BWMN6P M24256-BWMN6TP M24256-BRDW6P M24256-BRDW6TP M24256-BWDW6TP M24256-BFMC6TG M24256-BFDW6TP M24256-DFDW6TP M24256-DFMN6TP M24256-DFMC6TG
Product description	256 Kbit serial I²C bus EEPROM
Product group	MMS
Product division	MMY - Memory
Silicon process technology	CMOSF8H
Wafer fabrication location	RS8F - ST Rousset 8”, France
Electrical Wafer Sort test plant location	ST Rousset, France ST Toa Payoh, Singapore

Table 2. Package description

Package description	Assembly plant location	Final test plant location
SO8N	ST Shenzhen, China	ST Shenzhen, China
	subcon Amkor, Philippines	subcon Amkor, Philippines
TSSOP8	ST Shenzhen, China	ST Shenzhen, China
	subcon Amkor, Philippines	subcon Amkor, Philippines
UFDFPN8 (MLP8) 2 x 3 mm	ST Calamba, Philippines	ST Calamba, Philippines
	subcon Amkor, Philippines	subcon Amkor, Philippines
WLCSP	subcon Stats ChipPac, Singapore	subcon Stats ChipPac, Singapore

Reliability assessment: PASS

1 Reliability evaluation overview

1.1 Objectives

This qualification report summarizes the results of the reliability trials that were performed to qualify the improved design M24256 using the CMOSF8H silicon process technology in the ST Rousset 8” diffusion fab.

The voltage and temperature ranges covered by this document are:

- 2.5 to 5.5 V at –40 to 85 °C for W devices
- 1.8 to 5.5 V at –40 to 85 °C for R devices
- 1.7 to 5.5 V at –40 to 85 °C for F devices

The CMOSF8H is a new advanced silicon process technology that has already been qualified in the STMicroelectronics Rousset 8” diffusion plant, and is in production for M24M02/M95M02, M24M01/M95M01, M24512/M95512, M24256/M95256, M24C64/M95640 and M24C32/M95320 EEPROM products. This document serves for the qualification of the named product using the named silicon process technology in the named diffusion plant.

1.2 Conclusion

The improved design M24256 using the CMOSF8H silicon process technology in the ST Rousset 8” diffusion fab has passed all the reliability requirements.

Refer to *Section 3: Reliability test results* for details.

2 Device characteristics

Device description

The M24256-x devices are I^2C-compatible electrically erasable programmable memories (EEPROM). They are organized as 32 Kb × 8 bits.

The M24256-D also offers an additional page, named the Identification Page (128 bytes) which can be written and (later) permanently locked in Read-only mode. This Identification Page offers flexibility in the application board production line, as it can be used to store unique identification parameters and/or parameters specific to the production line.

The device behaves as a slave in the I^2C protocol, with all memory operations synchronized by the serial clock. Read and Write operations are initiated by a Start condition, generated by the bus master. The Start condition is followed by a device select code and Read/Write bit (RW) terminated by an acknowledge bit.

When writing data to the memory, the device inserts an acknowledge bit during the 9th bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a Stop condition after an Ack for Write, and after a NoAck for Read.

Refer to the product datasheet for more details.

3 Reliability test results

This section contains a general description of the reliability evaluation strategy.

The named products are qualified using the standard STMicroelectronics corporate procedures for quality and reliability.

The product vehicle used for the die qualification is presented in *Table 3*.

Table 3. Product vehicles used for die qualification

Product	Silicon process technology	Wafer fabrication location	Package description	Assembly plant location
M24256	CMOSF8H	ST Rousset 8”	CDIP8	Engineering assy (1)

1. CDIP8 is a engineering ceramic package used only for die-oriented reliability trials.

The package qualifications were mainly obtained by similarity. The product vehicles and silicon process technologies used for package qualification are presented in *Table 4*.

Table 4. Product vehicles used for package qualification

Product	Silicon process technology	Wafer fabrication location	Package description	Assembly plant location
M95M02 (1)	CMOSF8H	ST Rousset 8”	SO8N	ST Shenzhen / subcon Amkor
M24M01 (2)	CMOSF8H	ST Rousset 8”	TSSOP8	ST Shenzhen / subcon Amkor
M24512	CMOSF8H	ST Rousset 8”	UFDFPN8 (MLP8) 2 x 3 mm	ST Calamba / subcon Amkor
M95M02 / M24512	CMOSF8H	ST Rousset 8”	WLCSP	subcon Stats ChipPac

1. Larger memory array using the same silicon process technology in the same diffusion fab - Package qualification results of M95M02 (2MB SPI) are applicable.
2. Larger memory array using the same silicon process technology in the same diffusion fab - Package qualification results of M24M01 (1MB I2C) are applicable.

3.1 Reliability test plan and result summary

The reliability test plan and the result summary are presented as follows:

- in *Table 5* for die-oriented tests
- in *Table 6* for SO8N ST Shenzhen package-oriented tests
- in *Table 7* for TSSOP8 ST Shenzhen package-oriented tests
- Reliability tests on all other packages are planned, but results are not yet available.

Table 5. Die-oriented reliability test plan and result summary (CDIP8 / Engineering package)(1)

Test	Test short description					
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size
						M24256
						Lot 1
EDR	High temperature operating life after endurance					
	AEC-Q100-005	1 Million E/W cycles at 25 °C then: HTOL 150 °C, 6 V	80	1	1008 hrs	0/80
	Data retention after endurance					
	AEC-Q100-005	1Million E/W cycles at 25 °C then: HTSL at 150 °C	80	1	1008 hrs	0/80
LTOL	Low temperature operating life					
	JESD22-A108	–40 °C, 6 V	80	1	1008 hrs	0/80
HTSL	High temperature storage life					
	JESD22-A103	Retention bake at 200 °C	80	1	1008 hrs	0/80
WEB	Program/erase endurance cycling + bake					
	Internal spec.	1 Million E/W cycles at 25 °C then: Retention bake at 200 °C / 48 hours	80	1	1 Million cycles / 48 hrs	0/80 (2)
ESD HBM	Electrostatic discharge (human body model)					
	AEC-Q100-002 JESD22-A114	C = 100 pF, R= 1500 Ω	27	1	N/A	Pass 4000 V
ESD MM	Electrostatic discharge (machine model)					
	AEC-Q100-003 JESD22-A115	C = 200 pF, R = 0 Ω	12	1	N/A	Pass 400 V
LU	Latch-up (current injection and overvoltage stress)					
	AEC-Q100-004 JESD78A	At maximum operating temperature (150 °C)	6	1	N/A	Class II - Level A

1. See *Table 8: List of terms* for a definition of abbreviations.
2. First rejects after 10 million E/W cycles + bake.

Table 6. Package-oriented reliability test plan and result summary (SO8N / ST Shenzhen) (1)

Test	Test short description								
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size			
						M95M02 (2)			M24256
						Lot1	Lot2	Lot3	Lot4
PC	Preconditioning: moisture sensitivity level 1								
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	1200	3	N/A	0/1200	0/1200	0/1200	-
THB (3)	Temperature humidity bias								
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.5 V	80	3	1008 hrs	0/80	0/80	0/80	-
TC (3)	Temperature cycling								
	AEC-Q100-JESD22-A104	–65 °C / +175 °C	80	3	1000 cycles	0/80	0/80	0/80	-
TMSK (3)	Thermal shocks								
	JESD22-A106	–55 °C / +125 °C	80	3	200 shocks	0/80	0/80	0/80	-
AC (3)	Autoclave (pressure pot)								
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	3	168 hrs	0/80	0/80	0/80	-
HTSL (3)	High temperature storage life								
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	3	1008 hrs	0/80	0/80	0/80	-
ELFR (3)	Early life failure rate								
	AEC-Q100-008	HTOL at 150 °C, 6V	800	3	48 hrs	0/800	0/800	0/800	-
ESD CDM	Electrostatic discharge (charge device model)								
	AEC-Q100-011 JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V	-	-	Pass >1500 V

1. See *Table 8: List of terms* for a definition of abbreviations.
2. Larger memory array using the same silicon process technology in the same diffusion fab - Package qualification results of M95M02 (2MB SPI) are applicable.
3. THB-, TC-, TMSK-, AC-, HTSL and ELFR- dedicated parts are first subject to preconditioning flow.

Table 7. Package-oriented reliability test plan and result summary (TSSOP8 / ST Shenzhen) (1)

Test	Test short description								
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size			
						M24M01 (2)			M24256
						Lot1	Lot2	Lot3	Lot4
PC	Preconditioning: moisture sensitivity level 1								
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	400	3	N/A	0/400	0/400	0/400	-
THB (3)	Temperature humidity bias								
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.5 V	80	3	1008 hrs	0/80	0/80	0/80	-
TC (3)	Temperature cycling								
	AEC-Q100-JESD22-A104	–65 °C / +175 °C	80	3	1000 cycles	0/80	0/80	0/80	-
TMSK (3)	Thermal shocks								
	JESD22-A106	–55 °C / +125 °C	80	3	200 shocks	0/80	0/80	0/80	-
AC (3)	Autoclave (pressure pot)								
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	3	168 hrs	0/80	0/80	0/80	-
HTSL (3)	High temperature storage life								
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	3	1008 hrs	0/80	0/80	0/80	-
ESD CDM	Electrostatic discharge (charge device model)								
	AEC-Q100-011 JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V	-	-	Pass >1500 V

1. See *Table 8: List of terms* for a definition of abbreviations.
2. Larger memory array using the same silicon process technology in the same diffusion fab - Package qualification results of M24M01 (1MB I2C) are applicable.
3. THB-, TC-, TMSK-, AC- and HTSL- dedicated parts are first subject to preconditioning flow.

4 Applicable and reference documents

- AEC-Q100: Stress test qualification for integrated circuits
- SOP 2.6.10: General product qualification procedure
- SOP 2.6.11: Program management fro product qualification
- SOP 2.6.12: Design criteria for product qualification
- SOP 2.6.14: Reliability requirements for product qualification
- SOP 2.6.19: Process maturity level
- SOP 2.6.2: Process qualification and transfer management
- SOP 2.6.20: New process / New product qualification
- SOP 2.6.7: Product maturity level
- SOP 2.6.9: Package and process maturity management in Back End
- SOP 2.7.5: Automotive products definition and status
- JESD22-A101: Steady state temperature humidity bias life test
- JESD22-A102: Accelerated moisture resistance - unbiased autoclave
- JESD22-A103: High temperature storage life
- JESD22-A104: Temperature cycling
- JESD22-A106: Thermal shock
- JESD22-A108: Temperature, bias, and operating life
- JESD22-A113: Preconditioning of nonhermetic surface mount devices prior to reliability testing
- JESD22-A114: Electrostatic discharge (ESD) sensitivity testing human body model (HBM)
- JESD22-A115: Electrostatic discharge (ESD) sensitivity testing machine model (MM)
- JESD78A: IC Latch-up test
- J-STD-020D: Moisture/reflow sensitivity classification for nonhermetic solid state surface mount devices

5 Glossary

Table 8. List of terms

Terms	Description
EDR	NVM endurance, data retention and operational life
HTOL	High temperature operating life
LTOL	Low temperature operating life
HTB	High temperature bake
WEB	Program/Erase endurance cycling + bake
ESD HBM	Electrostatic discharge (human body model)
ESD MM	Electrostatic discharge (machine model)
LU	Latch-up
PC	Preconditioning (solder simulation)
THB	Temperature humidity bias
TC	Temperature cycling
TMSK	Thermal shocks
AC	Autoclave (pressure pot)
HTSL	High temperature storage life
ELFR	Early life failure rate
ESD CDM	Electrostatic discharge (charge device model)

6 Revision history

Table 9. Document revision history

Date	Revision	Changes
21-May-2012	1	Initial release.

Document Revision History

Date	Rev.	Description of the Revision
May 02 , 2011	1.00	First draft creation

Source Documents & Reference Documents

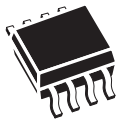
Source document Title	**Rev.:**	**Date:**

M24256-BF M24256-BR M24256-BW M24256-DR

256 Kbit serial I²C bus EEPROM with three Chip Enable lines

Features

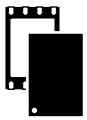
- Compatible with all I²C bus modes:
  - 1 MHz Fast-mode Plus
  - 400 kHz Fast mode
  - 100 kHz Standard mode
- Memory array:
  - 256 Kb (32 Kbytes) of EEPROM
  - Page size: 64 bytes
- M24xxx- DR: additional Write lockable Page (Identification page)
- Single supply voltage:
  - 1.7 V to 5.5 V
  - 1.8 V to 5.5 V
  - 2.5 V to 5.5 V
- Noise suppression
  - Schmitt trigger inputs
  - Input noise filter
- Write
  - Byte write within 5 ms
  - Page write within 5 ms
- Random and sequential read modes
- Write protect of the whole memory array
- Enhanced ESD/latch-up protection
- More than 1 million write cycles
- More than 40-year data retention
- Packages
  - ECOPACK2® (RoHS compliant and halogen-free)



SO8 (MN)
150 mils width

TSSOP8 (DW)

WLCSP (CS)



UFDFPN8
(MB, MC)

Contents

List of tables

List of figures

1 Description

The M24256-Bx devices are I^2C-compatible electrically erasable programmable memories (EEPROM). They are organized as 32 K × 8 bits.

The M24256-DR is also an I^2C-compatible EEPROM organized as 32 K × 8 bits, but it offers an additional page, named the Identification Page (64 bytes). The Identification Page can be used to store sensitive application parameters which can be (later) permanently locked in read-only mode.

Figure 1. Logic diagram

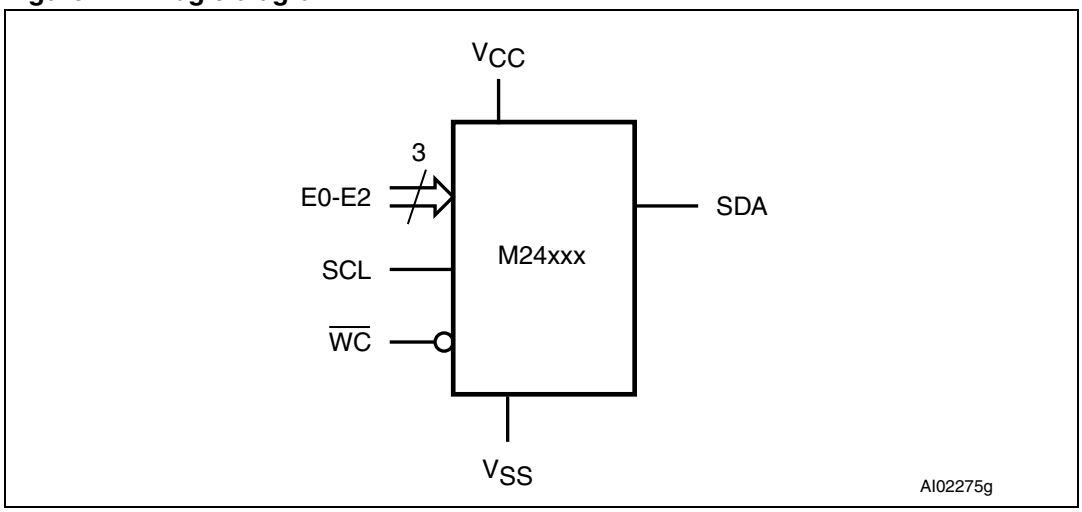
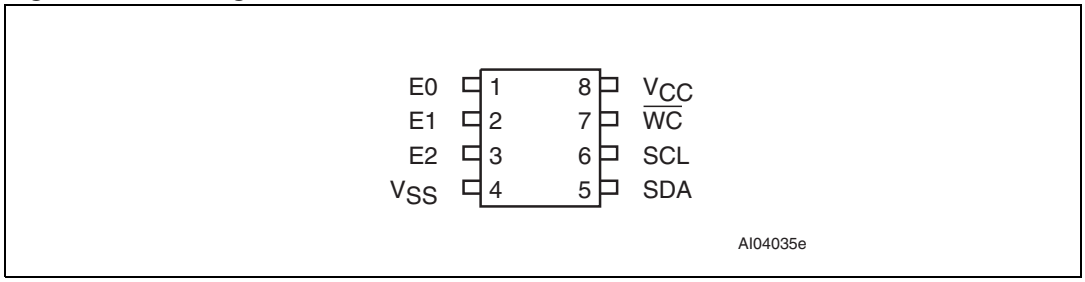


Table 1. Signal names

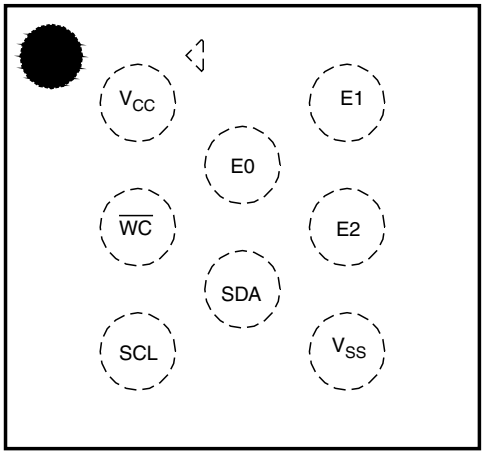
Signal name	Function	Direction
E0, E1, E2	Chip Enable	Inputs
SDA	Serial Data	I/O
SCL	Serial Clock	Input
$\overline{WC}$	Write Control	Input
V_{CC}	Supply voltage	
V_{SS}	Ground	

Figure 2. Package connections



1. See *Package mechanical data* section for package dimensions, and how to identify pin-1.

Figure 3. WLCSP connections (top view, marking side, with balls on the underside)



Caution: As EEPROM cells loose their charge (and so their binary value) when exposed to ultra violet (UV) light, EEPROM dice delivered in wafer form or in WLCSP package by STMicroelectronics must never be exposed to UVlight.

2 Signal description

2.1 Serial Clock (SCL)

This input signal is used to strobe all data in and out of the device. In applications where this signal is used by slave devices to synchronize the bus to a slower clock, the bus master must have an open drain output, and a pull-up resistor must be connected from Serial Clock (SCL) to V_{CC}. (*Figure 6* indicates how the value of the pull-up resistor can be calculated). In most applications, though, this method of synchronization is not employed, and so the pull-up resistor is not necessary, provided that the bus master has a push-pull (rather than open drain) output.

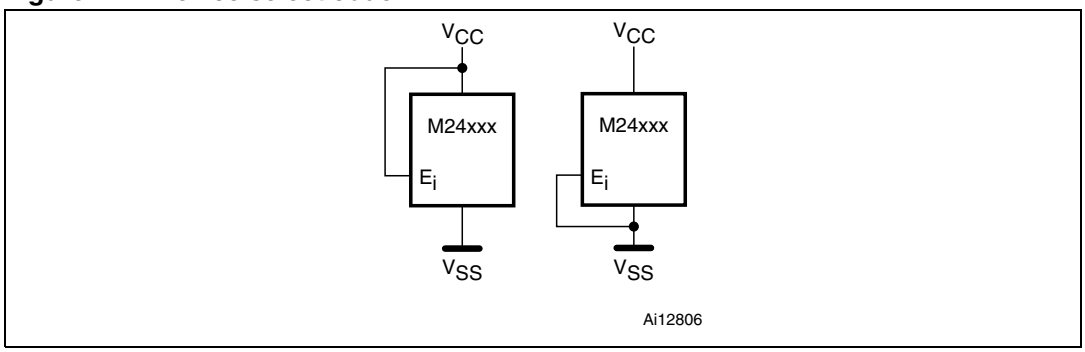
2.2 Serial Data (SDA)

This bidirectional signal is used to transfer data in or out of the device. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull up resistor must be connected from Serial Data (SDA) to V_{CC}. (*Figure 6* indicates how the value of the pull-up resistor can be calculated).

2.3 Chip Enable (E0, E1, E2)

These input signals are used to set the value that is to be looked for on the three least significant bits (b3, b2, b1) of the 7-bit device select code. These inputs must be tied to V_{CC} or V_{SS}, to establish the device select code. When not connected (left floating), these inputs are read as Low (0,0,0).

Figure 4. Device select code



2.4 Write Control ($\overline{WC}$)

This input signal is useful for protecting the entire contents of the memory from inadvertent write operations. Write operations are disabled to the entire memory array when Write Control ($\overline{WC}$) is driven High. When unconnected, the signal is internally read as V_{IL}, and Write operations are allowed.

When Write Control ($\overline{WC}$) is driven High, device select and address bytes are acknowledged, Data bytes are not acknowledged.

2.5 V_{SS} ground

V_{SS} is the reference for the V_{CC} supply voltage.

2.6 Supply voltage (V_{CC})

2.6.1 Operating supply voltage V_{CC}

Prior to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range must be applied (see *Table 7*, *Table 8* and *Table 9*). In order to secure a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually of the order of 10 nF to 100 nF) close to the V_{CC}/V_{SS} package pins.

This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle (t_W).

2.6.2 Power-up conditions

V_{CC} has to rise continuously from 0 V up to V_{CC}(min) (see *Table 7*, *Table 8* and *Table 9*), and the rise time must not vary faster than 1 V/µs.

2.6.3 Device reset

In order to prevent inadvertent write operations during power-up, a power on reset (POR) circuit is included. At power-up, the device does not respond to any instruction until V_{CC} reaches an internal reset threshold voltage. This threshold is lower than the minimum V_{CC} operating voltage defined in *Table 7*, *Table 8* and *Table 9*.

When V_{CC} passes over the POR threshold, the device is reset and enters the Standby Power mode. However, the device must not be accessed until V_{CC} reaches a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range.

In a similar way, during power-down (continuous decrease in V_{CC}), as soon as V_{CC} drops below the power on reset threshold voltage, the device stops responding to any instruction sent to it.

2.6.4 Power-down conditions

During power-down (where V_{CC} decreases continuously), the device must be in the Standby Power mode (mode reached after decoding a Stop condition, assuming that there is no internal Write cycle in progress).

Figure 5. I^2C Fast mode (f_C = 400 kHz): maximum R_{bus} value versus bus parasitic capacitance (C_{bus})

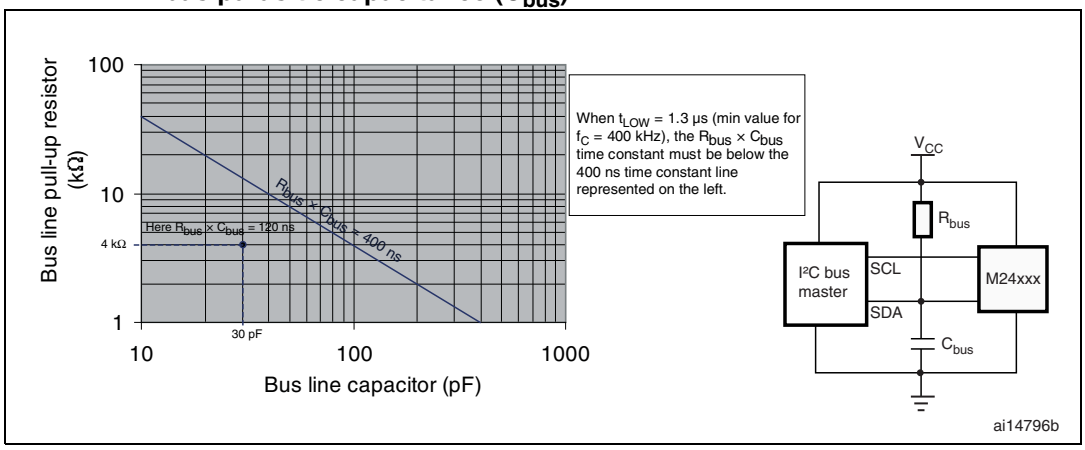


Figure 6. I^2C Fast mode Plus (f_C = 1 MHz): maximum R_{bus} value versus bus parasitic capacitance (C_{bus})

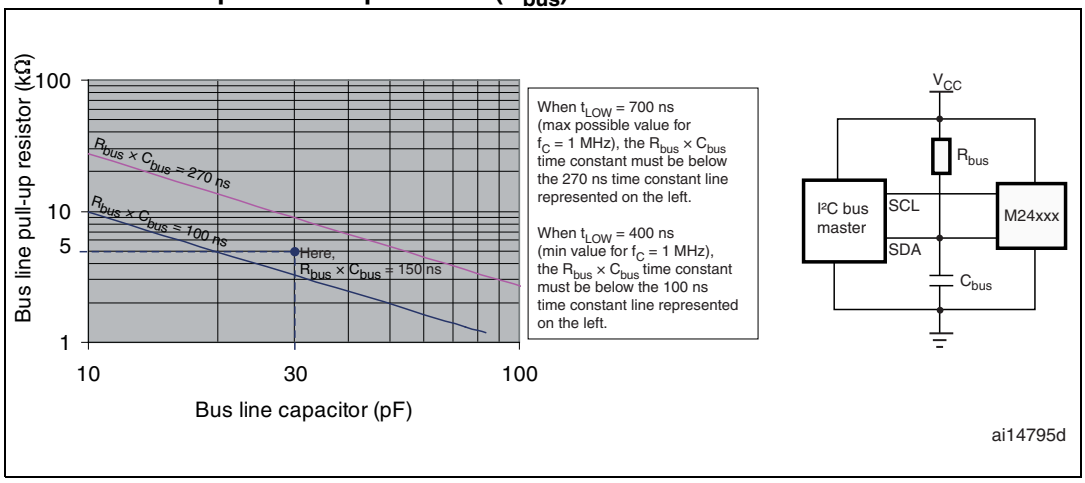


Figure 7. I^2C bus protocol

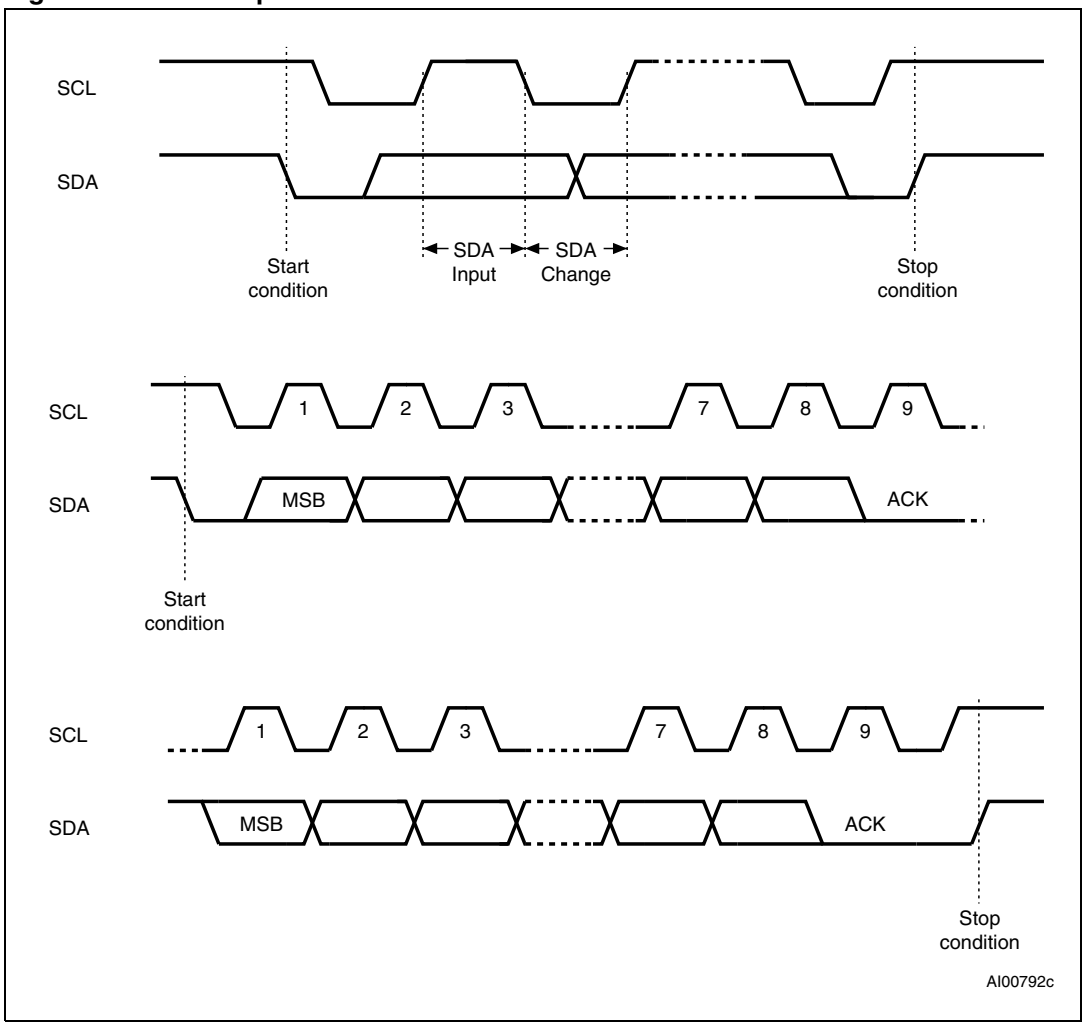


Table 2. Most significant address byte

b15	b14	b13	b12	b11	b10	b9	b8

Table 3. Least significant address byte

b7	b6	b5	b4	b3	b2	b1	b0

3 Device operation

The device supports the I^2C protocol. This is summarized in *Figure 7*. Any device that sends data on to the bus is defined to be a transmitter, and any device that reads the data to be a receiver. The device that controls the data transfer is known as the bus master, and the other as the slave device. A data transfer can only be initiated by the bus master, which will also provide the serial clock for synchronization. The device is always slave in all communications.

3.1 Start condition

Start is identified by a falling edge of Serial Data (SDA) while Serial Clock (SCL) is stable in the High state. A Start condition must precede any data transfer instruction. The device continuously monitors (except during a Write cycle) Serial Data (SDA) and Serial Clock (SCL) for a Start condition.

3.2 Stop condition

Stop is identified by a rising edge of Serial Data (SDA) while Serial Clock (SCL) is stable and driven High. A Stop condition terminates communication between the device and the bus master. A Read instruction that is followed by NoAck can be followed by a Stop condition to force the device into the Standby mode. A Stop condition at the end of a Write instruction triggers the internal Write cycle.

3.3 Acknowledge bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it be bus master or slave device, releases Serial Data (SDA) after sending eight bits of data. During the 9^{th} clock pulse period, the receiver pulls Serial Data (SDA) Low to acknowledge the receipt of the eight data bits.

3.4 Data input

During data input, the device samples Serial Data (SDA) on the rising edge of Serial Clock (SCL). For correct device operation, Serial Data (SDA) must be stable during the rising edge of Serial Clock (SCL), and the Serial Data (SDA) signal must change *only* when Serial Clock (SCL) is driven Low.

3.5 Addressing the memory array

To start communication between the bus master and the slave device, the bus master must initiate a Start condition. Following this, the bus master sends the device select code, shown in *Table 4* (on Serial Data (SDA), most significant bit first).

The 4-bit device type identifier 1010b selects the memory array, the 4-bit device type identifier 1011b selects the Identification page. A device select code handling a value different than 1010b or 1011b is not acknowledged by the device.

Table 4. Device select code (for memory array)

	Device type identifier(1)				Chip Enable address(2)			RW
	b7	b6	b5	b4	b3	b2	b1	b0
Device select code when addressing the memory array	1	0	1	0	E2	E1	E0	RW
Device select code when accessing the Identification page	1	0	1	1	E2	E1	E0	RW

1. The most significant bit, b7, is sent first.
2. E0, E1 and E2 are compared against the respective external pins on the memory device.

Up to eight memory devices can be connected on a single I^2C bus. Each one is given a unique 3-bit code on the Chip Enable (E0, E1, E2) inputs. When the device select code is received, the device only responds if the Chip Enable Address is the same as the value on the Chip Enable (E0, E1, E2) inputs.

The 8th bit is the Read/Write bit (RW). This bit is set to 1 for Read and 0 for Write operations.

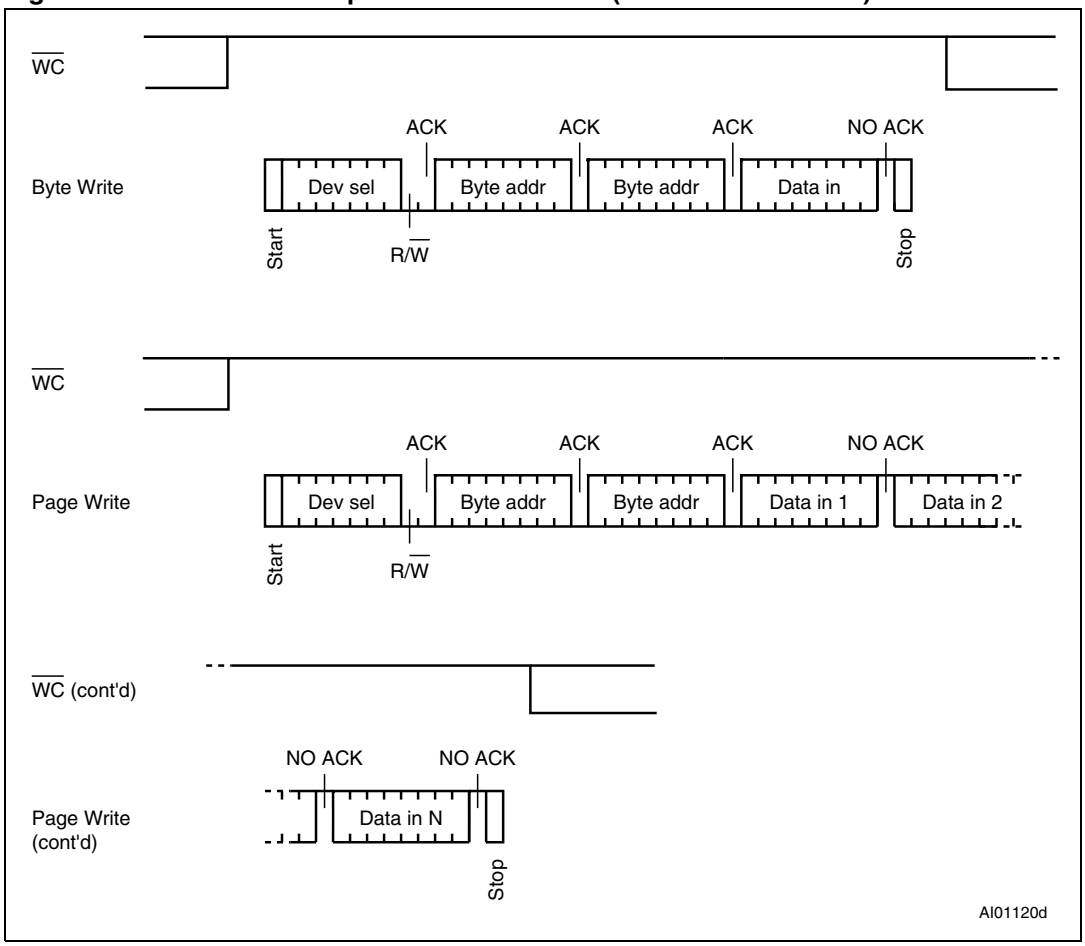
If a match occurs on the device select code, the corresponding device gives an acknowledgment on Serial Data (SDA) during the 9th bit time. If the device does not match the device select code, it deselects itself from the bus, and goes into Standby mode.

Table 5. Operating modes

Mode	RW bit	WC(1)	Bytes	Initial sequence
Current Address Read	1	X	1	Start, device select, RW = 1
Random Address Read	0	X	1	Start, device select, RW = 0, Address
	1	X		re-Start, device select, RW = 1
Sequential Read	1	X	≥ 1	Similar to Current or Random Address Read
Byte Write	0	V_{IL}	1	Start, device select, RW = 0
Page Write	0	V_{IL}	≤ 64	Start, device select, RW = 0

1. X = V_{IH} or V_{IL}.

Figure 8. Write mode sequences with $\overline{WC}$ = 1 (data write inhibited)



3.6 Write operations

Following a Start condition the bus master sends a device select code with the Read/$\overline{\text{Write}}$ bit ($\overline{\text{RW}}$) reset to 0. The device acknowledges this, as shown in *Figure 9*, and waits for two address bytes. The device responds to each address byte with an acknowledge bit, and then waits for the data byte.

Each data byte in the memory has a 16-bit (two byte wide) address. The most significant byte (*Table 2*) is sent first, followed by the least significant byte (*Table 3*). Bits b15 to b0 form the address of the byte in memory.

When the bus master generates a Stop condition immediately after a data byte Ack bit (in the "10^{th} bit" time slot), either at the end of a Byte Write or a Page Write, the internal Write cycle is triggered. A Stop condition at any other time slot does not trigger the internal Write cycle.

After the Stop condition, the delay t_W, and the successful completion of a Write operation, the device's internal address counter is incremented automatically, to point to the next byte address after the last one that was modified.

During the internal Write cycle, Serial Data (SDA) is disabled internally, and the device does not respond to any requests.

If the Write Control input (WC) is driven High, the Write instruction is not executed and the accompanying data bytes are not acknowledged, as shown in *Figure 8*.

3.7 Byte Write

After the device select code and the address bytes, the bus master sends one data byte. If the addressed location is Write-protected, by Write Control ($\overline{\text{WC}}$) being driven High, the device replies with NoAck, and the location is not modified. If, instead, the addressed location is not Write-protected, the device replies with Ack. The bus master terminates the transfer by generating a Stop condition, as shown in *Figure 9*.

3.8 Page Write (memory array)

The Page Write mode allows up to 64 bytes to be written in a single Write cycle, provided that they are all located in the same 'row' in the memory: that is, the most significant memory address bits (b15-b6) are the same. If more bytes are sent than will fit up to the end of the row, a condition known as 'roll-over' occurs. This should be avoided, as data starts to become overwritten in an implementation dependent way.

The bus master sends from 1 to 64 bytes of data, each of which is acknowledged by the device if Write Control ($\overline{\text{WC}}$) is Low. If Write Control ($\overline{\text{WC}}$) is High, the contents of the addressed memory location are not modified, and each data byte is followed by a NoAck. After each byte is transferred, the internal byte address counter (the 7 least significant address bits only) is incremented. The transfer is terminated by the bus master generating a Stop condition.

3.9 Write Identification Page (M24256-D only)

The Identification Page (64 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode. The identification page is written by issuing a Write Identification Page instruction. This instruction uses the same protocol and format as Page Write (into memory array), except for the following differences:

- Device Type Identifier = 1011b
- MSB address bits A15/A6 are don't care except for address bit A10 which must be ‘0’. LSB address bits A5/A0 define the byte address inside the identification page.

If the Identification page is locked, the data bytes transferred during the Write Identification Page instruction are not acknowledged (NoAck).

3.10 Lock Identification Page (M24256-D only)

The Lock Identification Page instruction (Lock ID) permanently locks the Identification page in read-only mode. The Lock ID instruction is similar to Byte Write (into memory array) with the following specific conditions:

- Device Type Identifier = 1011b
- Address bit A10 must be ‘1’; all other address bits are don't care
- The data byte must be equal to the binary value xxxx xx1x, where x is don't care.

If the Identification Page is locked, the data bytes transferred during the ID Write instruction are not acknowledged (NoAck).

3.11 ECC (error correction code) and write cycling

The M24256-Bx and M24256-D devices offer an ECC (error correction code) logic which compares each 4-byte word with its six associated ECC EEPROM bits. As a result, if a single bit out of 4 bytes of data happens to be erroneous during a Read operation, the ECC detects it and replaces it by the correct value. The read reliability is therefore much improved by the use of this feature.

Note however that even if a single byte has to be written, 4 bytes are internally modified (plus the ECC bits), that is, the addressed byte is cycled together with the other three bytes making up the word. It is therefore recommended to write data by word (4 bytes) at address 4*N (where N is an integer) in order to benefit from the larger amount of Write cycles.

The M24256-Bx and M24256-DR devices are qualified at 1 million (1 000 000) Write cycles, using a cycling routine that writes to the device by multiples of 4-bytes.

Figure 9. Write mode sequences with $\overline{WC}$ = 0 (data write enabled)

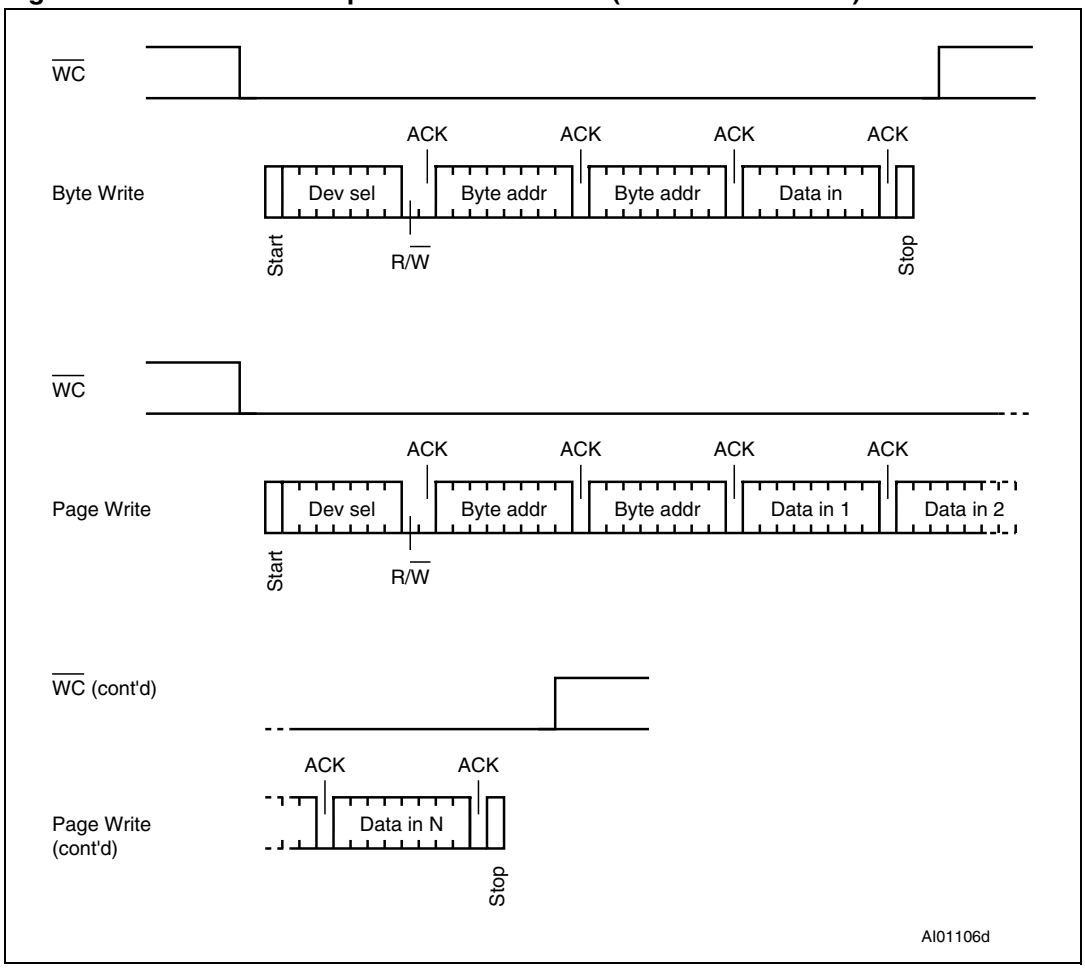
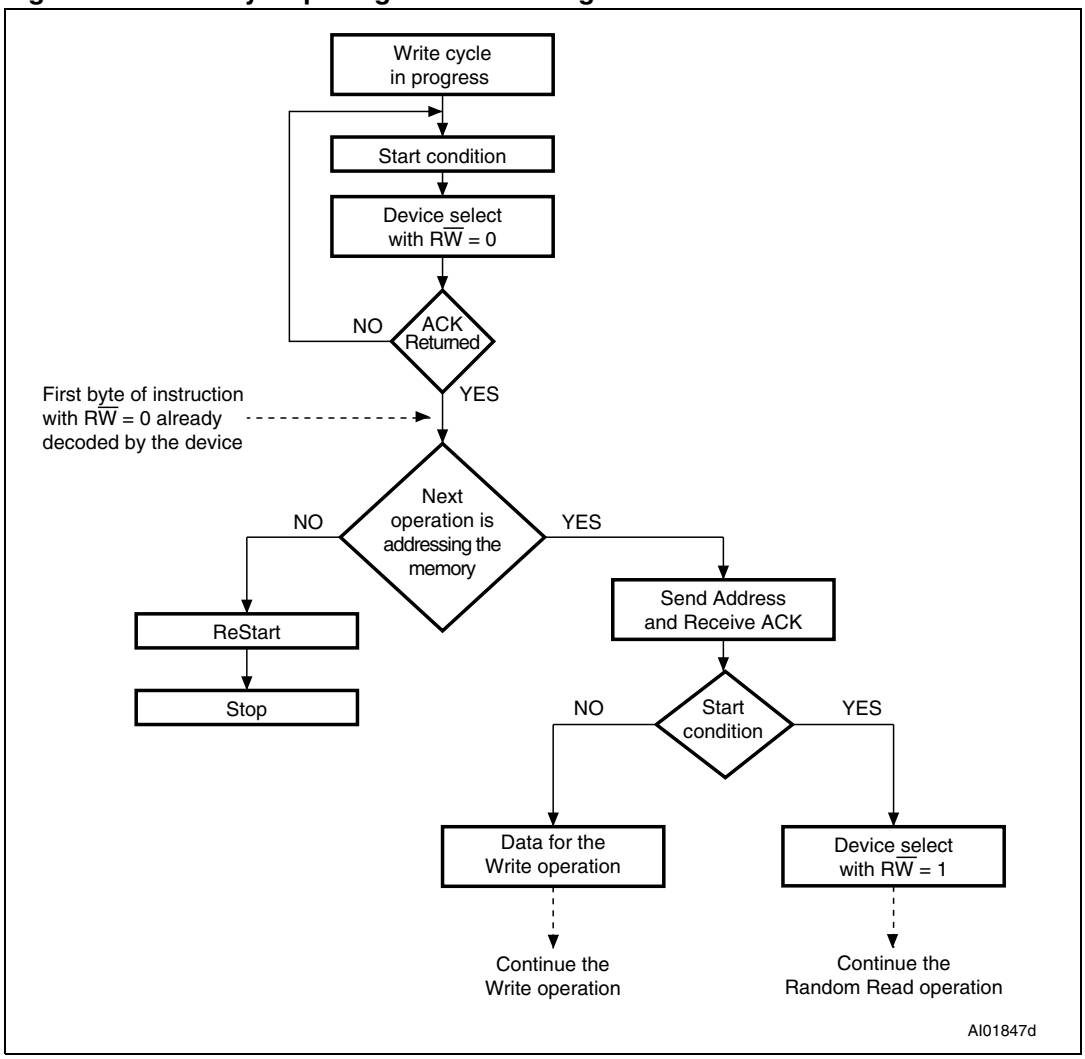


Figure 10. Write cycle polling flowchart using ACK



3.12 Minimizing system delays by polling on ACK

During the internal Write cycle, the device disconnects itself from the bus, and writes a copy of the data from its internal latches to the memory cells. The maximum Write time (t_w) is shown in tables *17* and *18*, but the typical time is shorter. To make use of this, a polling sequence can be used by the bus master.

The sequence, as shown in *Figure 10*, is:

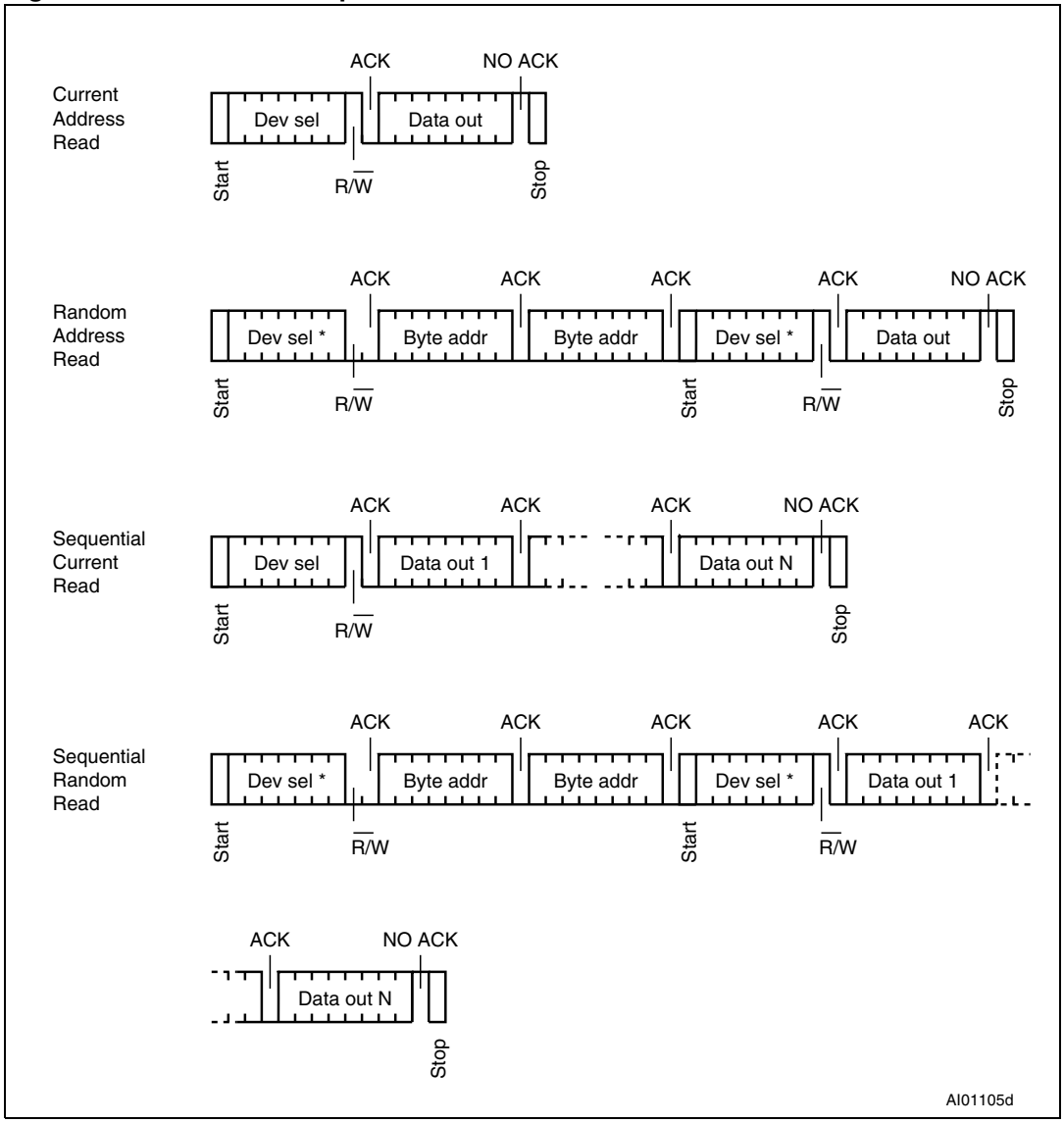
- Initial condition: a Write cycle is in progress.
- Step 1: the bus master issues a Start condition followed by a device select code (the first byte of the new instruction).
- Step 2: if the device is busy with the internal Write cycle, no Ack will be returned and the bus master goes back to Step 1. If the device has terminated the internal Write cycle, it responds with an Ack, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during Step 1).

3.13 Read operations

Read operations are performed independently of the state of the Write Control ($\overline{WC}$) signal.

After the successful completion of a Read operation, the device's internal address counter is incremented by one, to point to the next byte address.

Figure 11. Read mode sequences



3.14 Random Address Read (in memory array)

A dummy Write is first performed to load the address into this address counter (as shown in *Figure 11*) but *without* sending a Stop condition. Then, the bus master sends another Start condition, and repeats the device select code, with the Read/$\overline{Write}$ bit ($R\overline{W}$) set to 1. The device acknowledges this, and outputs the contents of the addressed byte. The bus master must *not* acknowledge the byte, and terminates the transfer with a Stop condition.

3.15 Current Address Read (in memory array)

For the Current Address Read operation, following a Start condition, the bus master only sends a device select code with the Read/$\overline{\text{Write}}$ bit (R$\overline{\text{W}}$) set to 1. The device acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus master terminates the transfer with a Stop condition, as shown in *Figure 11*, *without* acknowledging the byte.

3.16 Sequential Read

This operation can be used after a Current Address Read or a Random Address Read. The bus master *does* acknowledge the data byte output, and sends additional clock pulses so that the device continues to output the next byte in sequence. To terminate the stream of bytes, the bus master must *not* acknowledge the last byte, and *must* generate a Stop condition, as shown in *Figure 11*.

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter 'rolls-over', and the device continues to output data from memory address 00h.

3.17 Reading the Identification Page (M24256-D only)

The Identification Page (64 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode.

The Identification Page can be read by issuing a Read Identification Page instruction. This instruction uses the same protocol and format as the Random Address Read (from memory array) with device type identifier defined as 1011b. The MSB address bits A17/A6 are don't care, the LSB address bits A5/A0 define the byte address inside the Identification Page. The number of bytes to read in the ID page must not exceed the page boundary, otherwise unexpected data will be read (e.g.: when reading the Identification Page from location 10d, the number of bytes should be less than or equal to 54, as the ID page boundary is 64 bytes).

3.18 Reading the lock status (M24256-D only)

The locked/unlocked status of the Identification page can be checked by transmitting a specific truncated command [Identification Page Write instruction + one data byte] to the device. The device will return an acknowledge bit if the Identification page is unlocked, otherwise a NoAck bit if the Identification page is locked.

Right after this, it is recommended to transmit to the device a Start condition followed by a Stop condition, so that:

- Start: the truncated command is not executed because the Start condition resets the device internal logic,
- Stop: the device is then set back into Standby mode by the Stop condition.

3.19 Acknowledge in Read mode

For all Read instructions, the device waits, after each byte read, for an acknowledgment during the 9^{th} bit time. If the bus master does not drive Serial Data (SDA) Low during this time, the device terminates the data transfer and switches to its Standby mode.

4 Initial delivery state

The device is delivered with all bits in the memory array set to 1 (each byte contains FFh).

5 Maximum rating

Stressing the device outside the ratings listed in *Table 6* may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 6. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
	Ambient Temperature with power applied	–40	130	°C
T_{STG}	Storage temperature	–65	150	°C
T_{LEAD}	Lead temperature during soldering	See note (1)		°C
V_{IO}	Input or output range	–0.50	6.5	V
V_{CC}	Supply voltage	–0.50	6.5	V
I_{OL}	DC output current (SDA = 0)		5	mA
V_{ESD}	Electrostatic pulse voltage (Human Body Model) (2)		3000	V

1. Compliant with JEDEC Std J-STD-020 (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS) 2002/95/EC.
2. Positive and negative pulses applied on pin pairs, according to AEC-Q100-002 (compliant with JEDEC Std JESD22-A114, C1 = 100 pF, R1 = 1500 Ω, R2 = 500 Ω)

6 DC and AC parameters

This section summarizes the operating and measurement conditions, and the dc and ac characteristics of the device. The parameters in the DC and AC characteristic tables that follow are derived from tests performed under the measurement conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 7. Operating conditions (voltage range W)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	2.5	5.5	V
T_A	Ambient operating temperature (device grade 6)	–40	85	°C
	Ambient operating temperature (device grade 3)	–40	125	°C

Table 8. Operating conditions (voltage range R)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	1.8	5.5	V
T_A	Ambient operating temperature	–40	85	°C

Table 9. Operating conditions (voltage range F)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	1.7	5.5	V
T_A	Ambient operating temperature	–40	85	°C

Table 10. AC test measurement conditions

Symbol	Parameter	Min.	Max.	Unit
C_{bus}	Load capacitance	100		pF
	SCL input rise/fall time SDA input fall time		50	ns
	Input levels	$0.2V_{CC}$ to $0.8V_{CC}$		V
	Input and output timing reference levels	$0.3V_{CC}$ to $0.7V_{CC}$		V

Figure 12. AC test measurement I/O waveform

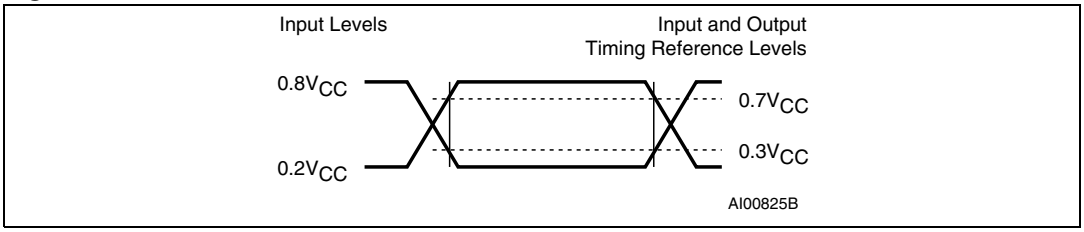


Table 11. Input parameters

Symbol	Parameter[1]	Test condition	Min.	Max.	Unit
C_{IN}	Input capacitance (SDA)			8	pF
C_{IN}	Input capacitance (other pins)			6	pF
Z_L[2]	Input impedance (E2, E1, E0, $\overline{WC}$)	$V_{IN} < 0.3V_{CC}$	30		kΩ
Z_H[2]	Input impedance (E2, E1, E0, $\overline{WC}$)	$V_{IN} > 0.7V_{CC}$	500		kΩ

1. Sampled only, not 100% tested.
2. E2,E1,E0: Input impedance when the memory is selected (after a Start condition).

Table 12. Memory cell characteristics

Symbol	Parameter	Test condition	Min.	Max.	Unit
N_{cycle}	Endurance	TA = 25°C, 1.8V < Vcc < 5.5V	1,000,000	-	Write cycle

Note: This parameter is not tested but established by characterization and qualification. To estimate endurance in a specific application, please refer to AN2014.

Table 13. DC characteristics (voltage range W, device grade 3)

Symbol	Parameter	Test conditions (in addition to those in *Table 7* and *Table 10*)	Min.	Max.	Unit
I_{LI}	Input leakage current (SCL, SDA, E0, E1, E2)	$V_{IN} = V_{SS}$ or V_{CC} device in Standby mode		± 2	µA
I_{LO}	Output leakage current	SDA in Hi-Z, external voltage applied on SDA: V_{SS} or V_{CC}		± 2	µA
I_{CC}	Supply current (Read)	f_c = 400 kHz		2	mA
I_{CC0}	Supply current (Write)	During t_W		5[1]	mA
I_{CC1}	Standby supply current	Device not selected[2], $V_{IN} = V_{SS}$ or V_{CC}		5	µA
V_{IL}	Input low voltage (SCL, SDA, WC)		–0.45	0.3 V_{CC}	V
V_{IH}	Input high voltage (SCL, SDA)		0.7V_{CC}	6.5	V
	Input high voltage (WC, E0, E1, E2)		0.7V_{CC}	V_{CC}+0.6	V
V_{OL}	Output low voltage	I_{OL} = 2.1 mA, V_{CC} = 2.5 V or I_{OL} = 3 mA, V_{CC} = 5.5 V		0.4	V

1. Characterized value, not tested in production.
2. The device is not selected after power-up, after a Read instruction (after the Stop condition), or after the completion of the internal write cycle t_W (t_W is triggered by the correct decoding of a Write instruction).

Table 14. DC characteristics (voltage range W, device grade 6)

Symbol	Parameter	Test conditions (see *Table 7* and *Table 10*)	Min.	Max.	Unit
I_{LI}	Input leakage current (SCL, SDA, E0, E1, E2)	$V_{IN} = V_{SS}$ or V_{CC} device in Standby mode		± 2	µA
I_{LO}	Output leakage current	SDA in Hi-Z, external voltage applied on SDA: V_{SS} or V_{CC}		± 2	µA
I_{CC}	Supply current (Read)	V_{CC} = 2.5 V, f_c = 400 kHz (rise/fall time < 50 ns)		1	mA
		V_{CC} = 5.5 V, f_c = 400 kHz (rise/fall time < 50 ns)		2	mA
		2.5 V < V_{CC} < 5.5 V, f_c = 1 MHz(1) (rise/fall time < 50 ns)		2.5	mA
I_{CC0}	Supply current (Write)	During t_W, 2.5 V < V_{CC} < 5.5 V		2(2)	mA
I_{CC1}	Standby supply current	Device not selected(3), $V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5 V		2	µA
		Device not selected(3), $V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5.5 V		3	µA
V_{IL}	Input low voltage (SCL, SDA, WC)		–0.45	$0.3V_{CC}$	V
V_{IH}	Input high voltage (SCL, SDA)		$0.7V_{CC}$	6.5	V
	Input high voltage (WC, E0, E1, E2)		$0.7V_{CC}$	V_{CC}+0.6	
V_{OL}	Output low voltage	I_{OL} = 2.1 mA, V_{CC} = 2.5 V or I_{OL} = 3 mA, V_{CC} = 5.5 V		0.4	V

1. Only for devices operating at f_C max = 1 MHz (see *Table 18*).
2. Characterized value, not tested in production.
3. The device is not selected after power-up, after a Read instruction (after the Stop condition), or after the completion of the internal write cycle t_W (t_W is triggered by the correct decoding of a Write instruction).

Table 15. DC characteristics (voltage range R)

Symbol	Parameter	Test conditions[1] (in addition to those in *Table 8* and *Table 10*)	Min.	Max.	Unit
I_{LI}	Input leakage current (E1, E2, SCL, SDA)	$V_{IN} = V_{SS}$ or V_{CC} device in Standby mode		± 2	µA
I_{LO}	Output leakage current	SDA in Hi-Z, external voltage applied on SDA: V_{SS} or V_{CC}		± 2	µA
I_{CC}	Supply current (Read)	V_{CC} = 1.8 V, f_c= 400 kHz		0.8	mA
		f_c= 1 MHz		2.5	mA
I_{CC0}	Supply current (Write)	During t_W, 1.8 V < V_{CC} < 2.5 V		2[2]	mA
I_{CC1}	Standby supply current	Device not selected[3], $V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 1.8 V		1	µA
V_{IL}	Input low voltage (SCL, SDA, WC)	1.8 V ≤ V_{CC} < 2.5 V	–0.45	0.25 V_{CC}	V
V_{IH}	Input high voltage (SCL, SDA)	1.8 V ≤ V_{CC} < 2.5 V	0.75V_{CC}	6.5	V
	Input high voltage (WC, E0, E1, E2)	1.8 V ≤ V_{CC} < 2.5 V	0.75V_{CC}	V_{CC}+0.6	V
V_{OL}	Output low voltage	I_{OL} = 1 mA, V_{CC} = 1.8 V		0.2	V

1. If the application uses the voltage range R device with 2.5 V < V_{cc} < 5.5 V and -40 °C < TA < +85 °C, please refer to *Table 14* instead of this table.
2. Characterized value, not tested in production
3. The device is not selected after power-up, after a Read instruction (after the Stop condition), or after the completion of the internal write cycle t_W (t_W is triggered by the correct decoding of a Write instruction).

Table 16. DC characteristics (voltage range F)

Symbol	Parameter	Test conditions (in addition to those in tables 9 and 10)(1)	Min.	Max.	Unit
I_{LI}	Input leakage current (E1, E2, SCL, SDA)	$V_{IN} = V_{SS}$ or V_{CC} device in Standby mode		± 2	µA
I_{LO}	Output leakage current	SDA in Hi-Z, external voltage applied on SDA: V_{SS} or V_{CC}		± 2	µA
I_{CC}	Supply current (Read)	V_{CC} = 1.7 V, f_c= 400 kHz		0.8	mA
		f_c= 1 MHz		2.5	mA
I_{CC0}	Supply current (Write)	During t_W, 1.7 V < V_{CC} < 2.5 V		2(2)	mA
I_{CC1}	Standby supply current	Device not selected(3), $V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 1.7 V		1	µA
V_{IL}	Input low voltage (SCL, SDA, WC)	1.7 V ≤ V_{CC} < 2.5 V	–0.45	0.25 V_{CC}	V
V_{IH}	Input high voltage (SCL, SDA)	1.7 V ≤ V_{CC} < 2.5 V	0.75V_{CC}	6.5	V
	Input high voltage (WC, E0, E1, E2)	1.7 V ≤ V_{CC} < 2.5 V	0.75V_{CC}	V_{CC}+0.6	V
V_{OL}	Output low voltage	I_{OL} = 1 mA, V_{CC} = 1.7 V		0.2	V

1. If the application uses the voltage range F device with 2.5 V < V_{cc} < 5.5 V and -40 °C < TA < +85 °C, please refer to *Table 14* instead of this table.
2. Characterized value, not tested in production.
3. The device is not selected after power-up, after a Read instruction (after the Stop condition), or after the completion of the internal write cycle tW (tW is triggered by the correct decoding of a Write instruction).

Table 17. 400 kHz AC characteristics

Test conditions specified in tables 7, 8, 9 and 10					
Symbol	**Alt.**	**Parameter**	**Min.(1)**	**Max.(1)**	**Unit**
f_C	f_{SCL}	Clock frequency		400	kHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	600		ns
t_{CLCH}	t_{LOW}	Clock pulse width low	1300		ns
t_{QL1QL2}(2)	t_F	SDA (out) fall time	20(3)	120	ns
t_{XH1XH2}	t_R	Input signal rise time	(4)	(4)	ns
t_{XL1XL2}	t_F	Input signal fall time	(4)	(4)	ns
t_{DXCX}	$t_{SU:DAT}$	Data in set up time	100		ns
t_{CLDX}	$t_{HD:DAT}$	Data in hold time	0		ns
t_{CLQX}(5)	t_{DH}	Data out hold time	100		ns
t_{CLQV} (6)	t_{AA}	Clock low to next data valid (access time)		900	ns
t_{CHDL}	$t_{SU:STA}$	Start condition setup time	600		ns
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	600		ns
t_{CHDH}	$t_{SU:STO}$	Stop condition set up time	600		ns
t_{DHDL}	t_{BUF}	Time between Stop condition and next Start condition	1300		ns
t_W	t_{WR}	Write time		5	ms
t_{NS}(7)		Pulse width ignored (input filter on SCL and SDA)		80	ns

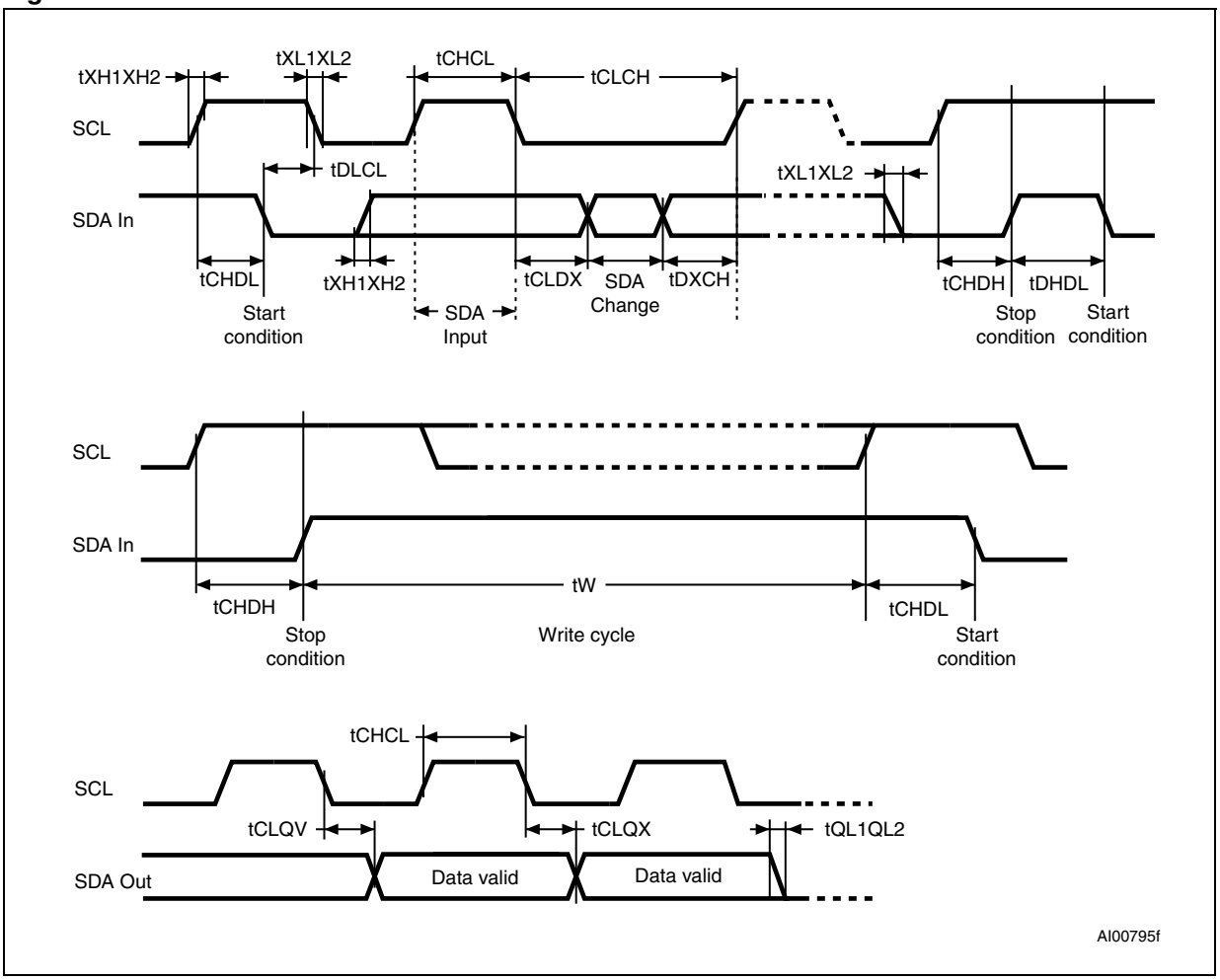
1. All values are referred to V_{IL}(max) and V_{IH}(min).
2. Characterized only, not tested in production.
3. With Cbus = 10 pF.
4. There is no min. or max. values for the input signal rise and fall times. It is however recommended by the I²C-bus specification that the input signal rise and fall times be more than 20 ns and less than 300 ns when f_C < 400 kHz.
5. The I²C-bus specification does not define a min value of the data hold time ($t_{HD:DAT}$). The min value of t_{CLQX} (Data out hold time) of the M24xxx devices offers a safe timing to bridge the undefined region of the falling edge SCL.
6. t_{CLQV} is the time (from the falling edge of SCL) required by the SDA bus line to reach either $0.3V_{CC}$ or $0.7V_{CC}$, assuming that $R_{bus} \times C_{bus}$ time constant is within the values specified in *Figure 5*.
7. Characterized only, not tested in production.

Table 18. 1 MHz AC characteristics(1)

Test conditions specified in tables 7, 8, 9 and 10					
Symbol	**Alt.**	**Parameter**	**Min.(2)**	**Max.(2)**	**Unit**
f_C	f_{SCL}	Clock frequency	0	1	MHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	300	-	ns
t_{CLCH}	t_{LOW}	Clock pulse width low	400	-	ns
t_{XH1XH2}	t_R	Input signal rise time	(3)	(3)	ns
t_{XL1XL2}	t_F	Input signal fall time	(3)	(3)	ns
t_{QL1QL2}(4)	t_F	SDA (out) fall time(5)	20	120	ns
t_{DXCX}	$t_{SU:DAT}$	Data in setup time	80	-	ns
t_{CLDX}	$t_{HD:DAT}$	Data in hold time	0	-	ns
t_{CLQX}(6)	t_{DH}	Data out hold time	50	-	ns
t_{CLQV}(7)	t_{AA}	Clock low to next data valid (access time)		500	ns
t_{CHDL}	$t_{SU:STA}$	Start condition setup time	250	-	ns
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	250	-	ns
t_{CHDH}	$t_{SU:STO}$	Stop condition setup time	250	-	ns
t_{DHDL}	t_{BUF}	Time between Stop condition and next Start condition	500	-	ns
t_W	t_{WR}	Write time	-	5	ms
t_{NS}(4)		Pulse width ignored (input filter on SCL and SDA)	-	50	ns

1. Only new devices identified by the process letter K are qualified at 1 MHz (refer to TN0440 for more).
2. All values are referred to V_{IL}(max) and V_{IH}(min).
3. There is no min. or max. values for the input signal rise and fall times. It is however recommended by the I²C-bus specification that the input signal rise and fall times be less than 120 ns when f_C < 1 MHz.
4. Characterized only, not tested in production.
5. With CL = 10 pF.
6. The I²C-bus specification does not define a min value of the data hold time ($t_{HD:DAT}$). The min value of t_{CLQX} (Data out hold time) of the M24xxx devices offers a safe timing to bridge the undefined region of the falling edge SCL.
7. t_{CLQV} is the time (from the falling edge of SCL) required by the SDA bus line to reach either $0.3V_{CC}$ or $0.7V_{CC}$, assuming that $R_{bus} \times C_{bus}$ time constant is within the values specified in *Figure 6*.

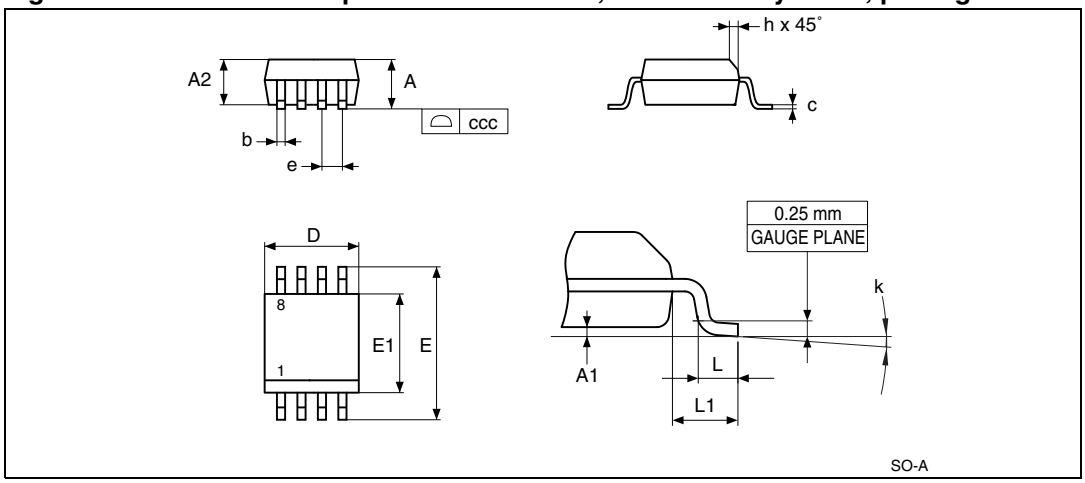
Figure 13. AC waveforms



7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 14. SO8N – 8-lead plastic small outline, 150 mils body width, package outline



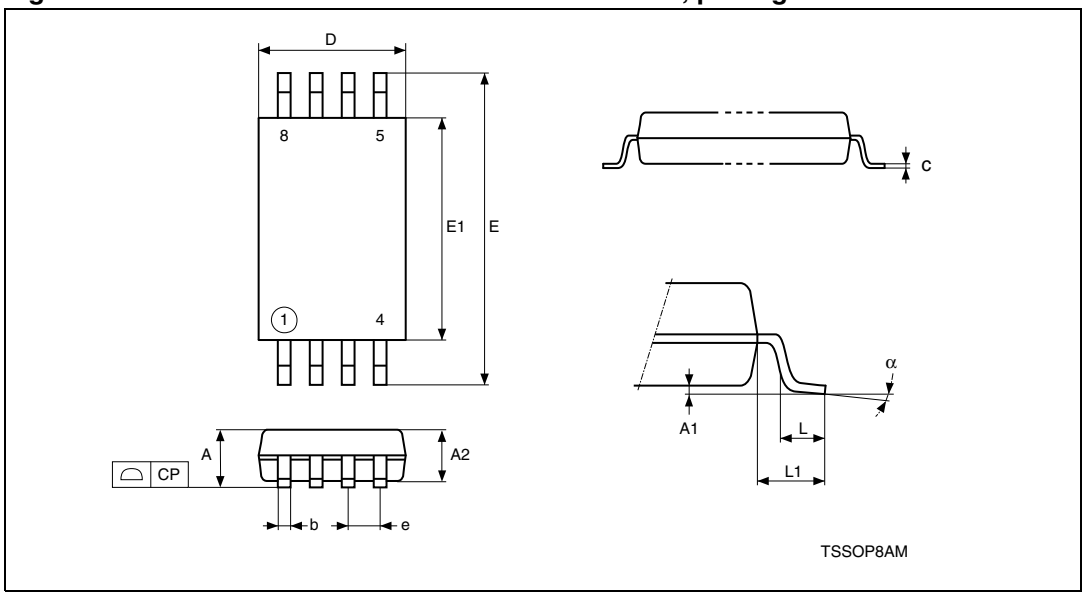
1. Drawing is not to scale.

Table 19. SO8N – 8-lead plastic small outline, 150 mils body width, package mechanical data

Symbol	millimeters			inches(1)		
	Typ	Min	Max	Typ	Min	Max
A			1.75			0.0689
A1		0.1	0.25		0.0039	0.0098
A2		1.25			0.0492	
b		0.28	0.48		0.011	0.0189
c		0.17	0.23		0.0067	0.0091
ccc			0.1			0.0039
D	4.9	4.8	5	0.1929	0.1890	0.1969
E	6	5.8	6.2	0.2362	0.2283	0.2441
E1	3.9	3.8	4	0.1535	0.1496	0.1575
e	1.27	-	-	0.05	-	-
h		0.25	0.5		0.0098	0.0197
k		0°	8°		0°	8°
L		0.4	1.27		0.0157	0.05
L1	1.04			0.0409		

1. Values in inches are converted from mm and rounded to four decimal digits.

Figure 15. TSSOP8 – 8-lead thin shrink small outline, package outline



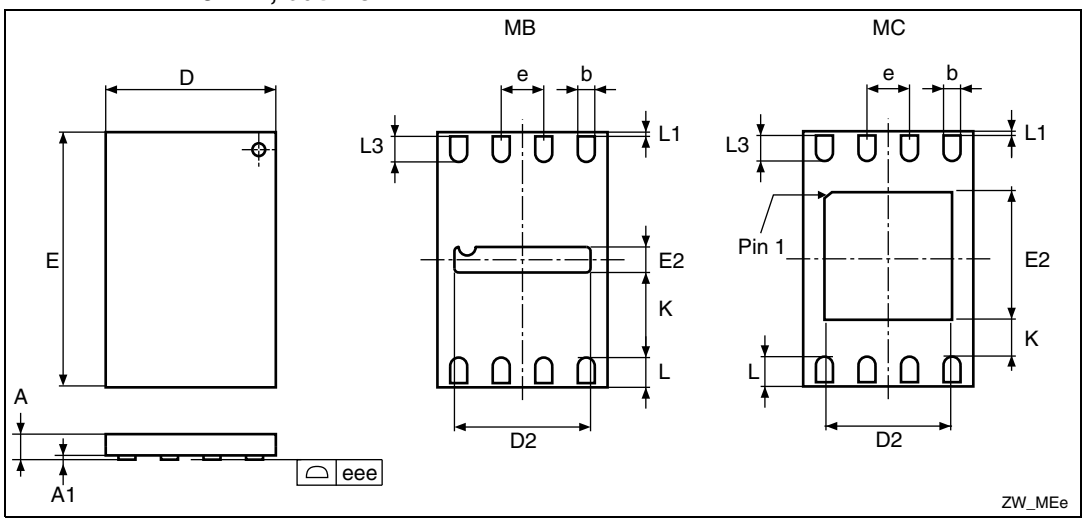
1. Drawing is not to scale.

Table 20. TSSOP8 – 8-lead thin shrink small outline, package mechanical data

Symbol	millimeters			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1		0.050	0.150		0.0020	0.0059
A2	1.000	0.800	1.050	0.0394	0.0315	0.0413
b		0.190	0.300		0.0075	0.0118
c		0.090	0.200		0.0035	0.0079
CP			0.100			0.0039
D	3.000	2.900	3.100	0.1181	0.1142	0.1220
e	0.650	–	–	0.0256	–	–
E	6.400	6.200	6.600	0.2520	0.2441	0.2598
E1	4.400	4.300	4.500	0.1732	0.1693	0.1772
L	0.600	0.450	0.750	0.0236	0.0177	0.0295
L1	1.000			0.0394		
α		0°	8°		0°	8°
N	8			8		

1. Values in inches are converted from mm and rounded to four decimal digits.

Figure 16. UFDFPN8 (MLP8) 8-lead ultra thin fine pitch dual flat package no lead 2 x 3 mm, outline



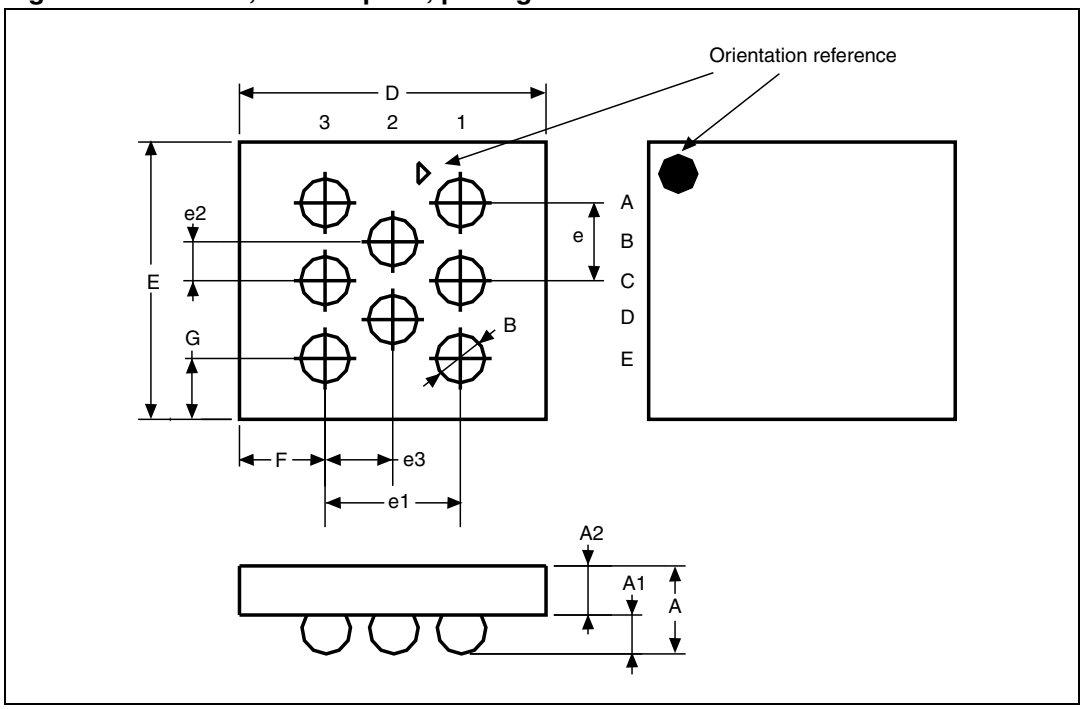
1. Drawing is not to scale.
2. The central pad (E2 × D2 area in the above illustration) is internally pulled to V_{SS}. It must not be allowed to be connected to any other voltage or signal line on the PCB, for example during the soldering process.
3. The circle in the top view of the package indicates the position of pin 1.

Table 21. UFDFPN8 (MLP8) 8-lead ultra thin fine pitch dual flat package no lead 2 x 3 mm, mechanical data

Symbol	millimeters			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A	0.550	0.450	0.600	0.0217	0.0177	0.0236
A1	0.020	0.000	0.050	0.0008	0.0000	0.0020
b	0.250	0.200	0.300	0.0098	0.0079	0.0118
D	2.000	1.900	2.100	0.0787	0.0748	0.0827
D2 (rev MB)	1.600	1.500	1.700	0.0630	0.0591	0.0669
D2 (rev MC)		1.200	1.600		0.0472	0.0630
E	3.000	2.900	3.100	0.1181	0.1142	0.1220
E2 (rev MB)	0.200	0.100	0.300	0.0079	0.0039	0.0118
E2 (rev MC)		1.200	1.600		0.0472	0.0630
e	0.500			0.0197		
K		0.300			0.0118	
L		0.300	0.500		0.0118	0.0197
L1			0.150			0.0059
L3		0.300			0.0118	
eee[2]		0.080			0.0031	

1. Values in inches are converted from mm and rounded to four decimal digits.
2. Applied for exposed die paddle and terminals. Exclude embedding part of exposed die paddle from measuring.

Figure 17. WLCSP, 0.5 mm pitch, package outline



1. Drawing is not to scale.

Table 22. WLCSP 0.5 mm pitch, package mechanical data(1)

Symbol	Millimeters			Inches(2)		
	Typ	Min	Max	Typ	Min	Max
A	0.60	0.55	0.65	0.0236	0.0217	0.0256
A1	0.245	0.22	0.27	0.0096	0.0087	0.0106
A2	0.355	0.330	0.380	0.0140	0.0130	0.0150
B	Ø 0.311			Ø 0.0122		
D	1.97	1.95	1.99	0.0776	0.0768	0.0783
E	1.785	1.765	1.805	0.0703	0.0695	0.0711
e	0.5			0.0197		
e1	0.866			0.0341		
e2	0.25			0.0098		
e3	0.433			0.0170		
F	0.552	0.502	0.602	0.0217	0.0198	0.0237
G	0.392	0.342	0.442	0.0154	0.0135	0.0174
N(3)	8			8		

1. Preliminary data.
2. Values in inches are converted from mm and rounded to four decimal digits.
3. N is the total number of terminals.

8 Part numbering

Table 23. Ordering information scheme

Example: M24256–B W MW 6 T P /AB

Device type
M24 = I^2C serial access EEPROM

Device function
256– = 256 Kbit (32 Kb × 8)

Device family
B: Without Identification page
D: With additional Identification page

Operating voltage
W = V_{CC} = 2.5 to 5.5 V
R = V_{CC} = 1.8 to 5.5 V
F = V_{CC} = 1.7 to 5.5 V

Package
MN = SO8 (150 mils body width)
DW = TSSOP8
MB or MC = UFDFPN8 (MLP8)
CS = WLCSP

Device grade
6 = Industrial temperature range, –40 to 85 °C. Device tested with standard test flow
3 = Automotive: device tested with high reliability certified flow(1)
over –40 to 125 °C

Option
blank = standard packing
T = tape and reel packing

Plating technology
P or G = ECOPACK® (RoHS compliant)

Process
/A = F8L process (for WLCSP package ordering only)
/AB = F8L process (for device grade 3 ordering only)

1. ST strongly recommends the use of the Automotive Grade devices for use in an automotive environment. The High Reliability Certified Flow (HRCF) is described in the quality note QNEE9801. Please ask your nearest ST sales office for a copy.

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

9 Revision history

Table 24. Document revision history

Date	Revision	Changes
29-Jan-2001	1.1	Lead Soldering Temperature in the Absolute Maximum Ratings table amended Write Cycle Polling Flow Chart using ACK illustration updated LGA8 and SO8(wide) packages added References to PSDIP8 changed to PDIP8, and Package Mechanical data updated
10-Apr-2001	1.2	LGA8 Package Mechanical data and illustration updated SO16 package removed
16-Jul-2001	1.3	LGA8 Package given the designator “LA”
02-Oct-2001	1.4	LGA8 Package mechanical data updated
13-Dec-2001	1.5	Document becomes Preliminary Data Test conditions for ILI, ILO, ZL and ZH made more precise VIL and VIH values unified. tNS value changed
12-Jun-2001	1.6	Document promoted to Full Datasheet
22-Oct-2003	2.0	Table of contents, and Pb-free options added. Minor wording changes in Summary Description, Power-On Reset, Memory Addressing, Write Operations, Read Operations. V_{IL}(min) improved to –0.45V.
02-Sep-2004	3.0	LGA8 package is Not for New Design. 5V and -S supply ranges, and Device Grade 5 removed. Absolute Maximum Ratings for V_{IO}(min) and V_{CC}(min) changed. Soldering temperature information clarified for RoHS compliant devices. Device grade information clarified. AEC-Q100-002 compliance. V_{IL} specification unified for SDA, SCL and WC
22-Feb-2005	4.0	*Initial delivery state* is FFh (not necessarily the same as Erased). LGA package removed, TSSOP8 and SO8N packages added (see *Package mechanical data* section and *Table 23: Ordering information scheme*). Voltage range R (1.8V to 5.5V) also offered. Minor wording changes. Z_L Test Conditions modified in *Table 11: Input parameters* and Note *2* added. I_{CC} and I_{CC1} values for V_{CC} = 5.5V added to *Table 13: DC characteristics (voltage range W)*. Note added to *Table 13: DC characteristics (voltage range W)*. *Power On Reset* paragraph specified. t_W max value modified in *Table 16: 400 kHz AC characteristics* and note 4 added. Plating technology changed in *Table 23: Ordering information scheme*. Resistance and capacitance renamed in *Figure 6*.

Table 24. Document revision history (continued)

Date	Revision	Changes
05-May-2006	5	*Power On Reset* paragraph replaced by *Section 2.6: Supply voltage (V_{CC})*. *Figure 4: Device select code* added. *ECC (error correction code) and write cycling* added and specified at 1 Million cycles. I_{CC0} added and I_{CC1} specified over the whole voltage range in *Table 13* and *Table 14*. PDIP8 package removed. Packages are ECOPACK® compliant. Small text changes.
16-Oct-2006	6	M24256-BW and M24256-BR part numbers added. *Section 3.11: ECC (error correction code) and write cycling* updated. I_{CC} and I_{CC1} modified in *Table 14: DC characteristics (voltage range R)*. t_W modified in *Table 16: 400 kHz AC characteristics*. SO8Narrow package specifications updated (see *Table 19* and *Figure 14*). Blank option removed from below *Plating technology* in *Table 23: Ordering information scheme*.
02-Jul-2007	7	*Section 2.6: Supply voltage (V_{CC})* modified. *Section 3.11: ECC (error correction code) and write cycling* modified. JEDEC standard and European directive references corrected below *Table 6: Absolute maximum ratings*. Rise/fall time conditions modified for I_{CC} and V_{IH} max modified in *Table 13: DC characteristics (voltage range W)* and *Table 14: DC characteristics (voltage range R)* Note 1 removed from *Table 13: DC characteristics (voltage range W)*. SO8W package specifications modified in *Section 7: Package mechanical data*. *Table 25: Available M24256-BR, M24256-BW, M24256-BF products (package, voltage range, temperature grade)* and *Table 26: Available M24512-x products (package, voltage range, temperature grade)* added.
16-Oct-2007	8	*Section 2.5: V_{SS} ground* added. Small text changes. V_{IO} max changed and *Note 1* updated to latest standard revision in *Table 6: Absolute maximum ratings*. Note removed from *Table 11: Input parameters*. V_{IH} min and V_{IL} max modified in *Table 14: DC characteristics (voltage range R)*. Removed t_{CH1CH2}, t_{CL1CL2} and t_{DH1DH2}, and added t_{XL1XL2}, t_{DL1DL2} and *Note 3* in *Table 16: 400 kHz AC characteristics*. t_{XH1XH2}, t_{XL1XL2} and *Note 2* added to *Table 17: 1 MHz AC characteristics*. *Figure 13: AC waveforms* modified. Package mechanical data inch values calculated from mm and rounded to 4 decimal digits (see *Section 7: Package mechanical data*).

Table 24. Document revision history (continued)

Date	Revision	Changes
14-Dec-2007	9	1 MHz frequency introduced (M24512-HR root part number). *Section 2.6.3: Device reset* modified. *Figure 5: I^2C Fast mode (f_C = 400 kHz): maximum R_{bus} value versus bus parasitic capacitance (C_{bus})* modified, *Figure 6: I^2C Fast mode Plus (f_C = 1 MHz): maximum R_{bus} value versus bus parasitic capacitance (C_{bus})* added. t_{NS} moved from *Table 11* to *Table 16*. I_{LO} test conditions modified in *Table 13*. *Table 14: DC characteristics (voltage range R)* and *Table 17: 1 MHz AC characteristics* modified. Small text changes.
27-Mar-2008	10	Small text changes. M24256-BHR root part number added. *Section 2.6.3: Device reset on page 9* updated. *Figure 6: I^2C Fast mode Plus (f_C = 1 MHz): maximum R_{bus} value versus bus parasitic capacitance (C_{bus}) on page 10* updated. Caution removed in *Section 3.11: ECC (error correction code) and write cycling*.
22-Apr-2008	11	M24512-W and M24256-BW offered in the device grade 3 option (automotive temperature range): – *Table 7: Operating conditions (voltage range W)*, – *Table 13: DC characteristics (voltage range W)*, – /AB Process letters added to *Table 23: Ordering information scheme*, – *Table 25: Available M24256-BR, M24256-BW, M24256-BF products (package, voltage range, temperature grade)* and – *Table 26: Available M24512-x products (package, voltage range, temperature grade)* updated accordingly). Small text changes.
22-Dec-2008	12	WLCSP package added (see *Figure 3: WLCSP connections (top view, marking side, with balls on the underside)* and *Section 7: Package mechanical data*).
21-Jan-2009	13	M24256-BF part number added (V_{CC} = 1.7 V to 5.5 V voltage range added, see *Table 9*, *Table 15*, *Table 16* and *Table 25*). I_{CC1} test conditions modified in *Table 13: DC characteristics (voltage range W)*, *Table 14: DC characteristics (voltage range R)* and *Table 15: DC characteristics (voltage range F)*.
05-Jun-2009	14	M24512-DR part number and Identification page feature added. Command replaced by instruction in the whole document. UFDFPN8 added. *Figure 6* updated. *Section 2.6.2: Power-up conditions* and *Section 2.6.3: Device reset* updated. t_{CLQX} and t_{CLQV} updated in *Table 16*, *Note 5* and *Note 8* added. t_{CLQX} and t_{CLQV} updated in *Table 17*, *Note 6* and *Note 9* added. *Section 8: Part numbering* updated. Reference to the SURE program removed in *Section 5: Maximum rating*. Previous 1 MHz M24512-HR and M24512-BHR devices replaced by new M24512-R and M24256-BR (process letter K).

Table 24. Document revision history (continued)

Date	Revision	Changes
16-Jun-2009	15	Part numbers updated in cover page header.
20-Aug-2009	16	I_{OL} added to *Table 7: Operating conditions (voltage range W)*. Note 1and I_{CC} modified in *Table 13: DC characteristics (voltage range W)*; Note and I_{CC} modified in *Table 14: DC characteristics (voltage range R)*;
13-Oct-2009	17	Datasheet split to leave only devices with 256 Kbit capacity. M24256-DR part number added (see *Table 26: Available M24256-DR products (package, voltage range, temperature grade)*. *Figure 4: Device select code* and *Figure 5: I^2C Fast mode (f_C = 400 kHz): maximum R_{bus} value versus bus parasitic capacitance (C_{bus})* updated. V_{IO} max modified in *Table 6: Absolute maximum ratings*. V_{IH} modified in *Table 13: DC characteristics (voltage range W)*, *Table 14: DC characteristics (voltage range R)* and *Table 15: DC characteristics (voltage range F)*. In *Table 16: 400 kHz AC characteristics* and *Table 17: 1 MHz AC characteristics*: – t_{DL1DL2} changed to t_{QL1QL2} – t_{CHDX} changed to t_{CHDL} – t_{XH1XH2} and t_{XL1XL2} values removed – Notes modified *Figure 13: AC waveforms* modified.
05-Nov-2009	18	*Section 3.9: Write Identification Page (M24256-D only)* corrected.*Section 3.17: Reading the Identification Page (M24256-D only)* clarified.
10-Dec-2009	19	UFDFPN8 package is now offered (see *Section 7: Package mechanical data*, *Table 23: Ordering information scheme* and *Table 25: Available M24256-BR, M24256-BW, M24256-BF products (package, voltage range, temperature grade)*.
19-Jan-2010	20	Revision number corrected at bottom of pages.
04-Mar-2010	21	Process description corrected in *Table 23: Ordering information scheme*.
21-Dec-2010	22	Updated text in: *Features*, *Section 1: Description*, *Section 3.1: Start condition*, *Section 3.6: Write operations*, *Section 3.9: Write Identification Page (M24256-D only)*, *Section 3.10: Lock Identification Page (M24256-D only)*, *Section 3.11: ECC (error correction code) and write cycling*, *Section 3.17: Reading the Identification Page (M24256-D only)*, *Section 3.18: Reading the lock status (M24256-D only)*, *Table 10: AC test measurement conditions*, *Section 8: Part numbering*. Updated the following according to the I²C_bus specification: *Table 17: 400 kHz AC characteristics*, *Table 18: 1 MHz AC characteristics*, *Figure 13: AC waveforms*.

Table 24. Document revision history (continued)

Date	Revision	Changes
14-Feb-2011	23	Added caution under *Figure 3: WLCSP connections (top view, marking side, with balls on the underside)*. Updated: – *Description* – *Section 3.5: Addressing the memory array* – *Section 3.17: Reading the Identification Page (M24256-D only)* – *Section 3.18: Reading the lock status (M24256-D only)* – *Table 2: Most significant address byte* – *Table 6: Absolute maximum ratings* – *Table 17: 400 kHz AC characteristics* – *Table 18: 1 MHz AC characteristics* Moved: – *Table 2: Most significant address byte* from *Section 2.6.4* to *Section 3.5* Deleted: – *Table 3: Device select code to access the Identification page (M24256-DR only)* – *Table 25: Available M24256-BR, M24256-BW, M24256-BF products (package, voltage range, temperature grade)* – *Table 26: Available M24256-DR products (package, voltage range, temperature grade)*
05-Jul-2011	24	Added *Table 12: Memory cell characteristics*. Updated: – *Section 1: Description* – *Table 6: Absolute maximum ratings* – I_{CC0} maximum value in *Table 14: DC characteristics (voltage range W, device grade 6)*, *Table 15: DC characteristics (voltage range R)* and *Table 16: DC characteristics (voltage range F)* Deleted all references to package SO8 (MW) 208 mils width.
16-Nov-2011	25	Updated UFDFPN8 silhouette on cover page, *Figure 16: UFDFPN8 (MLP8) 8-lead ultra thin fine pitch dual flat package no lead 2 x 3 mm, outline* and *Table 21: UFDFPN8 (MLP8) 8-lead ultra thin fine pitch dual flat package no lead 2 x 3 mm, mechanical data* to add MC version.

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