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PCN# : P257A
Issue Date : Jun. 25, 2012

DESIGN/PROCESS CHANGE NOTIFICATION

This is to inform you that a change is being made to the products listed below.

Unless otherwise indicated in the details of this notification, the identified change will have no impact on product quality, reliability, electrical, visual or mechanical performance and affected products will remain fully compliant to all published specifications. Products incorporating this change may be shipped interchangeably with existing unchanged products.

This change is planned to take effect in 90 calendar days from the date of this notification. Please work with your local Fairchild Sales Representative to manage your inventory of unchanged product if your evaluation of this change will require more than 90 calendar days.

Please contact your local Customer Quality Engineer within 30 days of receipt of this notification if you require any additional data or samples. Alternatively, you may send an email request for data, samples or other information to PCNSupport@fairchildsemi.com.

Implementation of change:

Expected First Shipment Date for Changed Product : Sep. 23, 2012

Expected First Date Code of Changed Product :1238

Description of Change (From) :
The products identified in the affected FSID list assembled at Fairchild Semiconductor in Suzhou, China(FSSZ).

Description of Change (To) :

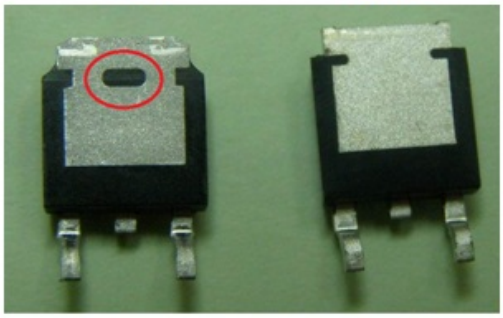
GEM Electronics Shanghai, China is qualified to produce the products identified in the affected FSID section on this PCN. GEM Electronics Shanghai, China has been a qualified assembly and test manufacturer for Fairchild since 2003.

BOM comparison between GEM and FSSZ:

Process/Material	GEM	FSSZ
Lead frame	Bare Cu	Bare Cu
Die attach material	Soft solder	Soft solder
Wire bonding material	Al wire	Al wire
Mold material	G631	EME6600CS

D-pak Package visual comparison as below:

GEM FSSZ



Note: There is a slot hole on GEM heat sink surface compared with Fairchild Suzhou (FSSZ) product. There is no impact to the application.

Reason for Change:
To have an alternate assembly and test site to increase manufacturing capacity.

Affected Product(s):

FDD050N03B	FDD10AN06A0	FDD120AN15A0
FDD13AN06A0	FDD16AN08A0	FDD850N10L
FFD20UP20S	FQD10N20CTM	FQD11P06TM
FQD12N20LTM	FQD12N20TM	FQD13N06LTM
FQD13N06TM	FQD13N10LTM	FQD13N10LTM_G
FQD13N10TM	FQD16N25CTM	FQD17P06TM
FQD19N10LTM	FQD19N10TM	FQD20N06TM
FQD2P40TM	FQD4N20TM	FQD4N25TM_WS
FQD4P25TM_WS	FQD5N20LTM	FQD5P10TM
FQD5P20TM	FQD6N25TM	FQD6N40CTM
FQD7N10LTM	FQD7N20LTM	FQD7P06TM
FQD7P20TM	FQD8P10TM	FQD9N25TM
HGTD1N120BNS9A	HGTD7N60C3S9A	HUF75321D3ST
HUF75329D3ST	HUF76407D3ST	HUF76609D3ST
HUF76629D3ST	RFD12N06RLESM9A	RFD14N05LSM
RFD14N05LSM9A	RFD14N05SM9A	RFD16N05LSM9A
RFD16N05SM9A	RFD16N06LESM9A	RFD3055LESM9A
RURD620CCS9A		

Qualification Plan	Device	Package	Process	No. of Lots
QP11041815	FDD16AN08A0	DPAK	Mosfet	1

Test Description:	Condition:	Standard :	Duration:	Results:
MSL1 Precondition	260C, 3 cycles	JESD22-A113		0/154
High Temperature Reverse Bias Test	175°C Tj, 80% of Rated BV	JESD22-A108	1000 hrs	0/77
High Temperature Gate Bias Test	175°C Tj, 100% of rated VGS	JESD22-A108	1000 hrs	0/77
Temperature Cycle	-65C, 150C	JESD22-A104	500 cycles	0/77
Temperature Humidity Bias Test	85°C, 85% RH , 80% of Rated BV (Max=100V)	JESD22-A101	1000 hrs	0/77
High Temperature Storage Life	150C	JESD22-A103	1000 hrs	0/77
Power Cycle	125°C TJC, delta Tj of 100 C, 2 min on, 2 min off	JESD22-A122	10k cycles	0/77

Qualification Plan	Device	Package	Process	No. of Lots
QP11041815	FQD6N40CTM	DPAK	Mosfet	1

Test Description:	Condition:	Standard :	Duration:	Results:
MSL1 Precondition	260C, 3 cycles	JESD22-A113		0/154
High Temperature Reverse Bias Test	150°C Tj, 80% of Rated BV	JESD22-A108	1000 hrs	0/77
High Temperature Gate Bias Test	150°C Tj, 100% of rated VGS	JESD22-A108	1000 hrs	0/77
Temperature Cycle	-65C, 150C	JESD22-A104	500 cycles	0/77
Temperature Humidity Bias Test	85°C, 85% RH , 80% of Rated BV (Max=100V)	JESD22-A101	1000 hrs	0/77
High Temperature Storage Life	150C	JESD22-A103	1000 hrs	0/77
Power Cycle	125°C TJC, delta Tj of 100 C, 2 min on, 2 min off	JESD22-A122	10k cycles	0/77

Qualification Plan	Device	Package	Process	No. of Lots
QP11041815	HUF75329D3ST	DPAK	Mosfet	1

Test Description:	Condition:	Standard :	Duration:	Results:
MSL1 Precondition	260C, 3 cycles	JESD22-A113		0/154
High Temperature Reverse Bias Test	175°C Tj, 80% of Rated BV	JESD22-A108	1000 hrs	0/77
High Temperature Gate Bias Test	175°C Tj, 100% of rated VGS	JESD22-A108	1000 hrs	0/77
Temperature Cycle	-65C, 150C	JESD22-A104	500 cycles	0/77
Temperature Humidity Bias Test	85°C, 85% RH , 80% of Rated BV(Max=100V)	JESD22-A101	1000 hrs	0/77
High Temperature Storage Life	150C	JESD22-A103	1000 hrs	0/77
Power Cycle	125°C TJC, delta Tj of 100 C, 2 min on, 2 min off	JESD22-A122	10k cycles	0/77

Qualification Plan	Device	Package	Process	No. of Lots
QP11041815	HGTD1N120BNS9A	DPAK	Mosfet	1

Test Description:	Condition:	Standard :	Duration:	Results:
MSL1 Precondition	260C, 3 cycles	JESD22-A113		0/154
High Temperature Reverse Bias Test	150°C Tj, 80% of Rated BV	JESD22-A108	1000 hrs	0/77
High Temperature Gate Bias Test	150°C Tj, 100% of rated VGS	JESD22-A108	1000 hrs	0/77
Temperature Cycle	-65C, 150C	JESD22-A104	500 cycles	0/77
Temperature Humidity Bias Test	85°C, 85% RH , 80% of Rated BV (Max=100V)	JESD22-A101	1000 hrs	0/77
High Temperature Storage Life	150C	JESD22-A103	1000 hrs	0/77
Power Cycle	125°C TJC, delta Tj of 100 C, 2 min on, 2 min off	JESD22-A122	10k cycles	0/77

Qualification Plan	Device	Package	Process	No. of Lots
QP11041815	RURD620CCS9A	DPAK	Diode	1

Test Description:	Condition:	Standard :	Duration:	Results:
MSL1 Precondition	260C, 3 cycles	JESD22-A113		0/154
High Temperature Reverse Bias Test	175°C Tj, 80% of Rated BV	JESD22-A108	1000 hrs	0/77
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