Product Change Notification / SYST-24YYJU400

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25-Mar-2022

Product Category:

8-bit Microcontrollers

PCN Type:

Document Change

Notification Subject:

ERRATA - AVR128DB28/32/48/64 Silicon Errata and Data Sheet Clarifications Errata Document Revision

Affected CPNs:

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SYST-24YYJU400_Affected_CPN_03252022.csv

Notification Text:

SYST-24YYJU400

Microchip has released a new Product Documents for the AVR128DB28/32/48/64 Silicon Errata and Data Sheet Clarifications of devices. If you are using one of these devices please read the document located at AVR128DB28/32/48/64 Silicon Errata and Data Sheet Clarifications.

Notification Status: Final

Description of Change:
Document: General editorial updates.
Added errata:

- Device: 2.2.3. CRC Check During Reset Initialization Is not Functional
- CLKCTRL: 2.5.3. PLL Status not Working as Expected
- DAC: 2.6.1. DAC Output Buffer Lifetime Drift
- NVMCTRL: 2.7.1. Flash Multi-Page Erase Can Erase Write Protected Section
- TCA: 2.11.1. Restart Will Reset Counter Direction in NORMAL and FRQ Mode
- TCD: 2.13.3. Halting TCD and Waiting for SW Restart Does Not Work if Compare Value A is 0 or Dual Slope Mode is Used
- TWI: 2.14.2. Flush Non-Functional

Updated Errata:

- 2.15.2. Start-of-Frame Detection Can Unintentionally Be Triggered in Active Mode

Added data sheet clarifications:

- 3.1.1. Features
- 3.1.2. FUSE - Configuration and User Fuses - SYSCFG0
- 3.1.3. Peripherals and Architecture - REVID
- 3.2.1. Voltage Regulator Control (VREGCTRL)
- 3.3.1. Single-Shot Mode
- 3.4.1. Analog Comparator Interrupt Control
- 3.5.1. DAC Output
- 3.6.1. Electrical Characteristics - Memory Programming Specifications

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 25 March 2022

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

AVR128DB28/32/48/64 Silicon Errata and Data Sheet Clarifications

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

AVR128DB28-E/SP
AVR128DB28-E/SS
AVR128DB28-E/SO
AVR128DB28-I/SP
AVR128DB28-I/SS
AVR128DB28-I/SO
AVR128DB28T-I/SS
AVR128DB28T-I/SO
AVR128DB28T-E/SS
AVR128DB28T-E/SO
AVR128DB32-E/RXB
AVR128DB32-E/PT
AVR128DB32-I/RXB
AVR128DB32-I/PT
AVR128DB32T-I/RXB
AVR128DB32T-I/PT
AVR128DB32T-E/RXB
AVR128DB32T-E/PT
AVR128DB48-E/6LX
AVR128DB48-E/PT
AVR128DB48-I/6LX
AVR128DB48-I/PT
AVR128DB48T-I/6LX
AVR128DB48T-I/PT
AVR128DB48T-E/6LX
AVR128DB48T-E/PT
AVR128DB64-E/MR
AVR128DB64-E/PT
AVR128DB64-I/MR
AVR128DB64-I/PT
AVR128DB64T-I/MR
AVR128DB64T-I/PT
AVR128DB64T-E/MR
AVR128DB64T-E/PT

AVR128DB28/32/48/64

Silicon Errata and Data Sheet Clarifications

The AVR128DB28/32/48/64 devices you have received conform functionally to the current device data sheet (www.microchip.com/DS40002247), except for the anomalies described in this document. The errata described in this document will likely be addressed in future revisions of the AVR128DB28/32/48/64 devices.

Notes:

- This document summarizes all the silicon errata issues from all the silicon revisions, previous and current
- Refer to the Device/Revision ID section in the current device data sheet (www.microchip.com/DS40002247) for more detailed information on Device Identification and Revision IDs for your specific device, or contact your local Microchip sales office for assistance

1. Silicon Issue Summary

Legend

- **-** Erratum is not applicable.
- **X** Erratum is applicable.

Peripheral	Short Description	Valid for Silicon Revision	
		Rev. A4(1)	Rev. A5
Device	2.2.1. Some Reserved Fuse Bits Are '1'	X	-
	2.2.2. Increased Current Consumption May Occur When VDD Drops	X	X
	2.2.3. CRC Check During Reset Initialization Is not Functional	X	-
ADC	2.3.1. Increased Offset in Single-Ended Mode	X	-
CCL	2.4.1. The CCL Must be Disabled to Change the Configuration of a Single LUT	X	X
	2.4.2. The LINK Input Source Selection for LUT3 Is not Functional on 28- and 32-Pin Devices	X	-
CLKCTRL	2.5.1. External Clock/Crystal Status Bit is Not Set When the External Clock Source is Ready	X	-
	2.5.2. RUNSTDBY is Not Functional When Using External Clock Sources	X	-
	2.5.3. PLL Status not Working as Expected	X	X
	2.5.4. The PLL Will Not Run when Using XOSCHF with an External Crystal	X	X
DAC	2.6.1. DAC Output Buffer Lifetime Drift	X	X
NVMCTRL	2.7.1. Flash Multi-Page Erase Can Erase Write Protected Section	X	X
OPAMP	2.8.1. OPAMP Consume More Power Than Expected	X	-
	2.8.2. The Input Range Select is Read-Only	X	-
PORT	2.9.1. PD0 Input Buffer is Floating	X	X
RSTCTRL	2.10.1. BOD Registers not Reset When UPDI Is Enabled	X	-
TCA	2.11.1. Restart Will Reset Counter Direction in NORMAL and FRQ Mode	X	X
TCB	2.12.1. CCMP and CNT Registers Act as 16-Bit Registers in 8-Bit PWM Mode	X	X
TCD	2.13.1. Asynchronous Input Events not Working When TCD Counter Prescaler Is Used	X	X
	2.13.2. CMPAEN Controls All WOx for Alternative Pin Functions	X	X
	2.13.3. Halting TCD and Waiting for SW Restart Does Not Work if Compare Value A is 0 or Dual Slope Mode is Used	X	X
TWI	2.14.1. The Output Pin Override Does not Function as Expected	X	X
	2.14.2. Flush Non-Functional	X	X

.....continued			
Peripheral	Short Description	Valid for Silicon Revision	
		Rev. A4(1)	Rev. A5
USART	2.15.1. Open-Drain Mode Does not Work When TXD Is Configured as Output	X	X
	2.15.2. Start-of-Frame Detection Can Unintentionally Be Triggered in Active Mode	X	X
ZCD	2.16.1. All ZCD Output Selection Bits Are Tied to the ZCD0 Bit	X	-

Note:

1. This revision is the initial release of the silicon.

2. Silicon Errata Issues

2.1 Errata Details

-	Erratum is not applicable.
X	Erratum is applicable.

2.2 Device

2.2.1 Some Reserved Fuse Bits Are '1'

For material with date code 2021 (manufactured in the year 2020, week 21) or older, the default fuse values are not compliant with the data sheet. The fuse values will read out as listed below:

- BODCFG = `0x10`
- OSCCFG = `0x78` (Device will use the OSCHF clock source)
- SYSCFG0 = `0xF6`
- SYSCFG1 = `0xE8`

Work Around

None.

Affected Silicon Revisions

Rev. A4	Rev. A5
X	-

2.2.2 Increased Current Consumption May Occur When V_{DD} Drops

The device may experience increased current consumption of approximately 1.5 mA if V_{DD} drops below 2.1V and is held in the range of 1.9-2.1V. This will only occur if V_{DD} is originally at a higher level and then drops down to the mentioned voltage range.

Work Around

Ensure V_{DD} is always kept above 2.1V by setting the BOR trigger level to 2.2V to keep the device from executing if V_{DD} drops towards the affected voltage range. If operation in voltage range 1.9-2.1V is required, make sure V_{DD} does not rise above 2.1V and then drops down again. Note that the voltage levels given are not absolute values but typical values.

Affected Silicon Revisions

Rev. A4	Rev. A5
X	X

2.2.3 CRC Check During Reset Initialization Is not Functional

For material with date code 2048 (manufactured in the year 2020, week 48) or older, the CRCSRC bit field in the SYSCFG0 fuse is ignored during Reset initialization. A CRC check will not be performed during Reset initialization. CRCSCAN is only available from the software.

Work Around

None.

Affected Silicon Revisions

Rev. A4	Rev. A5
X	-

2.3 ADC - Analog-to-Digital Converter

2.3.1 Increased Offset in Single-Ended Mode

The ADC result has a typical offset of -3 mV (V_{DD} = 3.0V, temp. = 25°C) when the ADC is operating in Single-Ended mode. The typical offset drift vs. V_{DD} is -0.3 mV/V, and the typical offset drift vs. temperature is -0.02 mV/°C.

Work Around

To reduce the offset, use the ADC in Differential mode and connect the negative ADC input pin externally to GND.

Affected Silicon Revisions

Rev. A4	Rev. A5
X	-

2.4 CCL - Configurable Custom Logic

2.4.1 The CCL Must be Disabled to Change the Configuration of a Single LUT

To reconfigure an LUT, the CCL peripheral must first be disabled (write ENABLE in CCL.CTRLA to '0'). Writing ENABLE to '0' will disable all the LUTs, and affects the LUTs not under reconfiguration.

Work Around

None

Affected Silicon Revisions

Rev. A4	Rev. A5
X	X

2.4.2 The LINK Input Source Selection for LUT3 Is not Functional on 28- and 32-Pin Devices

The LINK option (INSELn in LUT3CTRLB or LUT3CTRLC is '0x2') does not work; the output from LUT0 will not get connected as an input to LUT3. This occurs only on 28-pin and 32-pin devices.

Work Around

Connect LUT0 output to LUT3 input using the Event System.

Affected Silicon Revisions

Rev. A4	Rev. A5
X	-

2.5 CLKCTRL - Clock Controller

2.5.1 External Clock/Crystal Status Bit is Not Set When the External Clock Source is Ready

If an external clock source is selected (SELHF in XOSCHFCTRLA is '1') and the Run Standby (RUNSTDBY) bit in XOSCHFCTRLA is '1' without the clock source being requested, the External Clock/Crystal Status (EXTS) bit will not be set to '1' when the external clock source is ready.

Work Around
Request the clock from RTC or TCD before checking the EXTS bit.

Affected Silicon Revisions

Rev. A4	Rev. A5
X	-

2.5.2 RUNSTDBY is Not Functional When Using External Clock Sources

When using any of the External Clock Sources, the related Run Standby (RUNSTDBY) bit, found in the XOSC32KCTRLA register, will not force the oscillator source to stay on during sleep modes.

Work Around
Enable a peripheral, with the external oscillator as the clock source, to keep the clock source active during sleep modes.

Affected Silicon Revisions

Rev. A4	Rev. A5
X	-

2.5.3 PLL Status not Working as Expected

The PLL Status (PLLS) bit in the Main Clock Status (MCLKSTATUS) register will never be set to '1' if the Run Standby (RUNSTDBY) bit in PLL Control A (PLLCTRLA) register is set to '1' and no peripherals are requesting the PLL oscillator.

Work Around
None.

Affected Silicon Revisions

Rev. A4	Rev. A5
X	X

2.5.4 The PLL Will Not Run when Using XOSCHF with an External Crystal

When the PLL is configured to run from an external source (SOURCE in CLKCTRL.PLLCTRLA is '1'), the PLL will only run if XOSCHF is configured to use an external clock (SELHF in CLKCTRL.XOSCHFCTRLA is '1'). It will not work with an external crystal.

Work Around
None.

Affected Silicon Revisions

Rev. A4	Rev. A5
X	X

2.6 DAC - Digital-to-Analog Converter

2.6.1 DAC Output Buffer Lifetime Drift

The offset of the DAC output buffer can drift over the lifetime of the device if it is powered with the DAC output buffer disabled.

Work Around

Keep the DAC output buffer enabled (OUTEN in DACn.CTRLA is `'1'`) continuously or compensate by measuring the DAC output voltage offset with the ADC and adjust the DAC data register value (DATA[9:0] in DACn.DATA) accordingly.

Affected Silicon Revisions

Rev. A4	Rev. A5
X	X

2.7 NVMCTRL - Nonvolatile Memory Controller

2.7.1 Flash Multi-Page Erase Can Erase Write Protected Section

When using Flash Multi-Page Erase mode, only the first page in the selected address range is verified to be within a section that is not write-protected. If the address range includes any write-protected Application Data pages, it will erase them.

Work Around

None.

Affected Silicon Revisions

Rev. A4	Rev. A5
X	X

2.8 OPAMP - Analog Signal Conditioning

2.8.1 OPAMP Consume More Power Than Expected

The OPAMP peripheral consumes up to three times more current than specified when the output is driven closer to either the upper or lower rails.

Work Around

None.

Affected Silicon Revisions

Rev. A4	Rev. A5

X	-

2.8.2 The Input Range Select is Read-Only

The Input Range Select (IRSEL) bit is read-only. When the Analog Signal Conditioning (OPAMP) peripheral is active, the input voltage range will be rail-to-rail.

Work Around
None.

Affected Silicon Revisions

Rev. A4	Rev. A5
X	-

2.9 PORT - I/O Configuration

2.9.1 PD0 Input Buffer is Floating

On 28- and 32-pin package parts, the PD0 input buffer is floating. Because the default direction setting for PD0 is as an input pin, this may cause unexpected current consumption.

Work Around
Disable the PD0 input (ISC in PORTD.PIN0CTRL) or configure the pin as an output (bit 0 in PORTD.DIR).

Affected Silicon Revisions

Rev. A4	Rev. A5
X	X

2.10 RSTCTRL - Reset Controller

2.10.1 BOD Registers not Reset When UPDI Is Enabled

If the UPDI is enabled, the VLMCTRL, INTCTRL, and INTFLAGS registers in BOD will not be reset by other reset sources than POR.

Work Around
None

Affected Silicon Revisions

Rev. A4	Rev. A5
X	-

2.11 TCA - 16-Bit Timer/Counter Type A

2.11.1 Restart Will Reset Counter Direction in NORMAL and FRQ Mode

When the TCA is configured to a NORMAL or FRQ mode (WGMODE in TCAn.CTRLB is '0x0' or '0x1'), a RESTART command or Restart event will reset the count direction to default. The default is counting upwards.

Work Around
None.

Affected Silicon Revisions

Rev. A4	Rev. A5
X	X

2.12 TCB - 16-Bit Timer/Counter Type B

2.12.1 CCMP and CNT Registers Act as 16-Bit Registers in 8-Bit PWM Mode

When the TCB is operating in 8-bit PWM mode (CNTMODE in TCBn.CTRLB is '0x7'), the low and high bytes for the CCMP and CNT registers act as 16-bit registers for read and write. They cannot be read or written independently.

Work Around
Use 16-bit register access. Refer to the data sheet for further information.

Affected Silicon Revisions

Rev. A4	Rev. A5
X	X

2.13 TCD - 12-Bit Timer/Counter Type D

2.13.1 Asynchronous Input Events not Working When TCD Counter Prescaler Is Used

When configuring TCD to use asynchronous input events (CFG in TCDn.EVCTRLx is '0x2') and the TCD Counter Prescaler (CNTPRES in TCDn.CTRLA) is different from '0x0', events can be missed.

Work Around
Use the TCD Synchronization Prescaler (SYNCPRES in TCDn.CTRLA) instead of the TCD Counter Prescaler. Alternatively, use synchronous input events (CFG in TCDn.EVCTRLx is not '0x2') if the input events are longer than one CLK_TCD_CNT cycle.

Affected Silicon Revisions

Rev. A4	Rev. A5
X	X

2.13.2 CMPAEN Controls All WOx for Alternative Pin Functions

When TCD alternative pins are enabled (TCD0 in PORTMUX.TCDROUTEA is not '0x0'), all waveform outputs (WOx) are controlled by Compare A Enable (CMPAEN in TCDn.FAULTCTRL).

Work Around
None.

Affected Silicon Revisions

Rev. A4	Rev. A5
X	X

2.13.3 Halting TCD and Waiting for SW Restart Does Not Work if Compare Value A is 0 or Dual Slope Mode is Used

Halting TCD and waiting for software restart (INPUTMODE in TCDn.INPUTCTRLA is '0x7') does not work if compare value A is 0 (CMPASET in TCDn.CMPASET is '0x0') or Dual Slope mode is used (WGMODE in TCDn.CTRLB is '0x3').

Work Around
Configure the compare value A (CMPASET in TCDn.CMPASET) to be different from 0 and do not use Dual Slope mode (WGMODE in TCDn.CTRLB is not '0x3').

Affected Silicon Revisions

Rev. A4	Rev. A5
X	X

2.14 TWI - Two-Wire Interface

2.14.1 The Output Pin Override Does not Function as Expected

When TWI is enabled, it overrides the output pin driver but not the output value. The output on the line will always be high when the value in the PORTx.OUT register is '1' for the pins corresponding to the SDA or SCL.

Work Around
Ensure that the values in the PORTx.OUT register corresponding to the SCL and SDA pins are '0' before enabling the TWI.

Affected Silicon Revisions

Rev. A4	Rev. A5
X	X

2.14.2 Flush Non-Functional

Issuing a Flush by writing to the FLUSH bit in TWIn.MCTRLB can cause the TWI Host to be stuck in the Unknown bus state (see BUSSTATE in TWIn.MSTATUS).

Work Around
Disable and re-enable the Host using the ENABLE bit in TWIn.MCTRLA. A normal operation does not require the use of FLUSH.

Affected Silicon Revisions

Rev. A4	Rev. A5
X	X

2.15 USART - Universal Synchronous and Asynchronous Receiver and Transmitter

2.15.1 Open-Drain Mode Does not Work When TXD Is Configured as Output

When configured as an output, the USART TXD pin can drive the pin high regardless of whether the Open-Drain mode is enabled or not.

Work Around
Configure the TXD pin as an input by writing the corresponding bit in PORTx.DIR to '0' when using Open-Drain mode.

Affected Silicon Revisions

Rev. A4	Rev. A5
X	X

2.15.2 Start-of-Frame Detection Can Unintentionally Be Triggered in Active Mode

The Start-of-Frame Detection feature enables the USART to wake up from Standby sleep mode upon data reception. The Start-of-Frame Detector can unintentionally be triggered when the Start-of-Frame Detection Enable (SFDEN) bit in the USART Control B (USARTn.CTRLB) register is set, and the device is in Active mode. If the Receive Data (RXDATA) registers are read while receiving new data, the Receive Complete Interrupt Flag (RXCIF) in the USARTn.STATUS register is cleared. This triggers the Start-of-Frame Detector and falsely detects the next falling edge as a start bit. When the Start-of-Frame Detector detects a start condition, the frame reception is restarted, resulting in corrupt received data. Note that the USART Receive Start Interrupt Flag (RXSIF) always is '0' when in Active mode. No interrupt will be triggered.

Work Around
Disable Start-of-Frame Detection by writing '0' to the Start-of-Frame Detection Enable (SFDEN) bit in the USART Control B (USARTn.CTRLB) register when the device is in Active mode. Re-enable it by writing the bit to '1' before transitioning to Standby sleep mode. This work around depends on a protocol preventing a new incoming frame when re-enabling Start-of-Frame Detection. Re-enabling Start-of-Frame Detection, while a new frame is already incoming, will result in corrupted received data.

Affected Silicon Revisions

Rev. A4	Rev. A5
X	X

2.16 ZCD - Zero-Cross Detector

2.16.1 All ZCD Output Selection Bits Are Tied to the ZCD0 Bit

The Zero Cross Detector n Output (ZCDn) bits in the Pin Position (PORTMUX.ZCDROUTEA) register are tied to ZCD0. Any write to ZCD0 will be reflected in the ZCD1 and ZCD2 as well. Writing to ZCD1 and/or ZCD2 has no effect.

Work Around
Use the Event System or CCL to make the output of ZCD1 or ZCD2 available on a pin.

Affected Silicon Revisions

Rev. A4	Rev. A5
X	-

3. Data Sheet Clarifications

Note the following typographic corrections and clarifications for the latest version of the device data sheet (www.microchip.com/DS40002247).

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

3.1 Device

3.1.1 Features

A clarification has been made to change the Flash endurance specification in the *Memories* bullet point in the *Features* list.

- Memories
  - 128 KB in-system self-programmable Flash memory
  - 512B EEPROM
  - 16 KB SRAM
  - 32B of user row in nonvolatile memory that can keep data during chip-erase and be programmed while the device is locked
  - Write/erase endurance
    - Flash: **1,000** cycles
    - EEPROM: 100,000 cycles
  - Data retention: 40 years at 55°C

3.1.2 FUSE - Configuration and User Fuses - SYSCFG0

A clarification of the EEPROM Save During Chip Erase (EESAVE) fuse description in the System Configuration 0 (SYSCFG0, section 8.8.2.4) fuse has been made.

Bit 0 - EESAVE EEPROM Saved During Chip Erase

This bit controls if the EEPROM will be erased or saved during a chip erase.

Value	Name	Description
0	DISABLE	EEPROM is erased during a chip erase
1	ENABLE	EEPROM is saved during a chip erase **regardless of whether the device is locked or not**

3.1.3 Peripherals and Architecture - REVID

A clarification of the MAJOR bit field description in the Device Revision ID (REVID, section 10.3.2.1) Register has been made.

Bits 7:4 - MAJOR[3:0] Major revision

This bit field contains the major revision for the device. **0x01 = A, 0x02 = B**, and so on.

Bits 3:0 - MINOR[3:0] Minor revision

This bit field contains the minor revision for the device. 0x00 = 0, 0x01 = 1, and so on.

3.2 SLPCTRL - Sleep Controller

3.2.1 Voltage Regulator Control (VREGCTRL)

Clarifications to the High-Temperature Low Leakage Enable (HTTLEN) and Power Mode Select (PMODE) bit field descriptions for the Voltage Regulator Control (VREGCTRL, section 13.5.2) register of the Sleep Controller (SLPCTRL) peripheral has been made.

Bit 4 - HTLLEN High-Temperature Low Leakage Enable

This bit controls whether the current leakage is reduced or not when operating at temperatures above 70°C.

Value	Name	Description
0	OFF	High-temperature low leakage disabled(1)
1	ON	High-temperature low leakage enabled(2,3)

⚠WARNING

1. **If entering the Standby sleep mode, this bit must be '0'.**
2. **This will only have an effect when PMODE is set to AUTO and must only be used for the Power-Down sleep mode.**
3. **The TWI address match and CCL wake-up sources must be disabled before writing this bit to '1'.**

Bits 2:0 - PMODE[2:0] Power Mode Select

This bit field controls the drive strength of the voltage regulator.

Value	Name	Description
0x0	AUTO	**The regulator will run with maximum performance in active/ idle mode unless the 32.768 kHz oscillator source is selected. Power saving in deep sleep modes.**
0x1	FULL	**Maximum performance voltage regulator drive strength in all modes. Faster start-up from sleep modes.**
Other	-	Reserved

3.3 TCB - 16-Bit Timer/Counter Type B

3.3.1 Single-Shot Mode

Clarifications of the *Single-Shot Mode* sub-section in the *Functional Description* section and the EDGE bit field description in the Event Control (EVCTRL) register of the TCB peripheral have been made.

24.3.3.1.7 Single-Shot Mode

The Single-Shot mode can be used to generate a pulse with a duration defined by the Compare (TCBn.CCMP) register, every time a rising or falling edge is observed on a connected event channel.

This mode requires TCB to be configured as an event user and is explained in the Events section.

When the counter is stopped, the output pin is set low. If an event is detected on the connected event channel, the timer will reset and start counting from BOTTOM to TOP while driving its output high. The RUN bit in the Status (TCBn.STATUS) register can be read to see if the counter is counting or not. When CNT reaches the CCMP register value, the counter will stop, and the output pin will go low for at least one counter clock cycle (TCB_CLK), and a new

event arriving during this time will be ignored. After this, there is a delay of two peripheral clock cycles (PER_CLK) from when a new event is received until the output is set high. **When the EDGE bit of the TCB.EVCTRL register is written to '1', any edge can trigger the start of counter. If the EDGE bit is '0', only positive edges will trigger the start.**

The counter will start counting as soon as the peripheral is enabled, even without triggering by an event, or if the Event Edge (EDGE) bit in the Event Control (TCBn.EVCTRL) register is modified while the peripheral is enabled. This is prevented by writing TOP to the Counter register. Similar behavior is seen if the Event Edge (EDGE) bit in the Event Control (TCBn.EVCTRL) register is '1' while the module is enabled. Writing TOP to the Counter register prevents this as well.

If the Event Asynchronous (ASYNC) bit in the Control B (TCBn.CTRLB) register is written to '1', the timer will react asynchronously to an incoming event. An edge on the event will immediately cause the output signal to be set. The counter will still start counting two clock cycles after the event is received.

24.5.3 Event Control

Bit 4 - EDGE Event Edge

This bit is used to select the event edge. The effect of this bit is dependent on the selected Count Mode (CNTMODE) bit field in TCBn.CTRLB. "—" means that an event or edge has no effect in this mode.

Count Mode	EDGE	Positive Edge	Negative Edge
Periodic Interrupt mode	0	—	—
	1	—	—
Timeout Check mode	0	Start counter	Stop counter
	1	Stop counter	Start counter
Input Capture on Event mode	0	Input Capture, interrupt	—
	1	—	Input Capture, interrupt
Input Capture Frequency Measurement mode	0	Input Capture, clear and restart counter, interrupt	—
	1	—	Input Capture, clear and restart counter, interrupt
Input Capture Pulse-Width Measurement mode	0	Clear and restart counter	Input Capture, interrupt
	1	Input Capture, interrupt	Clear and restart counter
Input Capture Frequency and Pulse Width Measurement mode	0	• On the 1st Positive: Clear and restart counter • On the following Negative: Input Capture • On the 2nd Positive: Stop counter, interrupt	
	1	• On the 1st Negative: Clear and restart counter • On the following Positive: Input Capture • On the 2nd Negative: Stop counter, interrupt	
Single-Shot mode	0	Start counter	—
	1	**Start counter**	Start counter
8-Bit PWM mode	0	—	—
	1	—	—

3.4 AC - Analog Comparator

3.4.1 Analog Comparator Interrupt Control

A clarification of the Interrupt Mode (INTMODE) bit field of the AC Interrupt Control (ACn.INTCTRL, section 32.5.5) register has been made.

Table 32-4. Interrupt Generation with Single Comparator

Value	Name	Description
0x0	BOTHEDGE	Positive and negative inputs crosses
0x1	-	Reserved
0x2	NEGEDGE	Positive input goes **below** negative input
0x3	POSEDGE	Positive input goes **above** negative input

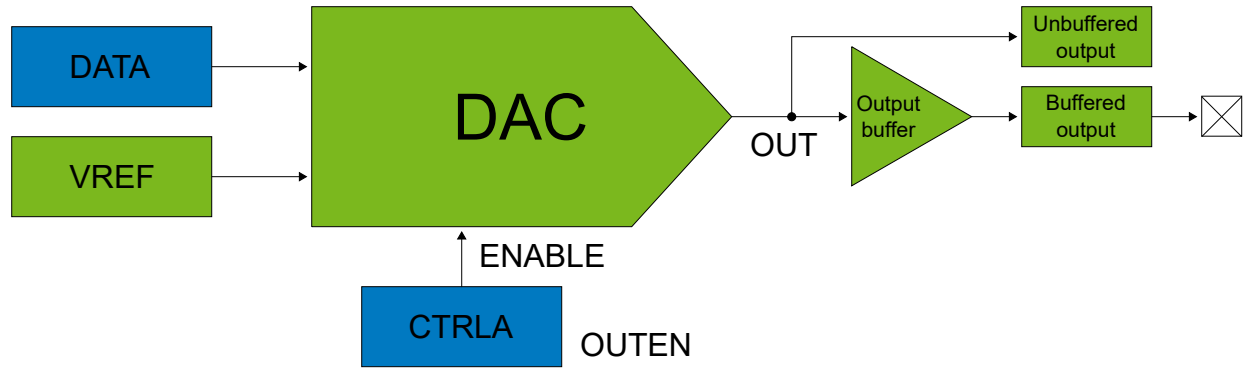
3.5 DAC - Digital to Analog Converter

3.5.1 DAC Output

Clarifications of the block diagram and the DAC Output sub-section of the DAC peripheral has been made:

1. The block diagram is updated with clarifications to the output signal routing (buffered/unbuffered) and will replace the original block diagram.
2. Sections 34.3.2.3 (DAC as Source For Internal Peripherals) and 34.3.2.4 (DAC Output on Pin) are replaced by section 34.3.2.3 DAC Output.

Figure 34-1. DAC Block Diagram



34.3.2.3 DAC Output

The DAC can be used as an output to a pin and as an input to the peripherals in the table below.

DAC Output	Peripheral Input	Notes
Unbuffered	• **Analog Comparator (AC)** • **Analog to Digital Converter (ADC)**	**The peripheral is connected to the unbuffered DAC output. See section 34.3.2.3.1. Unbuffered Output as Source For Internal Peripherals.**

.....continued		
DAC Output	**Peripheral Input**	**Notes**
Buffered	• **Analog Signal Conditioning (OPAMP)**	**The peripheral is connected to the DAC Output pin. See section 34.3.2.3.2. Buffered Output.**

34.3.2.3.1 Unbuffered Output as Source For Internal Peripherals

The unbuffered analog output of the DAC can be internally connected to other peripherals when the ENABLE bit in the Control A (DACn.CTRLA) register is written to '1'. When only the DAC unbuffered analog output is used, the Output Buffer Enable (OUTEN) bit in DACn.CTRLA can be '0', freeing the pin to be used by other peripherals.

34.3.2.3.2 Buffered Output

The buffered analog output of the DAC can be enabled by writing a '1' to the Output Buffer Enable (OUTEN) bit in the Control A (DACn.CTRLA) register. The pin used by the DAC must have the input disabled from the Port peripheral. Refer to the *Electrical Characteristics* section for information about the drive capabilities of the DAC output buffer.

3.6 Electrical Characteristics

3.6.1 Electrical Characteristics - Memory Programming Specifications

A clarification has been made to change the Flash memory cell endurance specification in the *Memory Programming Specifications* table.

Table 39-8. Memory Programming Specifications

Symbol	Description	Min.	Typ	Max.	Units	Conditions
Data EEPROM Memory Specifications						
E_D	Data EEPROM byte endurance	100k	—	—	Erase/Write cycles	-40°C ≤ T_A ≤ +85°C
t_{D_RET}	Characteristic retention	—	40	—	Year	Provided no other specifications are violated
N_{D_REF}	Total Erase/Write cycles before refresh	1M	4M	—	Erase/Write cycles	-40°C ≤ T_A ≤ +85°C
t_{D_CE}	Full EEPROM Erase	—	10	—	ms	
V_{D_RW}	V_{DD} for Read or Erase/Write operation	V_{DDMIN}	—	V_{DDMAX}	V	
t_{D_BEW}	Byte Erase and Write cycle time	—	11	—	ms	
Program Flash Memory Specifications						
E_P	**Flash memory cell endurance**	**1k**	—	—	Erase/Write cycles	-40°C ≤ T_A ≤ +85°C
t_{P_RET}	Characteristic retention	—	40	—	Year	Provided no other specifications are violated
V_{P_RD}	V_{DD} for Read operation	V_{DDMIN}	—	V_{DDMAX}	V	

.....continued						
Symbol	**Description**	**Min.**	**Typ**	**Max.**	**Units**	**Conditions**
V_{P_REW}	V_{DD} for Erase/Write operation	V_{DD}(2)	—	V_{DDMAX}	V	
t_{P_PE}	Page Erase	—	10	—	ms	
t_{P_CE}	Chip Erase	—	—	—	ms	
t_{P_WRD}	Byte/Word Write	—	70	—	µs	

Notes:

1. These parameters are not tested but ensured by design.
2. During Chip Erase, the Brown-out Detector (BOD) configured with BODLEVEL0 is forced ON. If the supply voltage V_{DD} is below V_{BOD} for BODLEVEL0, the erase attempt will fail.

3.7 Typical Characteristics

3.7.1 OPAMP

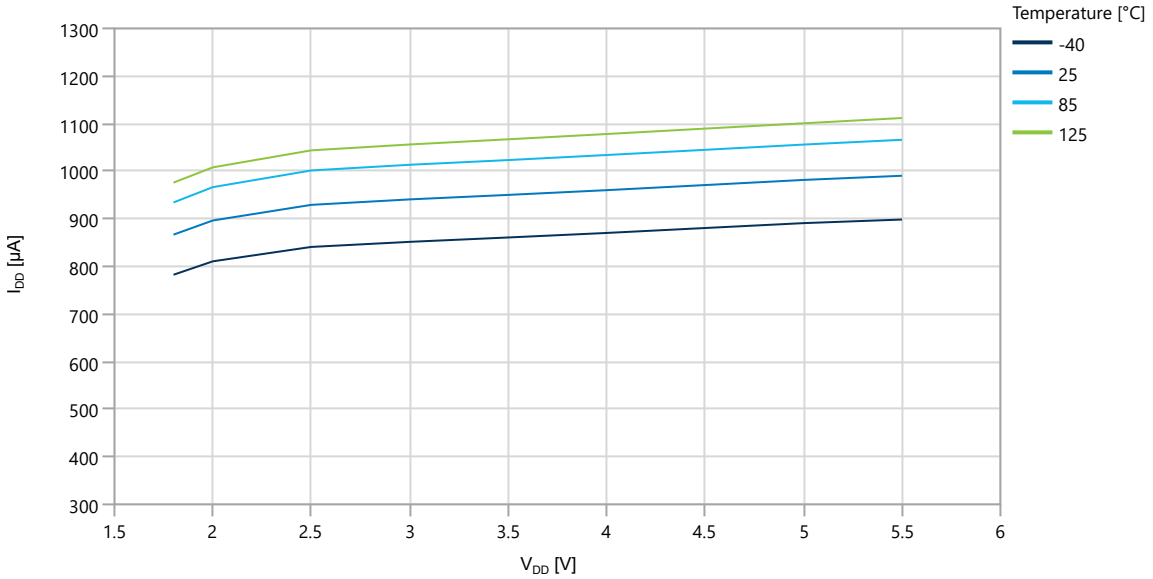
Some additional plots are added to the OPAMP section of the Typical Characteristics:

- I_{DD} over V_{DD} and temperature with IRSEL = 0
- I_{DD} over V_{DD} and temperature with IRSEL = 1
- Output sinking short-circuit current over V_{DD} and temperature
- Output sourcing short-circuit current over V_{DD} and temperature
- Output impedance over frequency at 3V and 25°C
- Small-signal non-inverting pulse response at 3V V_{DD}
- Large-signal non-inverting pulse response at 3V V_{DD}

Unless otherwise noted, the typical graphs are valid for the following conditions:

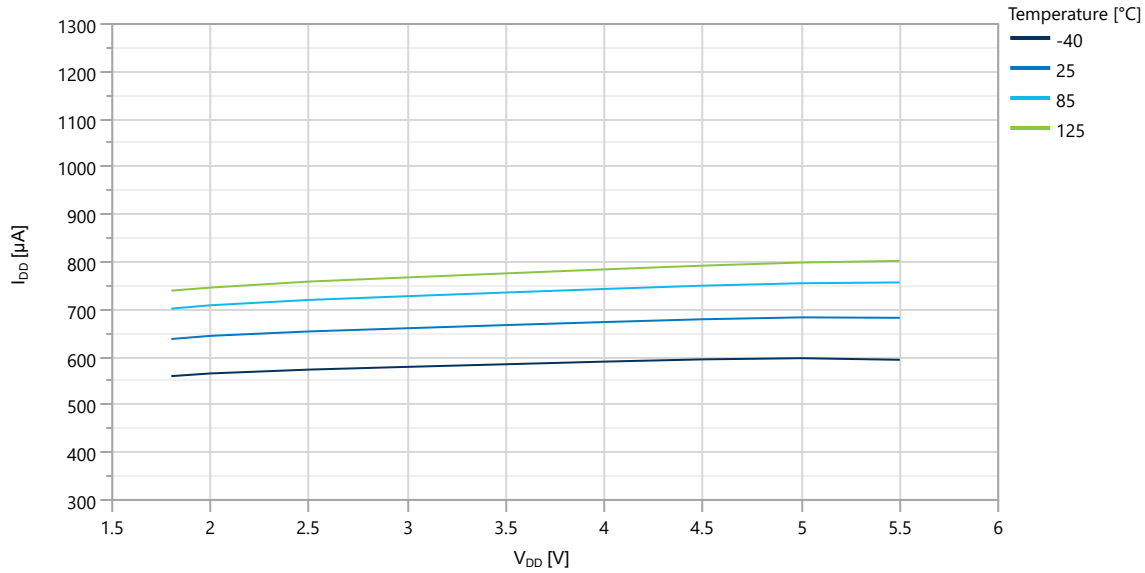
- Output load: 50 pF||3 kΩ
- Input common-mode voltage at V_{DD}/2
- Internal voltage follower mode
- IRSEL = 0

Figure 3-1. I_{DD} Over V_{DD} and Temperature With IRSEL = 0



Note: This plot is only valid for revision A5 and later.

Figure 3-2. I_{DD} Over V_{DD} and Temperature With IRSEL = 1



Note: This plot is only valid for revision A5 and later.

Figure 3-3. Output Sinking Short Circuit Current Over V_{DD} and Temperature

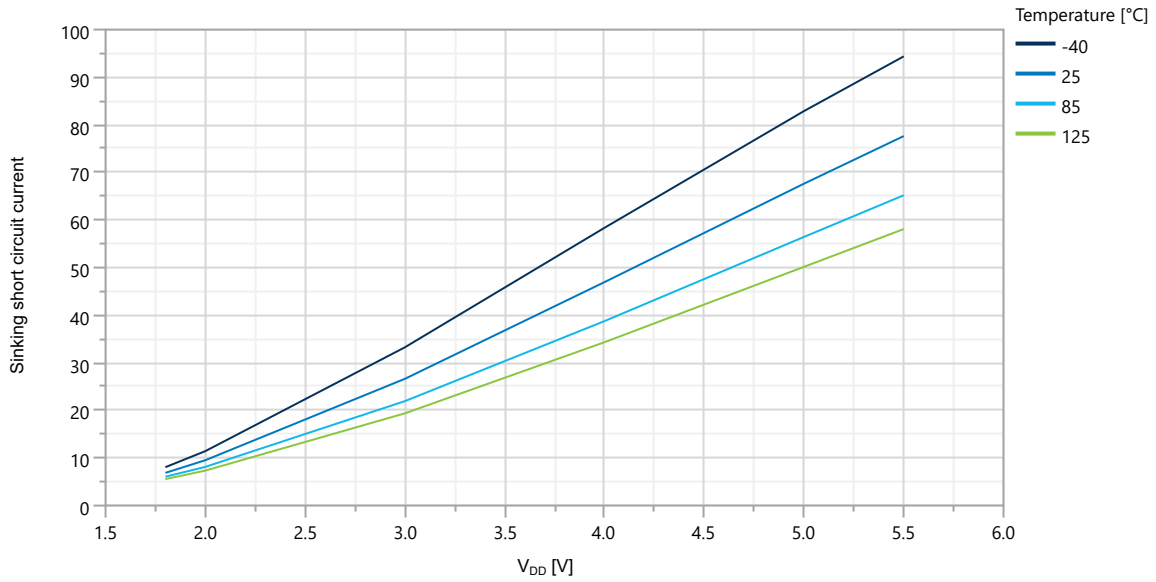


Figure 3-4. Output Sourcing Short Circuit Current Over V_{DD} and Temperature

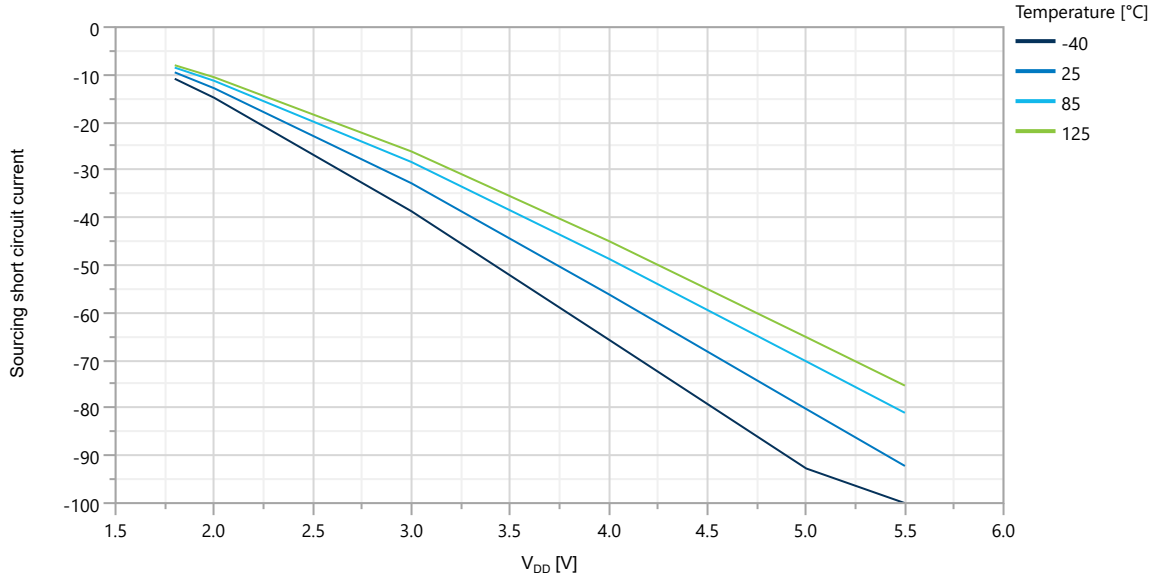


Figure 3-5. Output Impedance Over Frequency at 3V and 25°C

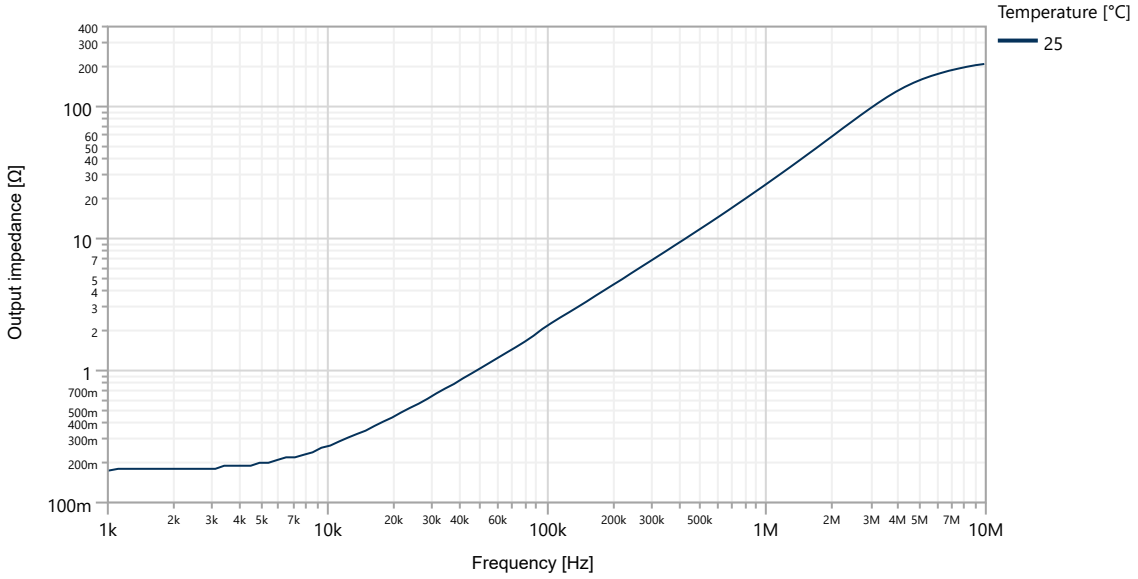


Figure 3-6. Small-signal Non-Inverting Pulse Response at 3V V_{DD} Using 10 kΩ Load

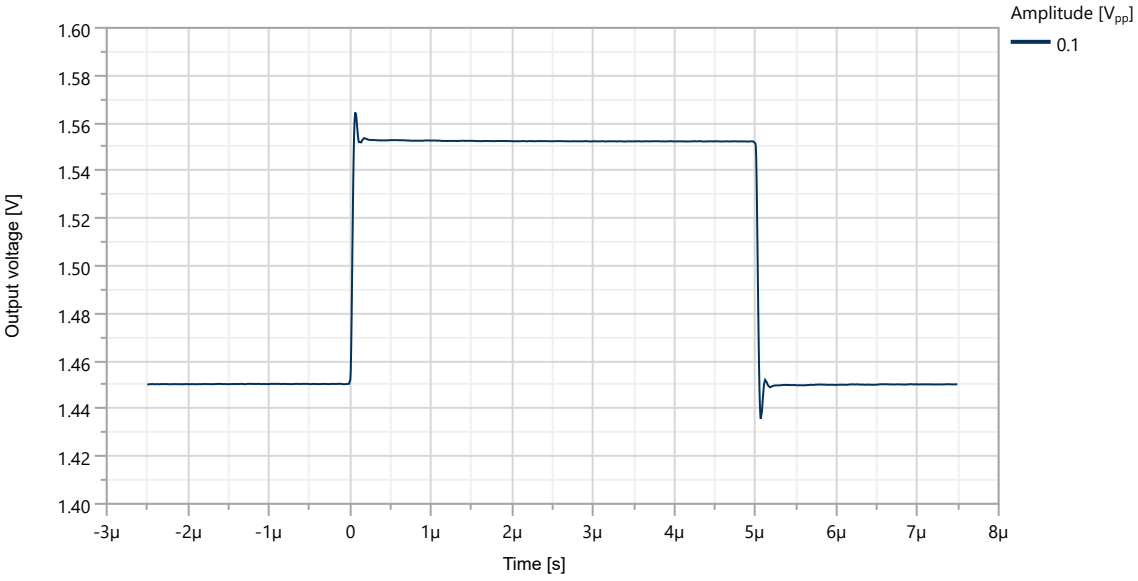
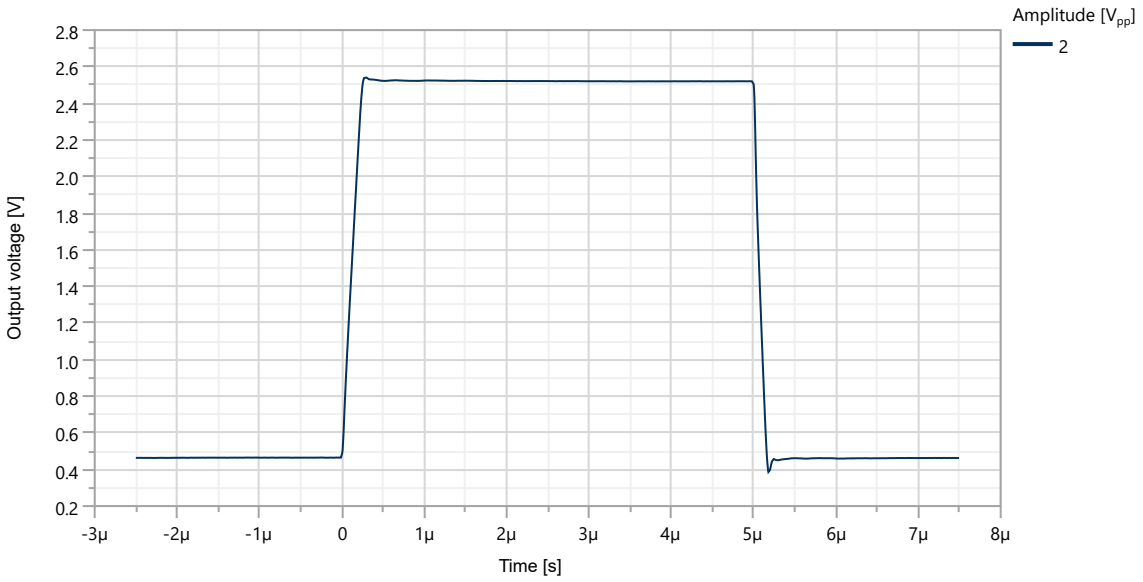


Figure 3-7. Large-Signal Non-Inverting Pulse Response at 3V V_{DD} Using 10 kΩ Load



4. Document Revision History

Note: The document revision is independent of the silicon revision.

4.1 Revision History

Doc. Rev.	Date	Comments
C	03/2022	Document: General editorial updates. Added errata: • Device: 2.2.3. CRC Check During Reset Initialization Is not Functional • CLKCTRL: 2.5.3. PLL Status not Working as Expected • DAC: 2.6.1. DAC Output Buffer Lifetime Drift • NVMCTRL: 2.7.1. Flash Multi-Page Erase Can Erase Write Protected Section • TCA: 2.11.1. Restart Will Reset Counter Direction in NORMAL and FRQ Mode • TCD: 2.13.3. Halting TCD and Waiting for SW Restart Does Not Work if Compare Value A is 0 or Dual Slope Mode is Used • TWI: 2.14.2. Flush Non-Functional Updated errata: • 2.15.2. Start-of-Frame Detection Can Unintentionally Be Triggered in Active Mode Added data sheet clarifications: • 3.1.1. Features • 3.1.2. FUSE - Configuration and User Fuses - SYSCFG0 • 3.1.3. Peripherals and Architecture - REVID • 3.2.1. Voltage Regulator Control (VREGCTRL) • 3.3.1. Single-Shot Mode • 3.4.1. Analog Comparator Interrupt Control • 3.5.1. DAC Output • 3.6.1. Electrical Characteristics - Memory Programming Specifications
B	10/2020	Added errata: • Device: *Increased Current Consumption May Occur When VDD Drops* • CLKCTRL: *The PLL Will Not Run When Using XOSCHF With an External Crystal* • TCB: *CCMP and CNT Registers Operate as 16-Bit Registers in 8-Bit PWM Mode* • TCD: – *Asynchronous Input Events Not Working When TCD Counter Prescaler is Used* – *CMPAEN Controls All WOx For Alternative Pin Functions* Updated errata: • CCL: – *The CCL Must be Disabled to Change the Configuration of a Single LUT* – *The LINK Input Source Selection for LUT3 is Not Functional on 28- and 32- pin Devices* • ZCD: *All ZCD Output Selection Bits are Tied to the ZCD0 Bit* Added data sheet clarification: Added Typical Characteristics section with additional plots for OPAMP peripheral.
A	08/2020	Initial document release

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