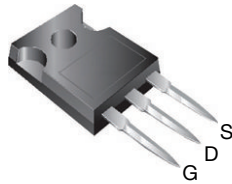


Power MOSFET

TO-247AC


N-Channel MOSFET

FEATURES

- Low figure-of-merit (FOM) $R_{on} \times Q_g$
- Low effective capacitance ($C_{o(er)}$)
- Reduced switching and conduction losses
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS
 COMPLIANT
 HALOGEN
FREE

APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial
 - Welding
 - Induction heating
 - Motor drives
 - Battery chargers
 - Solar (PV inverters)

PRODUCT SUMMARY

| | | |
|---|-----------------|-------|
| V_{DS} (V) at T_J max. | 550 | |
| $R_{DS(on)}$ typ. (Ω) at 25 °C | $V_{GS} = 10$ V | 0.234 |
| Q_g max. (nC) | 116 | |
| Q_{gs} (nC) | 22 | |
| Q_{gd} (nC) | 35 | |
| Configuration | Single | |

ORDERING INFORMATION

| | |
|---------------------------------|-------------|
| Package | TO-247AC |
| Lead (Pb)-free and halogen-free | IRFP460HPBF |

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)


| PARAMETER | SYMBOL | LIMIT | UNIT | |
|---|------------------|----------------|------|------|
| Drain-source voltage | V_{DS} | 500 | V | |
| Gate-source voltage | V_{GS} | ± 30 | | |
| Continuous drain current ($T_J = 150$ °C) | V_{GS} at 10 V | $T_C = 25$ °C | 20 | A |
| | | $T_C = 100$ °C | 13 | |
| Pulsed drain current ^a | I_{DM} | 54 | | |
| Linear derating factor | | 2.6 | W/°C | |
| Single pulse avalanche energy ^b | E_{AS} | 621 | mJ | |
| Maximum power dissipation | P_D | 329 | W | |
| Operating junction and storage temperature range | T_J, T_{stg} | -55 to +150 | °C | |
| Drain-source voltage slope | dv/dt | $T_J = 125$ °C | 66 | V/ns |
| Reverse diode dv/dt ^d | | 0.5 | | |
| Soldering recommendations (peak temperature) ^c | For 10 s | 260 | °C | |

Notes

- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{DD} = 120$ V, starting $T_J = 25$ °C, $L = 4.3$ mH, $R_g = 25$ Ω , $I_{AS} = 17$ A
- 1.6 mm from case
- $I_{SD} \leq I_D$, $di/dt = 100$ A/ μ s, starting $T_J = 25$ °C



| THERMAL RESISTANCE RATINGS | | | | |
|----------------------------------|------------|------|------|------|
| PARAMETER | SYMBOL | TYP. | MAX. | UNIT |
| Maximum junction-to-ambient | R_{thJA} | - | 40 | °C/W |
| Maximum junction-to-case (drain) | R_{thJC} | - | 0.45 | |

| SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted) | | | | | | | |
|---|---------------------|---|--|------|-------|-----------|---------------|
| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
| Static | | | | | | | |
| Drain-source breakdown voltage | V_{DS} | $V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$ | | 500 | - | - | V |
| V_{DS} temperature coefficient | $\Delta V_{DS}/T_J$ | Reference to $25\text{ }^\circ\text{C}, I_D = 1\text{ mA}$ | | - | 0.56 | - | V/°C |
| Gate-source threshold voltage (N) | $V_{GS(th)}$ | $V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$ | | 2.0 | - | 4.0 | V |
| Gate-source leakage | I_{GSS} | $V_{GS} = \pm 20\text{ V}$ | | - | - | ± 100 | nA |
| | | $V_{GS} = \pm 30\text{ V}$ | | - | - | ± 1 | μA |
| Zero gate voltage drain current | I_{DSS} | $V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$ | | - | - | 1 | μA |
| | | $V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$ | | - | - | 100 | |
| Drain-source on-state resistance | $R_{DS(on)}$ | $V_{GS} = 10\text{ V}$ | $I_D = 12\text{ A}$ | - | 0.234 | 0.270 | Ω |
| Forward transconductance ^a | g_{fs} | $V_{DS} = 10\text{ V}, I_D = 12\text{ A}$ | | - | 9.6 | - | S |
| Dynamic | | | | | | | |
| Input capacitance | C_{iss} | $V_{GS} = 0\text{ V}, V_{DS} = 100\text{ V}, f = 1\text{ MHz}$ | | - | 3208 | - | pF |
| Output capacitance | C_{oss} | | | - | 163 | - | |
| Reverse transfer capacitance | C_{rss} | | | - | 17 | - | |
| Effective output capacitance, energy related ^a | $C_{o(er)}$ | $V_{DS} = 0\text{ V to } 480\text{ V}, V_{GS} = 0\text{ V}$ | | - | 114 | - | pF |
| Effective output capacitance, time related ^b | $C_{o(tr)}$ | | | - | 206 | - | |
| Total gate charge | Q_g | $V_{GS} = 10\text{ V}$ | $I_D = 12\text{ A}, V_{DS} = 400\text{ V}$ | - | 77 | 116 | nC |
| Gate-source charge | Q_{gs} | | | - | 22 | - | |
| Gate-drain charge | Q_{gd} | | | - | 35 | - | |
| Turn-on delay time | $t_{d(on)}$ | $V_{DD} = 400\text{ V}, I_D = 12\text{ A}, V_{GS} = 10\text{ V}, R_g = 9.1\text{ }\Omega$ | | - | 29 | 58 | ns |
| Rise time | t_r | | | - | 60 | 90 | |
| Turn-off delay time | $t_{d(off)}$ | | | - | 67 | 101 | |
| Fall time | t_f | | | - | 47 | 94 | |
| Gate input resistance | R_g | $f = 1\text{ MHz}, \text{open drain}$ | | 0.37 | 0.75 | 1.5 | Ω |
| Drain-Source Body Diode Characteristics | | | | | | | |
| Continuous source-drain diode current | I_S | MOSFET symbol showing the integral reverse p - n junction diode  | | - | - | 22 | A |
| Pulsed diode forward current | I_{SM} | | | - | - | 54 | |
| Diode forward voltage | V_{SD} | $T_J = 25\text{ }^\circ\text{C}, I_S = 12\text{ A}, V_{GS} = 0\text{ V}$ | | - | - | 1.2 | V |
| Reverse recovery time | t_{rr} | $T_J = 25\text{ }^\circ\text{C}, I_F = I_S = 12\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, V_R = 25\text{ V}$ | | - | 384 | 768 | ns |
| Reverse recovery charge | Q_{rr} | | | - | 5.1 | 10.2 | μC |
| Reverse recovery current | I_{RRM} | | | - | 26 | - | A |

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

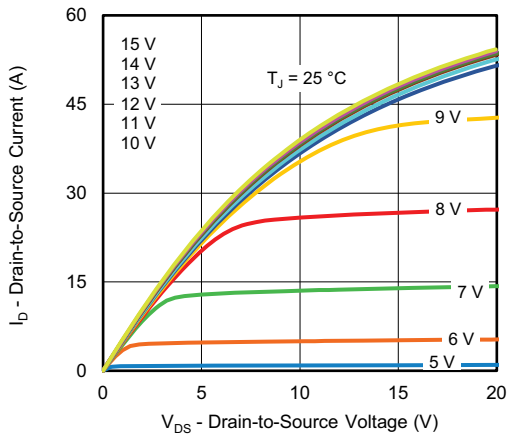


Fig. 1 - Typical Output Characteristics

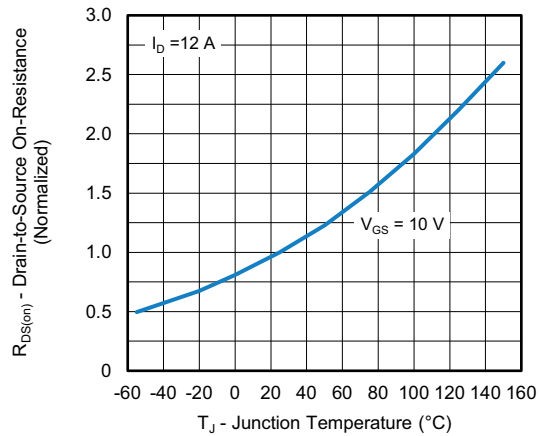


Fig. 4 - Normalized On-Resistance vs. Temperature

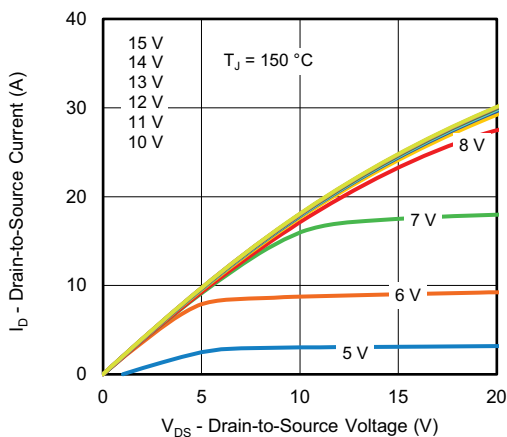


Fig. 2 - Typical Output Characteristics

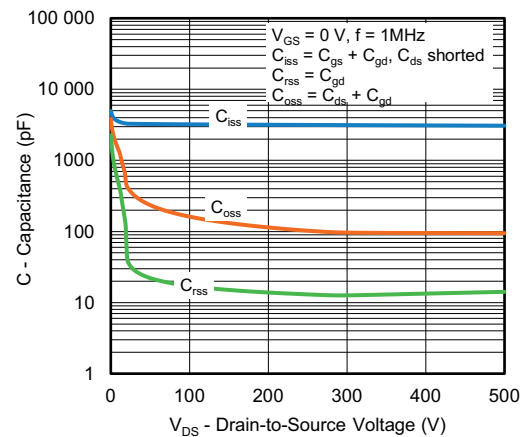


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

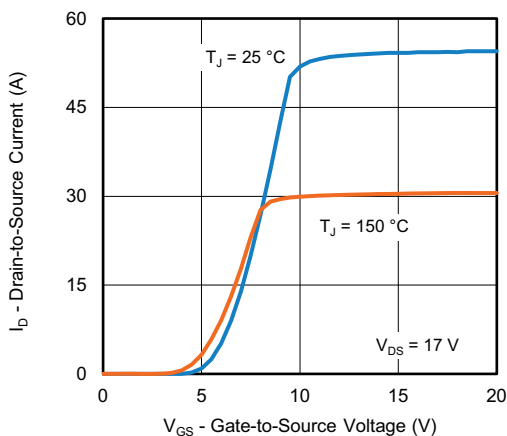


Fig. 3 - Typical Transfer Characteristics

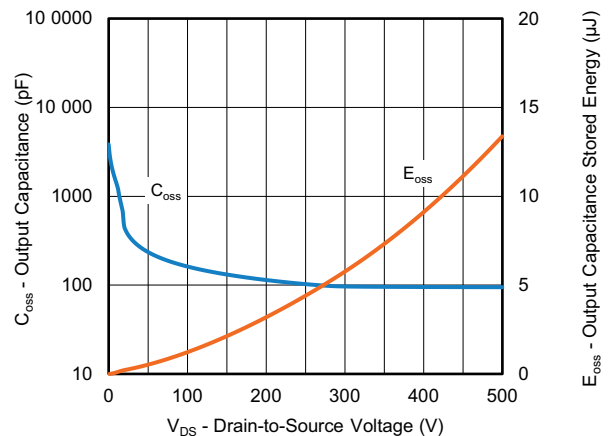


Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}

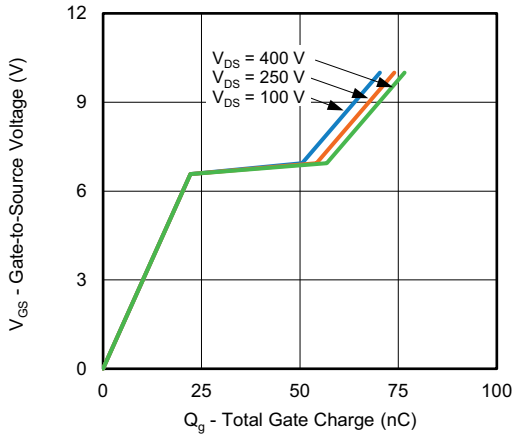


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

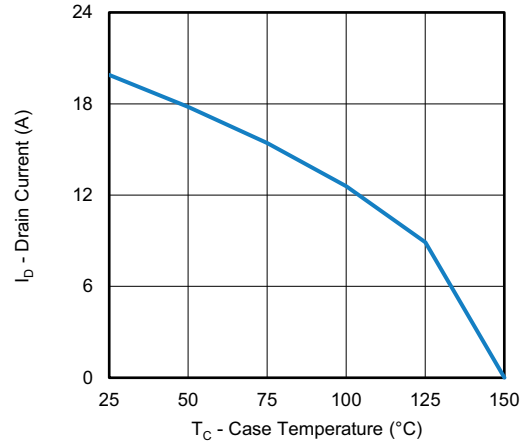


Fig. 10 - Maximum Drain Current vs. Case Temperature

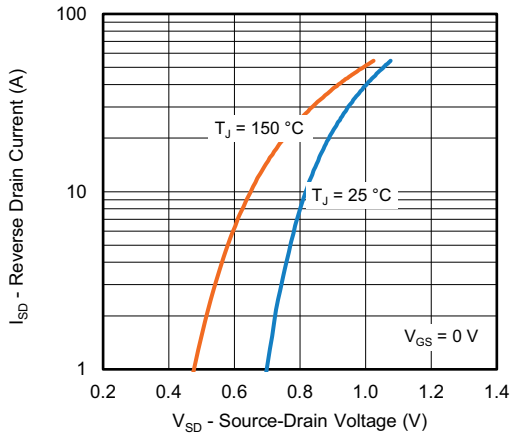


Fig. 8 - Typical Source-Drain Diode Forward Voltage

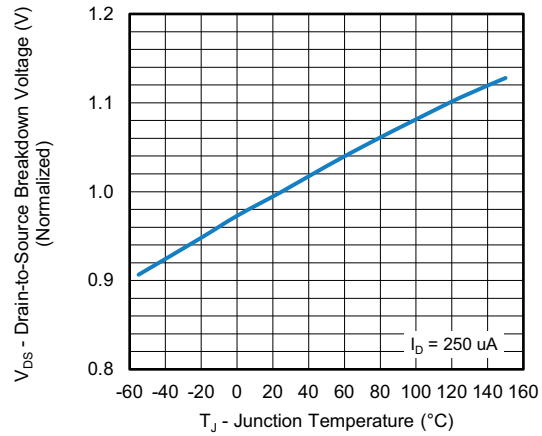


Fig. 11 - Temperature vs. Drain-to-Source Voltage

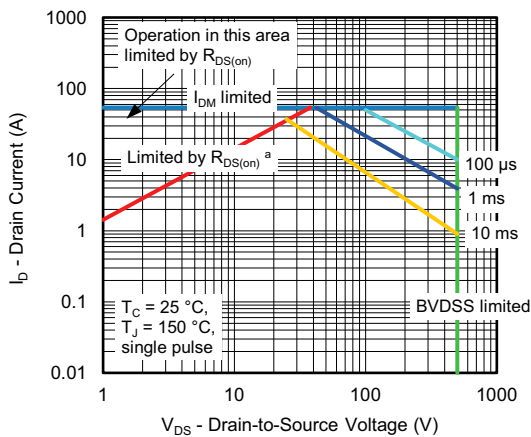


Fig. 9 - Maximum Safe Operating Area

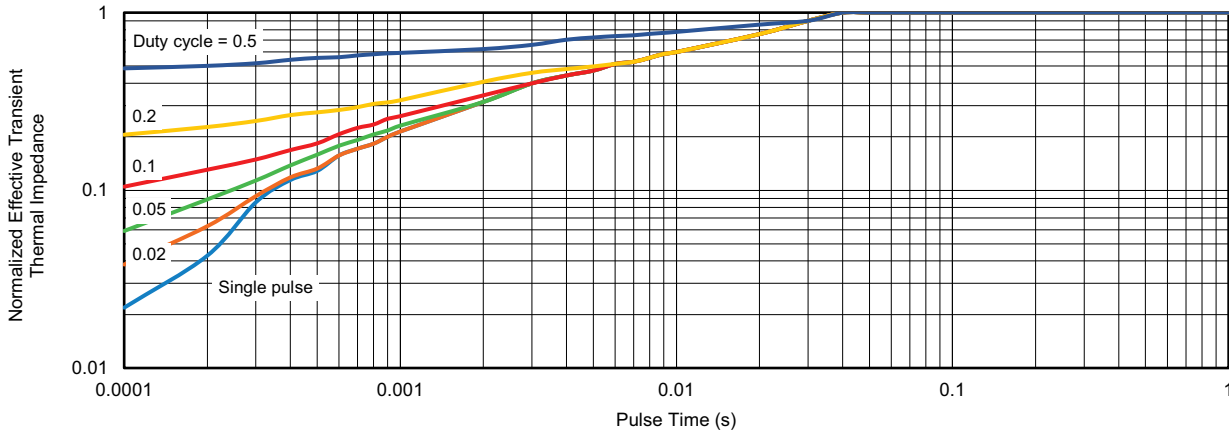


Fig. 12 - Normalized Transient Thermal Impedance, Junction-to-Case

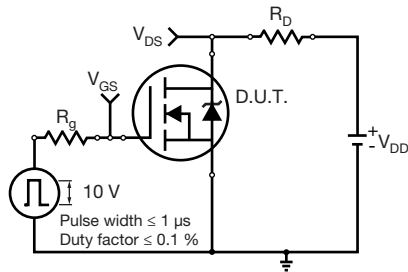


Fig. 13 - Switching Time Test Circuit

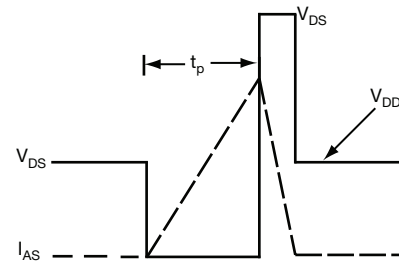


Fig. 16 - Unclamped Inductive Waveforms

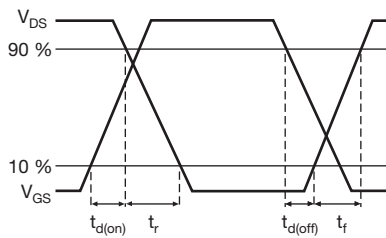


Fig. 14 - Switching Time Waveforms

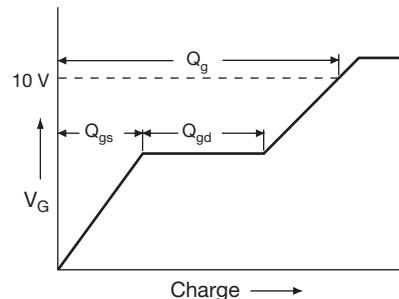


Fig. 17 - Basic Gate Charge Waveform

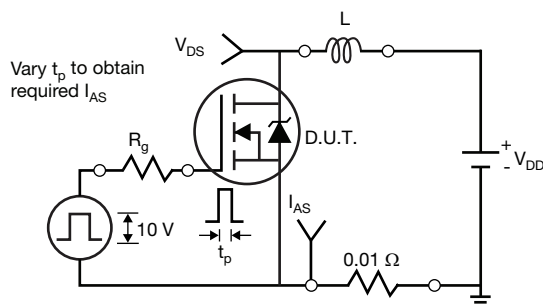


Fig. 15 - Unclamped Inductive Test Circuit

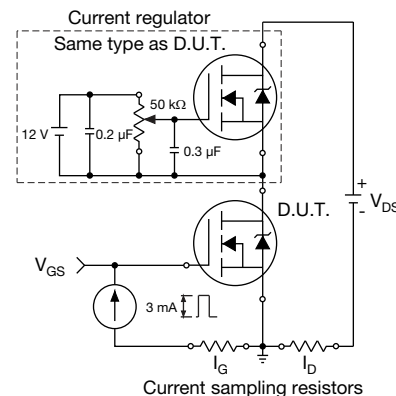
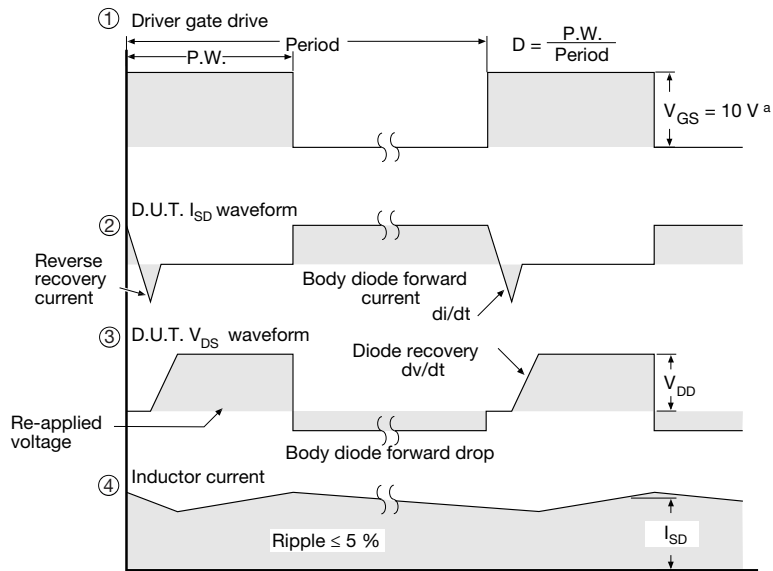
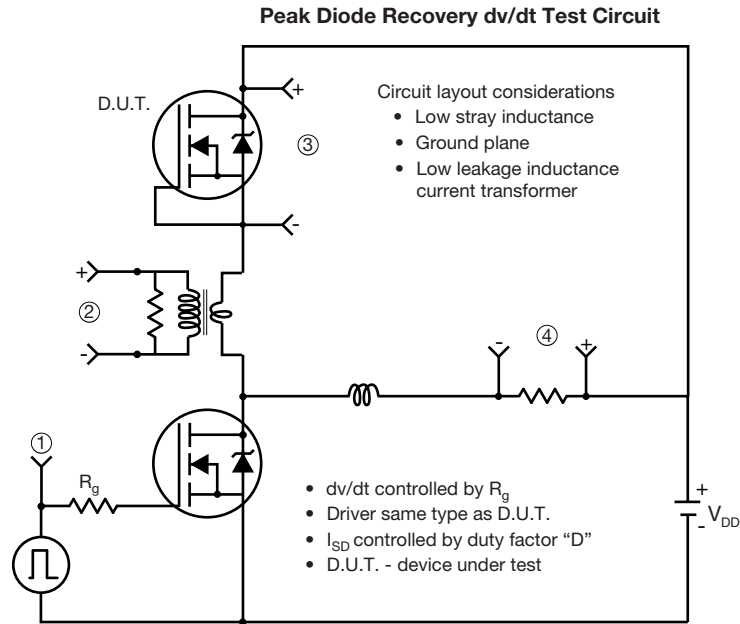


Fig. 18 - Gate Charge Test Circuit



Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 19 - For N-Channel

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Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?92440.



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