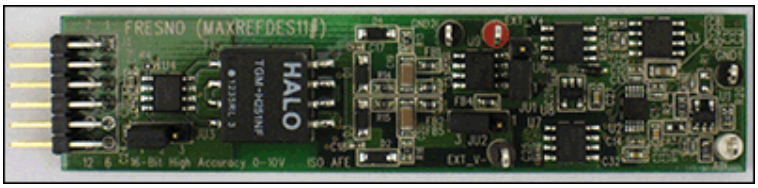
SUBSYSTEM BOARD 5563

Fresno (MAXREFDES11#): 16-Bit High-Accuracy 0 to 10V Input Isolated Analog Front End (AFE)

Jan 19, 2013

Abstract: This document explains how the Fresno (MAXREFDES11#) subsystem reference design meets the higher resolution and higher voltage needs of industrial control and industrial automation applications. Hardware and firmware design files as well as FFTs and histograms from lab measurements are provided.

Introduction



More detailed image (JPG)

Low resolution and low input voltage analog-to-digital converters (ADCs) are integrated in many of today's field programmable gate arrays (FPGAs) and microcontrollers. However, they fall short on meeting the needs of industrial control and industrial automation applications that require higher resolutions and higher input voltages. The Fresno (MAXREFDES11#) subsystem reference design is a 16-bit high-accuracy industrial analog front end (AFE) that accepts 0 to 10V signals and features isolated power and data—all integrated into a small form factor. The Fresno design integrates an ultra-precision low-noise buffer (MAX44250); a highly accurate ADC (MAX11100); an ultra-high-precision 4.096V voltage reference (MAX6126); 600V_{RMS} data isolation (MAX14850); and isolated/regulated +5.5V, +5V, and -3V power rails (MAX256/MAX1659/MAX1735). This AFE solution can be used in any application that needs high-accuracy analog-to-digital conversion, but it is mainly targeted for industrial sensors, industrial automation, process control, programmable logic controllers (PLCs), and medical applications.

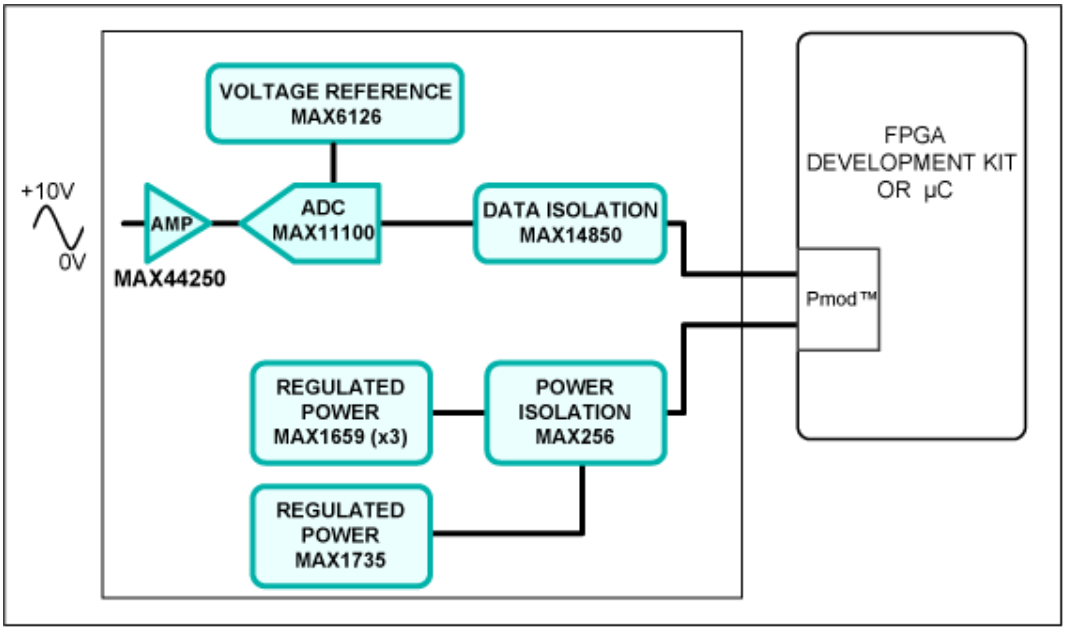


Figure 1. The Fresno subsystem design block diagram.

Features

- High accuracy
- 0 to 10V input range
- Isolated power and data
- Small printed circuit board (PCB) area
- Device drivers
- Example C source code
- Pmod™-compatible form factor

Applications

- Industrial sensors
- Process control
- Industrial automation
- PLC
- Medical

Detailed Description of Hardware

The Pmod specification allows for both 3.3V and 5V modules as well as various pin assignments. This module is designed only for a supply voltage of 3.3V and uses the SPI pin assignments as illustrated on the right.

The power requirements are shown in **Table 1**. The currently supported platforms and ports are shown in **Table 2**.

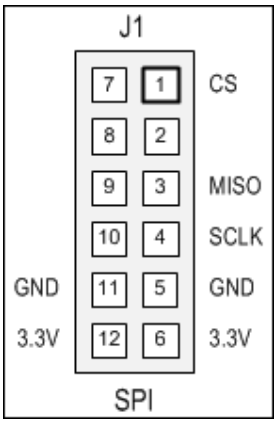


Table 1. Power Options for the Fresno Subsystem Reference Design

Power Type	Jumper Shunt	Input Voltage (V)	Input Current (mA, typ)
On-board isolated power	JU1: 1–2 JU2: 2–3 JU3: 1–2	3.3	71
External power	JU1: 2–3 JU2: 1–2 JU3: 2–3	6	10
		-5	2

Table 2. Supported Platforms and Ports

Supported Platforms	Port
Nexys™ 3 platform (Spartan®-6)	JB1
ZedBoard™ platform (Zynq®-7020)	JA1

The Fresno hardware design provides isolated power (MAX256) and isolated data (MAX14850) for a high-accuracy, 0 to 10V signal, analog-to-digital conversion application.

The MAX44250 (U1) op amp input circuit attenuates and buffers a 0 to10V signal to match the input range of the ADC (MAX11100), which is 0 to 4.096V.

The MAX11100 (U2) is a 16-bit, successive-approximation register (SAR) ADC with AutoShutdown™ and fast 1.1µs wake-up features. The ADC's reference input is driven by an ultra-high-precision 4.096V voltage reference, the MAX6126 (U3), with 0.02% initial accuracy and a 3ppm/°C maximum temperature coefficient (tempco).

The MAX256 (U4) provides an isolated, functional insulation class power solution that accepts 3.3V and converts it to ±6V using an off-the-shelf TGN-H251NF Halo® transformer with a 1:1 primary to secondary turns ratio plus an external on-board voltage-doubler circuit. Post-regulation is accomplished using the MAX1659 low dropout (LDO) regulator (for +5V) and the MAX1735 low dropout (LDO) regulator (for -3V). Data isolation is accomplished using the MAX14850 (U5) digital data isolator. The combined power and data isolation achieved is $600V_{RMS}$.

The signal input impedance of the Fresno subsystem is 5kΩ (R19 + R20). Ideally, the input impedance should be high, but larger resistors induce higher thermal noise and degrade the noise performance. Therefore, the values of the input resistors R19 and R20 are application dependent. Note that when choosing different values for the input resistors to properly attenuate a 10V signal to a 4V signal, R19 = 1.5 × R20.

To use the on-board isolated power supplies, move the shunts on jumper JU1 and JU3 to the 1–2 position and move the shunt on jumper JU2 to the 2–3 position. To use an external power supply, move the shunts on jumper JU1 and JU3 to the 2–3 position and move the shunt on jumper JU2 to the 1–2 position. Connect the ground terminal of the external power supply to the GND2 connector, the +6V to +12V supply to the EXT_V+ connector, and the -3.3V to -5V supply to the EXT_V- connector. See Table 1 for the jumper settings and the input current requirements.

Detailed Description of Firmware for Nexys 3 Platform

The Fresno firmware design was initially released for the Nexys 3 development kit and targeted a Microblaze™

soft core microcontroller placed inside a Xilinx® Spartan-6 FPGA. Support for additional platforms may be added periodically under Firmware Files in the All Design Files section. The currently supported platforms and ports are shown in Table 2.

The firmware is a working example of how to interface to the hardware, collect samples, and save them to memory. The simple process flow is shown in **Figure 2**. The firmware is written in C using the Xilinx SDK tool, which is based on the Eclipse™ open source standard. Custom Fresno-specific design functions were created utilizing the standard Xilinx XSpi core version 3.03a. The SPI clock frequency is set to 3.125MHz.

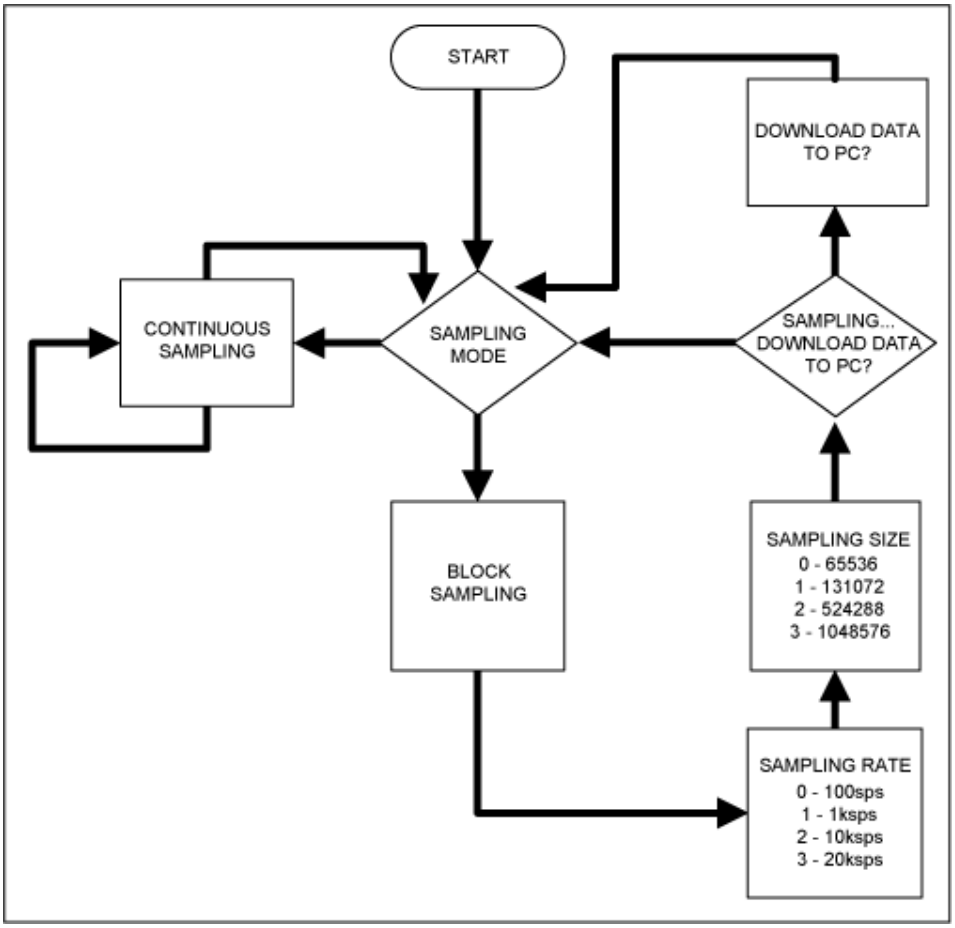


Figure 2. The Fresno firmware flowchart for Nexys 3 platform.

The firmware accepts commands, writes status, and is capable of downloading blocks of sampled data to a standard terminal program via a virtual COM port. The complete source code is provided to speed up customer development. Code documentation can be found in the corresponding firmware platform files.

Detailed Description of Firmware for ZedBoard Platform

The Fresno firmware design is also developed and tested for the ZedBoard kit and targets an ARM® Cortex®-A9 processor placed inside a Xilinx Zynq system-on-chip (SoC). An AXI MAX11100 custom IP core is created for this reference design to optimize the sampling rate and the SPI timing stability.

The firmware is a working example of how to interface to the hardware, collect samples, and save them to memory. The simple process flow is shown in Figure 3. The firmware is written in C using the Xilinx SDK tool,

which is based on the Eclipse open source standard. Custom Fresno-specific design functions were created utilizing the AXI MAX11100 custom IP core. The SPI clock frequency is set to 4.54MHz when a 189.4ksps sampling rate is selected. The SPI clock frequency is set to 2.5MHz for all other sampling rates.

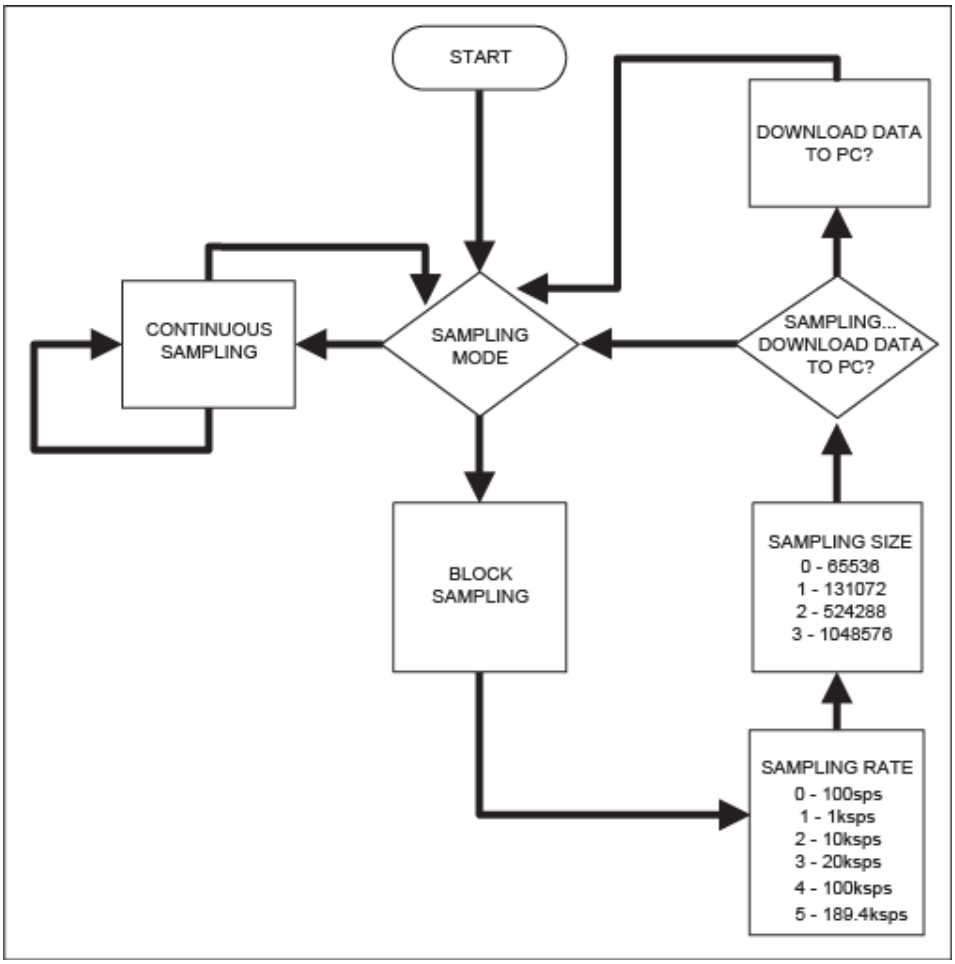


Figure 3. The Fresno firmware flowchart for ZedBoard platform.

The firmware accepts commands, writes statuses, and is capable of downloading blocks of sampled data to a standard terminal program via a virtual COM port. The complete source code is provided to speed up customer development. Code documentation can be found with the corresponding firmware platform files.

Quick Start

Required equipment:

- Windows® PC with two USB ports
- Fresno (MAXREFDES11#) Board
- Fresno-supported Platform (i.e., Nexys 3 development kit or ZedBoard kit)
- Industrial sensor or signal source

Download, read, and carefully follow each step in the appropriate Fresno Quick Start Guide:

- Fresno (MAXREFDES11#) Nexys 3 Quick Start Guide

- Fresno (MAXREFDES11#) ZedBoard Quick Start Guide

Lab Measurements

Equipment used:

- Audio Precision® SYS-2722 signal source or equivalent
- Voltage calibrator DVC-8500
- Windows PC with two USB ports
- Fresno (MAXREFDES11#) board
- Nexys 3 development kit
- +10V power supply
- -5V power supply

Special care must be taken and the proper equipment must be used when testing the Fresno design. The key to testing any high-accuracy design is to use sources and measurement equipment that are of higher accuracy than the design under test. A low distortion signal source is absolutely required in order to duplicate the presented results. The input signal was generated using the Audio Precision SYS-2722. The FFTs were created using the FFT control in SignalLab from Mitov Software.

AC and DC performance for on-board isolated power is shown in **Figure 4** and **Figure 5**. AC and DC performance for external power is shown in **Figure 6** and **Figure 7**.

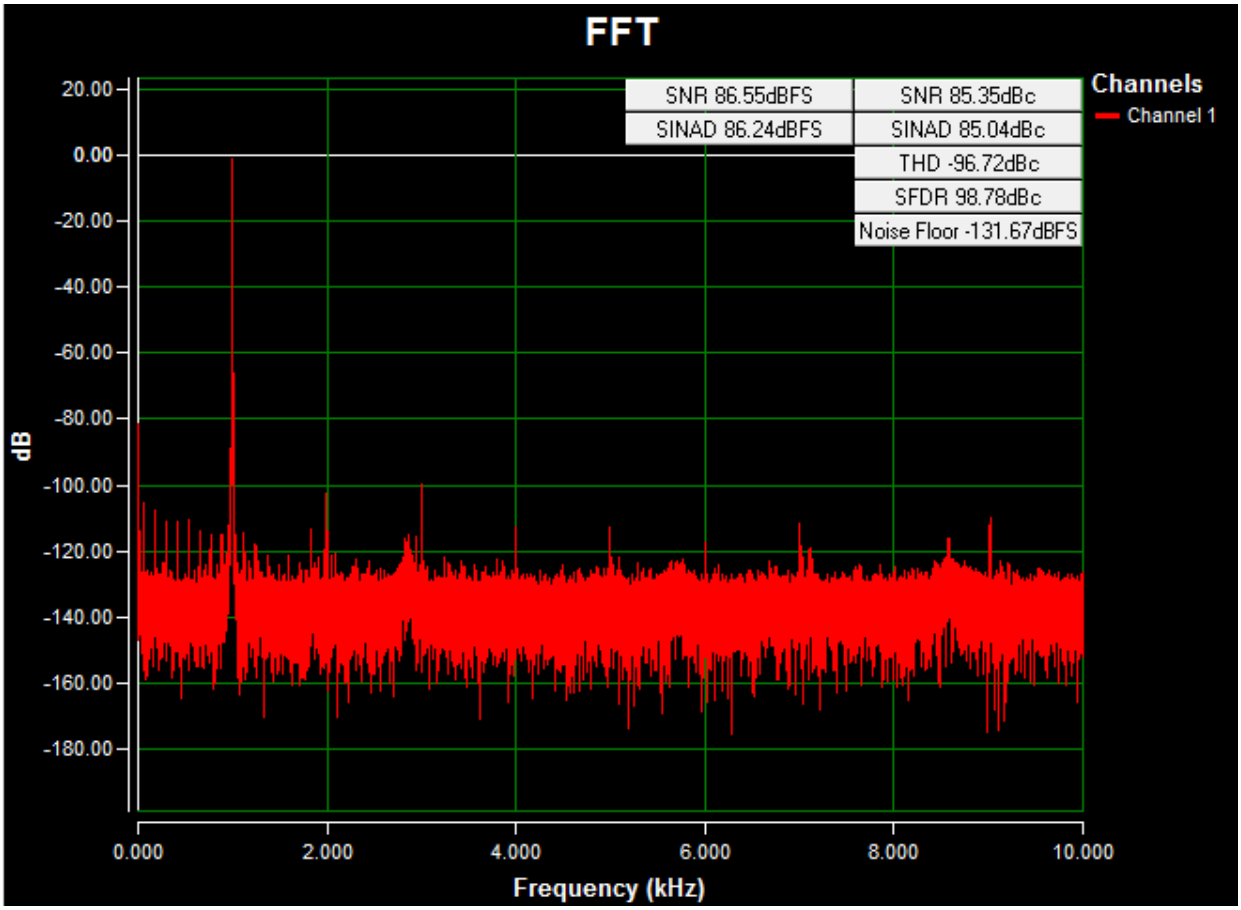


Figure 4. AC FFT using on-board isolated power, a 0 to 10V 1kHz sine wave input signal, high-impedance input, a 20ksps sample rate, and a Blackman-Harris window.

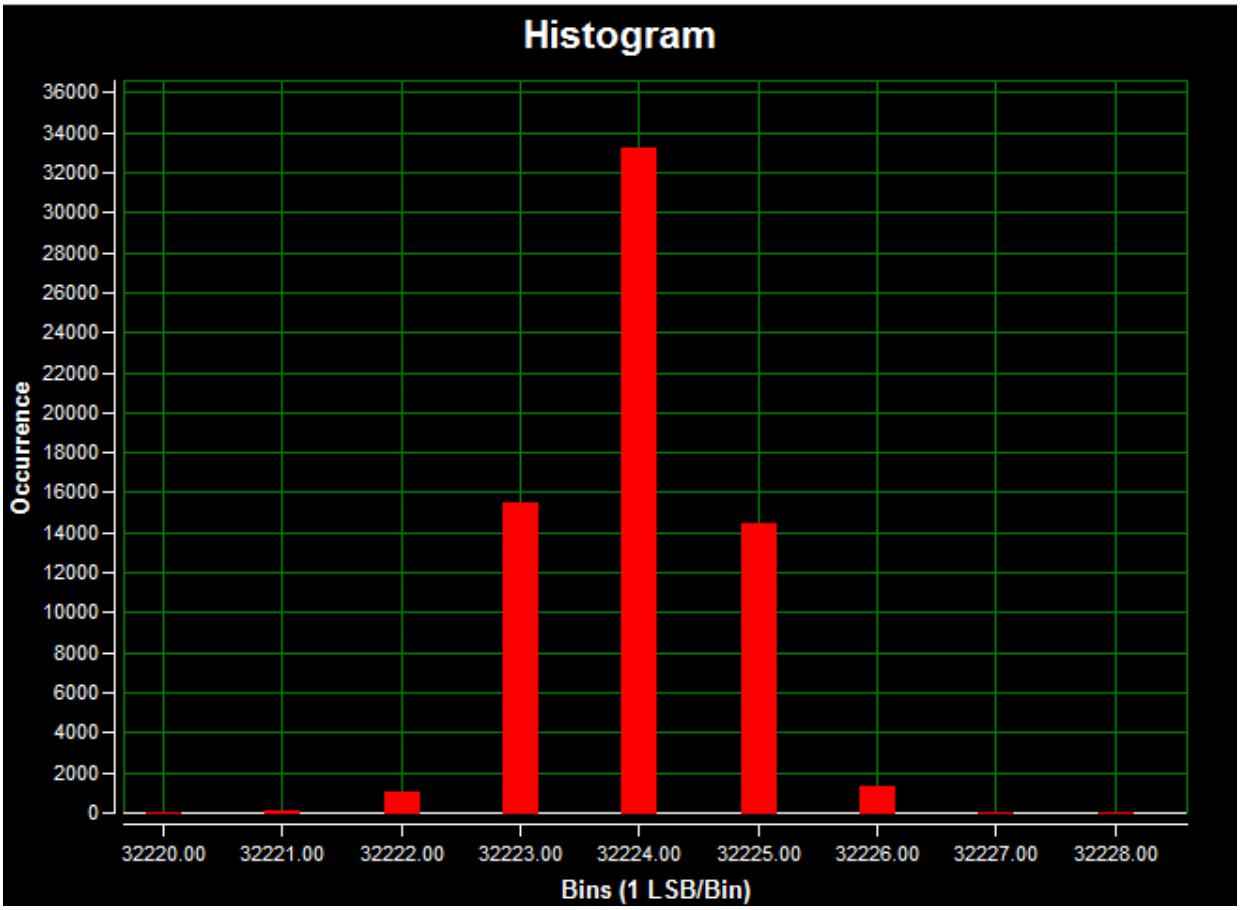


Figure 5. DC histogram using on-board isolated power; a 5V input signal; a 20ksps sample rate; 65,536 samples; a code spread of 8 LSBs with 96.3% of the codes falling within the three center LSBs; and a standard deviation of 0.785.

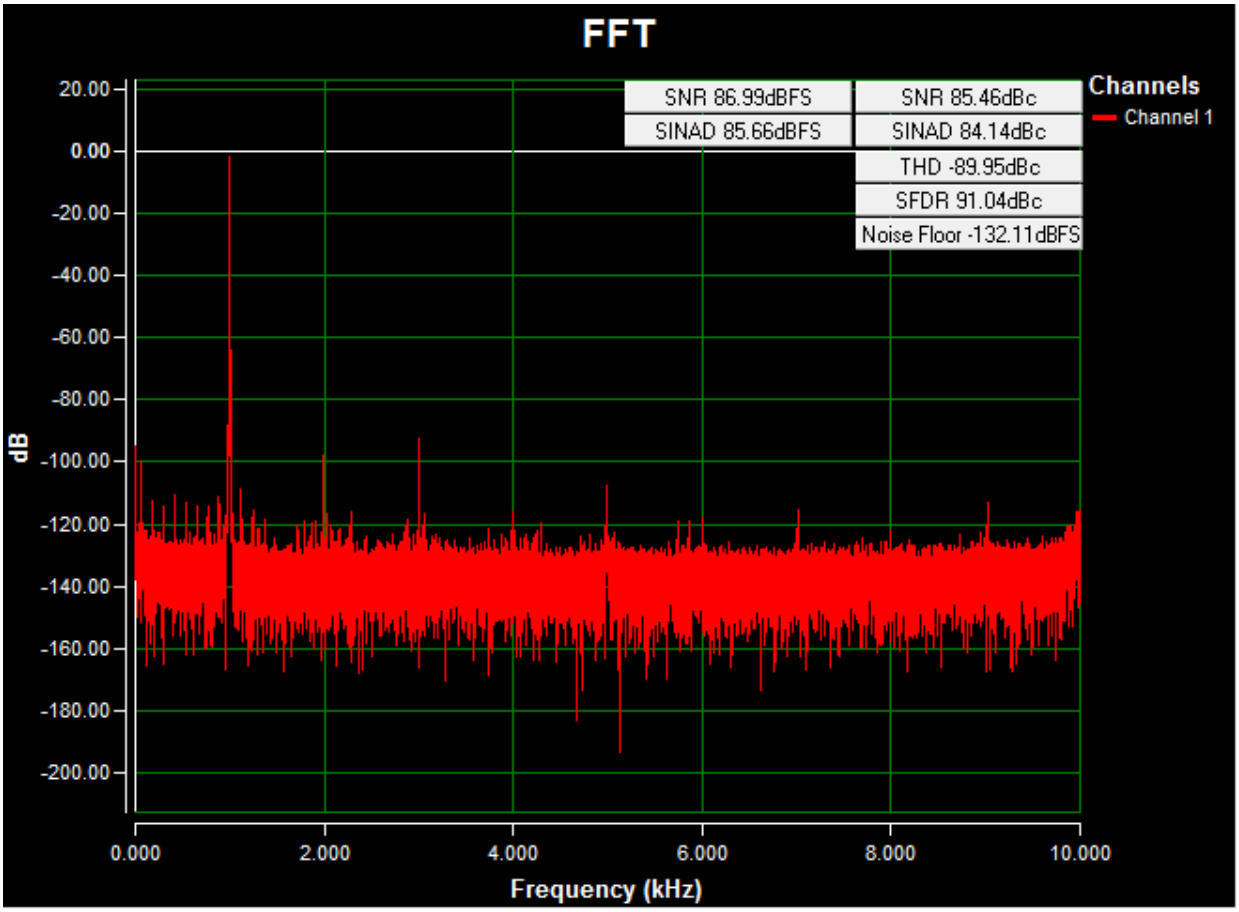


Figure 6. AC FFT using external power, a 0 to 10V 1kHz sine wave input signal, a 20ksps sample rate, and a Blackman-Harris window.

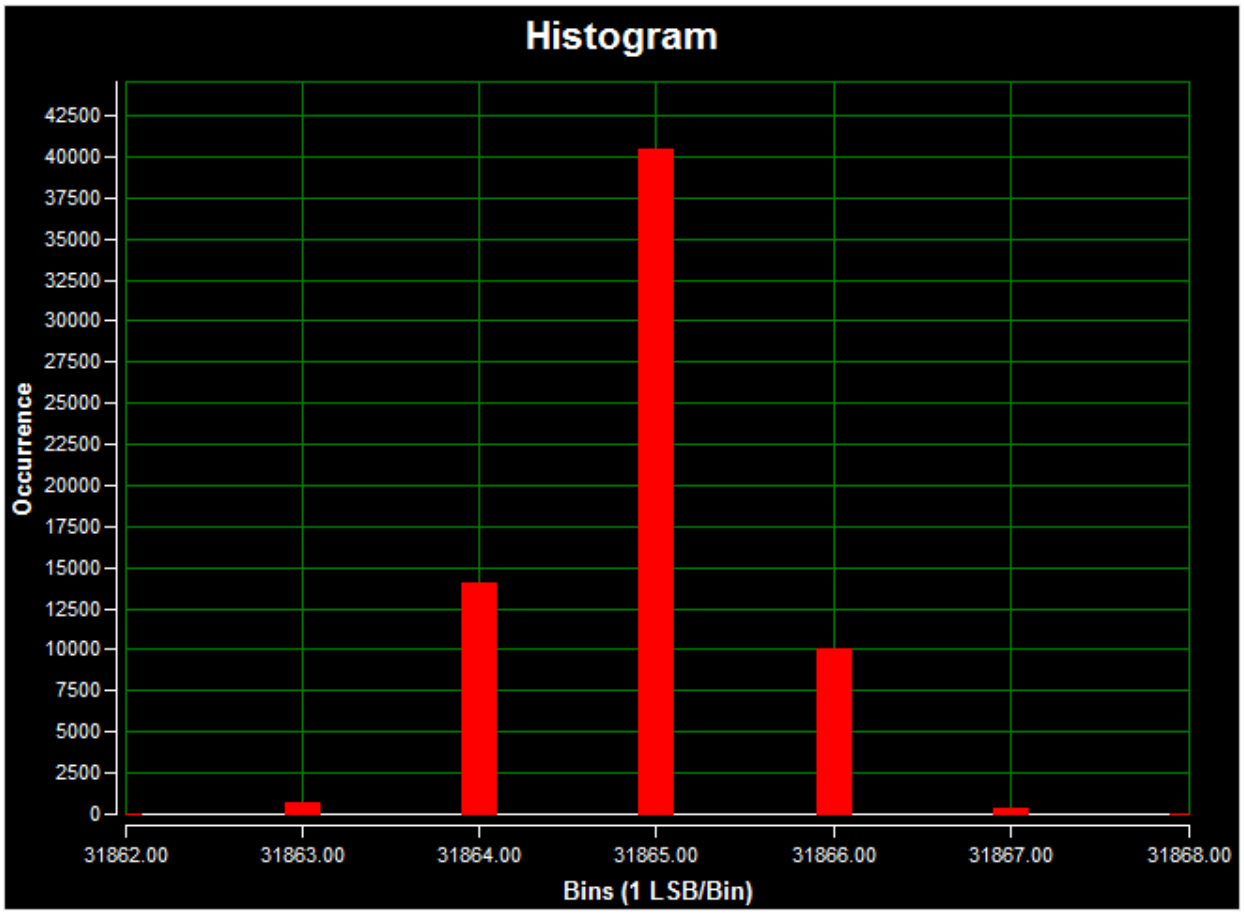


Figure 7. DC histogram using external power; a 5V input signal; a 20ksps sample rate; 65,536 samples; a code spread of 7 LSBs with 98.5% of the codes falling within the three center LSBs; and a standard deviation of 0.651.