DESCRIPTION

The MP8833 is a monolithic thermoelectric cooler controller with built-in internal power MOSFETs. It achieves 1.5A of continuous output current from a 2.7V to 5.5V input voltage range with a thermoelectric cooler (TEC) voltage range. The TEC voltage is linearly controlled by the analog voltage.

Features such as TEC voltage and current limiting are controlled by the 400kHz I^{2}C serial interface. The MP8833 is ideal for TEC device applications, such as optical laser diodes and fiber communication networks.

Full protection features include internal soft start, over-current protection (OCP), over-voltage protection (OVP), and over-temperature protection (OTP).

The MP8833 is available in a QFN-16 (2mmx3mm) package for a minimum solution size.

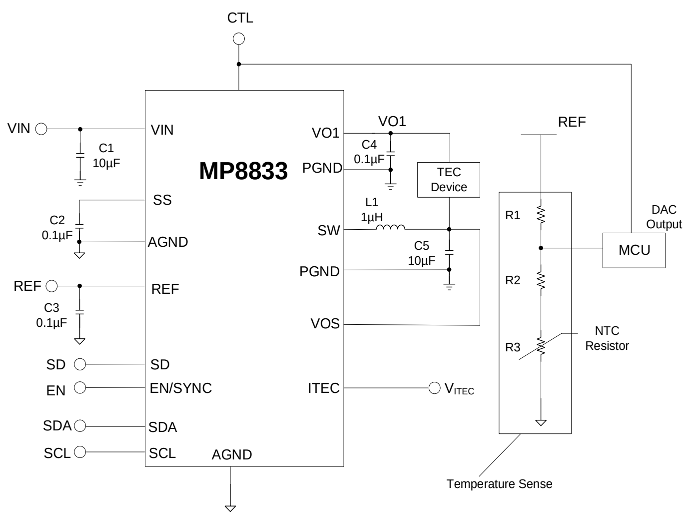
FEATURES

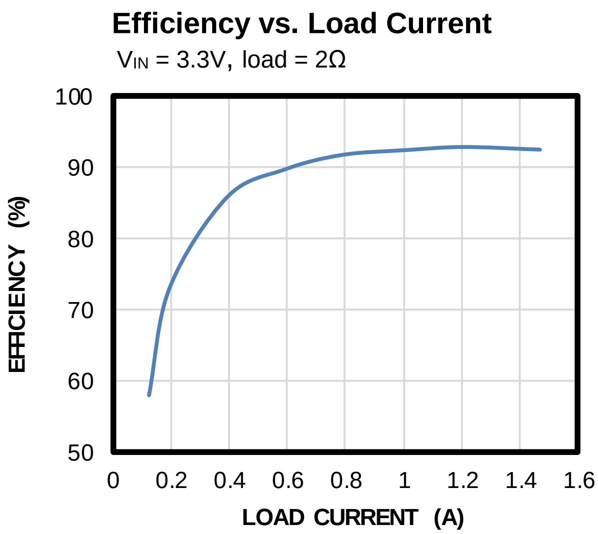
- 1% 2.5V REF Accuracy
- Wide 2.7V to 5.5V Operating Input Range
- Up to 1.5A TEC Current
- TEC Current Monitor
- 30mΩ Internal MOSFETs for PWM Switches and Linear Switches
- Default 1MHz Switching Frequency
- External SYNC Function
- EN/SD for Power Sequencing
- Available in a QFN-16 (2mmx3mm) Package

APPLICATIONS

- Optical Laser Diode Modules
- Fiber Communication Networks
- Systems with TEC Temperature Control

TYPICAL APPLICATION





OTP-EFUSE SELECTED TABLE BY DEFAULT (MP8833GD-0000-Z):

OTP Item	HEATING	COOLING
Enable Current Limit	Enable	Enable
Current Limit Value	1.521A	1.521A
Enable Voltage Limit	Enable	Enable
Voltage Limit Value	2.83V	2.83V
LDO High-Side Current Limit	1.8A	
LDO Low-Side Current Limit	1.8A	
BUCK High-Side Current Limit	3A	
BUCK Low-Side Current Limit	3A	
Discharge Time	35ms	
Enable Vin OVP	Enable	
SS Current	3uA(Typical)	
Power Stage On	ON	
I^2C Slave Address	0X60	

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP8833GD-xxxx**	QFN-16 (2mmx3mm)	*See Below*	
MP8833GD-0000	QFN-16 (2mmx3mm)	*See Below*	1
EVKT-MP8833	Evaluation kit		

* For Tape & Reel, add suffix –Z (e.g. MP8833GD-xxxx–Z).

** "xxxx" is the configuration code identifier for the register setting stored in the OTP. The default number is "0000". Each "x" can be a hexadecimal value between 0 and F. Work with an MPS FAE to create this unique number, even if ordering the "0000" code. MP8833GD-0000 is the default version.

TOP MARKING

BAP
YWW
LLL

BAP: Product code of MP8833GD
Y: Year code
WW: Week code
LLL: Lot number

EVALUATION KIT EVKT-MP8833

EVKT-MP8833 kit contents (the items listed below can be ordered separately, and the GUI installation file and supplemental documents can be downloaded from the MPS website.):

#	Part Number	Item	Quantity
1	EV8833-D-01B	MP8833GD-CCCC evaluation board	1
2	EVKT-USBI2C-02	Includes one USB to I²C communication interface, one USB cable, and one ribbon cable	1
3	MP8833GD-CCCC	MP8833 IC that can be used for OTP programming	2
4	Online resources	Include datasheet, user guide, product brief, and GUI	1

Order directly from MonolithicPower.com or our distributors.

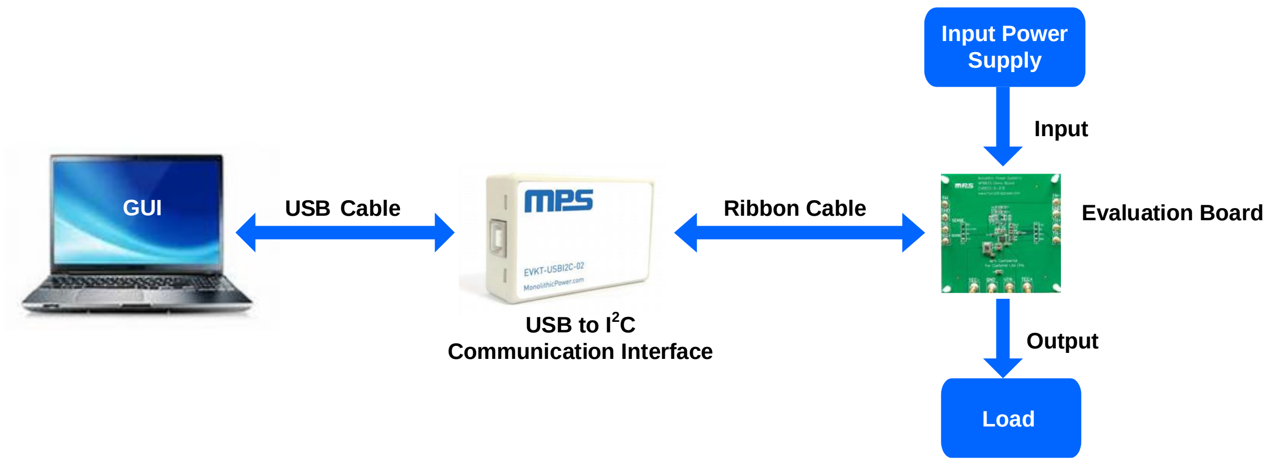
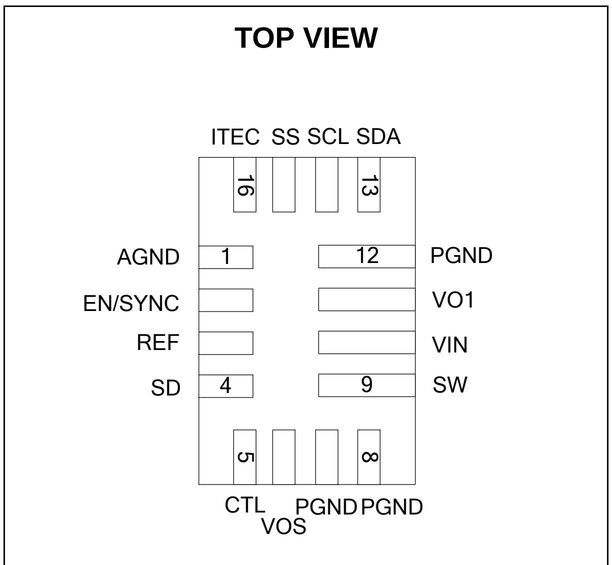


Figure 1: EVKT-MP8833 Evaluation Kit Set-Up

PACKAGE REFERENCE



QFN-16 (2mmx3mm)

PIN FUNCTIONS

Pin #	Name	Description
1	AGND	**Analog ground.**
2	EN/SYNC	**EN control.** High logic turns on the power stage. If external synchronization is used for the input, the internal switching frequency is masked.
3	REF	**2.5V reference output.**
4	SD	**Shutdown signal.**
5	CTL	**Voltage control pin.** The CTL pin's voltage regulates the voltages of VOS and VO1.
6	VOS	**PWM regulator output sense pin.**
7, 8, 12	PGND	**Power ground.**
9	SW	**Switch node.** Connect an inductor to this pin to regulate the VOS voltage.
10	VIN	**Power supply input.**
11	VO1	**One terminal of the TEC device.** VO1 sinks the current if CTL exceeds 1.25V. VO1 sources the current if CTL is below 1.25V.
13	SDA	**I^2C serial data.**
14	SCL	**I^2C serial clock.**
15	SS	**Soft start**. Connect a ceramic capacitor between SS and GND.
16	ITEC	**TEC current monitor output.** The output voltage is proportional to the VO1 current.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) 6.5V
V_{SW} ....
-0.3V (-5V for <10ns) to +6.5V (8V for <10ns)
All other pins............................... -0.3V to +6.5V
Junction temperature .... 150°C
Lead temperature .... 260°C
Continuous power dissipation (T_A = 25°C) (2) (4)
QFN……………..2.27W
Storage temperature................-65°C to +150°C

ESD Rating

Human body model (HBM) 2000V
Charged device model (CDM).................. 2000V

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .... 2.7V to 5.5V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance	θ_{JA}	θ_{JC}	
EV8833-D-01B (4)	55	12	°C/W
JESD51-7 (5)	70	15	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on MPS demo board, 4-layer 63mmx63mm PCB.
5) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 3.3V, T_J = -40°C to +125°C, typical value is tested at T_J = 25°C. The over-temperature limit is guaranteed by characterization, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
V_{IN} range			2.7		5.5	V
Under-voltage lockout rising threshold			2.5	2.6	2.7	V
Under-voltage lockout hysteresis threshold				150		mV
Reference voltage	V_{REF}	V_{IN} = 3.3V, I_{REF} = 2mA, T_J = 25°C	2.49	2.5	2.51	V
		V_{IN} = 3.3V, I_{REF} = 2mA, T_J = -40°C to +125°C	2.475	2.5	2.525	
Supply current (shutdown)		V_{EN} = 0V		600		µA
Supply current (quiescent)		Not switching		1		mA
Power MOSFETs						
VO1 PFET switch on resistance	R_{DSON_P1}	V_{IN} = 5V		30		mΩ
		V_{IN} = 3.3V		40		
VO1 NFET switch on resistance	R_{DSON_N1}	V_{IN} = 5V		30		mΩ
		V_{IN} = 3.3V		40		
Buck PFET switch on resistance	R_{DSON_P2}	V_{IN} = 5V		30		mΩ
		V_{IN} = 3.3V		40		
Buck NFET switch on resistance	R_{DSON_N2}	V_{IN} = 5V		30		mΩ
		V_{IN} = 3.3V		40		
VO1 leakage		V_{EN} = 0V, V_{IN} = 6V, remove discharge path, V_{SW} = 0V or 6V, T_J = 25°C		0	2	µA
Buck SW leakage		V_{EN} = 0V, V_{IN} = 6V, V_{VO1} = 0V or 6V, T_J = 25°C		0	2	µA
Maximum VO1 PFET source current (first limit range)		By I^2C or OTP trim	0.039		2.028	A
Maximum VO1 NFET sink current (first limit range)		By I^2C or OTP trim	0.039		2.028	A
Maximum VO1 PFET source current (second limit range)		By I^2C or OTP trim	1.2		2.1	A
Maximum VO1 NFET sink current (second limit range)		By I^2C or OTP trim	1.2		2.1	A
Maximum positive TEC voltage range [(8)]	V_{TEC_LIM1}	By I^2C or OTP trim		Min (V_{IN} x 85% or V_{IN} - 0.5V)		V
Maximum negative TEC voltage range [(8)]	V_{TEC_LIM2}	By I^2C or OTP trim		Min (V_{IN} x 85% or V_{IN} - 0.5V)		V
Hiccup off time				24		ms
TEC voltage gain to CTL				5		V/V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, T_J = -40°C to +125°C, Typical value is tested at T_J = 25°C. The over-temperature limit is guaranteed by characterization, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Frequency Setting						
Buck duty cycle range		1MHz switching frequency	10		85	%
Switching frequency	f_{SW}		700	1000	1100	kHz
Minimum off time	$t_{MIN-OFF}$			65		ns
Minimum on time	t_{MIN-ON}			90		ns
EN/SYNC input logic low voltage	EN_L				0.4	V
EN/SYNC input logic high voltage	EN_H		1.2			V
SYNC frequency range			1		3	MHz
SYNC input duty range			20		80	%
Turn on check time		EN turn on IC to start SW		36		ms
SYNC rising delay (7)		From SYNC rising to SW rising		20		ns
EN/SYNC input current	I_{EN}	V_{EN} = 2V		1.5		µA
		V_{EN} = 0V		0		µA
SD input logic low voltage	EN_L				0.4	V
SD input logic high voltage	EN_H		1.2			V
SD pull-down resistor				1.3		MΩ
SD turn-on delay		SD turn on IC		36		ms
TEC						
ITEC initial voltage		I_{VO1} = 0		1.25		V
ITEC current gain				0.5		V/A
ITEC monitor voltage accuracy		I_{VO1} sink (or source) > 500mA, V_{IN} = 3.3V	-20		+20	%
ITEC output current				0.3		mA
VTEC voltage limit accuracy		>700mV and < -700mV, V_{IN} = 3.3V	-15		+15	%
ITEC current limit accuracy		I_{VO1} sink (or source) >700mA, V_{IN} = 3.3V	-20		+20	%
Analog						
Discharge time		I²C Reg00 SYS_SET[D4] = 0		70		ms
		I²C Reg00 SYS_SET[D4] = 1		35		ms
Soft-start current	I_{SS}		1.5	3	4.5	µA
Output discharge				100		Ω

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, T_J = -40°C to +125°C, Typical value is tested at T_J = 25°C. The over-temperature limit is guaranteed by characterization, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
I²C						
Heating mode threshold (7)		V_{O1} minus V_{OS}		30		mV
Cooling mode threshold (7)		V_{O1} minus V_{OS}		30		mV
SCL, SDA input high voltage (6)			1.2			V
SCL, SDA input low voltage (6)					0.4	V
I²C clock frequency (6)				400		kHz
Protection						
Thermal shutdown (7)				160		°C
Thermal hysteresis (7)				20		°C
Temperature warning threshold (7)	T_{OTW}			120		°C
OTW hysteresis (7)	T_{OTW_H}			20		°C
Input over-voltage threshold		I²C enable		5.9	6.5	V
Input over-voltage hysteresis		I²C enable		0.3		V
VTEC over-voltage threshold (7)		V_{O1} minus V_{OS}, absolute value		1		V
System (8)						
Recommended input capacitance			10	22		µF
Recommended inductance			0.47	1	2.2	µH
V_{OS} recommended output capacitance			10	22		µF
V_{O1} recommended output capacitance				0.1		µF
V_{OS} output voltage ripple		V_{IN} = 3.3V, V_{OS} = 2.5V, L = 1µH, C_{VOS} = 10µF, default 1MHz		8		mV
V_{O1} output voltage ripple		V_{IN} = 3.3V, V_{O1} = 3.3V, C_{VO1} = 1µF			1	mV
Efficiency		V_{IN} = 3.3V, V_{O1} = 3.3V, V_{OS} = 2V, default 1MHz, I_O = 1A, L_{DCR} = 27mΩ		94		%

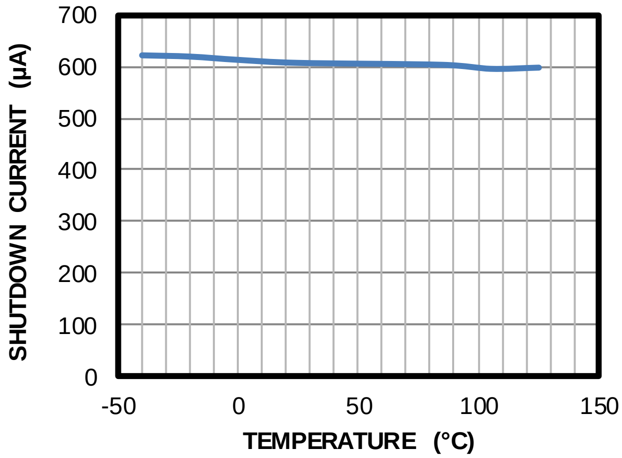
Notes:

6) I/O level characteristics.
7) Guaranteed by characterization test, not tested in production.
8) Guaranteed by EVB characterization test, not tested in production.

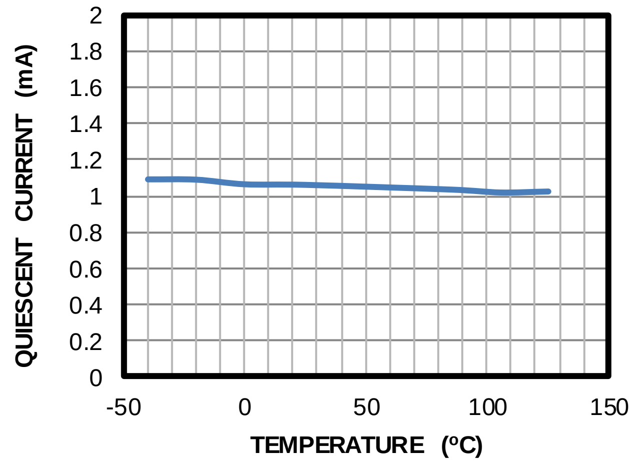
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.3V, L = 1µH, C_{OUT} = 10µF, T_A = 25°C, unless otherwise noted.

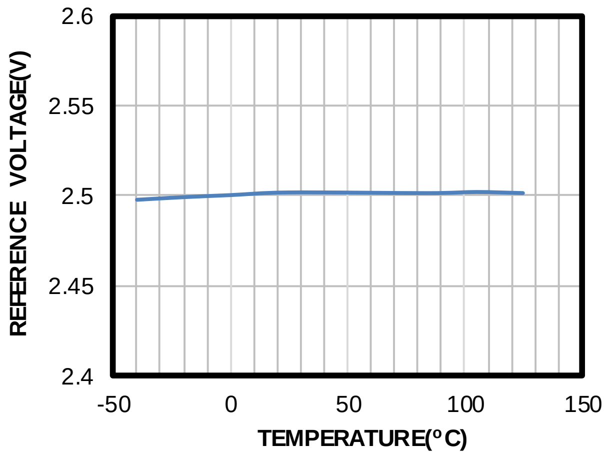
Shutdown Current vs. Temperature



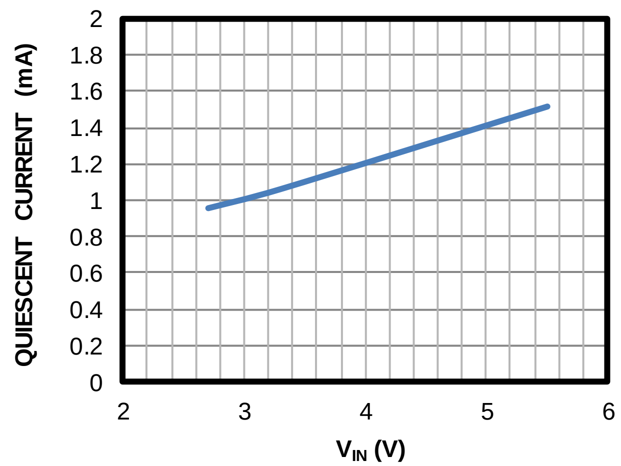
Quiescent Current vs. Temperature



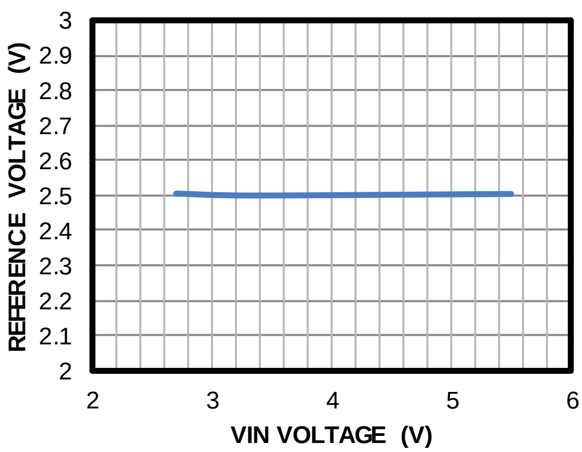
Reference Voltage vs. Temperature



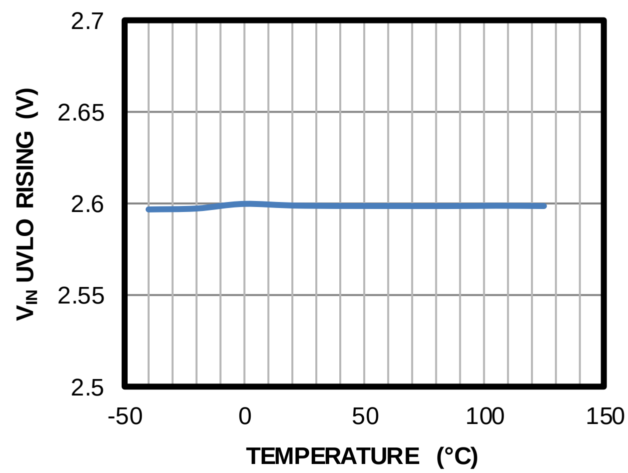
Quiescent Current vs. V_{IN}



Reference Voltage vs. V_{IN}

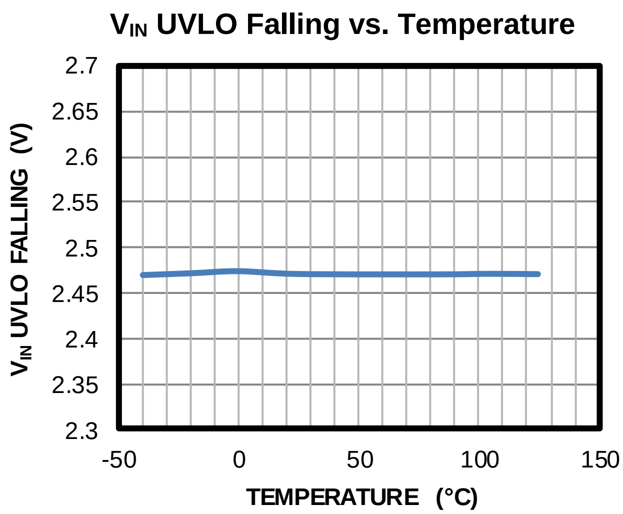


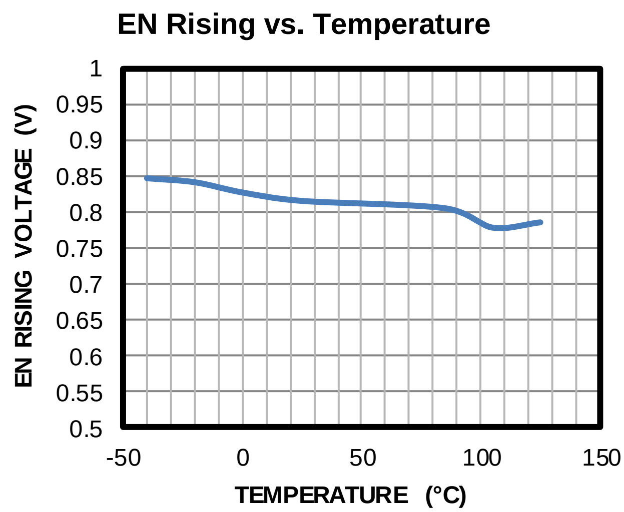
V_{IN} UVLO Rising vs. Temperature

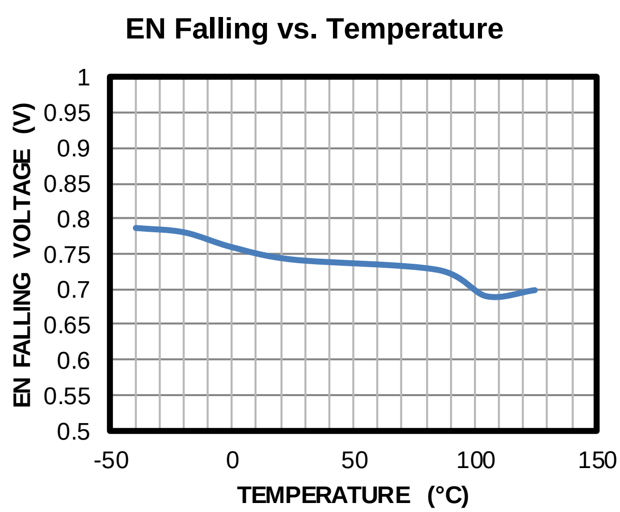


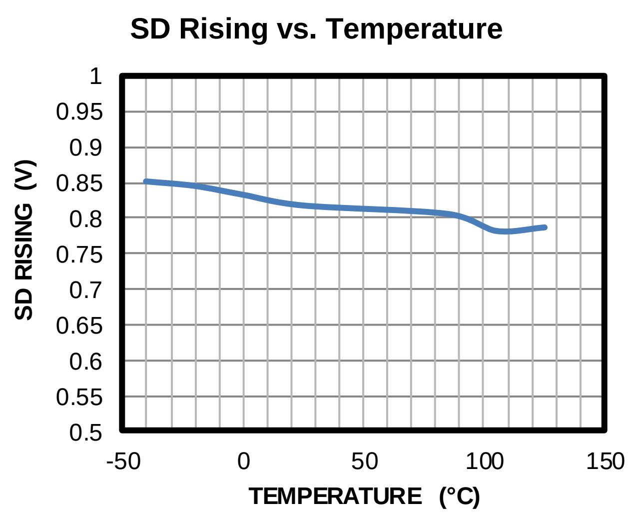
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

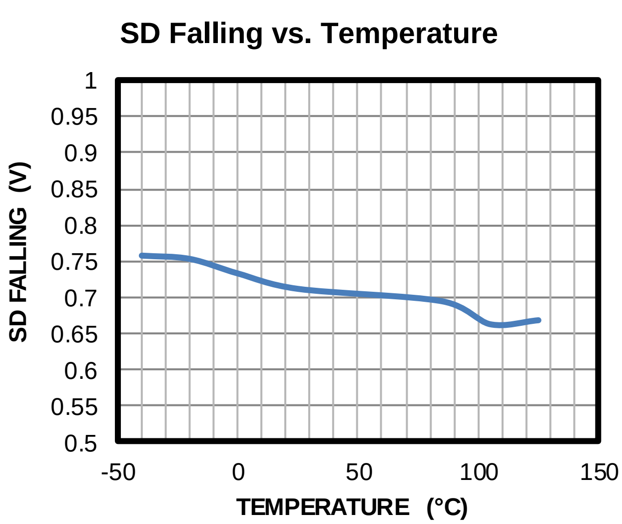
V_{IN} = 3.3V, L = 1µH, C_{OUT} = 10µF, T_A = 25°C, unless otherwise noted.











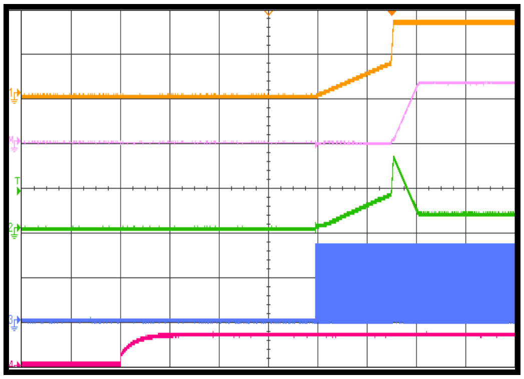
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, L = 1µH, C_{OUT} = 10µF, T_A = 25°C, unless otherwise noted.

VIN Start-Up

V_{IN} = 3.3V, I_{OUT} = 0A, cooling

CH1: TEC+ 2V/div.
M: TEC+ to TEC- 2V/div.
CH2: TEC- 2V/div.
CH3: SW 2V/div.
CH4: V_{IN} 5V/div.

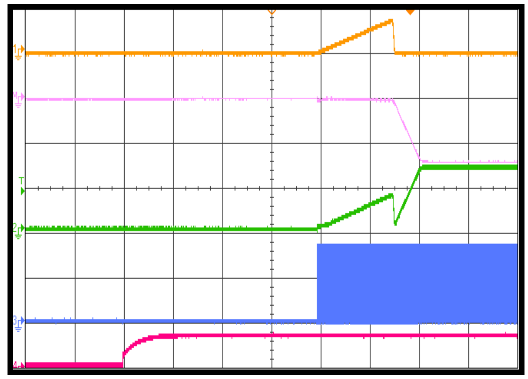


10ms/div.

VIN Start-Up

V_{IN} = 3.3V, I_{OUT} = 0A, heating

CH1: TEC+ 2V/div.
M: TEC+ to TEC- 2V/div.
CH2: TEC- 2V/div.
CH3: SW 2V/div.
CH4: V_{IN} 5V/div.

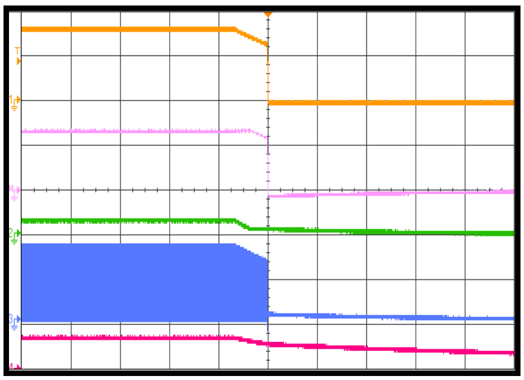


10ms/div.

VIN Shutdown

V_{IN} = 3.3V, I_{OUT} = 0A, cooling

CH1: TEC+ 2V/div.
M: TEC+ to TEC- 2V/div.
CH2: TEC- 2V/div.
CH3: SW 2V/div.
CH4: V_{IN} 5V/div.

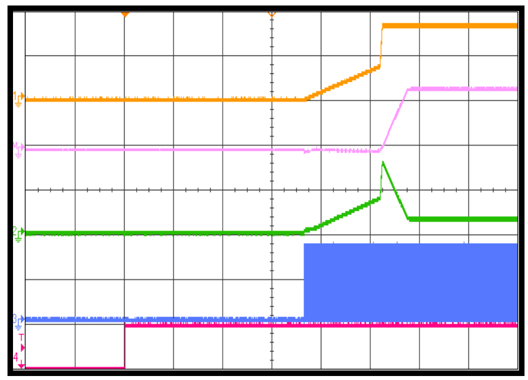


20ms/div.

EN Start-Up

V_{IN} = 3.3V, I_{OUT} = 0A, cooling

CH1: TEC+ 2V/div.
M: TEC+ to TEC- 2V/div.
CH2: TEC- 2V/div.
CH3: SW 2V/div.
CH4: V_{EN} 5V/div.

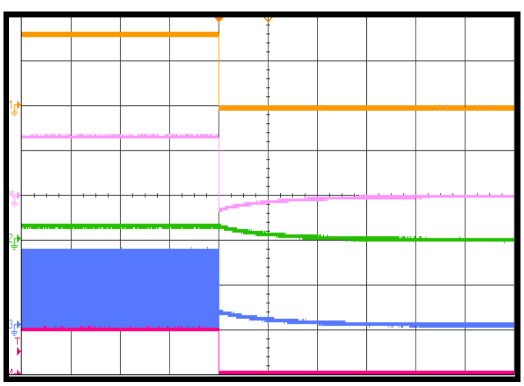


10ms/div.

EN Shutdown

V_{IN} = 3.3V, I_{OUT} = 0A, cooling

CH1: TEC+ 2V/div.
M: TEC+ to TEC- 2V/div.
CH2: TEC- 2V/div.
CH3: SW 2V/div.
CH4: V_{EN} 5V/div.

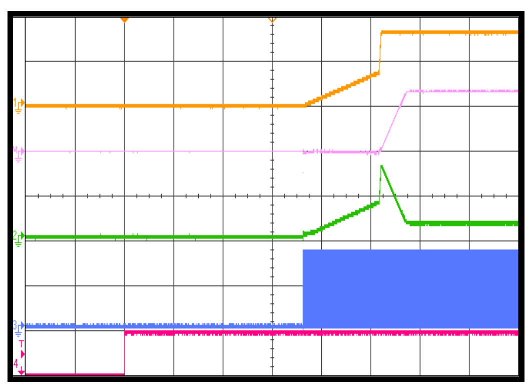


50ms/div.

SD Start-Up

V_{IN} = 3.3V, I_{OUT} = 0A, cooling

CH1: TEC+ 2V/div.
M: TEC+ to TEC- 2V/div.
CH2: TEC- 2V/div.
CH3: SW 2V/div.
CH4: V_{SD} 5V/div.



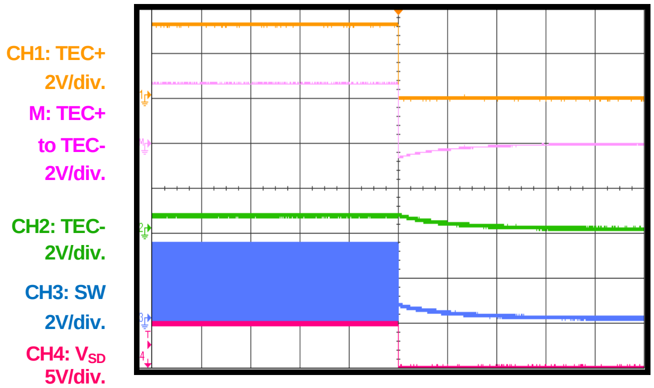
10ms/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, L = 1μH, C_{OUT} = 10μF, T_A = 25°C, unless otherwise noted.

SD Shutdown

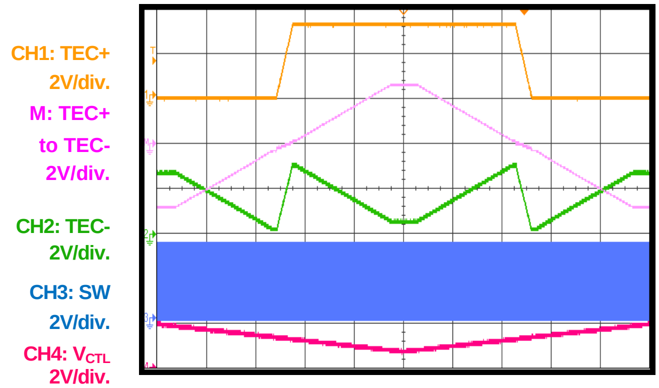
V_{IN} = 3.3V, I_{OUT} = 0A



50ms/div.

CTL Transient

V_{IN} = 3.3V, I_{OUT} = 0A



100ms/div.

FUNCTIONAL BLOCK DIAGRAM

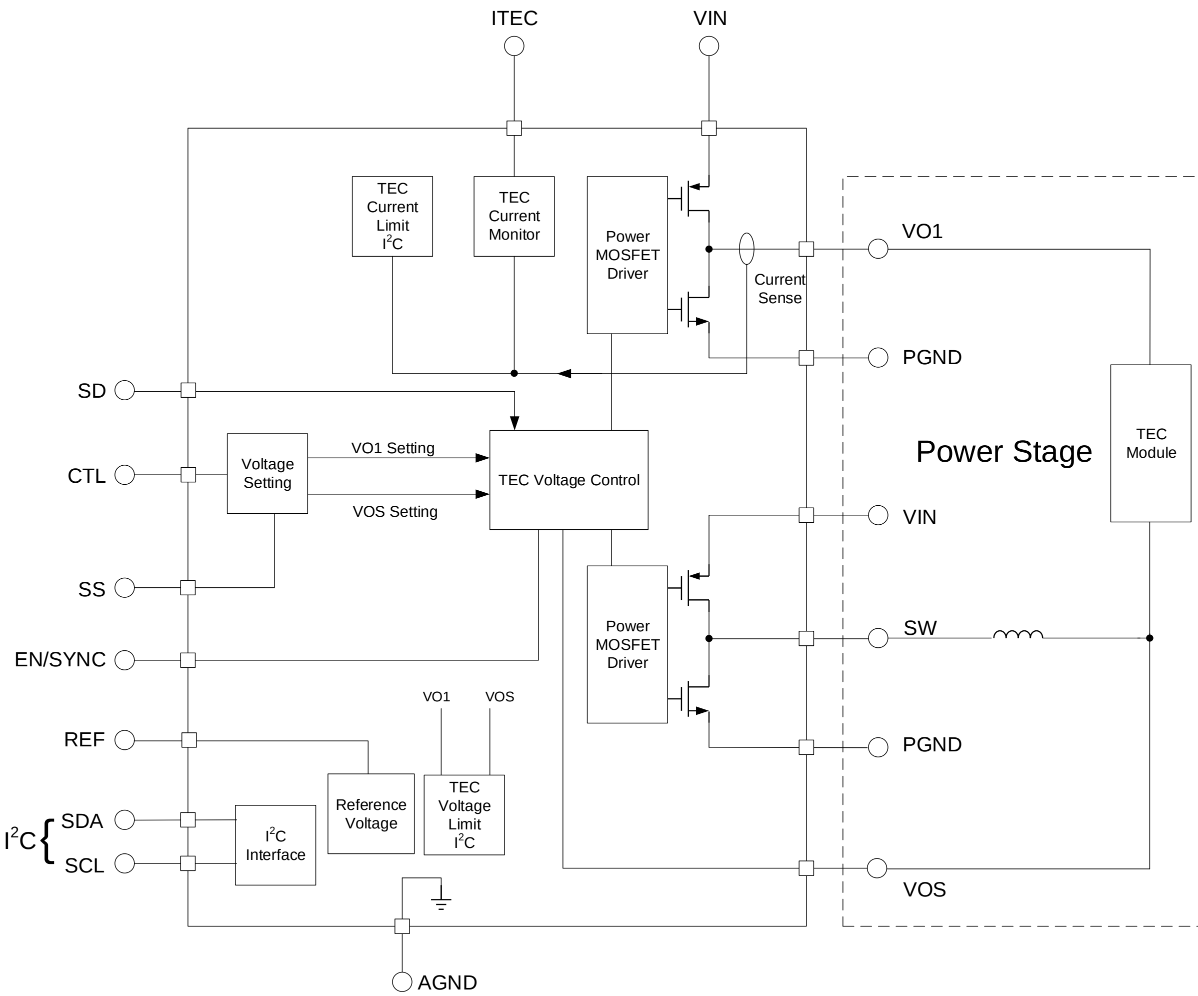


Figure 2: Functional Block Diagram

OPERATION

The MP8833 is a monolithic thermoelectric cooler controller with built-in internal power MOSFETs. It achieves 1.5A of continuous output current across a 2.7V to 5.5V input voltage range. The thermoelectric cooler (TEC) voltage is linearly controlled by the analog voltage.

Features such as TEC voltage and current limiting are controlled on the fly through the 400kHz I^2C serial interface, which requires minimal external components. Contained within a 2mmx3mm QFN package, the MP8833 offers a minimum solution size.

Full protection features include internal soft start, over-current protection (OCP), over-voltage protection (OVP), and over-temperature protection (OTP).

TEC Voltage Control

The TEC voltage (V_{TEC}) is formed by the VO1 and VOS voltage gap. VO1 is the linear regulator output, and VOS senses the pulse-width modulation (PWM) regulator output voltage. The VO1 and VOS voltages (as well as the TEC device's voltage) are controlled by the CTL pin's voltage (see Figure 3). Use a CTL input from a digital PID controller or an external analog control loop to automatically set the VO1 and VOS voltages internally.

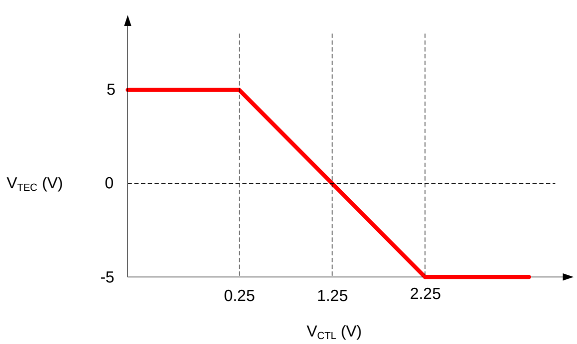


Figure 3: V_{CTL} vs. V_{TEC}

V_{TEC} is limited by V_{IN} and V_{LIMIT}. It can be calculated with Equation (1):

$$V_{TEC}(V) = -5 \times (V_{CTL}(V) - 1.25V) \quad (1)$$

The VO1 voltage (V_{VO1}) can be calculated with Equation (2):

$$V_{VO1}(V) = V_{MID} - 40 \times (V_{CTL}(V) - 1.25V) \quad (2)$$

Where V_{MID} is 1.5V.

The VOS voltage (V_{VOS}) can be estimated with Equation (3):

$$V_{VOS}(V) = V_{VO1}(V) + 5 \times (V_{CTL}(V) - 1.25V) \quad (3)$$

VO1 and VOS are also limited by V_{IN} and V_{LIMIT}. For example, if V_{CTL} is 0.8V, V_{VO1} should be 19.5V when using Equation (2). If V_{IN} is the highest voltage at about 3.3V, V_{VO1} is 3.3V, and V_{VOS} is about 1.05V.

Both the linear and PWM regulators have a current source and sink capability up to 1.5A. The device's TEC voltage can be positive or negative, depending on the application.

TEC Current Monitor

The MP8833 provides a current monitoring function through the TEC. The ITEC pin outputs a voltage proportional to the device's current.

The ITEC voltage is calculated with Equation (4) and Equation (5) for cooling and heating, respectively:

$$V_{ITEC}(V) = 1.25V + I_{OUT}(A) \times 0.5(V/A) \quad (4)$$

$$V_{ITEC}(V) = 1.25V - I_{OUT}(A) \times 0.5(V/A) \quad (5)$$

The accuracy of the equation degrades when I_{OUT} is below 500mA. The TEC current monitor also provides current info to the TEC current limit comparator. The TEC current limit value is set by the I^2C.

Reference

The MP8833 provides a 1% accuracy reference voltage (V_{REF}). V_{REF} outputs 2.5V if V_{IN} exceeds 2.7V on the EN/SYNC, SD, and I^2C bits.

Power Stage

The MP8833 provides an H-bridge integrated power stage. The power stage includes an LDO and buck converter. The power stage activates if all of the following conditions are met:

1. V_{IN} and V_{CC} exceed their UVLO thresholds.
2. EN/SYNC is high or has an external synchronization input.
3. The SD voltage is high.
4. The I^2C on bit (Reg00 D[0]) is set to 1.

EN/SYNC

When the input voltage exceeds the under-voltage lockout (UVLO) threshold (typically 2.6V), the MP8833 power stage can be enabled by pulling the EN pin above 1.2V. Float EN or pull it down to ground to disable the MP8833. There is an internal 1.3MΩ resistor from the EN pin to ground.

When EN is on, the MP8833 discharges the TEC pre-biased voltage to 0V and begins to ramp up the VO1 and VOS voltages.

By pulling EN high, the switching frequency of the PWM regulator is set by a default internal setting. For external clock synchronization, connect a clock with a frequency range between 1MHz and 3MHz to EN/SYNC. When the frequency is too high, the buck voltage may be limited by a minimum on time and minimum off time, so a 1MHz to 1.5MHz range is recommended. After the output voltage is set, the internal clock rising edge synchronizes with the external clock rising edge.

By pulling EN low, the power stage is disabled after the EN turn-off delay.

Shutdown

The MP8833 has a shutdown pin to turn off the power stage. When it is low, it disables the power stage.

Soft Start (SS)

The MP8833 has a soft start (SS) function that ramps up the output voltage at a controlled slew rate to avoid overshoot at start-up.

Start-up includes three stages. First, after EN turns on, the power stage discharges VO1 and VOS to guarantee there is no TEC voltage. The discharge time is about 35ms or 70ms, based on the value set by the I^2C.

When VO1 and VOS reach 0V (or drop below 0.4V) after the discharge time, the MP8833 initiates start-up. The first start-up slew rate is controlled by an external SS capacitor. The SS pin sources a current and charges to V_{MID}. VO1 and VOS follow the SS pin voltage.

When VO1 and VOS reach V_{MID}, the second start-up procedure begins. VO1 and VOS are regulated to the target TEC voltage. The second slew rate is also controlled by the SS pin. For both procedures, the SS capacitor is charged or discharged by a fixed current (the I^2C sets the capacitor to discharge by 1x, 2x, 4x, or 8x the charge current). The SS voltage eventually equals $V_{CTL} + V_{MID}$ - 1.25V.

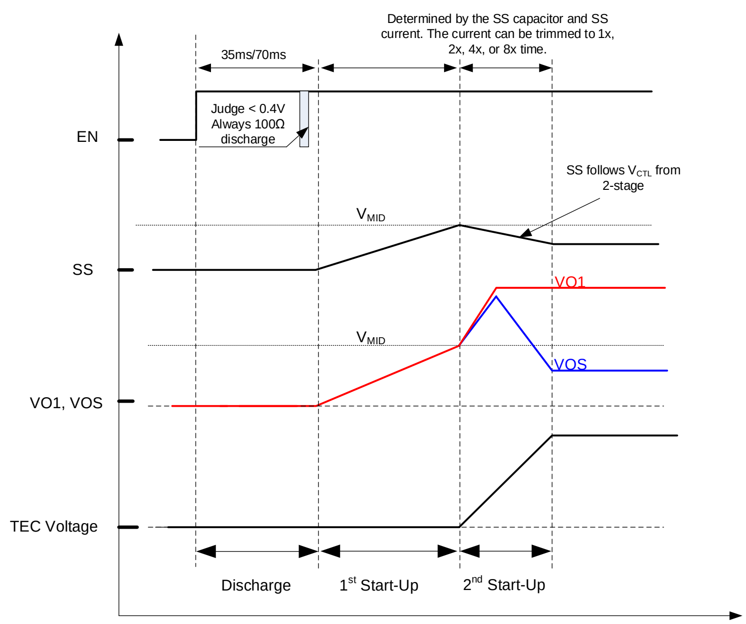


Figure 4: Soft Start

TEC Voltage Limit

The MP8833 has TEC voltage limit protection. The limit value can be set by the I²C without an external component.

When the TEC voltage exceeds the value set by the I²C (see Table 1), the buck output voltage for VOS is regulated to the limit value and not controlled by CTL. The limited voltage helps avoid risky operations (see Figure 5).

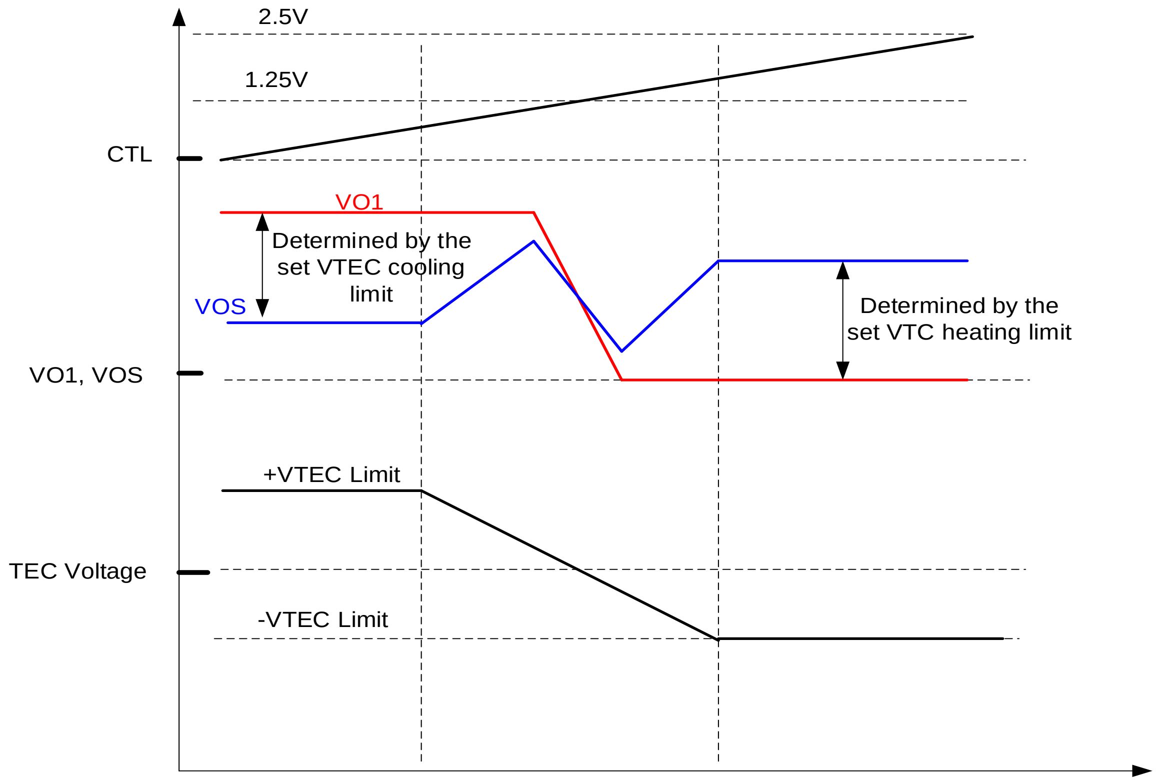


Figure 5: TEC Voltage Limit Protection

The TEC heating and cooling voltage limit is set by the I²C (Reg03 VLIM_HEAT [D5:D0], Reg04 VLIM_COOL [D5:D0]), respectively (see Table 1). The voltage limit has a 97.6mV step from 100mV to 5.5V. The MP8833 has a secondary TEC voltage limit that is set internally. Its typical value is the TEC voltage limit plus 1V. When a short condition occurs (e.g. one TEC terminal shorts to VIN or GND), the TEC voltage exceeds its secondary limit. The MP8833 immediately stops switching and enters hiccup mode.

Table 1: I²C Table

Addr	Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
03	VLIM_HEAT	R/W	ENVLIM_HEAT	VIN_OVP	VLIM_HEAT SET					
04	VLIM_COOL	R/W	ENVLIM_COOL	Reserved	VLIM_COOL SET					

TEC Current Limit

The MP8833 has two-level current limit protection. The limit value can be set by the I²C without an external component. The full current limit protection can be set and adjusted by the I²C (see Table 2).

The I²C (Reg01 ILIM_HEAT [D5:D0], Reg02 ILIM_COOL [D5:D0]) can set the first current limit level, respectively. The current limit has a 39mA step from 40mA to 2A. The MP8833 also has an LDO secondary TEC current limit and a buck current limit that are set by I²C (Reg05 LIMIT[D7:D6]). Address 05 in Table 2 show the secondary current limit for each.

Table 2: I²C Table

Addr	Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
01	ILIM_HEAT	R/W	ENILIM_HEAT	Reserved	ILIM_HEAT SET					
02	ILIM_COOL	R/W	ENILIM_COOL	Reserved	ILIM_COOL SET					
05	LIMIT	R/W	LDO_ILIM_HS		LDO_ILIM_LS		BUCK_ILIM_HS		BUCK_ILIM_LS	

When the TEC current exceeds its first current limit, the buck output voltage for VOS is regulated to the limit value and cannot be controlled by CTL.

The MP8833's VO1 pin has two-level current limiting with a first and second current limit. If the load ramp reaches VO1's first current limit, the MP8833 maintains VO1's output voltage and regulates VOS's output voltage. By limiting the TEC voltage, the TEC current is limited to the first current limit (see Figure 6).

When VO1 has error conditions, such as short to VIN or GND, the current ramps up very quickly and exceeds the second current limit. It triggers fast-off and enters hiccup mode immediately.

The MP8833's VOS has one-level current limiting. If the load ramp reaches the VOS current limit, the MP8833 tries to recover. The device enters hiccup mode if the short condition is not removed during the 100µs waiting period (see Table 3).

Table 3: Current Limiting

Rail	Current Level	Action After Trigger
VO1	First current limit	Maintain VO1 output, regulate VOS output
	Second current limit	Fast off immediately, enter hiccup mode
VOS	Current limit	Enter hiccup mode after 100µs waiting period

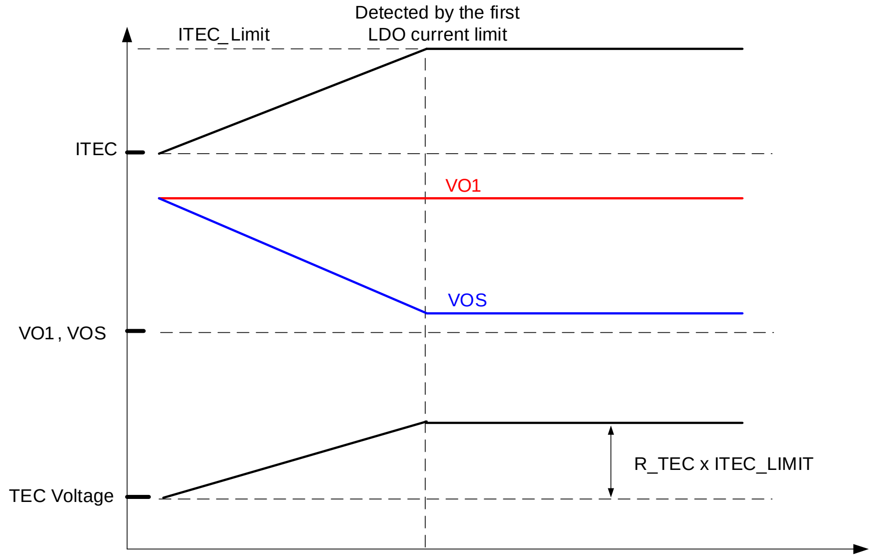


Figure 6: Current Limit Protection

Hiccup Protection

The MP8833 enters hiccup protection in certain conditions. These conditions include:

- VO1 exceeds its second current limit
- VOS exceeds its current limit
- V_{TEC} exceeds its second voltage limit

After confirming the condition, the MP8833 enters hiccup mode.

With this strategy, the MP8833 has full current protection for different risk conditions.

V_{IN} Over-Voltage Protection (OVP)

The MP8833 has V_{IN} over-voltage detection and protection, enabled by OTP. When V_{IN} exceeds 5.9V, the MP8833 stops the power stage and discharges VO1 and VOS until V_{IN} drops to 5.6V. After V_{IN} drops to 5.6V, the MP8833 starts a hiccup procedure. When the fault is removed, hiccup mode stops and soft start initiates.

Over-Temperature Protection (OTP)

The MP8833 employs thermal shutdown by internally monitoring the junction temperature of the IC. If the junction temperature exceeds the thermal shutdown threshold (typically 160°C), the IC shuts down. After the junction temperature drops to its recovery threshold, the MP8833 auto-restarts.

I²C Slave Address

The I²C slave address of the MP8833 is 0xC0H and 0xC1H internally. If another slave address is required, contact the factory. The I²C address can be adjusted by the factory OTP fuse (See Table 4).

Table 4: Address Register

A7	A6	A5	A4	A3	A2	A1	A0
1	1	0	0	0	0	0	R/W
Address (0x60)							

I²C Control Power Stage

The EN/SYNC and SD pins can start up and shut down the device. The I²C bit I2C_ON can also control the device. Reg00 SYS_SET D0 bit is an I²C-controlled pin. When writing D0 = 0, the power stage is off. When writing D0 = 1, the power stage is on. The power stage is operational only when SD or I2C_ON is high, or when EN/SYNC is high or in the SYNC frequency range (see Table 5).

Table 5: Power Stages

EN/SYNC	SD	I2C_ON	Power Stage
High	High	High	Active
Low	High	High	Standby
High	Low	High	Standby
High	High	Low	Standby
Ext. SYNC	High	High	Active

Switching Frequency

The MP8833's default internal switching frequency is 1MHz. If an external EN/SYNC pin has external synchronization input, the internal frequency is auto-masked. The recommended external synchronization range is 1MHz to 1.5MHz. With external EN/SYNC functionality, the MP8833 can be used in parallel with different slave addresses and the same switching frequency.

Soft-Start Time

The MP8833 can adjust the soft-start current using the I²C. By writing soft-start current bits (Reg00 SYS_SET [D3:D2]), the soft-start time can be programmed to one of four possible values. After changing the values with the I²C, the soft-start current can be set to 1x, 2x, 4x, or 8x the soft current. It can accelerate the set-up time.

Discharge

The MP8833 has a discharge function. The discharge path exists through both VO1 and VOS. The MP8833 discharges VO1 and VOS by its internal resistance to pull down its voltage. The discharge path is always on during the hiccup off time.

TEC Current and Voltage Limit

Adjust the TEC cooling and heating current limit using the I²C (Reg01 ILIM_HEAT [D5:D0], Reg02 ILIM_COOL [D5:D0]). When the current limit enable signal (Reg01 ILIM_HEAT [D7], Reg02 ILIM_COOL [D7]) is high, the current limit is active.

The MP8833 can adjust the TEC cooling and heating voltage limit through the I²C bits (Reg03 VLIM_HEAT [D5:D0], Reg04 VLIM_COOL [D5:D0]). When the voltage limit enable signal (Reg03 VLIM_HEAT [D7], Reg04 VLIM_COOL [D7]) is high, the voltage limit is active.

When the TEC current and voltage exceed the values set by the I²C (see Table 2), the buck output voltage VOS is regulated to the limit value and not controlled by CTL. The TEC current and voltage are limited, and risky operations are avoided.

When considering the TEC voltage and current limit accuracy, it is recommended to leave a 25% margin for limit setting. For example, if the maximum TEC current is 1A, set the current limit over 1.25A.

TEC Current Monitor

Except the ITEC voltage, the MP8833 provides the TEC current info by an internal 8-bit ADC. It can be read by the I²C (Reg07 IMON [D7:D0]). Compared with the ITEC voltage, the 8-bit ADC is easily used; however, its resolution is not higher than the analog ITEC voltage.

The TEC current (I_{TEC}) can be calculated with Equation (6):

$$I_{TEC}(mA) = ABS(19.53mA \times (128 - DEC(IMON[D7:D0]))) \quad (6)$$

The equation's accuracy decreases when I_{TEC}'s sink or source current is below 500mA. I_{TEC} is an absolute positive value, and its direction is designated by Reg09 Status [D7:D6]. These bits show heating or cooling mode.

TEC Voltage Monitor

The MP8833 provides the TEC voltage (V_{TEC}) through an internal, 8-bit ADC. It can be read by the I²C (Reg08 VTEC [D7:D0]). V_{TEC} can be calculated with Equation (7):

$$V_{TEC}(mA) = ABS(50mV \times (128 - DEC(VTEC[D7:D0]))) \quad (7)$$

A small V_{TEC} decreases the equation's accuracy. As with the TEC current monitor, the TEC voltage monitor also provides an absolute positive value. Its direction is also informed in Reg09 Status [D7:D6].

I²C Status

The MP8833 provides a status register to indicate the TEC operation status. The register is Reg09 Status [D7:D0].

Status [D7:D6] is a bit that indicates whether the TEC device is heating or cooling. If the bits are 10, it indicates heating mode. If the bits are 01, it indicates cooling mode. When it is 00, it means the IC works near the cooling and heating mode boundary. The 2 bits are changed in real time to describe the TEC device operation mode.

Status [D5] is the VLIM status. If VLIM is triggered, it is high. The bit latches if VLIM changes from low to high. The latch is removed by the refresh bit defined in Reg00

SYS_SET[D1]. Its default value is 0 and does not refresh the status. When it is set to 1, it refreshes the status bit and auto-recovers to 0 after writing code.

Status [D4] is an ILIM status. If ILIM is triggered, it is high. The bit latches if VLIM changes from low to high. The latch is removed by a refresh bit.

Status [D3] is PWOR. The high logic output means its power stage is operating normally. The bit latches low if protections occur.

This bit changes in real time. The following events make PWOR low:

- EN/SYNC or SD or I^2C_ON is low
- Over-temperature shutdown
- Normal start before the first soft-start stage completes

Status [D1] is an over-temperature (OT) status. When an over-temperature fault occurs, this bit latches to 1 and the MP8833 shuts down.

The latch is removed by a refresh bit. Status [D0] is an over-temperature warning (OTW) status. When the OTW threshold is triggered, it does not shut down the MP8833, but makes the OTW bit high. This is also a latch bit that requires a refresh bit for recovery.

Refresh Bit

The MP8833 provides a status byte to indicate the TEC device operation condition. When a fault condition occurs, it indicates this via the status byte. Some bits latch after an action occurs, and an eraser bit is required to remove the latch. Write the Reg00 Refresh [D1] Eraser bit to logic high to refresh the latched status in the status register once. The bit should be set to high if a refresh is once again required.

I²C INTERFACE

I²C Serial Interface Description

The I²C is a two-wire, bidirectional, serial interface consisting of a data line (SDA) and a clock line (SCL). The lines are externally pulled to a bus voltage when they are idle. A master device connected to the line generates the SCL signal and the device address, and arranges the communication sequence.

The MP8833 interface is an I²C slave that can support fast mode (400kHz). The I²C interface adds flexibility to the power supply solution. The TEC voltage limit, TEC current limit, and other parameters are instantaneously controlled by the I²C interface. When the master sends the address as an 8-bit value, the 7-bit address should be followed by 0 or 1 to indicate a write or read operation, respectively.

Start and Stop Conditions

Start (S) and stop (P) conditions are signaled by the master device to indicate the beginning and the end of the I²C transfer. A start condition is defined as the SDA signal transitioning from high to low while the SCL is high. A stop condition is defined as the SDA signal transitioning from low to high while the SCL is high (see Figure 7).

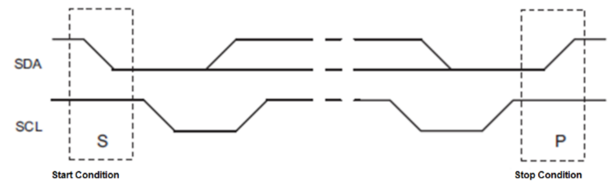


Figure 7: Start and Stop Conditions

After the start condition, the master generates the SCL clocks, then transmits the device address and the read/write direction bit (R/W) on the SDA line.

Transfer Data

Data is transferred in 8-bit bytes by the SDA line. Each byte of data should be followed by an acknowledge (ACK) bit.

I²C Update Sequence

The MP8833 requires a start condition, valid I²C address, register address byte, and data byte for a single data update. After receiving each byte, the MP8833 acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the MP8833. The MP8833 then performs an update on the falling edge of the LSB byte. Figure 8, Figure 9, and Figure 10 show examples of an I²C write and read sequence.

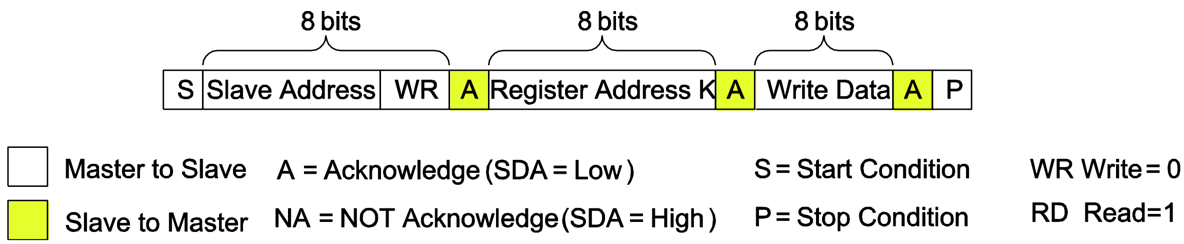


Figure 8: I²C Write Example (Write Single Register)

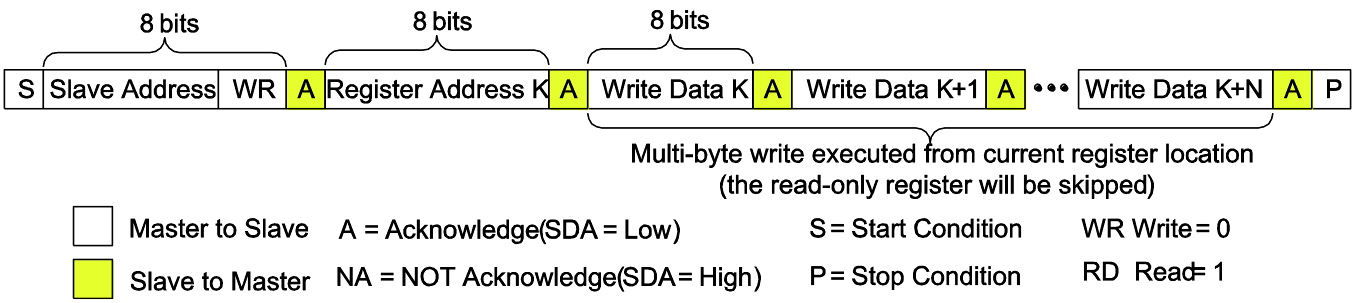


Figure 9: I²C Write Example (Write Multi Register)

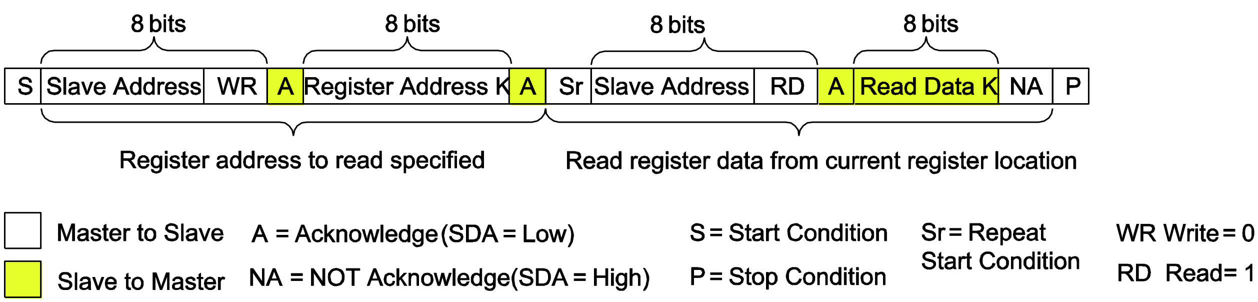


Figure 10: I²C Read Example (Read Single Register)

APPLICATION INFORMATION

COMPONENT SELECTION

Selecting the Inductor

It is recommended to use a 0.68µH to 1.5µH inductor for the 1MHz switching frequency. Select an inductor with a DC resistance below 20mΩ to optimize efficiency.

A high-frequency, switch-mode power supply with a magnetic device has strong electromagnetic inference (EMI). Any unshielded power inductors should be avoided. Metal alloy or multiplayer chip power inductors are ideal shielded inductors since they can decrease the influence effectively.

For most designs, estimate the inductance value with Equation (8):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (8)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor current to be approximately 30% of the maximum load current. Calculate the maximum inductor peak current with Equation (9):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (9)$$

A 1µH inductor is recommended.

Selecting the Input Capacitor

The device has a discontinuous input current, and requires a capacitor to supply the AC current to the device while maintaining the DC input voltage. Use low-ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 10µF capacitor is sufficient.

The input capacitor requires an adequate ripple current rating because it absorbs the input switching current. Estimate the RMS current in the input capacitor with Equation (10):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (10)$$

The worst-case scenario occurs at $V_{IN} = 2V_{OUT}$, calculated by Equation (11):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (11)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality 0.1µF ceramic capacitor as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated with Equation (12):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (12)$$

Selecting the Output Capacitor

The output capacitor stabilizes the DC output voltage. Ceramic capacitors are recommended. Low-ESR capacitors are preferred to limit the output voltage ripple. Estimate the output voltage ripple of the PWM regulator with Equation (13):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C2}\right) \quad (13)$$

Where L_1 is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes most of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (14):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^{2} \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (14)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be estimated with Equation (15):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (15)$$

The characteristics of the output capacitor also affect the stability of the regulation system. It is recommended to use a 1µF LDO output capacitor.

Selecting the ITEC Filter

The ITEC filter can be ignored if the ITEC pin and IMON function in the I^2C are not used.

For general applications, a 0.1µF decoupling capacitor is sufficient.

In some applications, an appropriate filter improves the MP8833's ITEC monitor accuracy. In general applications, it is recommended to use a low-pass RC filter (see Figure 11).

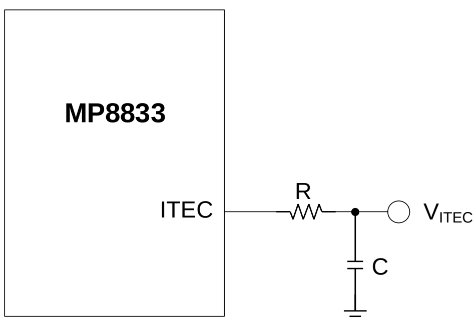


Figure 11: ITEC Filter

The cutoff frequency of the RC filter can be calculated with Equation (16):

$$f_C = \frac{1}{2\pi RC} \quad (16)$$

For most applications, a 100Hz cut-off frequency is sufficient, so a 15kΩ resistor and 0.1µF capacitor are recommended.

Selecting the Soft-Start (SS) Capacitor

The MP8833 has two stages during the soft start (SS) process. These stages prevent VTEC overshoot and nonlinearity. The MP8833 has two ways to adjust the SS time: I^2C Reg00 SYS SET D[3:2] and the SS capacitor. If the SS current is set to 1x through the I^2C, the SS current is typically 3µA. The first stage time can be calculated with Equation (17):

$$t_{SS\_1} = \frac{V_{MID} \times C_{SS}}{I_{SS}} \quad (17)$$

Where V_{MID} is 1.5V, and I_{SS} is typically 3µA with a 1x SS current.

For the second stage, the SS time can be calculated with Equation (18):

$$t_{SS\_2} = \frac{(1.25V - V_{CTL}) \times C_{SS}}{I_{SS}} \quad (18)$$

Where V_{CTL} is the CTL voltage, and I_{SS} is typically 3µA with a 1x soft-start current. For general applications, a 0.1µF soft-start capacitor is recommended.

Selecting the REF Pin Capacitor

The decoupling capacitor on the REF pin stabilizes the device. Adding a 0.1µF capacitor is recommended.

Design Example

Table 6 shows the recommended component values for general applications.

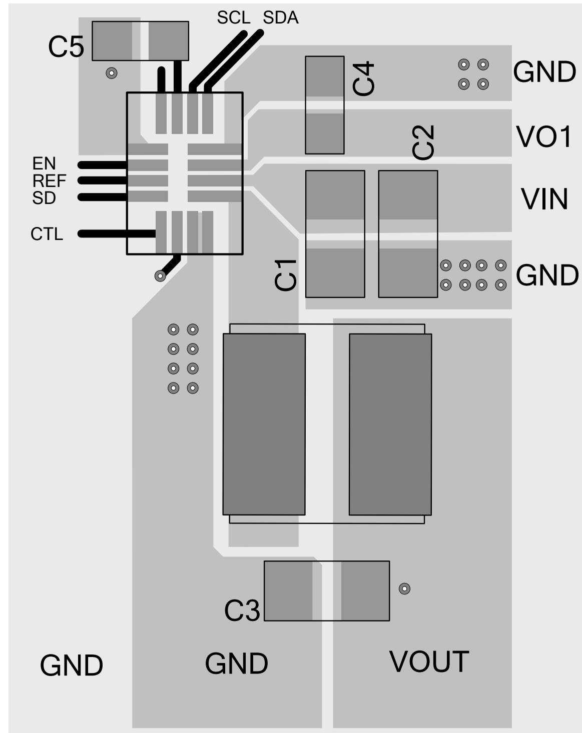
Table 6: Recommended Component Values

Component	Recommended Value
C1	10µF
C2	0.1µF
C3	0.1µF
C4	1µF
C5	10µF
C6	0.1µF
R4	15kΩ
L1	1µH

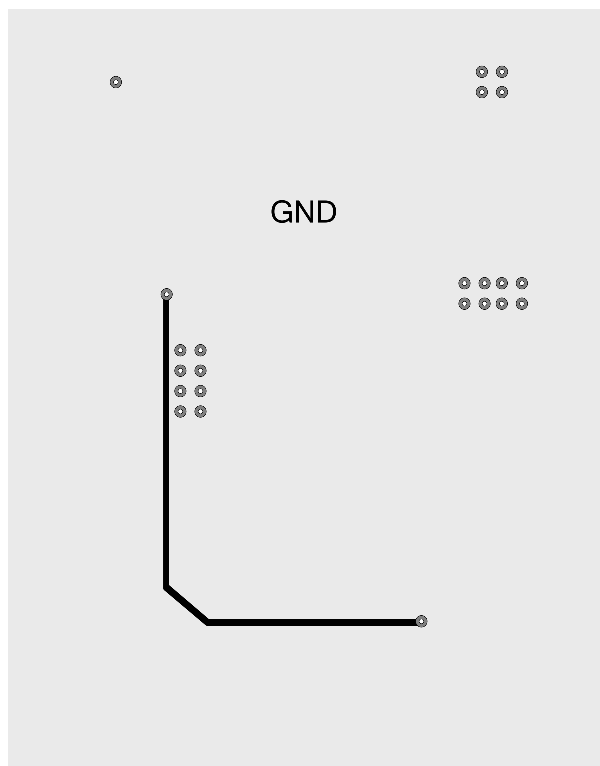
PCB Layout Guidelines

Proper PCB is important for proper functioning. For a high-frequency switching converter, poor layout design can result in poor line or load regulation and stability issues. For the best results, refer to Figure 12 and follow the guidelines below:

1. Place the high-current paths (PGND, VIN, and SW) very close to the device with short, direct, and wide traces.
2. Place the input capacitor as close as possible to the IN and PGND pins.
3. Ensure all the PGND pins are connected together by the PCB.
4. Keep the switching (SW) node short, and route it away from the feedback network.
5. Keep the V_{OUT} sense line as short as possible, and route it away from all power inductors.



Top PCB Layer



Bottom PCB Layer

Figure 12: Recommended PCB Layout

OTP eFuse Configuration Table

ADD	NAME	D7	D6	D5	D4	D3	D2	D1	D0
00	CTL1	Reserved	Reserved		DIS TIME	SS CURRENT		Reserved	I²C on
01	CTL2	ENILIM_HEAT	Reserved	HEAT_ILIM SET					
02	CTL3	ENILIM_COOL	Reserved	COOL_ILIM SET					
03	CTL4	ENVLIM_HEAT	VIN OVP	HEAT_VLIM SET					
04	CTL5	ENVLIM_COOL	Reserved	COOL_VLIM SET					
05	CTL6	LDO_ILIM_HS		LDO_ILIM_LS		BUCK_ILIM_HS		BUCK_ILIM_LS	
06	Add	Slave address							Reserved

OTP REGISTER DESCRIPTION

OTP00 Register

Bits	Bit Name	Description
D[7]	Reserved	Reserved.
D[6:5]	Reserved	Reserved.
D[4]	DIS TIME	Discharge time set bit. The default setting is 1. 0: 70ms 1: 35ms
D[3:2]	SS CURRENT	Second start-up time (the TEC voltage is 3.3V). The default setting is 00. 00: 1x 01: 2x 10: 4x 11: 8x
D[1]	Reserved	Reserved.
D[0]	I²C_ON	System-on control. The default setting is 1. 0: Power stage off 1: Power stage on

OTP01 Register

Bits	Bit Name	Description
D[7]	ENILIM_HEAT	Enable signal of the TEC current limit setting in heating mode. The default setting is 1.
D[6]	Reserved	Reserved.
D[5:0]	HEAT_ILIM SET	See Table 7 on page 27. The default setting is 100110.

OTP02 Register

Bits	Bit Name	Description
D[7]	ENILIM_COOL	Enable signal of the TEC current limit setting in cooling mode. The default setting is 1.
D[6]	Reserved	Reserved.
D[5:0]	COOL_ILIM SET	See Table 7 on page 27. The default setting is 100110.

OTP03 Register

Bits	Bit Name	Description
D[7]	ENVLIM_HEAT	Enable signal of the TEC voltage limit setting in heating mode. The default setting is 1.
D[6]	VIN OVP	Vin OVP protection enable. The default setting is 1. 0: Disable 1: Enable
D[5:0]	HEAT_VLIM SET	See Table 8 on page 27. The default setting is 011100.

OTP04 Register

Bits	Bit Name	Description
D[7]	ENVLIM_COOL	Enable signal of the TEC voltage limit setting in cooling mode. The default setting is 1.
D[6]	Reserved	Reserved.
D[5:0]	COOL_VLIMSET	See Table 8 on page 27. The default setting is 011100.

OTP05 Register

Bits	Bit Name	Description
D[7:6]	LDO_ILIM_HEAT	Secondary current limit of the LDO high-side MOSFET. The default setting is 10. 00: 1.2A 01: 1.5A 10: 1.8A 11: 2.1A
D[5:4]	LDO_ILIM_COOL	Secondary current limit of the LDO low-side MOSFET. The default setting is 10. 00: 1.2A 01: 1.5A 10: 1.8A 11: 2.1A
D[3:2]	BUCK_ILIM_ HEAT	Current limit of the buck high-side MOSFET. The default setting is 01. 00: 2.5A 01: 3A 10: 3.5A 11: 4A
D[1:0]	BUCK_ILIM_ COOL	Current limit of the buck low-side MOSFET. The default setting is 01. 00: 2.5A 01: 3A 10: 3.5A 11: 4A

OTP06 Register

Bits	Bit Name	Description
D[7:1]	Slave address	I^2C slave address. The default setting is 1100000.
D[0]	Reserved	Reserved.

Table 7: ILIM Table

D[5:0]	ILIM (mA)	D[5:0]	ILIM (mA)	D[5:0]	ILIM (mA)	D[5:0]	ILIM (mA)
00 0000	39	01 0000	663	10 0000	1287	11 0000	1911
00 0001	78	01 0001	702	10 0001	1326	11 0001	1950
00 0010	117	01 0010	741	10 0010	1365	11 0010	1989
00 0011	156	01 0011	780	10 0011	1404	11 0011	2028
00 0100	195	01 0100	819	10 0100	1443	11 0100	Reserved
00 0101	234	01 0101	858	10 0101	1482	11 0101	Reserved
00 0110	273	01 0110	897	10 0110	1521	11 0110	Reserved
00 0111	312	01 0111	936	10 0111	1560	11 0111	Reserved
00 1000	351	01 1000	975	10 1000	1599	11 1000	Reserved
00 1001	390	01 1001	1014	10 1001	1638	11 1001	Reserved
00 1010	429	01 1010	1053	10 1010	1677	11 1010	Reserved
00 1011	468	01 1011	1092	10 1011	1716	11 1011	Reserved
00 1100	507	01 1100	1131	10 1100	1755	11 1100	Reserved
00 1101	546	01 1101	1170	10 1101	1794	11 1101	Reserved
00 1110	585	01 1110	1209	10 1110	1833	11 1110	Reserved
00 1111	624	01 1111	1248	10 1111	1872	11 1111	Reserved

Table 8: VLIM Table

D[5:0]	VLIM (mV)	D[5:0]	VLIM (mV)	D[5:0]	VLIM (mV)	D[5:0]	VLIM (mV)
00 0000	97.6	01 0000	1659.2	10 0000	3220.8	11 0000	4782.4
00 0001	195.2	01 0001	1756.8	10 0001	3318.4	11 0001	4880
00 0010	292.8	01 0010	1854.4	10 0010	3416	11 0010	4977.6
00 0011	390.4	01 0011	1952	10 0011	3513.6	11 0011	5075.2
00 0100	488	01 0100	2049.6	10 0100	3611.2	11 0100	5172.8
00 0101	585.6	01 0101	2147.2	10 0101	3708.8	11 0101	5270.4
00 0110	683.2	01 0110	2244.8	10 0110	3806.4	11 0110	5368
00 0111	780.8	01 0111	2342.4	10 0111	3904	11 0111	5465.6
00 1000	878.4	01 1000	2440	10 1000	4001.6	11 1000	5563.2
00 1001	976	01 1001	2537.6	10 1001	4099.2	11 1001	Reserved
00 1010	1073.6	01 1010	2635.2	10 1010	4196.8	11 1010	Reserved
00 1011	1171.2	01 1011	2732.8	10 1011	4294.4	11 1011	Reserved
00 1100	1268.8	01 1100	2830.4	10 1100	4392	11 1100	Reserved
00 1101	1366.4	01 1101	2928	10 1101	4489.6	11 1101	Reserved
00 1110	1464	01 1110	3025.6	10 1110	4587.2	11 1110	Reserved
00 1111	1561.6	01 1111	3123.2	10 1111	4684.8	11 1111	Reserved

I²C REGISTER MAP

Addr	Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
00	SYS_SET	R/W	Reserved	Reserved		Dis time	SS current		Refresh	I²C on
01	ILIM_HEAT	R/W	ENILIM_ HEAT	Reserved	ILIM_HEAT SET					
02	ILIM_COOL	R/W	ENILIM_ COOL	Reserved	ILIM_COOL SET					
03	VLIM_HEAT	R/W	ENVLIM_ HEAT	VIN OVP	VLIM_HEAT SET					
04	VLIM_COOL	R/W	ENVLIM_ COOL	Reserved	VLIM_COOL SET					
05	LIMIT	R/W	LDO_ILIM_HS		LDO_ILIM_LS		BUCK_ILIM_HS		BUCK_ILIM_LS	
06	ADDR	R	Slave address							Reserved
07	IMON	R	TEC current monitor							
08	VTEC	R	TEC voltage monitor							
09	STATUS	R	Mode		VLIM	ILIM	PWOR	Reserve d	OT	OTW
0A	ID	R	Vendor ID				Version ID			

Default Register Values

Addr	Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
00	SYS_SET	R/W	0	0	0	1	0	0	0	1
01	ILIM_HEAT	R/W	1	0	1	0	0	1	1	0
02	ILIM_COOL	R/W	1	0	1	0	0	1	1	0
03	VLIM_HEAT	R/W	1	1	0	1	1	1	0	0
04	VLIM_COOL	R/W	1	0	0	1	1	1	0	0
05	LIMIT	R/W	1	0	1	0	0	1	0	1
06	ADDR	R	1	1	0	0	0	0	0	0
07	IMON	R	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
08	VTEC	R	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
09	STATUS	R	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
M0A	ID	R	0	0	1	0	0	0	0	1

I2C REGISTER DESCRIPTION

Reg00 SYS_SET

Bits	Bit Name	Description
D7	Reserved	Reserved.
D[6:5]	Reserved	Reserved.
D4	DIS TIME	Sets the discharge time before start-up. The default setting is 1. 0: 70ms 1: 35ms
D[3:2]	SS CURRENT	Sets the soft-start current time. The default setting is 00. 00: 1x 01: 2x 10: 4x 11: 8x
D1	REFRESH	Status byte refresh bit. The default setting is 0. 0: Disable 1: Enable Setting this bit to 1 will only refresh the status register once.
D0	I^2C ON	Power stage enable signal. High logic turns on power stage.

Reg01 ILIM_HEAT

Bits	Bit Name	Description
D[7]	ENILIM_HEAT	Enable signal of the TEC current-limit setting in heating mode. The default setting is 1. 0: Disable the protection 1: Enable the protection
D[6]	Reserved	Reserved.
D[5:0]	ILIM_HEAT SET	See Table 7 on page 27. The default setting is 100110.

Reg02 ILIM_COOL

Bits	Bit Name	Description
D[7]	ENILIM_COOL	Enable signal of the TEC current-limit setting in cooling mode. The default setting is 1. 0: Disable the protection 1: Enable the protection
D[6]	Reserved	Reserved.
D[5:0]	ILIM_COOL SET	See Table 7 on page 27. The default setting is 100110.

Reg03 VLIM_HEAT

Bits	Bit Name	Description
D[7]	ENVLIM_HEAT	Enable signal of the TEC voltage-limit setting in heating mode. The default setting is 1. 0: Disable the protection 1: Enable the protection
D[6]	VIN OVP	0: Disable V_{IN} OVP function 1: Enable V_{IN} OVP function. This is the default setting.
D[5:0]	VLIM_HEAT SET	See Table 8 on page 27. The default setting is 011100.

Reg04 VLIM_COOL

Bits	Bit Name	Description
D[7]	ENVLIM_COOL	Enable signal of the TEC voltage-limit setting in cooling mode. The default setting is 1. 1: Enable this protection 0: Disable this protection
D[6]	Reserved	Reserved.
D[5:0]	VLIM_COOL SET	See Table 7 on page 27. The default setting is 011100.

Reg05 LIMIT

Bits	Bit Name	Description
D[7:6]	LDO_ILIM_HS	Sets the secondary current limit of the LDO high-side MOSFET. Triggering this over-current protection (OCP) forces the MP8833 into hiccup mode. The default setting is 10. 00: 1.2A 01: 1.5A 10: 1.8A 11: 2.1A
D[5:4]	LDO_ILIM_LS	Sets the secondary current limit of the LDO low-side MOSFET. Triggering this over-current protection (OCP) forces the MP8833 into hiccup mode. The default setting is 10. 00: 1.2A 01: 1.5A 10: 1.8A 11: 2.1A
D[3:2]	BUCK_ILIM_HS	Sets the current limit of the buck high-side MOSFET. Triggering this over-current protection (OCP) forces the MP8833 into hiccup mode. The default setting is 01. 00: 2.5A 01: 3A 10: 3.5A 11: 4A
D[1:0]	BUCK_ILIM_LS	Sets the current limit of the buck low-side MOSFET. Triggering this over-current protection (OCP) forces the MP8833 into hiccup mode. The default setting is 01. 00: 2.5A 01: 3A 10: 3.5A 11: 4A

Reg06 Address

Bits	Bit Name	Description
D[7:1]	ADDRESS	These bits feed back the slave address.
D[0]	Reserved	Reserved.

Reg07 IMON

Bits	Bit Name	Description
D[7:0]	TEC CURRENT MONITOR	The byte shows the LDO current. The LDO current is monitored and read by an 8-bit ADC. When the current is 0A, this byte is equal to 128(1000 0000). In cooling mode, the byte increases with the current. In heating mode, the byte decreases while the current increases.

Reg08 VTEC

Bits	Bit Name	Description
D[7:0]	TEC VOLTAGE MONITOR	The byte shows the TEC voltage. The TEC voltage is monitored and read by an 8-bit ADC. When the TEC voltage is 0V, this byte is equal to 128(1000 0000). In cooling mode, the byte increases with the voltage. In heating mode, the byte decreases while the voltage increases.

Reg09 Status

Bits	Bit Name	Description
D[7:6]	MODE	The bits shows if the device is in heating or cooling mode. If the bits are 10, it indicates heating mode. If the bits are 01, it indicates cooling mode. When it is 00, it means the IC is near the cooling and heating mode boundary.
D[5]	VLIM	The bit shows the TEC voltage status. If the TEC voltage reaches any TEC first voltage limit set by the I^2C, it will be high.
D[4]	ILIM	The bit shows the TEC current status. If the TEC current reaches any TEC first current limit set by the I^2C, it will be high.
D[3]	PWOR	The bit shows the power stage status. Logic high means the power stage has an output.
D[2]	Reserved	Reserved.
D[1]	OT	The bit shows the over-temperature status. If the die temperature rises above 150°C and over-temperature occurs, the OT bit goes high and latches.
D[0]	OTW	The bit shows the over-temperature warning. If the die temperature rises above 120°C, it goes high.

Reg0A ID

Bits	Bit Name	Description
D[7:4]	VENDOR ID	Vendor ID. The default setting is 0010.
D[3:0]	VERSION ID	Version ID. The default setting is 0001.

TYPICAL APPLICATION CIRCUITS

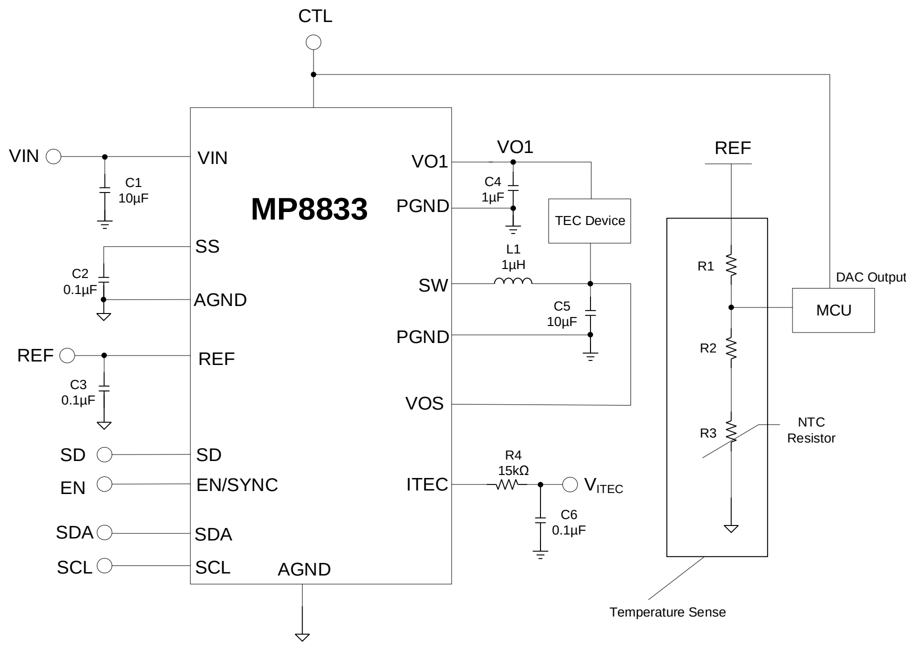
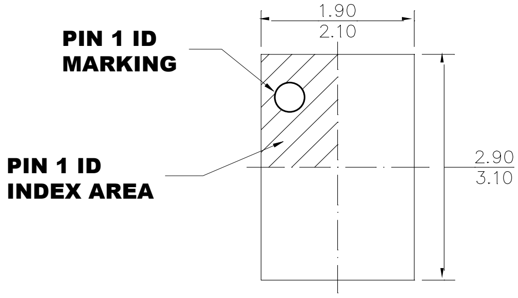


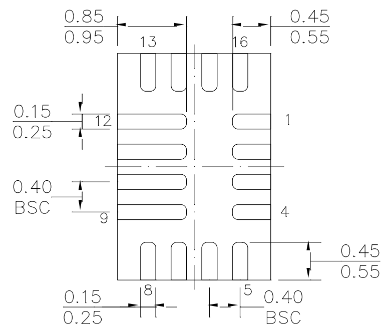
Figure 13: Typical Application Circuit

PACKAGE INFORMATION

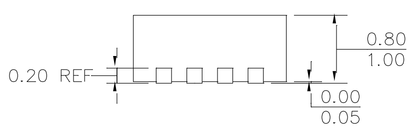
QFN-16 (2mmx3mm)



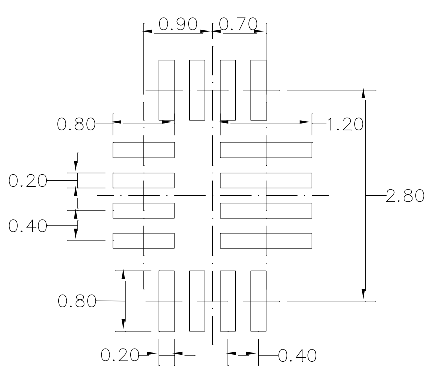
TOP VIEW



BOTTOM VIEW



SIDE VIEW

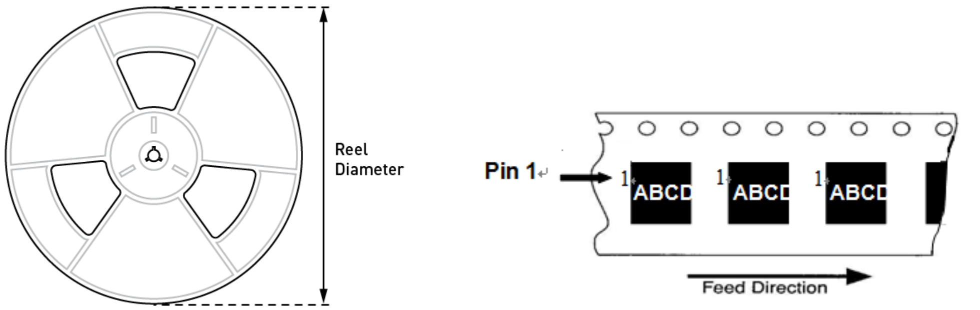


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/Reel	Quantity/Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP8833GD-xxxx-Z	QFN-16 (2mmx3mm)	5000	N/A	13in	12mm	8mm