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32-bit Arm® Cortex®-M7 Microcontroller Traveo™ II Family

General Description

CYT4BF is a family of Traveo™ II microcontrollers targeted at automotive systems such as high-end body-control units. CYT4BF has two Arm® Cortex®-M7 CPUs for primary processing, and an Arm Cortex-M0+ CPU for peripheral and security processing. These devices contain embedded peripherals supporting Controller Area Network with Flexible Data rate (CAN FD), Local Interconnect Network (LIN), Gigabit Ethernet, and FlexRay. Traveo II devices are manufactured on an advanced 40-nm process. CYT4BF incorporates Cypress' low-power flash memory, multiple high-performance analog and digital peripherals, and enables the creation of a secure computing platform.

Features

■ CPU Subsystem

- Two 350-MHz 32-bit Arm® Cortex-M7 CPUs, each with
 - Single-cycle multiply
 - Single/double-precision floating point unit (FPU)
 - 16-KB data cache, 16-KB instruction cache
 - Memory Protection Unit (MPU)
 - 16-KB instruction and 16-KB data Tightly-Coupled Memories (TCM)
- 100-MHz 32-bit Arm Cortex M0+ CPU with
 - Single-cycle multiply
 - Memory Protection Unit
- Inter-processor communication in hardware
- Three DMA controllers
 - Peripheral DMA controller #0 (P-DMA0) with 143 channels
 - Peripheral DMA controller #1 (P-DMA1) with 65 channels
 - Memory DMA controller (M-DMA0) with 8 channels

■ Integrated Memories

- 8384 KB of code-flash with an additional 256 KB of work-flash
 - Read-While-Write (RWW) allows updating the code-flash/work-flash while executing from it
 - Single- and dual-bank modes (specifically for Firmware update Over The Air [FOTA])
 - Flash programming through SWD/JTAG interface
- 1024-KB of SRAM with selectable retention granularity

■ Cryptography Engine

- Supports Enhanced Secure Hardware Extension (eSHE) and Hardware Security Module (HSM)
- Secure boot and authentication
 - Using digital signature verification
 - Using fast secure boot
- AES: 128-bit blocks, 128-/192-/256-bit keys
- 3DES: 64-bit blocks, 64-bit key
- Vector unit supporting asymmetric key cryptography such as Rivest-Shamir-Adleman (RSA) and Elliptic Curve (ECC)
- SHA-1/2/3: SHA-512, SHA-256, SHA-160 with variable length input data
- CRC: supports CCITT CRC16 and IEEE-802.3 CRC32
- True random number generator (TRNG) and pseudo random number generator (PRNG)
- Galois/Counter Mode (GCM)

■ Functional Safety for ASIL-B

- Memory Protection Unit (MPU)
- Shared Memory Protection Unit (SMPU)
- Peripheral Protection Unit (PPU)
- Watchdog Timer (WDT)
- Multi-Counter Watchdog Timer (MCWDT)
- Low-Voltage Detector (LVD)
- Brown-Out Detection (BOD)
- Overvoltage Detection (OVD)
- Clock Supervisor (CSV)
- Hardware error correction (SECDED ECC) on all safety-critical memories (SRAM, flash, TCM)

■ Low-Power 2.7-V to 5.5-V Operation

- Low-power Active, Sleep, Low-power Sleep, DeepSleep, and Hibernate modes for fine-grained power management
- Configurable options for robust BOD
 - Two threshold levels (2.7 V and 3.0 V) for BOD on V_{DD} and V_{DDA}
 - One threshold level (1.1 V) for BOD on V_{CCD}

■ Wakeup

- Up to four pins to wake from Hibernate mode
- Up to 240 GPIO pins to wake from Sleep modes
- Event Generator, SCB, Watchdog Timer, RTC alarms to wake from DeepSleep modes

■ Clocks

- Internal Main Oscillator (IMO)
- Internal Low-Speed Oscillator (ILO)
- External Crystal Oscillator (ECO)
- Watch Crystal Oscillator (WCO)
- Phase-Locked Loop (PLL)
- Frequency-Locked Loop (FLL)

■ Communication Interfaces

- Up to 10 CAN FD channels
 - Increased data rate (up to 8 Mbps) compared to classic CAN, limited by physical layer topology and transceivers
 - Compliant to ISO 11898-1:2015
 - Supports all the requirements of Bosch CAN FD Specification V1.0 for non-ISO CAN FD
 - ISO 16845:2015 certificate available
- Up to 11 runtime-reconfigurable SCB (serial communication block) channels, each configurable as I²C, SPI, or UART

- Up to 20 independent LIN channels
 - LIN protocol compliant with ISO 17987
 - Up to two 10/100/1000 Mbps Ethernet MAC interfaces conforming to IEEE-802.3az
 - Supports the following PHY interfaces:
 - Media-independent interface (MII)
 - Reduced media-independent interface (RMII)
 - Gigabit media-independent interface (GMII)
 - Reduced gigabit media-independent interface (RGMII)
 - Compliant with IEEE-802.1BA Audio Video Bridging (AVB)
 - Compliant with IEEE-1588 Precision Time Protocol (PTP)
 - FlexRay interface (V2.1) configurable for single or dual data-channels for fault tolerance, supporting data rates up to 10 Mbps
- **External Memory Interface**
- One SPI (Single, Dual, Quad, or Octal) or HyperBus interface
 - On-the-fly encryption and decryption
 - Execute-In-Place (XIP) from external memory
- **SDHC Interface**
- One Secure Digital High Capacity (SDHC) interface supporting embedded MultiMediaCard (eMMC), Secure Digital (SD), or SDIO (Secure Digital Input Output)
 - Compliant to eMMC 5.1, SD 6.0, and SDIO 4.10 specifications
 - Data rates up to SD High Speed 50 MHz, or eMMC 52 MHz DDR
- **Audio Interface**
- Three Inter-IC Sound (I²S) Interfaces (based on the NXP I²S bus specification) for connecting digital audio devices
 - I²S, left justified, or Time Division Multiplexed (TDM) audio formats
 - Independent transmit or receive operation, each in master or slave mode
- **Timers**
- Up to 102 16-bit and 16 32-bit Timer/Counter Pulse-Width Modulator (TCPWM) blocks
 - Up to 15 16-bit counters for motor control
 - Up to 87 16-bit counters and 16 32-bit counters for regular operations
 - Supports timer, capture, quadrature decoding, pulse-width modulation (PWM), PWM with dead time (PWM_DT), pseudo-random PWM (PWM_PR), and shift-register (SR) modes
 - Up to 16 Event Generation (EVTGEN) timers supporting cyclic wakeup from DeepSleep
 - Events trigger a specific device operation (such as execution of an interrupt handler, a SAR ADC conversion, and so on)
- **Real Time Clock (RTC)**
- Year/Month/Date, Day-of-week, Hour:Minute:Second fields
 - 12- and 24-hour formats
 - Automatic leap-year correction
- **I/O**
- Up to 240 Programmable I/Os
 - Three I/O types
 - GPIO Standard (GPIO_STD)
 - GPIO Enhanced (GPIO_ENH)
 - High-Speed I/O Standard (HSIO_STD)
- **Regulators**
- Generates a 1.1-V nominal core supply from a 2.7-V to 5.5-V input supply
 - Three regulators:
 - DeepSleep
 - Core internal
 - Core external
- **Programmable Analog**
- Three SAR A/D converters with up to 99 external channels (96 I/Os + 3 I/Os for motor control)
 - Each ADC supports 32 logical channels, with 32 + 1 physical connections. Any external channel can be connected to any logical channel in the respective SAR.
 - Each ADC supports 12-bit resolution and sampling rates of up to 1 Msps
 - Each ADC also supports six internal analog inputs like
 - Bandgap reference to establish absolute voltage levels
 - Calibrated diode for junction temperature calculations
 - Two AMUXBUS inputs and two direct connections to monitor supply levels
 - Each ADC supports addressing of external multiplexers
 - Each ADC has a sequencer supporting autonomous scanning of configured channels
 - Synchronized sampling of all ADCs for motor-sense applications
- **Smart I/O**
- Up to five Smart I/O blocks, which can perform Boolean operations on signals going to and from I/Os
 - Up to 36 I/Os (GPIO_STD) supported
- **Debug Interface**
- JTAG controller and interface compliant to IEEE-1149.1-2001
 - Arm SWD (Serial Wire Debug) port
 - Supports Arm Embedded Trace Macrocell (ETM) Trace
 - Data trace using SWD
 - Instruction and data trace using JTAG
- **Compatible with Industry-Standard Tools**
- GHS MULTI or IAR EWARM for code development and debugging
- **Packages**
- 176-TEQFP, 24 × 24 × 1.7 mm (max), 0.5-mm lead pitch
 - 272-BGA, 16 × 16 × 1.7 mm (max), 0.8-mm ball pitch
 - 320-BGA, 17 × 17 × 1.7 mm (max), 0.8-mm ball pitch

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1. Features List

Table 1-1. CYT4BF Feature List for All Packages

| Features | Packages | | |
|---|---|--|--|
| | 176-TEQFP | 272-BGA | 320-BGA |
| CPU | | | |
| Core | Two 32-bit Arm Cortex-M7 CPUs and a 32-bit Arm Cortex M0+ CPU | | |
| Functional Safety | ASIL-B | | |
| Operating Voltage | 2.7 V to 5.5 V | | |
| Operating Voltage for HSIO_STD | Not supported | 2.7 V to 3.6 V | |
| Core Voltage | 1.05 V to 1.15 V | | |
| Operating frequency | Arm Cortex-M7 350 MHz (max for each) and Arm Cortex-M0+ 100 MHz (max) | | |
| MPU, PPU | Supported | | |
| FPU | Supports both single (32-bit) and double (64-bit) precision | | |
| DSP-MUL/DIV/MAC | Supported by Arm Cortex-M7 CPUs | | |
| TCM | 16-KB instruction and 16-KB data for each Cortex-M7 CPU | | |
| Memory | | | |
| Code-flash | 8384 KB (8128 KB + 256 KB) | | |
| Work-flash | 256 KB (192 KB + 64 KB) | | |
| SRAM (configurable for retention) | 1024 KB | | |
| ROM | 64 KB | | |
| Communication Interfaces | | | |
| CAN0 (CAN-FD: Up to 8 Mbps) | 5 ch | | |
| CAN1 (CAN-FD: Up to 8 Mbps) | 5 ch | | |
| CAN RAM | 40 KB per instance (5 ch), 80 KB in total | | |
| Serial Communication Block (SCB/UART) | 10 ch | 11 ch | |
| Serial Communication Block (SCB/I ² C) | 10 ch | 11 ch | |
| Serial Communication Block (SCB/SPI) | 10 ch | 11 ch | |
| LIN0 | 17 ch | 20 ch | |
| Ethernet MAC | 1 ch × 10/100 | 2 ch (option) × 10/100/1000 | |
| | ETH0: MII/RMII on GPIO_STD | ETH0: MII/RMII on GPIO_STD, ETH1: RGMII on HSIO_STD | ETH0: MII/RMII on GPIO_STD, ETH1: MII/RMII/GMII/RGMII on HSIO_STD |
| | | | ETH0: RGMII on HSIO_STD, ETH1: RGMII on HSIO_STD |
| FlexRay | 1 interface of FlexRay supporting ch A and ch B (option) | | |
| Memory Interfaces | | | |
| eMMC/SD | 1 ch (GPIO_STD at 26 MHz) | 1 ch (HSIO_STD at 50 MHz, GPIO_STD at 26 MHz) | |
| Single SPI / Dual SPI / Quad SPI / Octal SPI / HyperBus | 1 ch (GPIO_STD at 32 MHz) | 1 ch (HSIO_STD at 100 MHz, GPIO_STD at 32 MHz) | |
| Timers | | | |
| RTC | 1 ch | | |

Table 1-1. CYT4BF Feature List for All Packages (continued)

| Features | Packages | | |
|---|--|---|---------|
| | 176-TEQFP | 272-BGA | 320-BGA |
| TCPWM (16-bit) (Motor Control) | 15 ch (TCPWM0/3, TCPWM1/12) | | |
| TCPWM (16-bit) | 87 ch (TCPWM0/3, TCPWM1/84) | | |
| TCPWM (32-bit) | 16 ch (TCPWM0/3, TCPWM1/13) | | |
| External Interrupts | 148 | 220 | 240 |
| Analog | | | |
| 12-bit, 1 Msps SAR ADC | 3 Units (SAR0/32, SAR1/32, SAR2/32 logical channels) | | |
| | 81 external channels (SAR0/24 ch, SAR1/32 ch, SAR2/25 ch) | 96 external channels (each SAR supports 32 ch) | |
| | 18 ch (6 per ADC) Internal sampling | | |
| Motor Control Input | 3 ch (synchronous sampling of one channel on each of the 3 ADCs) | | |
| Security | | | |
| Flash Security (program/work read protection) | Supported | | |
| Flash Chip erase enable | Configurable | | |
| eSHE / HSM | By separate firmware ^[1] | | |
| Audio | | | |
| I ² S / TDM | Tx 3 ch, Rx 3 ch | | |
| System | | | |
| DMA Controller | P-DMA0 with 143 channels (16 general purpose), P-DMA1 with 65 channels (8 general purpose), and M-DMA0 with 8 channels | | |
| Internal Main Oscillator | 8 MHz | | |
| Internal Low speed Oscillator | 32.768 kHz (nominal) | | |
| PLL | Input: 3.988 to 33.34 MHz, PLL output: up to 350 MHz | | |
| FLL | Input: 0.25 to 80 MHz, FLL output: up to 100 MHz | | |
| Watchdog Timer and Multi-counter Watchdog Timer | Supported | | |
| Clock Supervisor | Supported | | |
| Cyclic wakeup from DeepSleep | Supported | | |
| GPIO_STD | 144 | 187 | 191 |
| GPIO_ENH | 4 | | |
| HSIO_STD | Not supported | 29 | 45 |
| Smart I/O (Blocks) | 5 blocks, mapped through 36 I/Os | | |
| Low-Voltage Detect | Two, 26 selectable levels | | |
| Maximum Ambient Temperature | 105 °C for S-grade, 125 °C for E-grade | | |
| Debug Interface | SWD/JTAG | | |
| Debug Trace | Arm Cortex-M7 ETB size of 8 KB, Arm Cortex M0+ MTB size of 4 KB | | |

Note

- Enhanced Secure Hardware Extension (eSHE) and Hardware Security Module (HSM) support are enabled by third-party firmware.

1.1 Communication Peripheral Instance List

The following table lists the instances supported under each package for communication peripherals, based on the minimum pins needed for the functionality.

Table 1-2. Communication Peripheral Instance List

| Module | 176-TEQFP | 272-BGA | 320-BGA | Minimum Pin Functions |
|----------|-----------|-----------|-----------|--------------------------|
| CAN0 | 0/1/2/3/4 | 0/1/2/3/4 | 0/1/2/3/4 | TX, RX |
| CAN1 | 0/1/2/3/4 | 0/1/2/3/4 | 0/1/2/3/4 | TX, RX |
| LIN0 | 0 to 16 | 0 to 19 | 0 to 19 | TX, RX |
| SCB/UART | 0 to 9 | 0 to 10 | 0 to 10 | TX, RX |
| SCB/I2C | 0 to 9 | 0 to 10 | 0 to 10 | SCL, SDA |
| SCB/SPI | 0 to 9 | 0 to 10 | 0 to 10 | MISO, MOSI, SCK, SELECT0 |

2. Blocks and Functionality

Figure 2-1. Architecture Block Diagram

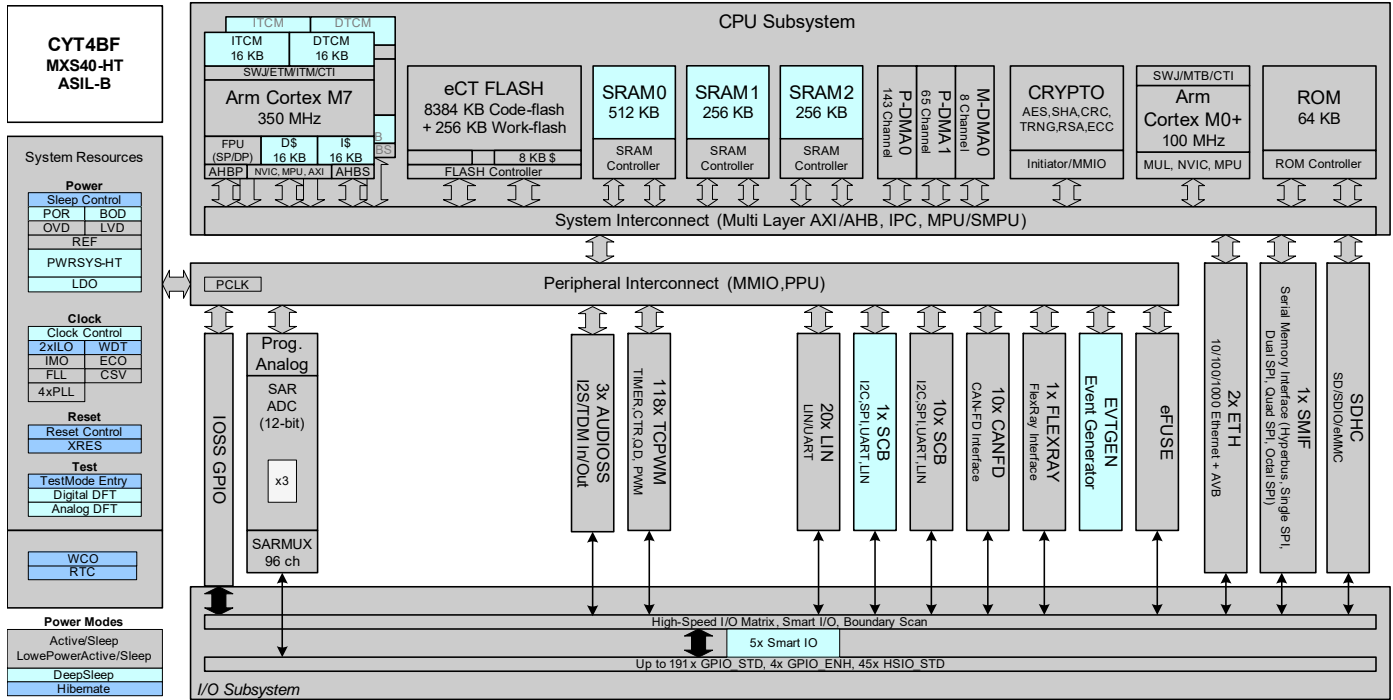


Figure 2-1. shows the CYT4BF architecture block diagram, giving a simplified view of the interconnection between subsystems and blocks. CYT4BF has four major subsystems: CPU, system resources, peripherals, and I/O^[2, 3, 4]. The color-coding shows the lowest power mode where the particular block is still functional.

CYT4BF provides extensive support for programming, testing, debugging, and tracing of both hardware and firmware.

Debug-on-chip functionality enables in-system debugging using the production device. It does not require special interfaces, debugging pods, simulators, or emulators.

The JTAG interface is fully compatible with industry-standard third-party probes such as I-jet, J-Link, and GHS.

The debug circuits are enabled by default.

CYT4BF provides a high level of security with robust flash protection and the ability to disable features such as debug.

Additionally, each device interface can be permanently disabled for applications concerned with phishing attacks from a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. All programming, debug, and test interfaces are disabled when maximum device security is enabled.

Notes

2. GPIO_STD supports 2.7 V to 5.5 V V_{DDIO} range.
3. GPIO_ENH supports 2.7 V to 5.5 V V_{DDIO} range with higher currents at lower voltages.
4. HSIO_STD supports 2.7 V to 3.6 V V_{DDIO} range with high-speed signalling and programmable drive strength.

3. Functional Description

3.1 CPU Subsystem

3.1.1 CPU

The CYT4BF CPU subsystem contains a 32-bit Arm Cortex-M0+ CPU with MPU, and two 32-bit Arm Cortex-M7 CPUs, each with MPU, single/double-precision FPU, and 16-KB data and instruction caches. This subsystem also includes P-/M-DMA controllers, a cryptographic accelerator, 8384 KB of code-flash, 256 KB of work-flash, 1024 KB of SRAM, and 64 KB of ROM.

The Cortex-M0+ CPU provides a secure, un-interruptible boot function. This guarantees that, following completion of the boot function, system integrity is valid and privileges are enforced. Shared resources (flash, SRAM, peripherals, and so on) can be accessed through bus arbitration, and exclusive accesses are supported by an inter-processor communication (IPC) mechanism using hardware semaphores.

Each Cortex-M7 CPU has 16 KB of instruction and 16 KB of data TCM with programmable read wait states. Each TCM is clocked by the associated Cortex-M7 CPU clock.

3.1.2 DMA Controllers

CYT4BF has three DMA controllers: P-DMA0 with 16 general purpose and 127 dedicated channels, P-DMA1 with 8 general purpose and 57 dedicated channels, and M-DMA0 with eight channels. P-DMA is used for peripheral-to-memory and memory-to-peripheral data transfers and provides low latency for a large number of channels. Each P-DMA controller uses a single data-transfer engine that is shared by the associated channels. General purpose channels have a rich interconnect matrix including P-DMA cross triggering which enables demanding data-transfer scenarios. Dedicated channels have a single triggering input (such as an ADC channel) to handle common transfer needs. M-DMA is used for memory-to-memory data transfers and provides high memory bandwidth for a small number of channels. M-DMA uses a dedicated data-transfer engine for each channel. They support independent accesses to peripherals using the AHB multi-layer bus.

3.1.3 Flash

CYT4BF has 8384 KB (8128 KB with a 32-KB sector size, and 256 KB with an 8-KB sector size) of code-flash with an additional work-flash of 256 KB (192 KB with a 2-KB sector size, and 64 KB with a 128-B sector size). Work-flash is optimized for reprogramming many more times than code-flash. Code-flash supports Read-While-Write (RWW) operation allowing flash to be updated while the CPU is active. Both the code-flash and work-flash areas support dual-bank operation for over-the-air (OTA) programming.

3.1.4 SRAM

CYT4BF has 1024 KB of SRAM with three independent controllers. SRAM0 provides DeepSleep retention in 32-KB increments while SRAM1/2 are selectable between fully retained and not retained.

3.1.5 ROM

CYT4BF has 64 KB of ROM that contains boot and configuration routines. This ROM enables secure boot and authentication of user flash to guarantee a secure system.

3.1.6 Cryptography Accelerator for Security

The cryptography accelerator implements (3)DES block cipher, AES block cipher, SHA hash, cyclic redundancy check, pseudo random number generation, true random number generation, galois/counter mode, and a vector unit to support asymmetric key cryptography such as RSA and ECC.

3.2 System Resources

3.2.1 Power System

The power system ensures that the supply voltage levels meet the requirements of each power mode, and provides a full-system reset when these levels are not valid. Internal power-on reset (POR) guarantees full-chip reset during the initial power ramp.

Three BOD circuits monitor the external supply voltages (V_{DD} , V_{DDA} , V_{CCD}). The BOD on V_{DD} and V_{CCD} is initially enabled and cannot be disabled. The BOD on V_{DDA} is initially disabled and can be enabled by the user. For the external supplies V_{DD} and V_{DDA} , BOD circuits are software-configurable with two settings; a 2.7-V minimum voltage that is robust for all internal signaling, and a 3.0-V minimum voltage, which is also robust for all I/O specifications (which are guaranteed at 2.7 V). The BOD on V_{CCD} is provided as a safety measure and is not a robust detector.

Three overvoltage detection (OVD) circuits are provided for monitoring external supplies (V_{DD} , V_{DDA} , V_{CCD}), and overcurrent detection circuits (OCD) for monitoring internal and external regulators. OVD thresholds on V_{DD} and V_{DDA} are configurable with two settings; a 5.0-V and 5.5-V maximum voltage.

Two voltage detection circuits are provided to monitor the external supply voltage (V_{DD}) for falling and rising levels, each configurable for one of the 26 selectable levels.

All BOD, OVD, and OCD circuits on V_{DD} and V_{CCD} generate a reset, because these protect the CPUs and fault logic. The BOD and OVD circuits on V_{DDA} can be configured to generate either a reset, or a fault.

3.2.2 Regulators

CYT4BF contains three regulators that provide power to the low-voltage core transistors: DeepSleep, core internal, and core external. These regulators accept a 2.7-V to 5.5-V V_{DD} supply and provide a low-noise 1.1-V supply to various parts of the device. These regulators are automatically enabled and disabled by hardware and firmware when switching between power modes. The core internal and core external regulators operate in Active mode, and provide power to the CPU subsystem and associated peripherals.

DeepSleep

The DeepSleep regulator is used to maintain power in a small number of blocks when in DeepSleep mode. These blocks include the ILO and WDT timers, BOD detector, SCB0, SRAM memories, Smart I/O, and other configuration memories. The DeepSleep regulator is enabled when in DeepSleep mode, and the core internal regulator is disabled. It is disabled when XRES_L is asserted (LOW) and when the core internal regulator is disabled.

Core internal

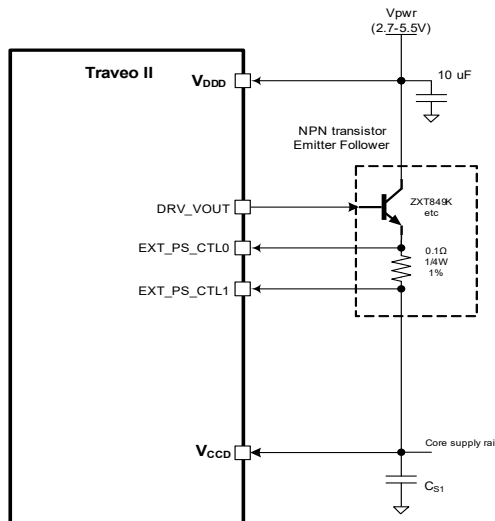
The core internal regulator supports load currents up to 300 mA, and is operational during device start-up (boot process), and in Active/Sleep modes.

Core external^[5]

To support worst-case loading, with both M7 CPUs and the M0+ CPU at their maximum clock frequency and all integrated peripherals operating, a core external regulator is required, capable of load currents up to 600 mA. While the control and monitor circuits for the core external regulator are internal to CYT4BF, the power regulating element (NPN pass transistor, PMIC, or LDO) is external. This reduces the overall power dissipation within the CYT4BF package, while maintaining a well-regulated core supply.

The core external regulator may be implemented with either an external NPN pass transistor, PMIC, or linear regulator (LDO). Each implementation requires different external components on the PCB, and different connections to CYT4BF for both regulation and control.

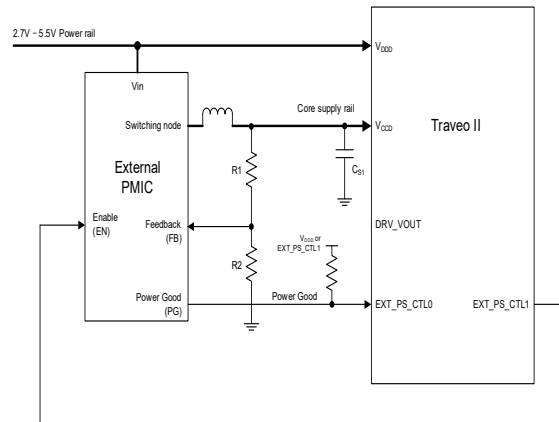
Figure 3-1. Sample Core External Regulator with NPN Transistor



Note

- When CYT4BF is in Hibernate mode, the GPIO used to control the core external regulator are High-Z. This may require an external pull-up or pull-down resistor to disable the external regulator and configure it for minimum operating current.

Figure 3-2. Sample Core External Regulator with PMIC/LDO



- PMIC EN pin polarity is HIGH for enable, PMIC PG pin polarity is HIGH for power good.
- If EN pin of PMIC does not have the internal pull-down resistor, an external pull-down resistor must be placed to keep the PMIC disabled during power-on reset.
- See the Traveo II device datasheet for CS1.
- Output voltage setting resistors (R1, R2) are needed according to the selected PMIC.

Both the core internal and core external regulators require an external bulk storage capacitor connected to the VCCD pin. This capacitor provides charge under the dynamic loads of the low-voltage core transistors.

3.2.3 Clock System

The CYT4BF clock system provides clocks to all subsystems that require them, and glitch-free switching between different clock sources. In addition, the clock system ensures that no metastable conditions occur.

The clock system for CYT4BF consists of the 8-MHz IMO, two ILOs, four watchdog timers, four PLLs, an FLL, five clock supervisors (CSV), a 8- to 33.34-MHz ECO, and a 32.768-kHz WCO.

The clock system supports three main clock domains: CLK_HF, CLK_SLOW, and CLK_LF.

- CLK_HF are the Active mode clocks. Each can use any of the high frequency clock sources including IMO, EXT_CLK, ECO, FLL, or PLL
- CLK_SLOW provides a reference clock for the Cortex-CM0+ CPU, CRYPTO, P-/M-DMA, and other slow infrastructure blocks of CPU subsystem
- CLK_LF is a DeepSleep domain clock and provides a reference clock for the MCWDT or RTC modules. The reference clock for the CLK_LF domain is either disabled or selectable from ILO0, ILO1, or WCO.

Table 3-1. CLK_HF Destinations

| Name | Description |
|---------|---|
| CLK_HF0 | CPUSS (Memories, CLK_SLOW, Peripherals) |
| CLK_HF1 | CPUSS (Cortex-M7 CPU 0, 1) |
| CLK_HF2 | CAN FD, FlexRay, LIN, TCPWM, SCB, SAR |
| CLK_HF3 | Event Generator |
| CLK_HF4 | Ethernet |
| CLK_HF5 | Audio Subsystem (I ² S) |
| CLK_HF6 | SDHC Interface, SMIF |

IMO Clock Source

The IMO is the frequency reference in CYT4BF when no external reference is available or enabled. The IMO operates at a frequency of 8 MHz \pm 1%. The internal trim settings for the IMO can be dynamically updated to provide a tolerance < 1%.

ILO Clock Source

An ILO is a low-power oscillator, nominally 32.768 kHz, which generates clocks for a watchdog timer when in DeepSleep mode. There are two ILOs to ensure clock supervisor (CSV) capability in DeepSleep mode. ILO-driven counters can be calibrated to the IMO, WCO, or ECO to improve their accuracy. ILO1 is also used for clock supervision.

PLL and FLL

A PLL (one of the two 200 MHz and two 400 MHz) or FLL may be used to generate high-speed clocks from the IMO, ECO, or an EXT_CLK. The FLL provides a much faster lock than the PLL (5 μ s instead of 45 μ s) in exchange for a small amount (\pm 2%) of frequency error^[6]. The 400-MHz PLL supports spread spectrum clock generation (SSCG) with down spreading.

Clock Supervisor

Each clock supervisor (CSV) allows one clock (reference) to supervise the behavior of another clock (monitored). Each CSV has counters for both the monitored and reference clocks. Parameters for each counter determine the frequency of the reference clock as well as the upper and lower frequency limits of the monitored clock. If the frequency range comparator detects a stopped clock or a clock outside the specified frequency range, an abnormal state is signaled and either a reset or an interrupt is generated.

EXT_CLK

One of three GPIO_STD I/Os can be used to provide an external clock input of up to 80 MHz. This clock can be used as the source clock for either the PLL or FLL, or can be used directly by the CLK_HF domain.

ECO

The ECO provides high-frequency clocking using an external crystal connected to the ECO_IN and ECO_OUT pins. It supports fundamental mode (non-overtone) quartz crystals, in the range of 8 to 33.34 MHz. When used in conjunction with the

PLL, it generates CPU and peripheral clocks up to device's maximum frequency. ECO accuracy depends on the selected crystal. If the ECO is disabled, the associated pins can be used for any of the available I/O functions.

WCO

The WCO is a low-power, watch-crystal oscillator intended for real-time-clock applications. It requires an external 32.768-kHz crystal connected to the WCO_IN and WCO_OUT pins. The WCO can also be configured as a clock reference for CLK_LF, which is the clock source for the MCWDT and RTC.

3.2.4 Reset

CYT4BF can be reset from a variety of sources, including software. Most reset events are asynchronous and guarantee reversion to a known state. The reset cause (POR, BOD, OVD, overcurrent, XRES_L, WDT, MCWDT, software reset, fault, CSV, Hibernate wakeup, debug) is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES_L pin is available for external reset.

3.2.5 Watchdog Timer

CYT4BF has one watchdog timer (WDT) and three multi-counter watchdog timers (MCWDT).

The WDT is a free-running counter clocked only by ILO0, which allows it to be used as a wakeup source from Hibernate. Watchdog operation is possible during all power modes. To prevent a device reset from a WDT timeout, the WDT must be serviced during a configured window. A watchdog reset is recorded in the reset cause register.

An MCWDT is available for each of the CPU cores. These timers provide more capabilities than the WDT, and are only available in Active, Sleep, and DeepSleep modes. These timers have multiple counters that can be used separately or cascaded to trigger interrupts and/or resets. They are clocked from ILO0 or the WCO.

3.2.6 Power Modes

CYT4BF has six power modes.

- Active – all peripherals are available
- Low-Power Active (LPACTIVE) – Low-power profile of Active mode where all peripherals and the CPUs are available, but with limited capability
- Sleep – all peripherals except the CPUs are available
- Low-Power Sleep (LPSLEEP) – Low-power profile of Sleep mode where all peripherals except the CPUs are available, but with limited capability
- DeepSleep – only peripherals which work with CLK_LF are available
- Hibernate – the device and I/Os are in High-Z state, the device resets on wakeup

Note

6. Operation of reference-timed peripherals (like a UART) with an FLL-based reference is not recommended due the allowed frequency error.

3.3 Peripherals

3.3.1 Peripheral Clock Dividers

Integer and fractional clock dividers are provided for peripheral and timing purposes.

Table 3-2. Clock Dividers - CPUSS Group (Nr. 0)

| Divider Type | Instances | Description |
|--------------|-----------|--|
| div_8 | 4 | Integer divider, 8 bits |
| div_16 | 3 | Integer divider, 16 bits |
| div_24_5 | 1 | Fractional divider, 24.5 bits (24 integer bits, 5 fractional bits) |

Table 3-3. Clock Dividers - COMM Group (Nr. 1)

| Divider Type | Instances | Description |
|--------------|-----------|--|
| div_8 | 19 | Integer divider, 8 bits |
| div_16 | 20 | Integer divider, 16 bits |
| div_24_5 | 21 | Fractional divider, 24.5 bits (24 integer bits, 5 fractional bits) |

3.3.2 Peripheral Protection Unit

The Peripheral Protection Unit (PPU) controls and monitors unauthorized access from all masters (CPU, P-/M-DMA, CRYPTO, and any enabled debug interface) to the peripherals. It allows or restricts data transfers on the bus infrastructure. The access rules are enforced based on specific properties of a transfer, such as an address range for the transfer and access attributes (such as read/write, user/privilege, and secure/non-secure).

3.3.3 12-bit SAR ADC

CYT4BF contains three 1-Msps SAR ADCs. These ADCs can be clocked at up to 26.67 MHz and provide a 12-bit result in 26 clock cycles. The references for all three SAR ADCs come from a dedicated pair of inputs: VREFH and VREFL^[7].

CYT4BF supports up to 117 logical ADC channels, and external inputs from up to 99 I/Os. Each ADC also supports six internal connections for diagnostic and monitoring purposes. The number of ADC channels (per ADC and package type) are listed in [Table 1-1](#).

Each ADC has a sequencer, which autonomously cycles through the configured channels (sequencer scan) with zero-switching overhead (that is, the aggregate sampling bandwidth, when clocked at 26.67 MHz, is equal to 1 Msps whether it is for a single channel or distributed over several channels). The sequencer switching is controlled through a state machine or firmware. The sequencer prioritizes trigger requests, enables the appropriate analog channel, controls ADC sampling, initiates ADC data conversion, manages results, and initiates subsequent conversions for repetitive or group conversions without CPU intervention.

Each SAR ADC has an analog multiplexer used to connect the signals to be measured to the ADC. It has 32 GPIO_STD inputs, one special GPIO_STD input for motor-sense, and six additional inputs to measure internal signals such as a band-gap reference,

a temperature sensor, and power supplies. The device supports synchronous sampling of one motor-sense channel on each of the three ADCs.

CYT4BF has one temperature sensor that is shared by all three ADCs. The temperature sensor must only be sampled by one ADC at a time. Software post processing is required to convert the temperature sensor reading into kelvin or Celsius values.

To accommodate signals with varying source impedances and frequencies, you can have different sample times programmed for each channel. Each ADC also supports range comparison, which allows fast detection of out-of-range values without having to wait for a sequencer scan to complete and for the CPU firmware to evaluate the measurement for out-of-range values.

The ADCs are not usable in DeepSleep and Hibernate modes as they require a high-speed clock. The ADC input reference voltage VREFH range is 2.7 V to V_{DDA} and VREFL is V_{SSA} .

3.3.4 Timer/Counter/PWM Block (TCPWM)

The TCPWM block consists of 16-bit (102 channels) and 32-bit (16 channels) counters with user-programmable period. Fifteen of the 16-bit counters are optimized for motor-control operations. Each TCPWM counter contains a capture register to record the count at the time of an event, a period register (used to either stop or auto-reload the counter when its count is equal to the period register), and compare registers to generate signals that are used as PWM duty-cycle outputs.

Each counter within the TCPWM block supports several functional modes such as timer, capture, quadrature, PWM, PWM with dead-time insertion (PWM_DT, 8-bit), pseudo-random PWM (PWM_PR), and shift-register.

In motor-control applications, the counter within the TCPWM block supports enhanced quadrature mode with features such as asymmetric PWM generation, dead-time insertion (16-bit), and association of different dead times for PWM output signals.

The TCPWM block also provides true and complement outputs, with programmable offset between them, to allow their use as deadband complementary PWM outputs. The TCPWM block also has a kill input (only for the PWM mode) to force outputs to a predetermined state; for example, this may be used in motor-drive systems when an overcurrent state is detected and the PWMs driving the FETs need to be shut off immediately (no time for software intervention).

3.3.5 Serial Communication Blocks (SCB)

CYT4BF contains 11 serial communication blocks, each configurable to support I²C, UART, or SPI.

I²C Interface

An SCB can be configured to implement a full I²C master (capable of multi-master arbitration) or slave interface. Each SCB configured for I²C can operate at speeds of up to 1 Mbps (Fast-mode Plus) and has flexible buffering options to reduce the interrupt overhead and latency of the CPU. In addition, each SCB supports FIFO buffering for receive and transmit data, which, by increasing the time for the CPU to read the data, reduces the need for clock stretching. The I²C interface

Note

7. VREF_L prevents IR drops in the VSSIO and VSSA paths from impacting the measurements. VREF_L, when properly connected, reduces or removes the impact of IR drops in the VSSIO and VSSA paths from measurements.

is compatible with Standard, Fast-mode, and Fast-mode Plus devices as specified in the NXP I²C-bus specification and user manual (UM10204). The I²C-bus I/O is implemented with GPIO in open-drain modes^[8, 9].

UART Interface

When configured as a UART, each SCB provides a full-featured UART with maximum signalling rate determined by the configured peripheral-clock frequency and over-sampling rate. It supports infrared interface (IrDA) and SmartCard (ISO 7816) protocols, which are minor variants of the UART protocol. It also supports the 9-bit multiprocessor mode that allows the addressing of peripherals connected over common Rx and Tx lines. Common UART functions such as parity, number of stop bits, break detect, and frame error are supported. FIFO buffering of transmit and receive data allows greater CPU service latencies to be tolerated.

The LIN protocol is supported by the UART. LIN is based on a single-master multi-slave topology. There is one master node and multiple slave nodes on the LIN bus. The SCB UART supports only LIN slave functionality. Compared to the dedicated LIN blocks, an SCB/UART used for LIN requires a higher level of software interaction and increased CPU load.

SPI Interface

The SPI configuration supports full Motorola SPI, TI Synchronous Serial Protocol (SSP, essentially adds a start pulse that is used to synchronize SPI-based codecs), and National Microwire (a half-duplex form of SPI). The SPI interface can use the FIFO. The SPI interface operates with up to a 12.5-MHz SPI Clock. SCB also supports EZSP^[10] mode.

SCB0 supports the following additional features:

- Operable as a slave in DeepSleep mode
- I²C slave EZ (EZI²C^[11]) mode with up to 256-B data buffer for multi-byte communication without CPU intervention
- I²C slave externally-clocked operations
- Command/response mode with a 512-B data buffer for multi-byte communication without CPU intervention

3.3.6 CAN FD

CYT4BF contains two CAN FD controller blocks, each supporting five CAN FD channels. All CAN FD controllers are compliant with the ISO 11898-1:2015 standard; an ISO 16845:2015 certificate is available. It also implements the time-triggered CAN (TTCAN) protocol specified in ISO 11898-4 (TTCAN protocol levels 1 and 2) completely in hardware. All functions concerning the handling of messages are implemented by the Rx and Tx handlers. The Rx handler manages message acceptance filtering, transfer of received messages from the CAN core to a message RAM, and provides receive-message status. The Tx handler is responsible for the transfer of transmit messages from the message RAM to the CAN core, and provides transmit-message status.

Notes

8. This is not 100% compliant with the I²C-bus specification; I/Os are not overvoltage-tolerant, do not support the 20-mA sink requirement of Fast-mode Plus, and violate the leakage specification when no power is applied.
9. Only Port 0 with the slew rate control enabled meets the minimum fall time requirement.
10. The Easy SPI (EZSPI) protocol is based on the Motorola SPI protocol operating in any mode (0, 1, 2, or 3). It allows communication between master and slave while reducing the need for CPU intervention.
11. The Easy I²C (EZI²C) protocol is a unique communication scheme built on top of the I²C protocol by Cypress. It uses a meta protocol around the standard I²C protocol to communicate to an I²C slave using indexed memory transfers. This reduces the need for CPU intervention.
12. Only 10/100 Mbps is available in the 176-TEQFP packaged devices.

3.3.7 Local Interconnect Network (LIN)

CYT4BF contains up to 20 LIN blocks. Each block supports transmission/reception of data following the LIN protocol according to ISO standard 17987. Each LIN block connects to an external transceiver through a 3-pin interface (including an enable function) and supports master and slave functionality. Each block also supports classic and enhanced checksum, along with break detection during message reception and wake-up signaling. Break detection, sync field, checksum calculations, and error interrupts are handled in hardware.

3.3.8 FlexRay Interface

CYT4BF supports one FlexRay interface with channel A and an optional channel B, conforming to FlexRay protocol specification 2.1, and supports up to a 10-Mbps data rate. Message buffers are configurable as Tx, Rx, or RXFIFO, and are filtered based on FrameID, cycle count, and message ID.

3.3.9 Ethernet MAC

CYT4BF supports two Ethernet channels with transfer rates of 10, 100, or 1000 Mbps^[12]. The input/output frames and flow control are compliant to the Ethernet/IEEE 802.3az standard and also IEEE-1588 precision-time protocol (PTP). CYT4BF supports half/full-duplex data transport using external PHY devices. The MAC supports glue-free connection to PHYs through IEEE standard MII, RMII, GMII, and RGMII interfaces. The device also supports Audio-Video Bridging (AVB). The MAC supports standard 6-byte programmable addresses.

3.3.10 External Memory Interface

In addition to the internal flash memory, CYT4BF supports direct connection to as much as 128-MB of external flash or RAM memory. This connection is made through either a HyperBus or serial peripheral interface (SPI). HyperBus allows connection to HyperFlash and HyperRAM devices, while SPI (single, dual, quad, or octal SPI at up to 80 MHz) can connect with serial flash memory. Code stored in memory connected through this interface allows execute-in-place (XIP) operation, which does not require the instructions to be first copied to internal memory, and on-the-fly encryption and decryption for environments requiring secure external data and code.

3.3.11 SDHC Interface

CYT4BF supports one Secure Digital High Capacity (SDHC) interface, which conforms to Secure Digital (SD) 6.0, Secure Digital Input Output (SDIO) 4.10, and Embedded Multimedia Card (eMMC) 5.1 specifications, along with Host Control Interface (HCI) 4.2 specification. The interface supports System DMA (SDMA), Advance DMA (ADMA2, ADMA3), and command queuing (CQ) features. This interface supports data rates of SD DS (Default Speed, 4-bits at 25 MHz), SD HS (High Speed, 4-bits at 50 MHz, and eMMC 52-MHz DDR (8-bits at 52-MHz card clock).

3.3.12 Audio Interface

CYT4BF supports three instances of Inter-IC Sound Bus (I²S) interface to connect to digital audio devices. Implements Philips® semiconductor I²S bus specification: February 1986, revised June 5, 1996. Supports standard Philips I²S, Left Justified (LJ), and eight-channel Time Division Multiplexed (TDM) digital audio interface formats in both master and slave modes with independent operations in receive and transmit directions.

3.3.13 One-Time-Programmable (OTP) eFuse

CYT4BF contains a 1024-bit OTP eFuse memory that can be used to store and access a unique and unalterable identifier or serial number for each device. eFuses are also used to control the device life-cycle (manufacturing, programming, normal operation, end-of-life, and so on) and the security state. Of the 1024 bits, 192 are available for user purposes.

3.3.14 Event Generator

The event generator supports generation of interrupts and triggers in Active mode and interrupts in DeepSleep mode. The event generators are used to trigger a specific device operation (execution of an interrupt handler, a SAR ADC conversion, and so on) and to provide a cyclic wakeup mechanism from DeepSleep mode. They provide CPU-free triggers for device functions, and reduce CPU involvement in triggering device functions, thus reducing overall power consumption and processing overhead.

3.3.15 Trigger Multiplexer

CYT4BF supports connecting various peripherals using trigger signals. Triggers are used to inform a peripheral of the occurrence of an event or change of state. These triggers are used to affect or initiate some action in other peripherals. The trigger multiplexer is used to route triggers from a source peripheral to a destination. Triggers provide active logic functionality and are typically supported in Active mode.

3.4 I/Os

CYT4BF has up to 240 programmable I/Os.

The I/Os are organized as logical entities called ports, which are a maximum of 8 bits wide. During power-on, Hibernate, and reset, the I/Os are forced to the High-Z state.

Every I/O can generate an interrupt (if enabled) and each port has an interrupt request (IRQ) and interrupt service routine (ISR) associated with it.

I/O port power source mapping is listed in [Table 3-4](#). The associated supply determines the V_{OH}, V_{OL}, V_{IH}, and V_{IL} levels when configured for CMOS and Automotive thresholds.

Table 3-4. I/O Port Power Source

| Supply Pins | Ports |
|-------------|--|
| VDDD | P0, P1, P2, P3, P4, P5, P16, P17, P18, P19, P20, P21, P22, P23, P28, P29, P30, P31 |
| VDDIO_1 | P6, P7, P8, P9, P32 |
| VDDIO_2 | P10, P11, P12, P13, P14, P15 |
| VDDIO_3 | P24, P25 |
| VDDIO_4 | P26, P27, P33, P34 |

3.4.1 Port Nomenclature

Px.y describes a particular bit “y” available within an I/O port “x.” For example, P4.2 reads “port 4, bit 2”.

Each I/O implements the following:

- Programmable drive mode
 - High impedance
 - Resistive pull-up
 - Resistive pull-down
 - Open drain with strong pull-down
 - Open drain with strong pull-up
 - Strong pull-up or pull-down
 - Weak pull-up or pull-down

CYT4BF has three types of programmable I/Os: GPIO Standard, GPIO Enhanced, and HSIO Standard.

3.4.2 GPIO Standard (GPIO_STD)

Supports standard automotive signaling across the 2.7-V to 5.5-V V_{DDIO} range. GPIO Standard I/Os have multiple configurable drive levels, drive modes, and selectable input levels.

3.4.3 GPIO Enhanced (GPIO_ENH)

Supports extended functionality automotive signalling across the 2.7-V to 5.5-V V_{DDIO} range with higher currents at lower voltages (full I²C timing support, slew-rate control).

Both GPIO_STD and GPIO_ENH implement the following:

- Configurable input threshold (CMOS, TTL, or Automotive)
- Hold mode for latching previous state (used for retaining the I/O state in DeepSleep mode)
- Analog input mode (input and output buffers disabled)

3.4.4 HSIO Standard (HSIO_STD)

These I/Os are optimized exclusively for high-speed signaling and do not support slew-rate control, DeepSleep operation, POR mode control, analog connections, or non-CMOS signaling levels. HSIO_STD supports high-speed peripherals such as QSPI, HyperBus, Ethernet, and SDHC controller. HSIO_STD also supports programmable drive strength. These I/Os are available only in Active mode and retain state in DeepSleep mode.

3.4.5 Smart I/O

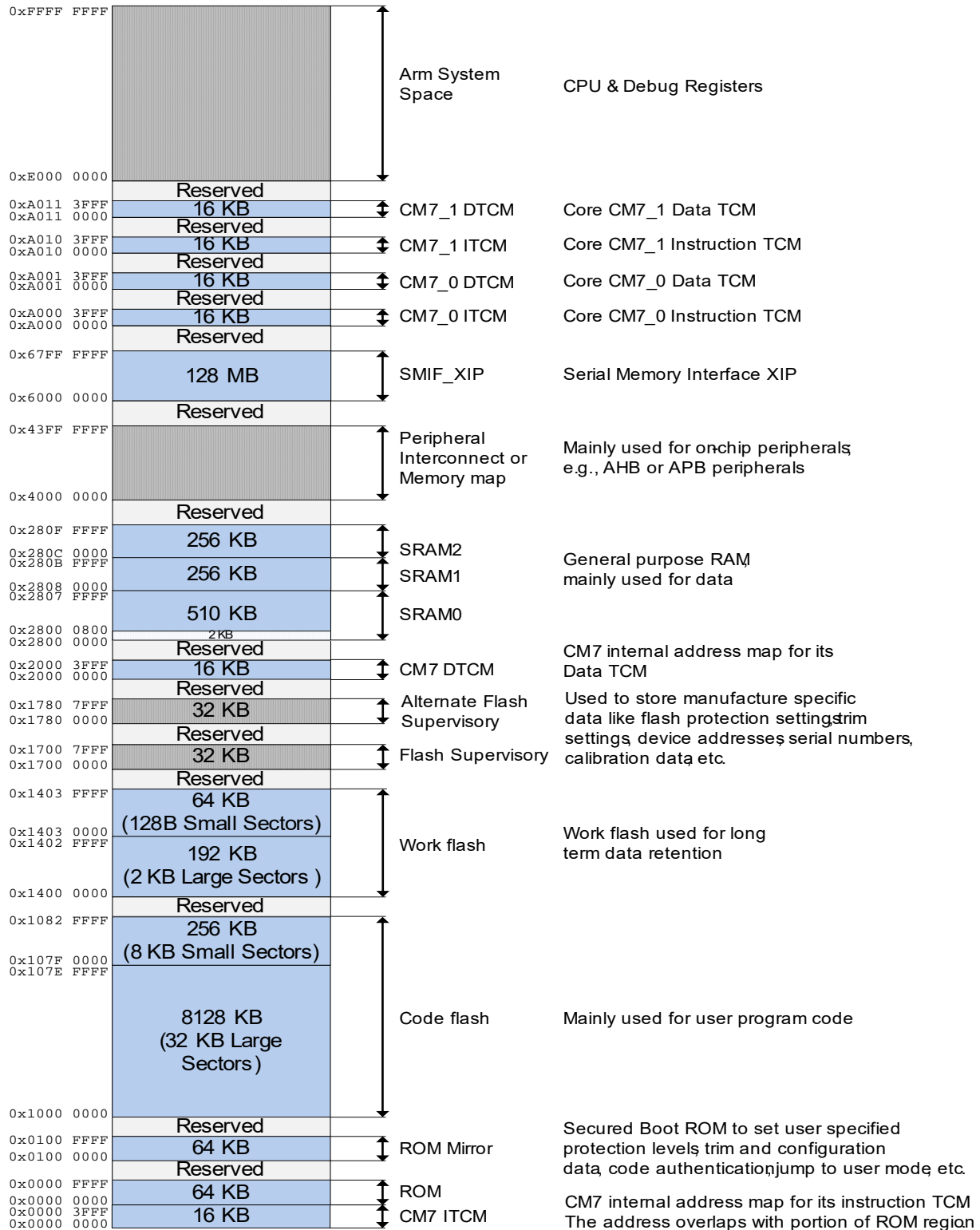
Smart I/O allows Boolean operations on signals going to the I/O from the subsystems of the chip or on signals coming into the chip. CYT4BF has five Smart I/O blocks. Operation can be synchronous or asynchronous and the blocks operate in all device power modes except for Hibernate.

4. CYT4BF Address Map

The CYT4BF microcontroller supports the memory spaces shown in [Figure 4-1](#).

- 8384 KB (8128 KB + 256 KB) of code-flash, used in the single- or dual-bank mode based on the associated bit in the flash control register
 - Single-bank mode: 8384 KB
 - Dual-bank mode: 4192 KB per bank
- 256 KB (192 KB + 64 KB) of work-flash, used in the single- or dual-bank mode based on the associated bit in the flash control register
 - Single-bank mode: 256 KB
 - Dual-bank mode: 128 KB per bank
- 64 KB of secure ROM
- 1024 KB of SRAM (First 2 KB is reserved for internal usage)
- 16 KB of Instruction TCM for each Cortex-M7 CPU
- 16 KB of Data TCM for each Cortex-M7 CPU
- 128 MB SMIF XIP

Figure 4-1.CYT4BF Address Map^[13, 14]



Notes

- 13. The size representation is not up to scale.
- 14. First 2KB of SRAM is reserved, not available for users. User must keep the power of first 32-KB block of SRAM0 in enabled or retained in all Active, LP Active, Sleep, LP Sleep, DeepSleep modes.

5. Flash Base Address Map

Table 5-1 through Table 5-6 give information about the sector mapping of the code- and work-flash regions along with their respective base addresses.

Table 5-1. Code-flash Address Mapping in Single-Bank Mode

| Code-flash Size (KB) | Large Sectors (LS) | Small Sectors (SS) | Large Sector Base Address | Small Sector Base Address |
|----------------------|--------------------|--------------------|---------------------------|---------------------------|
| 8384 | 32 KB × 254 | 8 KB × 32 | 0x1000 0000 | 0x107F 0000 |

Table 5-2. Work-flash Address Mapping in Single-Bank Mode

| Work-flash Size (KB) | Large Sectors | Small Sectors | Large Sector Base Address | Small Sector Base Address |
|----------------------|---------------|---------------|---------------------------|---------------------------|
| 256 | 2 KB × 96 | 128 B × 512 | 0x1400 0000 | 0x1403 0000 |

Table 5-3. Code-flash Address Mapping in Dual-Bank Mode (Mapping A)

| Code-flash Size (KB) | First Half LS | First Half SS | Second Half LS | Second Half SS | First Half LS Base Address | First Half SS Base Address | Second Half LS Base Address | Second Half SS Base Address |
|----------------------|---------------|---------------|----------------|----------------|----------------------------|----------------------------|-----------------------------|-----------------------------|
| 8384 | 32 KB × 127 | 8 KB × 16 | 32 KB × 127 | 8 KB × 16 | 0x1000 0000 | 0x103F 8000 | 0x1200 0000 | 0x123F 8000 |

Table 5-4. Code-flash Address Mapping in Dual-Bank Mode (Mapping B)

| Code-flash Size (KB) | First Half LS | First Half SS | Second Half LS | Second Half SS | First Half LS Base Address | First Half SS Base Address | Second Half LS Base Address | Second Half SS Base Address |
|----------------------|---------------|---------------|----------------|----------------|----------------------------|----------------------------|-----------------------------|-----------------------------|
| 8384 | 32 KB × 127 | 8 KB × 16 | 32 KB × 127 | 8 KB × 16 | 0x1200 0000 | 0x123F 8000 | 0x1000 0000 | 0x103F 8000 |

Table 5-5. Work-flash Address Mapping in Dual-Bank Mode (Mapping A)

| Work-flash Size (KB) | First Half LS | First Half SS | Second Half LS | Second Half SS | First Half LS Base Address | First Half SS Base Address | Second Half LS Base Address | Second Half SS Base Address |
|----------------------|---------------|---------------|----------------|----------------|----------------------------|----------------------------|-----------------------------|-----------------------------|
| 256 | 2 KB × 48 | 128 B × 256 | 2 KB × 48 | 128 B × 256 | 0x1400 0000 | 0x1401 8000 | 0x1500 0000 | 0x1501 8000 |

Table 5-6. Work-flash Address Mapping in Dual-Bank Mode (Mapping B)

| Work-flash Size (KB) | First Half LS | First Half SS | Second Half LS | Second Half SS | First Half LS Base Address | First Half SS Base Address | Second Half LS Base Address | Second Half SS Base Address |
|----------------------|---------------|---------------|----------------|----------------|----------------------------|----------------------------|-----------------------------|-----------------------------|
| 256 | 2 KB × 48 | 128 B × 256 | 2 KB × 48 | 128 B × 256 | 0x1500 0000 | 0x1501 8000 | 0x1400 0000 | 0x1401 8000 |

6. Peripheral I/O Map

Table 6-1. CYT4BF Peripheral I/O Map

| Section | Description | Base Address | Instances | Instance Size | Group | Slave |
|-----------|--|--------------|--------------------|---------------|-------|-------|
| PERI | Peripheral interconnect | 0x4000 0000 | | | 0 | 0 |
| | Peripheral group (0, 1, 2, 3, 4, 5, 6, 8, 9) | 0x4000 4000 | 9 | 0x40 | | |
| | Peripheral trigger group | 0x4000 8000 | 13 | 0x400 | | |
| | Peripheral 1:1 trigger group | 0x4000 C000 | 14 | 0x400 | | |
| PERI_MS | Peripheral interconnect, master interface | 0x4002 0000 | | | 0 | 1 |
| | PERI Programmable PPU | 0x4002 0000 | 10 ^[15] | 0x40 | | |
| | PERI Fixed PPU | 0x4002 0800 | 700 | 0x40 | | |
| PERI_PCLK | Peripheral Clock Groups | 0x4004 0000 | 2 | 0x2000 | 0 | 2 |
| CRYPTO | Cryptography component | 0x4010 0000 | | | 1 | 0 |
| CPUSS | CPU subsystem (CPUSS) | 0x4020 0000 | | | 2 | 0 |
| FAULT | Fault structure subsystem | 0x4021 0000 | | | 2 | 1 |
| | Fault structures | 0x4021 0000 | 4 | 0x100 | | |
| IPC | Inter process communication | 0x4022 0000 | | | 2 | 2 |
| | IPC structures | 0x4022 0000 | 8 | 0x20 | | |
| | IPC interrupt structures | 0x4022 1000 | 8 | 0x20 | | |
| PROT | Protection | 0x4023 0000 | | | 2 | 3 |
| | Shared memory protection unit structures | 0x4023 2000 | 16 | 0x40 | | |
| | Memory protection unit structures | 0x4023 4000 | 16 | 0x400 | | |
| FLASHC | Flash controller | 0x4024 0000 | | | 2 | 4 |
| SRSS | System Resources Sub-System Core Registers | 0x4026 0000 | | | 2 | 5 |
| | Clock Supervision High Frequency | 0x4026 1400 | 8 | 0x10 | | |
| | Clock Supervision Reference Frequency | 0x4026 1710 | 1 | | | |
| | Clock Supervision Low Frequency | 0x4026 1720 | 1 | | | |
| | Clock Supervision Internal Low Frequency | 0x4026 1730 | 1 | | | |
| | Clock PLL 400 MHz | 0x4026 1900 | 2 | 0x10 | | |
| | Multi Counter WDT | 0x4026 8000 | 3 | 0x100 | | |
| | Free Running WDT | 0x4026 C000 | 1 | | | |
| BACKUP | SRSS Backup Domain/RTC | 0x4027 0000 | | | 2 | 6 |
| | Backup Register | 0x4027 1000 | 4 | 0x04 | | |
| P-DMA | P-DMA0 Controller | 0x4028 0000 | | | 2 | 7 |
| | P-DMA0 channel structures | 0x4028 8000 | 143 | 0x40 | | |
| | P-DMA1 Controller | 0x4029 0000 | | | 2 | 8 |
| | P-DMA1 channel structures | 0x4029 8000 | 65 | 0x40 | | |
| M-DMA | M-DMA0 Controller | 0x402A 0000 | | | 2 | 9 |
| | M-DMA0 channels | 0x402A 1000 | 8 | 0x100 | | |
| eFUSE | eFUSE Customer Data (192 bits) | 0x402C 0868 | 6 | 0x04 | 2 | 10 |

Note

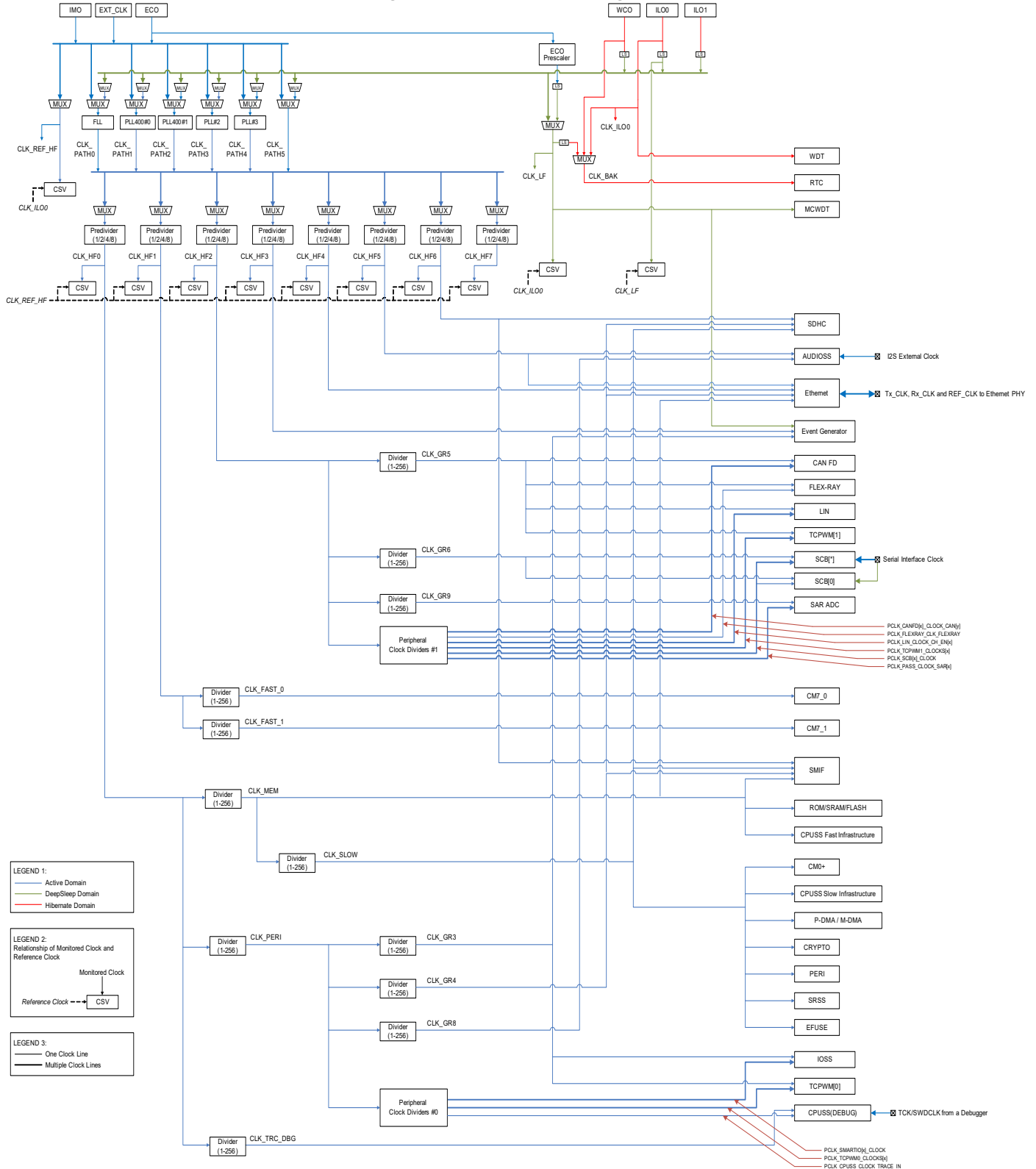
15. These Programmable PPUs are configured by the Boot ROM and are available for the user based on the access rights. Refer to the device-specific TRM to know more about the configuration of these programmable PPUs.

Table 6-1. CYT4BF Peripheral I/O Map (continued)

| Section | Description | Base Address | Instances | Instance Size | Group | Slave |
|------------------|---|--------------|-----------|---------------|-------|-------|
| HSIOM | High-Speed I/O Matrix (HSIOM) | 0x4030 0000 | 35 | 0x10 | 3 | 0 |
| GPIO | GPIO port control/configuration | 0x4031 0000 | 35 | 0x80 | 3 | 1 |
| SMARTIO | Programmable I/O configuration | 0x4032 0000 | | | 3 | 2 |
| | SMARTIO port configuration | 0x4032 0C00 | 5 | 0x100 | | |
| TCPWM | Timer/Counter/PWM 0 (TCPWM0) | 0x4038 0000 | | | 3 | 3 |
| | TCPWM0 Group #0 (16-bit) | 0x4038 0000 | 3 | 0x80 | | |
| | TCPWM0 Group #1 (16-bit, Motor control) | 0x4038 8000 | 3 | 0x80 | | |
| | TCPWM0 Group #2 (32-bit) | 0x4039 0000 | 3 | 0x80 | | |
| EVTGEN | Event generator 0 (EVTGEN0) | 0x403F 0000 | | | 3 | 4 |
| | Event generator 0 comparator structures | 0x403F 0800 | 16 | 0x20 | | |
| SMIF | Serial Memory Interface 0 (SMIF0) | 0x4042 0000 | | | 4 | 0 |
| | SMIF0 Devices | 0x4042 0800 | 1 | 0x80 | | |
| SDHC | Secure Digital High Capacity 0 (SDHC0) | 0x4046 0000 | | | 4 | 1 |
| | SDHC0 Wrap | 0x4046 0000 | | | | |
| | SDHC0 Core | 0x4046 1000 | | | | |
| ETH | Ethernet 0 (ETH0) | 0x4048 0000 | 2 | 0x10000 | 4 | 2 |
| LIN | Local Interconnect Network 0 (LIN0) | 0x4050 0000 | | | 5 | 0 |
| | LIN0 Channels | 0x4050 8000 | 20 | 0x100 | | |
| TTCANFD | CAN0 controller | 0x4052 0000 | 5 | 0x200 | 5 | 1 |
| | Message RAM CAN0 | 0x4053 0000 | | 0x9FFF | | |
| | CAN1 controller | 0x4054 0000 | 5 | 0x200 | 5 | 2 |
| | Message RAM CAN1 | 0x4055 0000 | | 0x9FFF | | |
| FLEXRAY | FlexRay 0 | 0x4056 0000 | | | 5 | 3 |
| TCPWM | Timer/Counter/PWM 1 (TCPWM1) | 0x4058 0000 | | | 5 | 4 |
| | TCPWM1 Group #0 (16-bit) | 0x4058 0000 | 84 | 0x80 | | |
| | TCPWM1 Group #1 (16-bit, Motor control) | 0x4058 8000 | 12 | 0x80 | | |
| | TCPWM1 Group #2 (32-bit) | 0x4059 0000 | 13 | 0x80 | | |
| SCB | Serial Communications Block (SPI/UART/I ² C) | 0x4060 0000 | 11 | 0x10000 | 6 | 0-10 |
| I ² S | I ² S Audio SubSystem | 0x4080 0000 | 3 | 0x1000 | 8 | 0-2 |
| SAR PASS | Programmable Analog Subsystem (PASS0) | 0x4090 0000 | | | 9 | 0 |
| | SAR0 channel controller | 0x4090 0000 | | | | |
| | SAR1 channel controller | 0x4090 1000 | | | | |
| | SAR2 channel controller | 0x4090 2000 | | | | |
| | SAR0 channel structures | 0x4090 0800 | 32 | 0x40 | | |
| | SAR1 channel structures | 0x4090 1800 | 32 | 0x40 | | |
| | SAR2 channel structures | 0x4090 2800 | 32 | 0x40 | | |

7. CYT4BF Clock Diagram

Figure 7-1.CYT4BF Clock Diagram



8. CYT4BF CPU Start-up Sequence

The start-up sequence is described in the following steps:

1. System Reset (@0x0000 0000)
2. CM0+ executes ROM boot (@0x0000 0004)
 - i. Applies trims
 - ii. Applies Debug Access port (DAP) access restrictions and system protection from eFuse and supervisory flash
 - iii. Authenticates flash boot (only in SECURE life-cycle stage) and transfers control to it
3. CM0+ executes flash boot (from Supervisory flash @0x1700 2000)
 - i. Debug pins are configured based on the SWD/JTAG spec^[16]
 - ii. Sets CM0+ vector offset register (CM0_VTOR part of the Arm system space) to the beginning of flash (@0x1000 0000)
 - iii. CM0+ branches to its Reset handler
4. CM0+ starts execution of application
 - i. Moves CM0+ vector table to SRAM (updates CM0+ vector table base)
 - i. Sets clocks for CM7_0 (CLK_HF1) and CM7_1 (CLK_HF2)
 - ii. Sets CM7_0 (CM7_0_VECTOR_TABLE_BASE @0x4020 0200) and CM7_1 (CM7_1_VECTOR_TABLE_BASE @0x4020 0600) vector tables to the respective locations, also and mentioned in flash (specified in the linker definition file)
 - iii. Enables the power for both the CPU cores CM7_0 and CM7_1
 - iv. Disables CPU_WAIT to allow accesses from the debugger
 - v. Releases CM7_0 and/or CM7_1 from reset
 - vi. Continues execution of CM0+ user application
5. CM7_0 and/or CM7_1 executes directly from either code-flash or SRAM
 - i. CM7_0/CM7_1 branches to its Reset handler
 - ii. Continues execution of the user application

Note

¹⁶. Port configuration of SWD/JTAG pins will be changed from the default GPIO mode to support debugging after the boot process, refer to [Table 11-1](#) for pin assignments.

9. Pin Assignment

Note: Thermal pad needs to be connected to VSSD.

Figure 9-1.176-TEQFP Pin Assignment

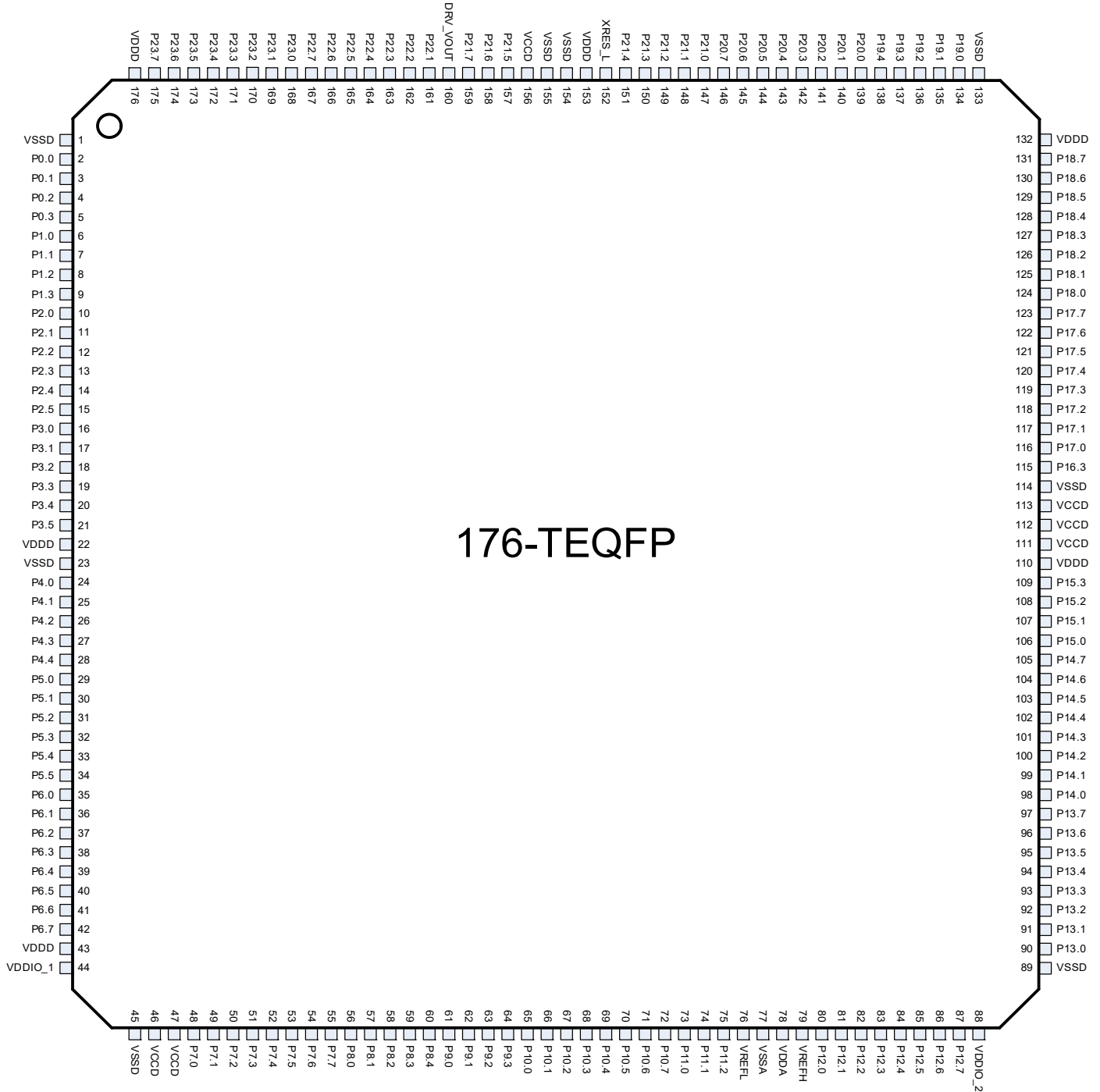


Figure 9-2.176-TEQFP Pin Assignment with Alternate Functions (preliminary)

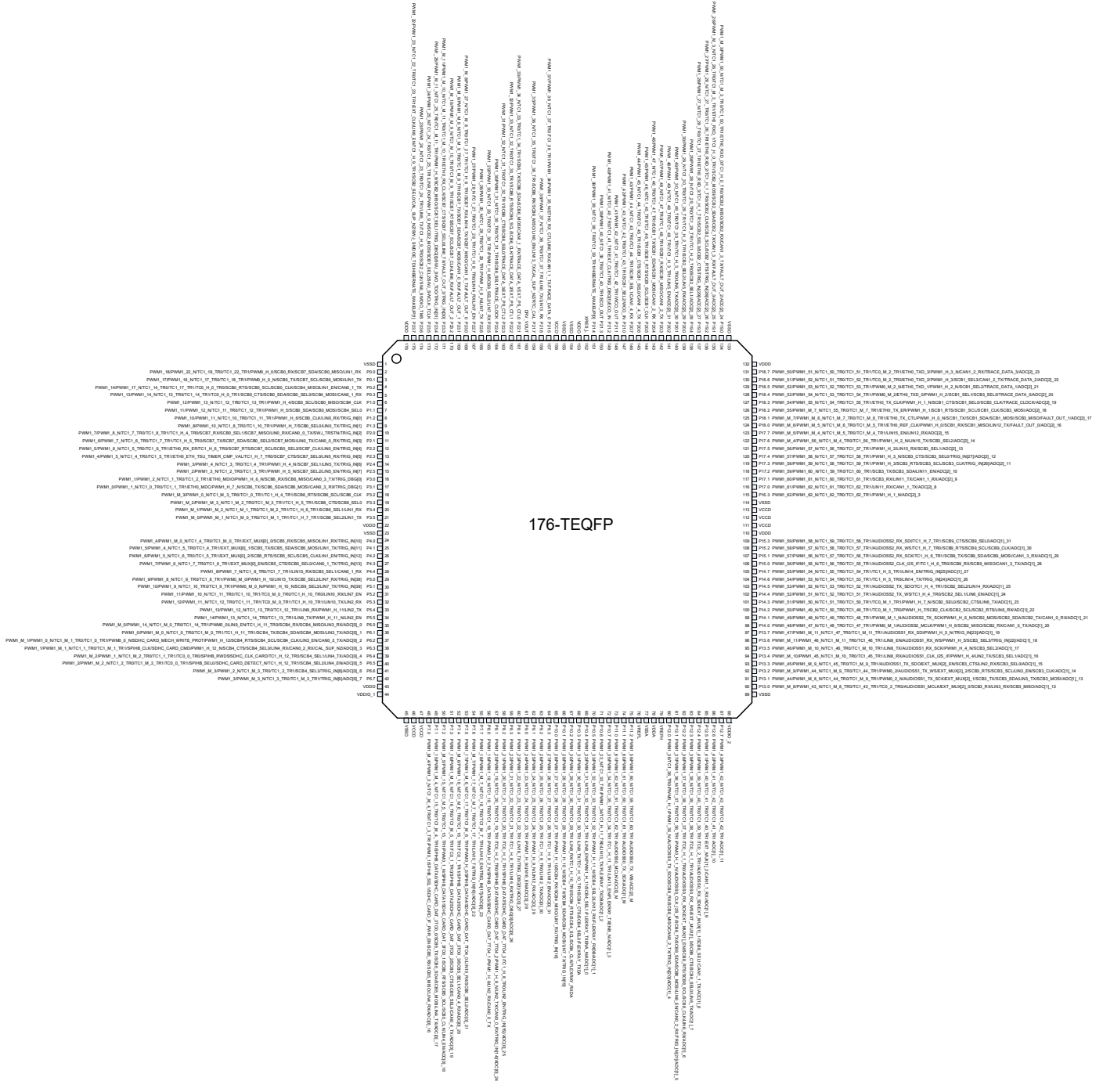


Figure 9-3.272-BGA Ball Map

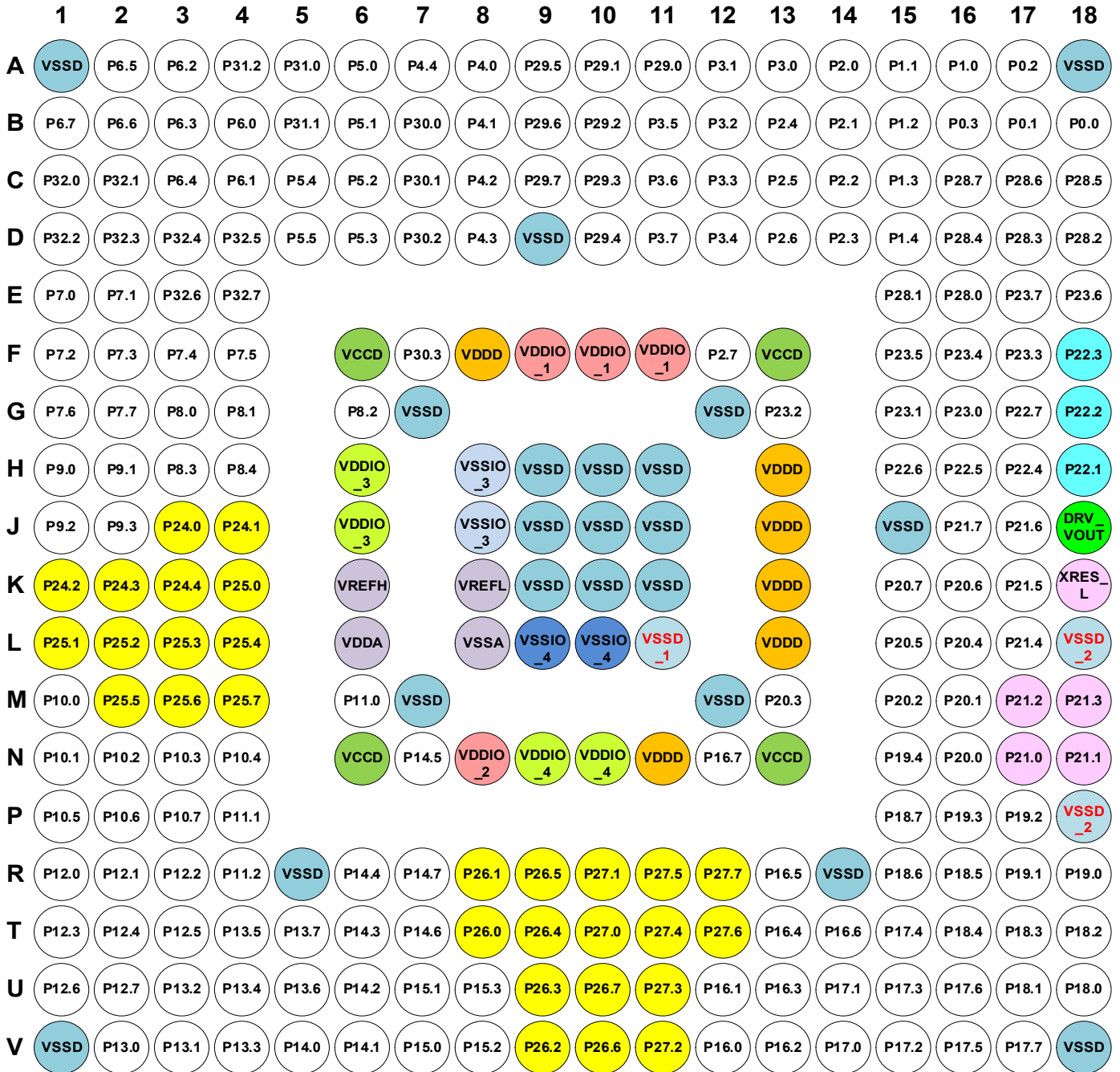
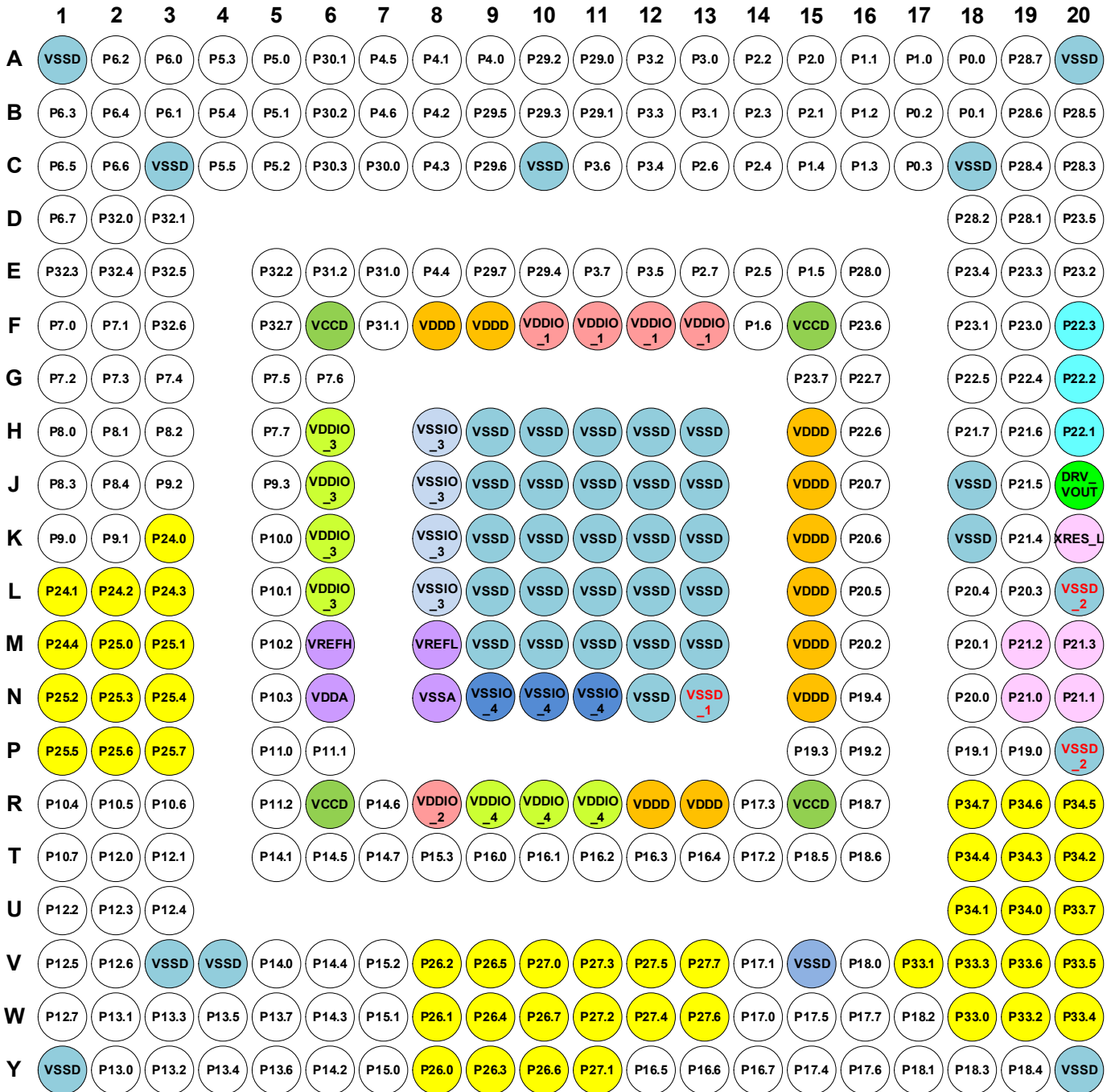


Figure 9-4.320-BGA Ball Map



10. High-Speed I/O Matrix Connections

Table 10-1. HSIOM Connections Reference

| Name | Number | Description |
|---------------------|--------|---|
| HSIOM_SEL_GPIO | 0 | GPIO controls 'out' |
| HSIOM_SEL_GPIO_DSI | 1 | GPIO controls 'out', DSI controls 'output enable' |
| HSIOM_SEL_DSI_DSI | 2 | DSI controls 'out' and 'output enable' |
| HSIOM_SEL_DSI_GPIO | 3 | DSI controls 'out', GPIO controls 'output enable' |
| HSIOM_SEL_AMUXA | 4 | Analog multiplexer bus A |
| HSIOM_SEL_AMUXB | 5 | Analog multiplexer bus B |
| HSIOM_SEL_AMUXA_DSI | 6 | Analog multiplexer bus A, DSI control |
| HSIOM_SEL_AMUXB_DSI | 7 | Analog multiplexer bus B, DSI control |
| HSIOM_SEL_ACT_0 | 8 | Active functionality 0 |
| HSIOM_SEL_ACT_1 | 9 | Active functionality 1 |
| HSIOM_SEL_ACT_2 | 10 | Active functionality 2 |
| HSIOM_SEL_ACT_3 | 11 | Active functionality 3 |
| HSIOM_SEL_DS_0 | 12 | DeepSleep functionality 0 |
| HSIOM_SEL_DS_1 | 13 | DeepSleep functionality 1 |
| HSIOM_SEL_DS_2 | 14 | DeepSleep functionality 2 |
| HSIOM_SEL_DS_3 | 15 | DeepSleep functionality 3 |
| HSIOM_SEL_ACT_4 | 16 | Active functionality 4 |
| HSIOM_SEL_ACT_5 | 17 | Active functionality 5 |
| HSIOM_SEL_ACT_6 | 18 | Active functionality 6 |
| HSIOM_SEL_ACT_7 | 19 | Active functionality 7 |
| HSIOM_SEL_ACT_8 | 20 | Active functionality 8 |
| HSIOM_SEL_ACT_9 | 21 | Active functionality 9 |
| HSIOM_SEL_ACT_10 | 22 | Active functionality 10 |
| HSIOM_SEL_ACT_11 | 23 | Active functionality 11 |
| HSIOM_SEL_ACT_12 | 24 | Active functionality 12 |
| HSIOM_SEL_ACT_13 | 25 | Active functionality 13 |
| HSIOM_SEL_ACT_14 | 26 | Active functionality 14 |
| HSIOM_SEL_ACT_15 | 27 | Active functionality 15 |
| HSIOM_SEL_DS_4 | 28 | DeepSleep functionality 4 |
| HSIOM_SEL_DS_5 | 29 | DeepSleep functionality 5 |
| HSIOM_SEL_DS_6 | 30 | DeepSleep functionality 6 |
| HSIOM_SEL_DS_7 | 31 | DeepSleep functionality 7 |

11. Package Pin List and Alternate Functions

Most pins have alternate functionality, as specified in [Table 11-1](#).

Port 11 has the following additional features,

- Ability to pass full-level analog signals to the SAR without clipping to V_{DDIO} in cases where $V_{DDIO} < V_{DDA}$
- Ability to simultaneously capture all three ADC signals with highest priority (ADC[0:2]_M)
- Lower noise, for the most sensitive sensors

Table 11-1. Pin Selector and Alternate Pin Functions in DeepSleep (DS) Mode, Analog, Smart I/O

| Name | Package | | | | DeepSleep Mapping | | | Analog | SMARTIO |
|------|------------------------|---------|---------|-----------|---------------------------|-----------|-----------|--------|---------|
| | HCon#0 ^[17] | 320-BGA | 272-BGA | 176-TEQFP | HCon#14 | HCon#29 | HCon#30 | | |
| | I/O Type | Pin | Pin | Pin | DS #0 ^[18, 19] | DS #1 | DS #2 | | |
| P0.0 | GPIO_ENH | A18 | B18 | 2 | | | SCB0_MISO | | |
| P0.1 | GPIO_ENH | B18 | B17 | 3 | | | SCB0_MOSI | | |
| P0.2 | GPIO_ENH | B17 | A17 | 4 | SCB0_SCL | | SCB0_CLK | | |
| P0.3 | GPIO_ENH | C17 | B16 | 5 | SCB0_SDA | | SCB0_SEL0 | | |
| P1.0 | GPIO_STD | A17 | A16 | 6 | SCB0_SCL | | SCB0_MISO | | |
| P1.1 | GPIO_STD | A16 | A15 | 7 | SCB0_SDA | | SCB0_MOSI | | |
| P1.2 | GPIO_STD | B16 | B15 | 8 | | | SCB0_CLK | | |
| P1.3 | GPIO_STD | C16 | C15 | 9 | | | SCB0_SEL0 | | |
| P1.4 | GPIO_STD | C15 | D15 | NA | | | | | |
| P1.5 | GPIO_STD | E15 | NA | NA | | | | | |
| P1.6 | GPIO_STD | F14 | NA | NA | | | | | |
| P2.0 | GPIO_STD | A15 | A14 | 10 | | SWJ_TRSTN | SCB0_SEL1 | | |
| P2.1 | GPIO_STD | B15 | B14 | 11 | | | SCB0_SEL2 | | |
| P2.2 | GPIO_STD | A14 | C14 | 12 | | | SCB0_SEL3 | | |
| P2.3 | GPIO_STD | B14 | D14 | 13 | | | | | |
| P2.4 | GPIO_STD | C14 | B13 | 14 | | | | | |
| P2.5 | GPIO_STD | E14 | C13 | 15 | | | | | |
| P2.6 | GPIO_STD | C13 | D13 | NA | | | | | |
| P2.7 | GPIO_STD | E13 | F12 | NA | | | | | |

Notes

17. HCon refers to High Speed I/O matrix connection reference as per [Table 10-1](#).

18. DeepSleep ordering (DS #0, DS #1, DS #2) does not have any impact on choosing any alternate functions; the HSIOM module handles the individual alternate function assignment.

19. All port pin functions available in DeepSleep mode are also available in Active mode.

Table 11-1. Pin Selector and Alternate Pin Functions in DeepSleep (DS) Mode, Analog, Smart I/O (continued)

| Name | Package | | | | DeepSleep Mapping | | | Analog | SMARTIO |
|------|------------------------|---------|---------|-----------|---------------------------|---------|---------|----------|---------|
| | HCon#0 ^[17] | 320-BGA | 272-BGA | 176-TEQFP | HCon#14 | HCon#29 | HCon#30 | | |
| | I/O Type | Pin | Pin | Pin | DS #0 ^[18, 19] | DS #1 | DS #2 | | |
| P3.0 | GPIO_STD | A13 | A13 | 16 | | | | | |
| P3.1 | GPIO_STD | B13 | A12 | 17 | | | | | |
| P3.2 | GPIO_STD | A12 | B12 | 18 | | | | | |
| P3.3 | GPIO_STD | B12 | C12 | 19 | | | | | |
| P3.4 | GPIO_STD | C12 | D12 | 20 | | | | | |
| P3.5 | GPIO_STD | E12 | B11 | 21 | | | | | |
| P3.6 | GPIO_STD | C11 | C11 | NA | | | | | |
| P3.7 | GPIO_STD | E11 | D11 | NA | | | | | |
| P4.0 | GPIO_STD | A9 | A8 | 24 | | | | | |
| P4.1 | GPIO_STD | A8 | B8 | 25 | | | | | |
| P4.2 | GPIO_STD | B8 | C8 | 26 | | | | | |
| P4.3 | GPIO_STD | C8 | D8 | 27 | | | | | |
| P4.4 | GPIO_STD | E8 | A7 | 28 | | | | | |
| P4.5 | GPIO_STD | A7 | NA | NA | | | | | |
| P4.6 | GPIO_STD | B7 | NA | NA | | | | | |
| P5.0 | GPIO_STD | A5 | A6 | 29 | | | | | |
| P5.1 | GPIO_STD | B5 | B6 | 30 | | | | | |
| P5.2 | GPIO_STD | C5 | C6 | 31 | | | | | |
| P5.3 | GPIO_STD | A4 | D6 | 32 | | | | | |
| P5.4 | GPIO_STD | B4 | C5 | 33 | | | | | |
| P5.5 | GPIO_STD | C4 | D5 | 34 | | | | | |
| P6.0 | GPIO_STD | A3 | B4 | 35 | | | | ADC[0]_0 | |
| P6.1 | GPIO_STD | B3 | C4 | 36 | | | | ADC[0]_1 | |
| P6.2 | GPIO_STD | A2 | A3 | 37 | | | | ADC[0]_2 | |
| P6.3 | GPIO_STD | B1 | B3 | 38 | | | | ADC[0]_3 | |
| P6.4 | GPIO_STD | B2 | C3 | 39 | | | | ADC[0]_4 | |
| P6.5 | GPIO_STD | C1 | A2 | 40 | | | | ADC[0]_5 | |
| P6.6 | GPIO_STD | C2 | B2 | 41 | | | | ADC[0]_6 | |

Table 11-1. Pin Selector and Alternate Pin Functions in DeepSleep (DS) Mode, Analog, Smart I/O (continued)

| Name | Package | | | | DeepSleep Mapping | | | Analog | SMARTIO |
|-------|------------------------|---------|---------|-----------|---------------------------|---------|---------|-----------|---------|
| | HCon#0 ^[17] | 320-BGA | 272-BGA | 176-TEQFP | HCon#14 | HCon#29 | HCon#30 | | |
| | I/O Type | Pin | Pin | Pin | DS #0 ^[18, 19] | DS #1 | DS #2 | | |
| P6.7 | GPIO_STD | D1 | B1 | 42 | | | | ADC[0]_7 | |
| P7.0 | GPIO_STD | F1 | E1 | 48 | | | | ADC[0]_16 | |
| P7.1 | GPIO_STD | F2 | E2 | 49 | | | | ADC[0]_17 | |
| P7.2 | GPIO_STD | G1 | F1 | 50 | | | | ADC[0]_18 | |
| P7.3 | GPIO_STD | G2 | F2 | 51 | | | | ADC[0]_19 | |
| P7.4 | GPIO_STD | G3 | F3 | 52 | | | | ADC[0]_20 | |
| P7.5 | GPIO_STD | G5 | F4 | 53 | | | | ADC[0]_21 | |
| P7.6 | GPIO_STD | G6 | G1 | 54 | | | | ADC[0]_22 | |
| P7.7 | GPIO_STD | H5 | G2 | 55 | | | | ADC[0]_23 | |
| P8.0 | GPIO_STD | H1 | G3 | 56 | | | | | |
| P8.1 | GPIO_STD | H2 | G4 | 57 | | | | ADC[0]_24 | |
| P8.2 | GPIO_STD | H3 | G6 | 58 | | | | ADC[0]_25 | |
| P8.3 | GPIO_STD | J1 | H3 | 59 | | | | ADC[0]_26 | |
| P8.4 | GPIO_STD | J2 | H4 | 60 | | | | ADC[0]_27 | |
| P9.0 | GPIO_STD | K1 | H1 | 61 | | | | ADC[0]_28 | |
| P9.1 | GPIO_STD | K2 | H2 | 62 | | | | ADC[0]_29 | |
| P9.2 | GPIO_STD | J3 | J1 | 63 | | | | ADC[0]_30 | |
| P9.3 | GPIO_STD | J5 | J2 | 64 | | | | ADC[0]_31 | |
| P10.0 | GPIO_STD | K5 | M1 | 65 | | | | | |
| P10.1 | GPIO_STD | L5 | N1 | 66 | | | | | |
| P10.2 | GPIO_STD | M5 | N2 | 67 | | | | | |
| P10.3 | GPIO_STD | N5 | N3 | 68 | | | | | |
| P10.4 | GPIO_STD | R1 | N4 | 69 | | | | ADC[1]_0 | |
| P10.5 | GPIO_STD | R2 | P1 | 70 | | | | ADC[1]_1 | |
| P10.6 | GPIO_STD | R3 | P2 | 71 | | | | ADC[1]_2 | |
| P10.7 | GPIO_STD | T1 | P3 | 72 | | | | ADC[1]_3 | |
| P11.0 | GPIO_STD | P5 | M6 | 73 | | | | ADC[0]_M | |
| P11.1 | GPIO_STD | P6 | P4 | 74 | | | | ADC[1]_M | |

Table 11-1. Pin Selector and Alternate Pin Functions in DeepSleep (DS) Mode, Analog, Smart I/O (continued)

| Name | Package | | | | DeepSleep Mapping | | | Analog | SMARTIO |
|-------|------------------------|---------|---------|-----------|---------------------------|---------|---------|-----------|-------------|
| | HCon#0 ^[17] | 320-BGA | 272-BGA | 176-TEQFP | HCon#14 | HCon#29 | HCon#30 | | |
| | I/O Type | Pin | Pin | Pin | DS #0 ^[18, 19] | DS #1 | DS #2 | | |
| P11.2 | GPIO_STD | R5 | R4 | 75 | | | | ADC[2]_M | |
| P12.0 | GPIO_STD | T2 | R1 | 80 | | | | ADC[1]_4 | SMARTIO12_0 |
| P12.1 | GPIO_STD | T3 | R2 | 81 | | | | ADC[1]_5 | SMARTIO12_1 |
| P12.2 | GPIO_STD | U1 | R3 | 82 | | | | ADC[1]_6 | SMARTIO12_2 |
| P12.3 | GPIO_STD | U2 | T1 | 83 | | | | ADC[1]_7 | SMARTIO12_3 |
| P12.4 | GPIO_STD | U3 | T2 | 84 | | | | ADC[1]_8 | SMARTIO12_4 |
| P12.5 | GPIO_STD | V1 | T3 | 85 | | | | ADC[1]_9 | SMARTIO12_5 |
| P12.6 | GPIO_STD | V2 | U1 | 86 | | | | ADC[1]_10 | SMARTIO12_6 |
| P12.7 | GPIO_STD | W1 | U2 | 87 | | | | ADC[1]_11 | SMARTIO12_7 |
| P13.0 | GPIO_STD | Y2 | V2 | 90 | | | | ADC[1]_12 | SMARTIO13_0 |
| P13.1 | GPIO_STD | W2 | V3 | 91 | | | | ADC[1]_13 | SMARTIO13_1 |
| P13.2 | GPIO_STD | Y3 | U3 | 92 | | | | ADC[1]_14 | SMARTIO13_2 |
| P13.3 | GPIO_STD | W3 | V4 | 93 | | | | ADC[1]_15 | SMARTIO13_3 |
| P13.4 | GPIO_STD | Y4 | U4 | 94 | | | | ADC[1]_16 | SMARTIO13_4 |
| P13.5 | GPIO_STD | W4 | T4 | 95 | | | | ADC[1]_17 | SMARTIO13_5 |
| P13.6 | GPIO_STD | Y5 | U5 | 96 | | | | ADC[1]_18 | SMARTIO13_6 |
| P13.7 | GPIO_STD | W5 | T5 | 97 | | | | ADC[1]_19 | SMARTIO13_7 |
| P14.0 | GPIO_STD | V5 | V5 | 98 | | | | ADC[1]_20 | SMARTIO14_0 |
| P14.1 | GPIO_STD | T5 | V6 | 99 | | | | ADC[1]_21 | SMARTIO14_1 |
| P14.2 | GPIO_STD | Y6 | U6 | 100 | | | | ADC[1]_22 | SMARTIO14_2 |
| P14.3 | GPIO_STD | W6 | T6 | 101 | | | | ADC[1]_23 | SMARTIO14_3 |
| P14.4 | GPIO_STD | V6 | R6 | 102 | | | | ADC[1]_24 | SMARTIO14_4 |
| P14.5 | GPIO_STD | T6 | N7 | 103 | | | | ADC[1]_25 | SMARTIO14_5 |
| P14.6 | GPIO_STD | R7 | T7 | 104 | | | | ADC[1]_26 | SMARTIO14_6 |
| P14.7 | GPIO_STD | T7 | R7 | 105 | | | | ADC[1]_27 | SMARTIO14_7 |
| P15.0 | GPIO_STD | Y7 | V7 | 106 | | | | ADC[1]_28 | SMARTIO15_0 |
| P15.1 | GPIO_STD | W7 | U7 | 107 | | | | ADC[1]_29 | SMARTIO15_1 |
| P15.2 | GPIO_STD | V7 | V8 | 108 | | | | ADC[1]_30 | SMARTIO15_2 |

Table 11-1. Pin Selector and Alternate Pin Functions in DeepSleep (DS) Mode, Analog, Smart I/O (continued)

| Name | Package | | | | DeepSleep Mapping | | | Analog | SMARTIO |
|-------|------------------------|---------|---------|-----------|---------------------------|---------|---------|-----------|-------------|
| | HCon#0 ^[17] | 320-BGA | 272-BGA | 176-TEQFP | HCon#14 | HCon#29 | HCon#30 | | |
| | I/O Type | Pin | Pin | Pin | DS #0 ^[18, 19] | DS #1 | DS #2 | | |
| P15.3 | GPIO_STD | T8 | U8 | 109 | | | | ADC[1]_31 | SMARTIO15_3 |
| P16.0 | GPIO_STD | T9 | V12 | NA | | | | ADC[2]_0 | |
| P16.1 | GPIO_STD | T10 | U12 | NA | | | | ADC[2]_1 | |
| P16.2 | GPIO_STD | T11 | V13 | NA | | | | ADC[2]_2 | |
| P16.3 | GPIO_STD | T12 | U13 | 115 | | | | ADC[2]_3 | |
| P16.4 | GPIO_STD | T13 | T13 | NA | | | | ADC[2]_4 | |
| P16.5 | GPIO_STD | Y12 | R13 | NA | | | | ADC[2]_5 | |
| P16.6 | GPIO_STD | Y13 | T14 | NA | | | | ADC[2]_6 | |
| P16.7 | GPIO_STD | Y14 | N12 | NA | | | | ADC[2]_7 | |
| P17.0 | GPIO_STD | W14 | V14 | 116 | | | | ADC[2]_8 | SMARTIO17_0 |
| P17.1 | GPIO_STD | V14 | U14 | 117 | | | | ADC[2]_9 | SMARTIO17_1 |
| P17.2 | GPIO_STD | T14 | V15 | 118 | | | | ADC[2]_10 | SMARTIO17_2 |
| P17.3 | GPIO_STD | R14 | U15 | 119 | | | | ADC[2]_11 | SMARTIO17_3 |
| P17.4 | GPIO_STD | Y15 | T15 | 120 | | | | ADC[2]_12 | SMARTIO17_4 |
| P17.5 | GPIO_STD | W15 | V16 | 121 | | | | ADC[2]_13 | SMARTIO17_5 |
| P17.6 | GPIO_STD | Y16 | U16 | 122 | | | | ADC[2]_14 | SMARTIO17_6 |
| P17.7 | GPIO_STD | W16 | V17 | 123 | | | | ADC[2]_15 | SMARTIO17_7 |
| P18.0 | GPIO_STD | V16 | U18 | 124 | | | | ADC[2]_16 | |
| P18.1 | GPIO_STD | Y17 | U17 | 125 | | | | ADC[2]_17 | |
| P18.2 | GPIO_STD | W17 | T18 | 126 | | | | ADC[2]_18 | |
| P18.3 | GPIO_STD | Y18 | T17 | 127 | | | | ADC[2]_19 | |
| P18.4 | GPIO_STD | Y19 | T16 | 128 | | | | ADC[2]_20 | |
| P18.5 | GPIO_STD | T15 | R16 | 129 | | | | ADC[2]_21 | |
| P18.6 | GPIO_STD | T16 | R15 | 130 | | | | ADC[2]_22 | |
| P18.7 | GPIO_STD | R16 | P15 | 131 | | | | ADC[2]_23 | |
| P19.0 | GPIO_STD | P19 | R18 | 134 | | | | ADC[2]_24 | |
| P19.1 | GPIO_STD | P18 | R17 | 135 | | | | ADC[2]_25 | |
| P19.2 | GPIO_STD | P16 | P17 | 136 | | | | ADC[2]_26 | |

Table 11-1. Pin Selector and Alternate Pin Functions in DeepSleep (DS) Mode, Analog, Smart I/O (continued)

| Name | Package | | | | DeepSleep Mapping | | | Analog | SMARTIO |
|-------|------------------------|---------|---------|-----------|---------------------------|---------|---------|-------------------------------------|---------|
| | HCon#0 ^[17] | 320-BGA | 272-BGA | 176-TEQFP | HCon#14 | HCon#29 | HCon#30 | | |
| | I/O Type | Pin | Pin | Pin | DS #0 ^[18, 19] | DS #1 | DS #2 | | |
| P19.3 | GPIO_STD | P15 | P16 | 137 | | | | ADC[2]_27 | |
| P19.4 | GPIO_STD | N16 | N15 | 138 | | | | ADC[2]_28 | |
| P20.0 | GPIO_STD | N18 | N16 | 139 | | | | ADC[2]_29 | |
| P20.1 | GPIO_STD | M18 | M16 | 140 | | | | ADC[2]_30 | |
| P20.2 | GPIO_STD | M16 | M15 | 141 | | | | ADC[2]_31 | |
| P20.3 | GPIO_STD | L19 | M13 | 142 | | | | | |
| P20.4 | GPIO_STD | L18 | L16 | 143 | | | | | |
| P20.5 | GPIO_STD | L16 | L15 | 144 | | | | | |
| P20.6 | GPIO_STD | K16 | K16 | 145 | | | | | |
| P20.7 | GPIO_STD | J16 | K15 | 146 | | | | | |
| P21.0 | GPIO_STD | N19 | N17 | 147 | | | | WCO_IN ^[20] | |
| P21.1 | GPIO_STD | N20 | N18 | 148 | | | | WCO_OUT ^[20] | |
| P21.2 | GPIO_STD | M19 | M17 | 149 | | | | ECO_IN ^[20] | |
| P21.3 | GPIO_STD | M20 | M18 | 150 | | | | ECO_OUT ^[20] | |
| P21.4 | GPIO_STD | K19 | L17 | 151 | | | | HIBERNATE_WAKEUP[0] ^[21] | |
| P21.5 | GPIO_STD | J19 | K17 | 157 | | | | | |
| P21.6 | GPIO_STD | H19 | J17 | 158 | | | | | |
| P21.7 | GPIO_STD | H18 | J16 | 159 | | RTC_CAL | | | |
| P22.1 | GPIO_STD | H20 | H18 | 161 | | | | EXT_PS_CTL0 | |
| P22.2 | GPIO_STD | G20 | G18 | 162 | | | | EXT_PS_CTL1 | |
| P22.3 | GPIO_STD | F20 | F18 | 163 | | | | EXT_PS_CTL2 | |
| P22.4 | GPIO_STD | G19 | H17 | 164 | | | | | |
| P22.5 | GPIO_STD | G18 | H16 | 165 | | | | | |
| P22.6 | GPIO_STD | H16 | H15 | 166 | | | | | |
| P22.7 | GPIO_STD | G16 | G17 | 167 | | | | | |

Notes

20. I/O pins that support an oscillator function (WCO or ECO) must be configured for high-impedance if the oscillator is enabled.

 21. This I/O has increased leakage to ground when the V_{DD} supply is below the POR threshold.

Table 11-1. Pin Selector and Alternate Pin Functions in DeepSleep (DS) Mode, Analog, Smart I/O (continued)

| Name | Package | | | | DeepSleep Mapping | | | Analog | SMARTIO |
|-------|------------------------|---------|---------|-----------|---------------------------|----------------|---------|---------------------|---------|
| | HCon#0 ^[17] | 320-BGA | 272-BGA | 176-TEQFP | HCon#14 | HCon#29 | HCon#30 | | |
| | I/O Type | Pin | Pin | Pin | DS #0 ^[18, 19] | DS #1 | DS #2 | | |
| P23.0 | GPIO_STD | F19 | G16 | 168 | | | | | |
| P23.1 | GPIO_STD | F18 | G15 | 169 | | | | | |
| P23.2 | GPIO_STD | E20 | G13 | 170 | | | | | |
| P23.3 | GPIO_STD | E19 | F17 | 171 | | | | | |
| P23.4 | GPIO_STD | E18 | F16 | 172 | | SWJ_SWO_TDO | | | |
| P23.5 | GPIO_STD | D20 | F15 | 173 | | SWJ_SWCLK_TCLK | | | |
| P23.6 | GPIO_STD | F16 | E18 | 174 | | SWJ_SWDIO_TMS | | | |
| P23.7 | GPIO_STD | G15 | E17 | 175 | | SWJ_SWDOE_TDI | | HIBERNATE_WAKEUP[1] | |
| P24.0 | HSIO_STD | K3 | J3 | NA | | | | | |
| P24.1 | HSIO_STD | L1 | J4 | NA | | | | | |
| P24.2 | HSIO_STD | L2 | K1 | NA | | | | | |
| P24.3 | HSIO_STD | L3 | K2 | NA | | | | | |
| P24.4 | HSIO_STD | M1 | K3 | NA | | | | | |
| P25.0 | HSIO_STD | M2 | K4 | NA | | | | | |
| P25.1 | HSIO_STD | M3 | L1 | NA | | | | | |
| P25.2 | HSIO_STD | N1 | L2 | NA | | | | | |
| P25.3 | HSIO_STD | N2 | L3 | NA | | | | | |
| P25.4 | HSIO_STD | N3 | L4 | NA | | | | | |
| P25.5 | HSIO_STD | P1 | M2 | NA | | | | | |
| P25.6 | HSIO_STD | P2 | M3 | NA | | | | | |
| P25.7 | HSIO_STD | P3 | M4 | NA | | | | | |
| P26.0 | HSIO_STD | Y8 | T8 | NA | | | | | |
| P26.1 | HSIO_STD | W8 | R8 | NA | | | | | |
| P26.2 | HSIO_STD | V8 | V9 | NA | | | | | |
| P26.3 | HSIO_STD | Y9 | U9 | NA | | | | | |
| P26.4 | HSIO_STD | W9 | T9 | NA | | | | | |
| P26.5 | HSIO_STD | V9 | R9 | NA | | | | | |
| P26.6 | HSIO_STD | Y10 | V10 | NA | | | | | |

Table 11-1. Pin Selector and Alternate Pin Functions in DeepSleep (DS) Mode, Analog, Smart I/O (continued)

| Name | Package | | | | DeepSleep Mapping | | | Analog | SMARTIO |
|-------|------------------------|---------|---------|-----------|---------------------------|---------|---------|--------|---------|
| | HCon#0 ^[17] | 320-BGA | 272-BGA | 176-TEQFP | HCon#14 | HCon#29 | HCon#30 | | |
| | I/O Type | Pin | Pin | Pin | DS #0 ^[18, 19] | DS #1 | DS #2 | | |
| P26.7 | HSIO_STD | W10 | U10 | NA | | | | | |
| P27.0 | HSIO_STD | V10 | T10 | NA | | | | | |
| P27.1 | HSIO_STD | Y11 | R10 | NA | | | | | |
| P27.2 | HSIO_STD | W11 | V11 | NA | | | | | |
| P27.3 | HSIO_STD | V11 | U11 | NA | | | | | |
| P27.4 | HSIO_STD | W12 | T11 | NA | | | | | |
| P27.5 | HSIO_STD | V12 | R11 | NA | | | | | |
| P27.6 | HSIO_STD | W13 | T12 | NA | | | | | |
| P27.7 | HSIO_STD | V13 | R12 | NA | | | | | |
| P28.0 | GPIO_STD | E16 | E16 | NA | | | | | |
| P28.1 | GPIO_STD | D19 | E15 | NA | | | | | |
| P28.2 | GPIO_STD | D18 | D18 | NA | | | | | |
| P28.3 | GPIO_STD | C20 | D17 | NA | | | | | |
| P28.4 | GPIO_STD | C19 | D16 | NA | | | | | |
| P28.5 | GPIO_STD | B20 | C18 | NA | | | | | |
| P28.6 | GPIO_STD | B19 | C17 | NA | | | | | |
| P28.7 | GPIO_STD | A19 | C16 | NA | | | | | |
| P29.0 | GPIO_STD | A11 | A11 | NA | | | | | |
| P29.1 | GPIO_STD | B11 | A10 | NA | | | | | |
| P29.2 | GPIO_STD | A10 | B10 | NA | | | | | |
| P29.3 | GPIO_STD | B10 | C10 | NA | | | | | |
| P29.4 | GPIO_STD | E10 | D10 | NA | | | | | |
| P29.5 | GPIO_STD | B9 | A9 | NA | | | | | |
| P29.6 | GPIO_STD | C9 | B9 | NA | | | | | |
| P29.7 | GPIO_STD | E9 | C9 | NA | | | | | |
| P30.0 | GPIO_STD | C7 | B7 | NA | | | | | |
| P30.1 | GPIO_STD | A6 | C7 | NA | | | | | |
| P30.2 | GPIO_STD | B6 | D7 | NA | | | | | |

Table 11-1. Pin Selector and Alternate Pin Functions in DeepSleep (DS) Mode, Analog, Smart I/O (continued)

| Name | Package | | | DeepSleep Mapping | | | Analog | SMARTIO | |
|-------|------------------------|---------|---------|-------------------|---------------------------|---------|-----------|---------|---------|
| | HCon#0 ^[17] | 320-BGA | 272-BGA | 176-TEQFP | HCon#14 | HCon#29 | | | HCon#30 |
| | I/O Type | Pin | Pin | Pin | DS #0 ^[18, 19] | DS #1 | | | DS #2 |
| P30.3 | GPIO_STD | C6 | F7 | NA | | | | | |
| P31.0 | GPIO_STD | E7 | A5 | NA | | | | | |
| P31.1 | GPIO_STD | F7 | B5 | NA | | | | | |
| P31.2 | GPIO_STD | E6 | A4 | NA | | | | | |
| P32.0 | GPIO_STD | D2 | C1 | NA | | | ADC[0]_8 | | |
| P32.1 | GPIO_STD | D3 | C2 | NA | | | ADC[0]_9 | | |
| P32.2 | GPIO_STD | E5 | D1 | NA | | | ADC[0]_10 | | |
| P32.3 | GPIO_STD | E1 | D2 | NA | | | ADC[0]_11 | | |
| P32.4 | GPIO_STD | E2 | D3 | NA | | | ADC[0]_12 | | |
| P32.5 | GPIO_STD | E3 | D4 | NA | | | ADC[0]_13 | | |
| P32.6 | GPIO_STD | F3 | E3 | NA | | | ADC[0]_14 | | |
| P32.7 | GPIO_STD | F5 | E4 | NA | | | ADC[0]_15 | | |
| P33.0 | HSIO_STD | W18 | NA | NA | | | | | |
| P33.1 | HSIO_STD | V17 | NA | NA | | | | | |
| P33.2 | HSIO_STD | W19 | NA | NA | | | | | |
| P33.3 | HSIO_STD | V18 | NA | NA | | | | | |
| P33.4 | HSIO_STD | W20 | NA | NA | | | | | |
| P33.5 | HSIO_STD | V20 | NA | NA | | | | | |
| P33.6 | HSIO_STD | V19 | NA | NA | | | | | |
| P33.7 | HSIO_STD | U20 | NA | NA | | | | | |
| P34.0 | HSIO_STD | U19 | NA | NA | | | | | |
| P34.1 | HSIO_STD | U18 | NA | NA | | | | | |
| P34.2 | HSIO_STD | T20 | NA | NA | | | | | |
| P34.3 | HSIO_STD | T19 | NA | NA | | | | | |
| P34.4 | HSIO_STD | T18 | NA | NA | | | | | |
| P34.5 | HSIO_STD | R20 | NA | NA | | | | | |
| P34.6 | HSIO_STD | R19 | NA | NA | | | | | |
| P34.7 | HSIO_STD | R18 | NA | NA | | | | | |

11.1 Power Pin Assignments

Table 11-2. Power Pin Assignments

| Pin Name | Package | | | Remarks |
|----------------------|--|--|-----------------------------------|---|
| | 320-BGA | 272-BGA | 176-TEQFP | |
| VDDD | F8, F9, H15, J15, K15, L15, M15, N15, R12, R13 | F8, H13, J13, K13, L13, N11 | 176, 153, 132, 110, 43, 22 | Main digital supply |
| VSSD | A1, A20, C3, C10, C18, H9, H10, H11, H12, H13, J9, J10, J11, J12, J13, J18, K9, K10, K11, K12, K13, K18, L9, L10, L11, L12, L13, M9, M10, M11, M12, M13, N12, V3, V4, V15, Y1, Y20 | A1, A18, D9, G7, G12, H9, H10, H11, J9, J10, J11, J15, K9, K10, K11, M7, M12, R5, R14, V1, V18 | 155, 154, 133, 114, 89, 45, 23, 1 | Main digital ground |
| VSSD_1 | N13 | L11 | NA | Digital Ground |
| VSSD_2 | L20, P20 | L18, P18 | NA | Noise guard for ECO inputs |
| VDDIO_1 | F10, F11, F12, F13 | F9, F10, F11 | 44 | I/O supply (except analog I/Os on V _{DDA}) |
| VDDIO_2 | R8 | N8 | 88 | I/O supply (except analog I/Os on V _{DDA}) |
| VDDIO_3 | H6, J6, K6, L6 | H6, J6 | NA | I/O supply for high speed domain#0 (HSIO_STD), P24, P25 |
| VDDIO_4 | R9, R10, R11 | N9, N10 | NA | I/O supply for high speed domain#1 (HSIO_STD), P26, P27, P33, P34 |
| VSSIO_3 | H8, J8, K8, L8 | H8, J8 | NA | HSIO ground |
| VSSIO_4 | N9, N10, N11 | L9, L10 | NA | HSIO ground |
| VCCD ^[22] | F6, F15, R6, R15 | F6, F13, N6, N13 | 46, 47, 111, 112, 113, 156 | Main regulated supply. Driven by LDO regulator (either internal LDO or external LDO/PMIC) |
| VREFH | M6 | K6 | 79 | High reference voltage for SAR ADCs |
| VREFL | M8 | K8 | 76 | Low reference voltage for SAR ADCs |
| VDDA | N6 | L6 | 78 | Main analog supply for SAR ADCs |
| VSSA | N8 | L8 | 77 | Main analog ground |
| XRES_L | K20 | K18 | 152 | Active LOW external reset input |
| DRV_VOUT | J20 | J18 | 160 | Dedicated external supply control pin |

Note

²². The V_{CCD} pins must be connected together to ensure a low-impedance connection. (see the requirement in Figure 25-2.)

12. Alternate Function Pin Assignments

Table 12-1. Alternate Pin Functions in Active Mode^[19, 25]

| Pin | Active Mapping | | | | | | | | | | | | | | | | |
|------|------------------------|-----------|-------------|------------|-------------|----------|----------|-----------|-----------|-----------|-------------|---------|----------------------------|---------|---------|------------|--------------|
| | HCon#8 ^[23] | HCon#9 | HCon#10 | HCon#11 | HCon#16 | HCon#17 | HCon#18 | HCon#19 | HCon#20 | HCon#21 | HCon#22 | HCon#23 | HCon#24 | HCon#25 | HCon#26 | HCon#27 | |
| Name | ACT #0 ^[24] | ACT #1 | ACT #2 | ACT #3 | ACT #4 | ACT #5 | ACT #6 | ACT #7 | ACT #8 | ACT #9 | ACT #10 | ACT #11 | ACT #12 | ACT #13 | ACT #14 | ACT #15 | |
| P0.0 | PWM1_18 | PWM1_22_N | TC1_18_TR0 | TC1_22_TR1 | | SCB0_RX | SCB7_SDA | | LIN1_RX | | PWM0_H_0 | | | | | | |
| P0.1 | PWM1_17 | PWM1_18_N | TC1_17_TR0 | TC1_18_TR1 | | SCB0_TX | SCB7_SCL | | LIN1_TX | | PWM0_H_0_N | | | | | | |
| P0.2 | PWM1_14 | PWM1_17_N | TC1_14_TR0 | TC1_17_TR1 | | SCB0_RTS | | SCB4_MISO | LIN1_EN | CAN0_1_TX | TC0_H_0_TR0 | | | | | | |
| P0.3 | PWM1_13 | PWM1_14_N | TC1_13_TR0 | TC1_14_TR1 | | SCB0_CTS | | SCB4_MOSI | | CAN0_1_RX | TC0_H_0_TR1 | | | | | | |
| P1.0 | PWM1_12 | PWM1_13_N | TC1_12_TR0 | TC1_13_TR1 | PWM1_H_4 | | | SCB4_CLK | | | | | | | | | |
| P1.1 | PWM1_11 | PWM1_12_N | TC1_11_TR0 | TC1_12_TR1 | PWM1_H_5 | | | SCB4_MISO | | | | | | | | | |
| P1.2 | PWM1_10 | PWM1_11_N | TC1_10_TR0 | TC1_11_TR1 | PWM1_H_6 | | | | LIN0_RX | | | | | | | TRIG_IN[0] | |
| P1.3 | PWM1_8 | PWM1_10_N | TC1_8_TR0 | TC1_10_TR1 | PWM1_H_7 | | | | LIN0_TX | | | | | | | | TRIG_IN[1] |
| P1.4 | PWM1_71 | PWM1_70_N | TC1_71_TR0 | TC1_70_TR1 | | | SCB8_RX | | SCB8_MISO | | | LIN8_RX | | | | | |
| P1.5 | | | | | | | SCB8_TX | SCB8_SDA | SCB8_MOSI | | | LIN8_TX | | | | | |
| P1.6 | | | | | | | SCB8_RTS | SCB8_SCL | SCB8_CLK | | | LIN8_EN | | | | | |
| P2.0 | PWM1_7 | PWM1_8_N | TC1_7_TR0 | TC1_8_TR1 | TC1_H_4_TR0 | SCB7_RX | | SCB7_MISO | LIN0_RX | CAN0_0_TX | | | | | | | TRIG_IN[2] |
| P2.1 | PWM1_6 | PWM1_7_N | TC1_6_TR0 | TC1_7_TR1 | TC1_H_5_TR0 | SCB7_TX | SCB7_SDA | SCB7_MOSI | LIN0_TX | CAN0_0_RX | | | | | | | TRIG_IN[3] |
| P2.2 | PWM1_5 | PWM1_6_N | TC1_5_TR0 | TC1_6_TR1 | TC1_H_6_TR0 | SCB7_RTS | SCB7_SCL | SCB7_CLK | LIN0_EN | | | | ETH0_RX_ER | | | | TRIG_IN[4] |
| P2.3 | PWM1_4 | PWM1_5_N | TC1_4_TR0 | TC1_5_TR1 | TC1_H_7_TR0 | SCB7_CTS | | SCB7_SEL0 | LIN5_RX | | | | ETH0_ETH_TSU_TIMER_CMP_VAL | | | | TRIG_IN[5] |
| P2.4 | PWM1_3 | PWM1_4_N | TC1_3_TR0 | TC1_4_TR1 | PWM1_H_4_N | | | SCB7_SEL1 | LIN5_TX | | | | | | | | TRIG_IN[6] |
| P2.5 | PWM1_2 | PWM1_3_N | TC1_2_TR0 | TC1_3_TR1 | PWM1_H_5_N | | | SCB7_SEL2 | LIN5_EN | | | | | | | | TRIG_IN[7] |
| P2.6 | PWM1_72 | PWM1_71_N | TC1_72_TR0 | TC1_71_TR1 | | SCB8_CTS | | SCB8_SEL0 | | | | | | | | | |
| P2.7 | PWM1_73 | PWM1_72_N | TC1_73_TR0 | TC1_72_TR1 | | | | SCB8_SEL1 | LIN11_RX | | | | | | | | |
| P3.0 | PWM1_1 | PWM1_2_N | TC1_1_TR0 | TC1_2_TR1 | PWM1_H_6_N | SCB6_RX | | SCB6_MISO | | CAN0_3_TX | | | ETH0_MDIO | | | | TRIG_DBG [0] |
| P3.1 | PWM1_0 | PWM1_1_N | TC1_0_TR0 | TC1_1_TR1 | PWM1_H_7_N | SCB6_TX | SCB6_SDA | SCB6_MOSI | | CAN0_3_RX | | | ETH0_MDC | | | | TRIG_DBG [1] |
| P3.2 | PWM1_M_3 | PWM1_0_N | TC1_M_3_TR0 | TC1_0_TR1 | TC1_H_4_TR1 | SCB6_RTS | SCB6_SCL | SCB6_CLK | | | | | | | | | |

Notes

23. High Speed I/O matrix connection (HCon) reference as per Table 10-1.

24. Active Mode ordering (ACT #0, ACT #1, and so on) does not have any impact on configuring alternate functions; the HSIOM module handles the alternate function assignments.

25. Refer to Table 12-2 for more information on pin multiplexer abbreviations used.

Table 12-1. Alternate Pin Functions in Active Mode (continued)^[19, 25]

| Pin | Active Mapping | | | | | | | | | | | | | | | |
|------|------------------------|------------|-------------|-------------|----------------|----------|----------|-----------|----------|-----------|-------------|------------|---------|----------------------------|---------|-------------|
| | HCon#8 ^[23] | HCon#9 | HCon#10 | HCon#11 | HCon#16 | HCon#17 | HCon#18 | HCon#19 | HCon#20 | HCon#21 | HCon#22 | HCon#23 | HCon#24 | HCon#25 | HCon#26 | HCon#27 |
| Name | ACT #0 ^[24] | ACT #1 | ACT #2 | ACT #3 | ACT #4 | ACT #5 | ACT #6 | ACT #7 | ACT #8 | ACT #9 | ACT #10 | ACT #11 | ACT #12 | ACT #13 | ACT #14 | ACT #15 |
| P3.3 | PWM1_M_2 | PWM1_M_3_N | TC1_M_2_TR0 | TC1_M_3_TR1 | TC1_H_5_TR1 | SCB6_CTS | | SCB6_SEL0 | | | | | | | | |
| P3.4 | PWM1_M_1 | PWM1_M_2_N | TC1_M_1_TR0 | TC1_M_2_TR1 | TC1_H_6_TR1 | | | SCB6_SEL1 | LIN1_RX | | | | | | | |
| P3.5 | PWM1_M_0 | PWM1_M_1_N | TC1_M_0_TR0 | TC1_M_1_TR1 | TC1_H_7_TR1 | | | SCB6_SEL2 | LIN1_TX | | | | | | | |
| P3.6 | PWM1_74 | PWM1_73_N | TC1_74_TR0 | TC1_73_TR1 | | | | SCB8_SEL2 | LIN11_TX | CAN1_2_TX | | | | | | |
| P3.7 | PWM1_75 | PWM1_74_N | TC1_75_TR0 | TC1_74_TR1 | | | | | LIN11_EN | CAN1_2_RX | | | | | | |
| P4.0 | PWM1_4 | PWM1_M_0_N | TC1_4_TR0 | TC1_M_0_TR1 | EXT_MUX[0]_0 | SCB5_RX | | SCB5_MISO | LIN1_RX | | | | | | | TRIG_IN[10] |
| P4.1 | PWM1_5 | PWM1_4_N | TC1_5_TR0 | TC1_4_TR1 | EXT_MUX[0]_1 | SCB5_TX | SCB5_SDA | SCB5_MOSI | LIN1_TX | | | | | | | TRIG_IN[11] |
| P4.2 | PWM1_6 | PWM1_5_N | TC1_6_TR0 | TC1_5_TR1 | EXT_MUX[0]_2 | SCB5_RTS | SCB5_SCL | SCB5_CLK | LIN1_EN | | | | | | | TRIG_IN[12] |
| P4.3 | PWM1_7 | PWM1_6_N | TC1_7_TR0 | TC1_6_TR1 | EXT_MUX[0]_E_N | SCB5_CTS | | SCB5_SEL0 | | CAN0_1_TX | | | | | | TRIG_IN[13] |
| P4.4 | PWM1_8 | PWM1_7_N | TC1_8_TR0 | TC1_7_TR1 | | | LIN15_RX | SCB5_SEL1 | | CAN0_1_RX | | | | | | |
| P4.5 | | | | | | SCB9_RX | | SCB9_MISO | | | | | | | | TRIG_IN[32] |
| P4.6 | | | | | | SCB9_TX | SCB9_SDA | SCB9_MOSI | | | | | | | | TRIG_IN[33] |
| P5.0 | PWM1_9 | PWM1_8_N | TC1_9_TR0 | TC1_8_TR1 | PWM1_H_10 | | LIN15_TX | SCB5_SEL2 | LIN7_RX | | PWM0_M_0 | | | | | TRIG_IN[38] |
| P5.1 | PWM1_10 | PWM1_9_N | TC1_10_TR0 | TC1_9_TR1 | PWM1_H_10_N | | | SCB9_SEL3 | LIN7_TX | | PWM0_M_0_N | | | | | TRIG_IN[39] |
| P5.2 | PWM1_11 | PWM1_10_N | TC1_11_TR0 | TC1_10_TR1 | TC1_H_10_TR0 | | LIN10_RX | | LIN7_EN | | TC0_M_0_TR0 | | | | | |
| P5.3 | PWM1_12 | PWM1_11_N | TC1_12_TR0 | TC1_11_TR1 | TC1_H_10_TR1 | | LIN10_TX | | LIN2_RX | | TC0_M_0_TR1 | | | | | |
| P5.4 | PWM1_13 | PWM1_12_N | TC1_13_TR0 | TC1_12_TR1 | PWM1_H_11 | | | | LIN2_TX | | | LIN9_RX | | | | |
| P5.5 | PWM1_14 | PWM1_13_N | TC1_14_TR0 | TC1_13_TR1 | PWM1_H_11_N | | | | LIN2_EN | | | LIN9_TX | | | | |
| P6.0 | PWM1_M_0 | PWM1_14_N | TC1_M_0_TR0 | TC1_14_TR1 | TC1_H_11_TR0 | SCB4_RX | | SCB4_MISO | LIN3_RX | | PWM0_0 | LIN9_EN | | | | |
| P6.1 | PWM1_0 | PWM1_M_0_N | TC1_0_TR0 | TC1_M_0_TR1 | TC1_H_11_TR1 | SCB4_TX | SCB4_SDA | SCB4_MOSI | LIN3_TX | | | | | | | |
| P6.2 | PWM1_M_1 | PWM1_0_N | TC1_M_1_TR0 | TC1_0_TR1 | PWM1_H_12 | SCB4_RTS | SCB4_SCL | SCB4_CLK | LIN3_EN | CAN0_2_TX | PWM0_0_N | | | SDHC_CARD_MEC_H_WRITE_PROT | | |
| P6.3 | PWM1_1 | PWM1_M_1_N | TC1_1_TR0 | TC1_M_1_TR1 | PWM1_H_12_N | SCB4_CTS | | SCB4_SEL0 | LIN4_RX | CAN0_2_RX | | SPIHB_CLK | | SDHC_CARD_CMD | | CAL_SUP_NZ |
| P6.4 | PWM1_M_2 | PWM1_1_N | TC1_M_2_TR0 | TC1_1_TR1 | TC1_H_12_TR0 | | | SCB4_SEL1 | LIN4_TX | | TC0_0_TR0 | SPIHB_RWDS | | SDHC_CLK_CARD | | |

Table 12-1. Alternate Pin Functions in Active Mode (continued)^[19, 25]

| Pin | Active Mapping | | | | | | | | | | | | | | | |
|-------|------------------------|------------|-------------|-------------|--------------|----------|----------|-----------|----------|-----------|-------------|-------------|---------|-----------------------|--------------|-------------|
| | HCon#8 ^[23] | HCon#9 | HCon#10 | HCon#11 | HCon#16 | HCon#17 | HCon#18 | HCon#19 | HCon#20 | HCon#21 | HCon#22 | HCon#23 | HCon#24 | HCon#25 | HCon#26 | HCon#27 |
| Name | ACT #0 ^[24] | ACT #1 | ACT #2 | ACT #3 | ACT #4 | ACT #5 | ACT #6 | ACT #7 | ACT #8 | ACT #9 | ACT #10 | ACT #11 | ACT #12 | ACT #13 | ACT #14 | ACT #15 |
| P6.5 | PWM1_2 | PWM1_M_2_N | TC1_2_TR0 | TC1_M_2_TR1 | TC1_H_12_TR1 | | | SCB4_SEL2 | LIN4_EN | | TC0_0_TR1 | SPIHB_SEL0 | | SDHC_CARD_DETECT_N | | |
| P6.6 | PWM1_M_3 | PWM1_2_N | TC1_M_3_TR0 | TC1_2_TR1 | | | | SCB4_SEL3 | | | | | | | TRIG_IN[8] | |
| P6.7 | PWM1_3 | PWM1_M_3_N | TC1_3_TR0 | TC1_M_3_TR1 | | | | | | | | | | | TRIG_IN[9] | |
| P7.0 | PWM1_M_4 | PWM1_3_N | TC1_M_4_TR0 | TC1_3_TR1 | | SCB5_RX | | SCB5_MISO | LIN4_RX | | PWM0_1 | SPIHB_SEL1 | | SDHC_CARD_IF_PWR_EN | | |
| P7.1 | PWM1_15 | PWM1_M_4_N | TC1_15_TR0 | TC1_M_4_TR1 | | SCB5_TX | SCB5_SDA | SCB5_MOSI | LIN4_TX | | | SPIHB_DATA0 | | SDHC_CARD_DATA_3TO0_0 | | |
| P7.2 | PWM1_M_5 | PWM1_15_N | TC1_M_5_TR0 | TC1_15_TR1 | | SCB5_RTS | SCB5_SCL | SCB5_CLK | LIN4_EN | | PWM0_1_N | SPIHB_DATA1 | | SDHC_CARD_DATA_3TO0_1 | | |
| P7.3 | PWM1_16 | PWM1_M_5_N | TC1_16_TR0 | TC1_M_5_TR1 | | SCB5_CTS | | | | CAN0_4_TX | TC0_1_TR0 | SPIHB_DATA2 | | SDHC_CARD_DATA_3TO0_2 | | |
| P7.4 | PWM1_M_6 | PWM1_16_N | TC1_M_6_TR0 | TC1_16_TR1 | | | | SCB5_SEL1 | | CAN0_4_RX | TC0_1_TR1 | SPIHB_DATA3 | | SDHC_CARD_DATA_3TO0_3 | | |
| P7.5 | PWM1_17 | PWM1_M_6_N | TC1_17_TR0 | TC1_M_6_TR1 | | | LIN10_RX | SCB5_SEL2 | | | PWM0_H_2 | SPIHB_DATA4 | | SDHC_CARD_DATA_7TO4_0 | | |
| P7.6 | PWM1_M_7 | PWM1_17_N | TC1_M_7_TR0 | TC1_17_TR1 | | | LIN10_TX | | | | | | | | TRIG_IN[16] | |
| P7.7 | PWM1_18 | PWM1_M_7_N | TC1_18_TR0 | TC1_M_7_TR1 | | | LIN10_EN | | | | | | | | TRIG_IN[17] | |
| P8.0 | PWM1_19 | PWM1_18_N | TC1_19_TR0 | TC1_18_TR1 | PWM1_H_8 | | | | LIN2_RX | CAN0_0_TX | PWM0_H_2_N | SPIHB_DATA5 | | SDHC_CARD_DATA_7TO4_1 | | |
| P8.1 | PWM1_20 | PWM1_19_N | TC1_20_TR0 | TC1_19_TR1 | PWM1_H_8_N | | | | LIN2_TX | CAN0_0_RX | TC0_H_2_TR0 | SPIHB_DATA6 | | SDHC_CARD_DATA_7TO4_2 | TRIG_IN[14] | |
| P8.2 | PWM1_21 | PWM1_20_N | TC1_21_TR0 | TC1_20_TR1 | TC1_H_8_TR0 | | | | LIN2_EN | | TC0_H_2_TR1 | SPIHB_DATA7 | | SDHC_CARD_DATA_7TO4_3 | TRIG_IN[15] | |
| P8.3 | PWM1_22 | PWM1_21_N | TC1_22_TR0 | TC1_21_TR1 | TC1_H_8_TR1 | | | | LIN16_RX | | | | | | | TRIG_DBG[0] |
| P8.4 | PWM1_23 | PWM1_22_N | TC1_23_TR0 | TC1_22_TR1 | | | | | LIN16_TX | | | | | | | TRIG_DBG[1] |
| P9.0 | PWM1_24 | PWM1_23_N | TC1_24_TR0 | TC1_23_TR1 | PWM1_H_9 | | | | LIN16_EN | | | | | | | |
| P9.1 | PWM1_25 | PWM1_24_N | TC1_25_TR0 | TC1_24_TR1 | PWM1_H_9_N | | | | | LIN12_RX | | | | | | |
| P9.2 | PWM1_26 | PWM1_25_N | TC1_26_TR0 | TC1_25_TR1 | TC1_H_9_TR0 | | | | | LIN12_TX | | | | | | |
| P9.3 | PWM1_27 | PWM1_26_N | TC1_27_TR0 | TC1_26_TR1 | TC1_H_9_TR1 | | | | | LIN12_EN | | | | | | |
| P10.0 | PWM1_28 | PWM1_27_N | TC1_28_TR0 | TC1_27_TR1 | PWM1_H_10 | SCB4_RX | | SCB4_MISO | LIN7_RX | | | | | | TRIG_IN[18] | |
| P10.1 | PWM1_29 | PWM1_28_N | TC1_29_TR0 | TC1_28_TR1 | PWM1_H_10_N | SCB4_TX | SCB4_SDA | SCB4_MOSI | LIN7_TX | | | | | | TRIG_IN[19] | |
| P10.2 | PWM1_30 | PWM1_29_N | TC1_30_TR0 | TC1_29_TR1 | TC1_H_10_TR0 | SCB4_RTS | SCB4_SCL | SCB4_CLK | | | LIN8_RX | | | | FLEXRAY_RXDA | |

Table 12-1. Alternate Pin Functions in Active Mode (continued)^[19, 25]

| Pin | Active Mapping | | | | | | | | | | | | | | | |
|-------|------------------------|-------------|--------------|--------------|---------------|----------|------------|------------|---------|-----------|-------------|-----------|---------|---------------------|-----------------|---------|
| | HCon#8 ^[23] | HCon#9 | HCon#10 | HCon#11 | HCon#16 | HCon#17 | HCon#18 | HCon#19 | HCon#20 | HCon#21 | HCon#22 | HCon#23 | HCon#24 | HCon#25 | HCon#26 | HCon#27 |
| Name | ACT #0 ^[24] | ACT #1 | ACT #2 | ACT #3 | ACT #4 | ACT #5 | ACT #6 | ACT #7 | ACT #8 | ACT #9 | ACT #10 | ACT #11 | ACT #12 | ACT #13 | ACT #14 | ACT #15 |
| P10.3 | PWM1_31 | PWM1_30_N | TC1_31_TR0 | TC1_30_TR1 | TC1_H_10_TR1 | SCB4_CTS | | SCB4_SEL0 | | | LIN8_TX | | | | FLEXRAY_TXDA | |
| P10.4 | PWM1_32 | PWM1_31_N | TC1_32_TR0 | TC1_31_TR1 | PWM1_H_11 | | | SCB4_SEL1 | | | LIN8_EN | | | | FLEXRAY_TXENA_N | |
| P10.5 | PWM1_33 | PWM1_32_N | TC1_33_TR0 | TC1_32_TR1 | PWM1_H_11_N | | | SCB4_SEL2 | | LIN13_RX | | | | | FLEXRAY_RXDB | |
| P10.6 | | PWM1_33_N | | TC1_33_TR1 | TC1_H_11_TR0 | | | TC1_34_TR0 | | LIN13_TX | PWM1_34 | | | | FLEXRAY_TXDB | |
| P10.7 | PWM1_35 | PWM1_34_N | TC1_35_TR0 | TC1_34_TR1 | TC1_H_11_TR1 | | | | | LIN13_EN | | | | | FLEXRAY_TXENB_N | |
| P11.0 | PWM1_61 | PWM1_62_N | TC1_61_TR0 | TC1_62_TR1 | | | | | | | | | | AUDIOSS0_MCLK | | |
| P11.1 | PWM1_60 | PWM1_61_N | TC1_60_TR0 | TC1_61_TR1 | | | | | | | | | | AUDIOSS0_TX_SCK | | |
| P11.2 | PWM1_59 | PWM1_60_N | TC1_59_TR0 | TC1_60_TR1 | | | | | | | | | | AUDIOSS0_TX_WS | | |
| P12.0 | PWM1_36 | | TC1_36_TR0 | | | SCB8_RX | TC1_35_TR1 | SCB8_MISO | | CAN0_2_TX | PWM0_H_1 | PWM1_35_N | | AUDIOSS0_TX_SDO | TRIG_IN[20] | |
| P12.1 | PWM1_37 | PWM1_36_N | TC1_37_TR0 | TC1_36_TR1 | | SCB8_TX | SCB8_SDA | SCB8_MOSI | LIN6_EN | CAN0_2_RX | PWM0_H_1_N | | | AUDIOSS0_CLK_I2S_IF | TRIG_IN[21] | |
| P12.2 | PWM1_38 | PWM1_37_N | TC1_38_TR0 | TC1_37_TR1 | EXT_MUX[1]_EN | SCB8_RTS | SCB8_SCL | SCB8_CLK | LIN6_RX | | TC0_H_1_TR0 | | | AUDIOSS0_RX_SCK | | |
| P12.3 | PWM1_39 | PWM1_38_N | TC1_39_TR0 | TC1_38_TR1 | EXT_MUX[1]_0 | SCB8_CTS | | SCB8_SEL0 | LIN6_TX | | TC0_H_1_TR1 | | | AUDIOSS0_RX_WS | | |
| P12.4 | PWM1_40 | PWM1_39_N | TC1_40_TR0 | TC1_39_TR1 | EXT_MUX[1]_1 | | | SCB8_SEL1 | | CAN1_1_TX | TC0_2_TR1 | | | AUDIOSS0_RX_SDI | | |
| P12.5 | PWM1_41 | PWM1_40_N | TC1_41_TR0 | TC1_40_TR1 | EXT_MUX[1]_2 | | | | | CAN1_1_RX | | | | | | |
| P12.6 | PWM1_42 | PWM1_41_N | TC1_42_TR0 | TC1_41_TR1 | | | | | | | | | | | | |
| P12.7 | PWM1_43 | PWM1_42_N | TC1_43_TR0 | TC1_42_TR1 | | | | | | | | | | | | |
| P13.0 | PWM1_M_8 | PWM1_43_N | TC1_M_8_TR0 | TC1_43_TR1 | EXT_MUX[2]_0 | SCB3_RX | | | | LIN3_RX | SCB3_MISO | TC0_2_TR0 | | AUDIOSS1_MCLK | | |
| P13.1 | PWM1_44 | PWM1_M_8_N | TC1_44_TR0 | TC1_M_8_TR1 | EXT_MUX[2]_1 | SCB3_TX | SCB3_SDA | | | LIN3_TX | SCB3_MOSI | PWM0_2_N | | AUDIOSS1_TX_SCK | | |
| P13.2 | PWM1_M_9 | PWM1_44_N | TC1_M_9_TR0 | TC1_44_TR1 | EXT_MUX[2]_2 | SCB3_RTS | SCB3_SCL | | | LIN3_EN | SCB3_CLK | PWM0_2 | | AUDIOSS1_TX_WS | | |
| P13.3 | PWM1_45 | PWM1_M_9_N | TC1_45_TR0 | TC1_M_9_TR1 | EXT_MUX[2]_EN | SCB3_CTS | | | | LIN2_RX | SCB3_SEL0 | | | AUDIOSS1_TX_SDO | | |
| P13.4 | PWM1_M_10 | PWM1_45_N | TC1_M_10_TR0 | TC1_45_TR1 | PWM1_H_4 | | | | | LIN2_TX | SCB3_SEL1 | LIN8_RX | | AUDIOSS1_CLK_I2S_IF | | |
| P13.5 | PWM1_46 | PWM1_M_10_N | TC1_46_TR0 | TC1_M_10_TR1 | PWM1_H_4_N | | | | | SCB3_SEL2 | LIN8_TX | | | AUDIOSS1_RX_SCK | | |
| P13.6 | PWM1_M_11 | PWM1_46_N | TC1_M_11_TR0 | TC1_46_TR1 | PWM1_H_5 | | | | | SCB3_SEL3 | LIN8_EN | | | AUDIOSS1_RX_WS | TRIG_IN[22] | |

Table 12-1. Alternate Pin Functions in Active Mode (continued)^[19, 25]

| Pin | Active Mapping | | | | | | | | | | | | | | | |
|-------|------------------------|-------------|------------|--------------|-------------|-----------|----------|-----------|----------|-----------|-------------|---------|---------|---------------------|-------------|---------|
| | HCon#8 ^[23] | HCon#9 | HCon#10 | HCon#11 | HCon#16 | HCon#17 | HCon#18 | HCon#19 | HCon#20 | HCon#21 | HCon#22 | HCon#23 | HCon#24 | HCon#25 | HCon#26 | HCon#27 |
| Name | ACT #0 ^[24] | ACT #1 | ACT #2 | ACT #3 | ACT #4 | ACT #5 | ACT #6 | ACT #7 | ACT #8 | ACT #9 | ACT #10 | ACT #11 | ACT #12 | ACT #13 | ACT #14 | ACT #15 |
| P13.7 | PWM1_47 | PWM1_M_11_N | TC1_47_TR0 | TC1_M_11_TR1 | PWM1_H_5_N | | | | | | | | | AUDIOSS1_RX_SD1 | TRIG_IN[23] | |
| P14.0 | PWM1_48 | PWM1_47_N | TC1_48_TR0 | TC1_47_TR1 | PWM1_H_6 | SCB2_MISO | | SCB2_RX | | CAN1_0_TX | PWM0_M_1 | | | AUDIOSS2_MCLK | | |
| P14.1 | PWM1_49 | PWM1_48_N | TC1_49_TR0 | TC1_48_TR1 | PWM1_H_6_N | SCB2_MOS1 | SCB2_SDA | SCB2_TX | | CAN1_0_RX | PWM0_M_1_N | | | AUDIOSS2_TX_SCK | | |
| P14.2 | PWM1_50 | PWM1_49_N | TC1_50_TR0 | TC1_49_TR1 | PWM1_H_7 | SCB2_CLK | SCB2_SCL | SCB2_RTS | LIN6_RX | | TC0_M_1_TR0 | | | | | |
| P14.3 | PWM1_51 | PWM1_50_N | TC1_51_TR0 | TC1_50_TR1 | PWM1_H_7_N | SCB2_SEL0 | | SCB2_CTS | LIN6_TX | | TC0_M_1_TR1 | | | | | |
| P14.4 | PWM1_52 | PWM1_51_N | TC1_52_TR0 | TC1_51_TR1 | TC1_H_4_TR0 | SCB2_SEL1 | | | LIN6_EN | | | | | AUDIOSS2_TX_WS | | |
| P14.5 | PWM1_53 | PWM1_52_N | TC1_53_TR0 | TC1_52_TR1 | TC1_H_4_TR1 | SCB2_SEL2 | LIN14_RX | | | | | | | AUDIOSS2_TX_SDO | | |
| P14.6 | PWM1_54 | PWM1_53_N | TC1_54_TR0 | TC1_53_TR1 | TC1_H_5_TR0 | | LIN14_TX | | | | | | | | TRIG_IN[24] | |
| P14.7 | PWM1_55 | PWM1_54_N | TC1_55_TR0 | TC1_54_TR1 | TC1_H_5_TR1 | | LIN14_EN | | | | | | | | TRIG_IN[25] | |
| P15.0 | PWM1_56 | PWM1_55_N | TC1_56_TR0 | TC1_55_TR1 | TC1_H_6_TR0 | SCB9_RX | | SCB9_MISO | | CAN1_3_TX | | | | AUDIOSS2_CLK_I2S_IF | | |
| P15.1 | PWM1_57 | PWM1_56_N | TC1_57_TR0 | TC1_56_TR1 | TC1_H_6_TR1 | SCB9_TX | SCB9_SDA | SCB9_MOSI | | CAN1_3_RX | | | | AUDIOSS2_RX_SCK | | |
| P15.2 | PWM1_58 | PWM1_57_N | TC1_58_TR0 | TC1_57_TR1 | TC1_H_7_TR0 | SCB9_RTS | SCB9_SCL | SCB9_CLK | | | | | | AUDIOSS2_RX_WS | | |
| P15.3 | PWM1_59 | PWM1_58_N | TC1_59_TR0 | TC1_58_TR1 | TC1_H_7_TR1 | SCB9_CTS | | SCB9_SELO | | | | | | AUDIOSS2_RX_SDI | | |
| P16.0 | PWM1_60 | PWM1_59_N | TC1_60_TR0 | TC1_59_TR1 | PWM1_H_0 | | | SCB9_SEL1 | LIN11_RX | | | | | | | |
| P16.1 | PWM1_61 | PWM1_60_N | TC1_61_TR0 | TC1_60_TR1 | PWM1_H_0_N | | | SCB9_SEL2 | LIN11_TX | | | | | | | |
| P16.2 | PWM1_62 | PWM1_61_N | TC1_62_TR0 | TC1_61_TR1 | PWM1_H_1 | | | SCB9_SEL3 | LIN11_EN | | | | | | | |
| P16.3 | PWM1_62 | PWM1_62_N | TC1_62_TR0 | TC1_62_TR1 | PWM1_H_1_N | | | | | | | | | | | |
| P16.4 | PWM1_68 | PWM1_69_N | TC1_68_TR0 | TC1_69_TR1 | | | | | | | | | | | | |
| P16.5 | PWM1_67 | PWM1_68_N | TC1_67_TR0 | TC1_68_TR1 | | | | | | | | | | | | |
| P16.6 | PWM1_66 | PWM1_67_N | TC1_66_TR0 | TC1_67_TR1 | | | | | | | | | | | | |
| P16.7 | PWM1_65 | PWM1_66_N | TC1_65_TR0 | TC1_66_TR1 | | | | | | | | | | | | |
| P17.0 | PWM1_61 | PWM1_62_N | TC1_61_TR0 | TC1_62_TR1 | | | | | LIN11_RX | CAN1_1_TX | | | | | | |
| P17.1 | PWM1_60 | PWM1_61_N | TC1_60_TR0 | TC1_61_TR1 | | SCB3_RX | | | LIN11_TX | CAN1_1_RX | | | | | | |
| P17.2 | PWM1_59 | PWM1_60_N | TC1_59_TR0 | TC1_60_TR1 | | SCB3_TX | SCB3_SDA | | LIN11_EN | | | | | | | |

Table 12-1. Alternate Pin Functions in Active Mode (continued)^[19, 25]

| Pin | Active Mapping | | | | | | | | | | | | | | | |
|-------|------------------------|------------|-------------|-------------|-------------|-----------|----------|-----------|---------|-----------|-------------|---------|--------------|---------|---------|--------------|
| | HCon#8 ^[23] | HCon#9 | HCon#10 | HCon#11 | HCon#16 | HCon#17 | HCon#18 | HCon#19 | HCon#20 | HCon#21 | HCon#22 | HCon#23 | HCon#24 | HCon#25 | HCon#26 | HCon#27 |
| Name | ACT #0 ^[24] | ACT #1 | ACT #2 | ACT #3 | ACT #4 | ACT #5 | ACT #6 | ACT #7 | ACT #8 | ACT #9 | ACT #10 | ACT #11 | ACT #12 | ACT #13 | ACT #14 | ACT #15 |
| P17.3 | PWM1_58 | PWM1_59_N | TC1_58_TR0 | TC1_59_TR1 | PWM1_H_3 | SCB3_RTS | SCB3_SCL | | | SCB3_CLK | | | | | | TRIG_IN[26] |
| P17.4 | PWM1_57 | PWM1_58_N | TC1_57_TR0 | TC1_58_TR1 | PWM1_H_3_N | SCB3_CTS | | | | SCB3_SEL0 | | | | | | TRIG_IN[27] |
| P17.5 | PWM1_56 | PWM1_57_N | TC1_56_TR0 | TC1_57_TR1 | PWM1_H_2 | | LIN15_RX | | | SCB3_SEL1 | | | | | | |
| P17.6 | PWM1_M_4 | PWM1_56_N | TC1_M_4_TR0 | TC1_56_TR1 | PWM1_H_2_N | | LIN15_TX | | | SCB3_SEL2 | | | | | | |
| P17.7 | PWM1_M_5 | PWM1_M_4_N | TC1_M_5_TR0 | TC1_M_4_TR1 | | | LIN15_EN | | | LIN12_RX | | | | | | |
| P18.0 | PWM1_M_6 | PWM1_M_5_N | TC1_M_6_TR0 | TC1_M_5_TR1 | PWM1_H_0 | SCB1_RX | | SCB1_MISO | | LIN12_TX | | | ETH0_REF_CLK | | | FAULT_OUT_0 |
| P18.1 | PWM1_M_7 | PWM1_M_6_N | TC1_M_7_TR0 | TC1_M_6_TR1 | PWM1_H_0_N | SCB1_TX | SCB1_SDA | SCB1_MOSI | | SCB3_MISO | | | ETH0_TX_CTL | | | FAULT_OUT_1 |
| P18.2 | PWM1_55 | PWM1_M_7_N | TC1_55_TR0 | TC1_M_7_TR1 | PWM1_H_1 | SCB1_RTS | SCB1_SCL | SCB1_CLK | | SCB3_MOSI | | | ETH0_TX_ER | | | |
| P18.3 | PWM1_54 | PWM1_55_N | TC1_54_TR0 | TC1_55_TR1 | PWM1_H_1_N | SCB1_CTS | | SCB1_SEL0 | | SCB3_CLK | | | ETH0_TX_CLK | | | TRACE_CLOCK |
| P18.4 | PWM1_53 | PWM1_54_N | TC1_53_TR0 | TC1_54_TR1 | PWM1_H_2 | | | SCB1_SEL1 | | SCB3_SEL0 | PWM0_M_2 | | ETH0_TXD_0 | | | TRACE_DATA_0 |
| P18.5 | PWM1_52 | PWM1_53_N | TC1_52_TR0 | TC1_53_TR1 | PWM1_H_2_N | | | SCB1_SEL2 | | | PWM0_M_2_N | | ETH0_TXD_1 | | | TRACE_DATA_1 |
| P18.6 | PWM1_51 | PWM1_52_N | TC1_51_TR0 | TC1_52_TR1 | PWM1_H_3 | | | SCB1_SEL3 | | CAN1_2_TX | TC0_M_2_TR0 | | ETH0_TXD_2 | | | TRACE_DATA_2 |
| P18.7 | PWM1_50 | PWM1_51_N | TC1_50_TR0 | TC1_51_TR1 | PWM1_H_3_N | | | | | CAN1_2_RX | TC0_M_2_TR1 | | ETH0_TXD_3 | | | TRACE_DATA_3 |
| P19.0 | PWM1_M_3 | PWM1_50_N | TC1_M_3_TR0 | TC1_50_TR1 | TC1_H_0_TR0 | SCB2_MISO | | SCB2_RX | | CAN1_3_TX | | | ETH0_RXD_0 | | | FAULT_OUT_2 |
| P19.1 | PWM1_26 | PWM1_M_3_N | TC1_26_TR0 | TC1_M_3_TR1 | TC1_H_0_TR1 | SCB2_MOSI | SCB2_SDA | SCB2_TX | | CAN1_3_RX | | | ETH0_RXD_1 | | | FAULT_OUT_3 |
| P19.2 | PWM1_27 | PWM1_26_N | TC1_27_TR0 | TC1_26_TR1 | TC1_H_1_TR0 | SCB2_CLK | SCB2_SCL | SCB2_RTS | | | | | ETH0_RXD_2 | | | TRIG_IN[28] |
| P19.3 | PWM1_28 | PWM1_27_N | TC1_28_TR0 | TC1_27_TR1 | TC1_H_1_TR1 | SCB2_SEL0 | | SCB2_CTS | | | | | ETH0_RXD_3 | | | TRIG_IN[29] |
| P19.4 | PWM1_29 | PWM1_28_N | TC1_29_TR0 | TC1_28_TR1 | TC1_H_2_TR0 | SCB2_SEL1 | | | | | | | | | | |
| P20.0 | PWM1_30 | PWM1_29_N | TC1_30_TR0 | TC1_29_TR1 | TC1_H_2_TR1 | SCB2_SEL2 | | | LIN5_RX | | | | | | | |
| P20.1 | PWM1_49 | PWM1_30_N | TC1_49_TR0 | TC1_30_TR1 | TC1_H_3_TR0 | | | | LIN5_TX | | | | | | | |
| P20.2 | PWM1_48 | PWM1_49_N | TC1_48_TR0 | TC1_49_TR1 | TC1_H_3_TR1 | | | | LIN5_EN | | | | | | | |
| P20.3 | PWM1_47 | PWM1_48_N | TC1_47_TR0 | TC1_48_TR1 | | SCB1_RX | | SCB1_MISO | | CAN1_2_TX | | | | | | |
| P20.4 | PWM1_46 | PWM1_47_N | TC1_46_TR0 | TC1_47_TR1 | | SCB1_TX | SCB1_SDA | SCB1_MOSI | | CAN1_2_RX | | | | | | |

Table 12-1. Alternate Pin Functions in Active Mode (continued)^[19, 25]

| Pin | Active Mapping | | | | | | | | | | | | | | | |
|-------|------------------------|-------------|--------------|--------------|-------------|-----------|------------|------------|---------|-----------|---------|-----------|-------------|---------|-------------|---------------|
| | HCon#8 ^[23] | HCon#9 | HCon#10 | HCon#11 | HCon#16 | HCon#17 | HCon#18 | HCon#19 | HCon#20 | HCon#21 | HCon#22 | HCon#23 | HCon#24 | HCon#25 | HCon#26 | HCon#27 |
| Name | ACT #0 ^[24] | ACT #1 | ACT #2 | ACT #3 | ACT #4 | ACT #5 | ACT #6 | ACT #7 | ACT #8 | ACT #9 | ACT #10 | ACT #11 | ACT #12 | ACT #13 | ACT #14 | ACT #15 |
| P20.5 | PWM1_45 | PWM1_46_N | TC1_45_TR0 | TC1_46_TR1 | | SCB1_RTS | SCB1_SCL | SCB1_CLK | | | | | | | | |
| P20.6 | PWM1_44 | PWM1_45_N | TC1_44_TR0 | TC1_45_TR1 | | SCB1_CTS | | SCB1_SEL0 | | CAN1_4_TX | | | | | | |
| P20.7 | PWM1_43 | PWM1_44_N | TC1_43_TR0 | TC1_44_TR1 | | | | SCB1_SEL1 | | CAN1_4_RX | | | | | | |
| P21.0 | PWM1_42 | PWM1_43_N | TC1_42_TR0 | TC1_43_TR1 | | | | SCB1_SEL2 | | | | | | | | |
| P21.1 | PWM1_41 | PWM1_42_N | TC1_41_TR0 | TC1_42_TR1 | | | | | | | | | | | | |
| P21.2 | PWM1_40 | PWM1_41_N | TC1_40_TR0 | TC1_41_TR1 | | | | | | | EXT_CLK | | | | | TRIG_DBG [1] |
| P21.3 | PWM1_39 | PWM1_40_N | TC1_39_TR0 | TC1_40_TR1 | | | | | | | | | | | | |
| P21.4 | PWM1_38 | PWM1_39_N | TC1_38_TR0 | TC1_39_TR1 | | | | | | | | | | | | |
| P21.5 | PWM1_37 | PWM1_38_N | TC1_37_TR0 | TC1_38_TR1 | | | TC1_35_TR1 | TC1_34_TR0 | LIN0_RX | CAN1_1_TX | PWM1_34 | PWM1_35_N | ETH0_RX_CTL | | | TRACE_D ATA_0 |
| P21.6 | PWM1_36 | PWM1_37_N | TC1_36_TR0 | TC1_37_TR1 | | | | | LIN0_TX | LIN13_RX | | | | | | |
| P21.7 | PWM1_35 | PWM1_36_N | TC1_35_TR0 | TC1_36_TR1 | | SCB6_RX | | SCB6_MISO | LIN0_EN | LIN13_TX | | | | | | CAL_SUP_NZ |
| P22.1 | PWM1_33 | PWM1_34_N | TC1_33_TR0 | TC1_34_TR1 | | SCB6_TX | SCB6_SDA | SCB6_MOSI | | CAN1_1_RX | | | | | | TRACE_D ATA_1 |
| P22.2 | PWM1_32 | PWM1_33_N | TC1_32_TR0 | TC1_33_TR1 | | SCB6_RTS | SCB6_SCL | SCB6_CLK | | | | | | | | TRACE_D ATA_2 |
| P22.3 | PWM1_31 | PWM1_32_N | TC1_31_TR0 | TC1_32_TR1 | | SCB6_CTS | | SCB6_SEL0 | | | | | | | | TRACE_D ATA_3 |
| P22.4 | PWM1_30 | PWM1_31_N | TC1_30_TR0 | TC1_31_TR1 | | | | SCB6_SEL1 | | | | | | | | TRACE_CLOCK |
| P22.5 | PWM1_29 | PWM1_30_N | TC1_29_TR0 | TC1_30_TR1 | PWM1_H_8 | | | SCB6_SEL2 | LIN7_RX | | | | | | | |
| P22.6 | PWM1_28 | PWM1_29_N | TC1_28_TR0 | TC1_29_TR1 | PWM1_H_8_N | | | | LIN7_TX | | | | | | | |
| P22.7 | PWM1_27 | PWM1_28_N | TC1_27_TR0 | TC1_28_TR1 | TC1_H_8_TR0 | | LIN14_RX | | LIN7_EN | | | | | | | |
| P23.0 | PWM1_M_8 | PWM1_27_N | TC1_M_8_TR0 | TC1_27_TR1 | TC1_H_8_TR1 | SCB7_RX | LIN14_TX | SCB7_MISO | | CAN1_0_TX | | | | | | FAULT_OUT_0 |
| P23.1 | PWM1_M_9 | PWM1_M_8_N | TC1_M_9_TR0 | TC1_M_8_TR1 | | SCB7_TX | SCB7_SDA | SCB7_MOSI | | CAN1_0_RX | | | | | | FAULT_OUT_1 |
| P23.2 | PWM1_M_10 | PWM1_M_9_N | TC1_M_10_TR0 | TC1_M_9_TR1 | | SCB7_RTS | SCB7_SCL | SCB7_CLK | LIN6_RX | | | | | | | FAULT_OUT_2 |
| P23.3 | PWM1_M_11 | PWM1_M_10_N | TC1_M_11_TR0 | TC1_M_10_TR1 | | SCB7_CTS | | SCB7_SEL0 | LIN6_TX | | | | ETH0_RX_CLK | | TRIG_IN[30] | FAULT_OUT_3 |
| P23.4 | PWM1_25 | PWM1_M_11_N | TC1_25_TR0 | TC1_M_11_TR1 | PWM1_H_9 | SCB2_MISO | | SCB7_SEL1 | | | | | | | TRIG_IN[31] | TRIG_DBG [0] |
| P23.5 | PWM1_24 | PWM1_25_N | TC1_24_TR0 | TC1_25_TR1 | PWM1_H_9_N | SCB2_MOSI | | SCB7_SEL2 | | | | LIN9_RX | | | | |

Table 12-1. Alternate Pin Functions in Active Mode (continued)^[19, 25]

| Pin | Active Mapping | | | | | | | | | | | | | | | |
|-------|------------------------|-----------|------------|------------|-------------|-----------|---------|---------|----------|---------|---------|-------------|---------|----------------------------|---------|--------------|
| | HCon#8 ^[23] | HCon#9 | HCon#10 | HCon#11 | HCon#16 | HCon#17 | HCon#18 | HCon#19 | HCon#20 | HCon#21 | HCon#22 | HCon#23 | HCon#24 | HCon#25 | HCon#26 | HCon#27 |
| Name | ACT #0 ^[24] | ACT #1 | ACT #2 | ACT #3 | ACT #4 | ACT #5 | ACT #6 | ACT #7 | ACT #8 | ACT #9 | ACT #10 | ACT #11 | ACT #12 | ACT #13 | ACT #14 | ACT #15 |
| P23.6 | PWM1_23 | PWM1_24_N | TC1_23_TR0 | TC1_24_TR1 | TC1_H_9_TR0 | SCB2_CLK | | | | | | LIN9_TX | | | | |
| P23.7 | PWM1_22 | PWM1_23_N | TC1_22_TR0 | TC1_23_TR1 | TC1_H_9_TR1 | SCB2_SEL0 | | | | | EXT_CLK | LIN9_EN | | | | CAL_SUP_NZ |
| P24.0 | | | | | | | | | LIN16_RX | | EXT_CLK | | | SDHC_CARD_DETECT_N | | |
| P24.1 | | | | | | | | | | | | SPIHB_CLK | | SDHC_CARD_MEC_H_WRITE_PROT | | |
| P24.2 | | | | | | | | | | | | SPIHB_RWDS | | SDHC_CLK_CARD | | |
| P24.3 | | | | | | | | | LIN16_TX | | | SPIHB_SEL0 | | SDHC_CARD_CMD | | |
| P24.4 | | | | | | | | | LIN16_EN | | | SPIHB_SEL1 | | SDHC_CARD_IF_PWR_EN | | |
| P25.0 | | | | | | | | | | | | SPIHB_DATA0 | | SDHC_CARD_DAT_3TO0_0 | | |
| P25.1 | | | | | | | | | | | | SPIHB_DATA1 | | SDHC_CARD_DAT_3TO0_1 | | |
| P25.2 | | | | | | | | | | | | SPIHB_DATA2 | | SDHC_CARD_DAT_3TO0_2 | | |
| P25.3 | | | | | | | | | | | | SPIHB_DATA3 | | SDHC_CARD_DAT_3TO0_3 | | |
| P25.4 | | | | | | | | | | | | SPIHB_DATA4 | | SDHC_CARD_DAT_7TO4_0 | | |
| P25.5 | | | | | | | | | | | | SPIHB_DATA5 | | SDHC_CARD_DAT_7TO4_1 | | |
| P25.6 | | | | | | | | | | | | SPIHB_DATA6 | | SDHC_CARD_DAT_7TO4_2 | | |
| P25.7 | | | | | | | | | | | | SPIHB_DATA7 | | SDHC_CARD_DAT_7TO4_3 | | |
| P26.0 | | | | | | | | | | | | | | | | ETH1_REF_CLK |
| P26.1 | | | | | | | | | | | | | | | | ETH1_TX_CTL |
| P26.2 | | | | | | | | | | | | | | | | ETH1_TX_CLK |
| P26.3 | | | | | | | | | | | | | | | | ETH1_TXD_0 |
| P26.4 | | | | | | | | | | | | | | | | ETH1_TXD_1 |
| P26.5 | | | | | | | | | | | | | | | | ETH1_TXD_2 |
| P26.6 | | | | | | | | | | | | | | | | ETH1_TXD_3 |

Table 12-1. Alternate Pin Functions in Active Mode (continued)^[19, 25]

| Pin | Active Mapping | | | | | | | | | | | | | | | |
|-------|------------------------|-----------|------------|------------|--------------|-----------|-----------|-------------|----------|---------|---------|---------|---------|---------|---------|----------------------------|
| | HCon#8 ^[23] | HCon#9 | HCon#10 | HCon#11 | HCon#16 | HCon#17 | HCon#18 | HCon#19 | HCon#20 | HCon#21 | HCon#22 | HCon#23 | HCon#24 | HCon#25 | HCon#26 | HCon#27 |
| Name | ACT #0 ^[24] | ACT #1 | ACT #2 | ACT #3 | ACT #4 | ACT #5 | ACT #6 | ACT #7 | ACT #8 | ACT #9 | ACT #10 | ACT #11 | ACT #12 | ACT #13 | ACT #14 | ACT #15 |
| P26.7 | | | | | | | | | | | | | | | | ETH1_RXD_0 |
| P27.0 | | | | | | | | | | | | | | | | ETH1_RXD_1 |
| P27.1 | | | | | | | | | | | | | | | | ETH1_RXD_2 |
| P27.2 | | | | | | | | | | | | | | | | ETH1_RXD_3 |
| P27.3 | | | | | | | | | | | | | | | | ETH1_RX_CTL |
| P27.4 | | | | | | | | | | | | | | | | ETH1_RX_CLK |
| P27.5 | | | | | | | | | | | | | | | | ETH1_MDI_O |
| P27.6 | | | | | | | | | | | | | | | | ETH1_MD_C |
| P27.7 | | | | | | | | | | | | | | | | ETH1_ETH_TSU_TIMER_CMP_VAL |
| P28.0 | PWM1_63 | PWM1_65_N | TC1_63_TR0 | TC1_65_TR1 | PWM1_H_12 | SCB10_RX | | SCB10_MIS_O | | | | | | | | |
| P28.1 | PWM1_64 | PWM1_63_N | TC1_64_TR0 | TC1_63_TR1 | PWM1_H_12_N | SCB10_TX | SCB10_SDA | SCB10_MOSI | LIN17_RX | | | | | | | |
| P28.2 | PWM1_65 | PWM1_64_N | TC1_65_TR0 | TC1_64_TR1 | TC1_H_12_TR0 | SCB10_RTS | SCB10_SCL | SCB10_CLK | LIN17_TX | | | | | | | |
| P28.3 | PWM1_66 | PWM1_65_N | TC1_66_TR0 | TC1_65_TR1 | TC1_H_12_TR1 | SCB10_CTS | | SCB10_SEL0 | LIN17_EN | | | | | | | |
| P28.4 | PWM1_67 | PWM1_66_N | TC1_67_TR0 | TC1_66_TR1 | | | | SCB10_SEL1 | LIN18_RX | | | | | | | |
| P28.5 | PWM1_68 | PWM1_67_N | TC1_68_TR0 | TC1_67_TR1 | | | | SCB10_SEL2 | LIN18_TX | | | | | | | |
| P28.6 | PWM1_69 | PWM1_68_N | TC1_69_TR0 | TC1_68_TR1 | | | | SCB10_SEL3 | LIN18_EN | | | | | | | |
| P28.7 | PWM1_70 | PWM1_69_N | TC1_70_TR0 | TC1_69_TR1 | | | | | LIN19_RX | | | | | | | |
| P29.0 | PWM1_76 | PWM1_75_N | TC1_76_TR0 | TC1_75_TR1 | | | | | LIN19_TX | | | | | | | |
| P29.1 | PWM1_77 | PWM1_76_N | TC1_77_TR0 | TC1_76_TR1 | | | | | LIN19_EN | | | | | | | |
| P29.2 | PWM1_78 | PWM1_77_N | TC1_78_TR0 | TC1_77_TR1 | | | | | | | | | | | | |
| P29.3 | PWM1_79 | PWM1_78_N | TC1_79_TR0 | TC1_78_TR1 | | | | | | | | | | | | |
| P29.4 | PWM1_80 | PWM1_79_N | TC1_80_TR0 | TC1_79_TR1 | | | | | | | | | | | | |

Table 12-1. Alternate Pin Functions in Active Mode (continued)^[19, 25]

| Pin | Active Mapping | | | | | | | | | | | | | | | |
|-------|------------------------|-----------|------------|------------|---------|-----------|-----------|------------|----------|-----------|---------|---------|--------------|---------|---------|-------------|
| | HCon#8 ^[23] | HCon#9 | HCon#10 | HCon#11 | HCon#16 | HCon#17 | HCon#18 | HCon#19 | HCon#20 | HCon#21 | HCon#22 | HCon#23 | HCon#24 | HCon#25 | HCon#26 | HCon#27 |
| Name | ACT #0 ^[24] | ACT #1 | ACT #2 | ACT #3 | ACT #4 | ACT #5 | ACT #6 | ACT #7 | ACT #8 | ACT #9 | ACT #10 | ACT #11 | ACT #12 | ACT #13 | ACT #14 | ACT #15 |
| P29.5 | PWM1_81 | PWM1_80_N | TC1_81_TR0 | TC1_80_TR1 | | | | | | | | | | | | |
| P29.6 | PWM1_82 | PWM1_81_N | TC1_82_TR0 | TC1_81_TR1 | | | | | | | | | | | | |
| P29.7 | PWM1_83 | PWM1_82_N | TC1_83_TR0 | TC1_82_TR1 | | | | | | | | | | | | |
| P30.0 | PWM1_83 | PWM1_83_N | TC1_83_TR0 | TC1_83_TR1 | | SCB9_RTS | SCB9_SCL | SCB9_CLK | | | | | | | | TRIG_IN[34] |
| P30.1 | PWM1_82 | PWM1_83_N | TC1_82_TR0 | TC1_83_TR1 | | SCB9_CTS | | SCB9_SEL0 | LIN16_RX | | | | | | | TRIG_IN[35] |
| P30.2 | PWM1_81 | PWM1_82_N | TC1_81_TR0 | TC1_82_TR1 | | | | SCB9_SEL1 | LIN16_TX | CAN1_3_TX | | | | | | TRIG_IN[36] |
| P30.3 | PWM1_80 | PWM1_81_N | TC1_80_TR0 | TC1_81_TR1 | | | | SCB9_SEL2 | LIN16_EN | CAN1_3_RX | | | | | | TRIG_IN[37] |
| P31.0 | PWM1_79 | PWM1_80_N | TC1_79_TR0 | TC1_80_TR1 | | | | | LIN17_RX | | | | | | | |
| P31.1 | PWM1_78 | PWM1_79_N | TC1_78_TR0 | TC1_79_TR1 | | | | | LIN17_TX | | | | | | | |
| P31.2 | PWM1_77 | PWM1_78_N | TC1_77_TR0 | TC1_78_TR1 | | | | | LIN17_EN | | | | | | | |
| P32.0 | PWM1_76 | PWM1_77_N | TC1_76_TR0 | TC1_77_TR1 | | SCB10_RX | | SCB10_MISO | | | | | | | | TRIG_IN[40] |
| P32.1 | PWM1_75 | PWM1_76_N | TC1_75_TR0 | TC1_76_TR1 | | SCB10_TX | SCB10_SDA | SCB10_MOSI | | | | | | | | TRIG_IN[41] |
| P32.2 | PWM1_74 | PWM1_75_N | TC1_74_TR0 | TC1_75_TR1 | | SCB10_RTS | SCB10_SCL | SCB10_CLK | LIN18_RX | | | | | | | TRIG_IN[42] |
| P32.3 | PWM1_73 | PWM1_74_N | TC1_73_TR0 | TC1_74_TR1 | | SCB10_CTS | | SCB10_SEL0 | LIN18_TX | | | | | | | TRIG_IN[43] |
| P32.4 | PWM1_72 | PWM1_73_N | TC1_72_TR0 | TC1_73_TR1 | | | LIN10_RX | SCB10_SEL1 | LIN18_EN | | | | | | | TRIG_IN[44] |
| P32.5 | PWM1_71 | PWM1_72_N | TC1_71_TR0 | TC1_72_TR1 | | | LIN10_TX | SCB10_SEL2 | LIN19_RX | | | | | | | TRIG_IN[45] |
| P32.6 | PWM1_70 | PWM1_71_N | TC1_70_TR0 | TC1_71_TR1 | | | LIN10_EN | SCB10_SEL3 | LIN19_TX | CAN1_4_TX | | | | | | TRIG_IN[46] |
| P32.7 | PWM1_69 | PWM1_70_N | TC1_69_TR0 | TC1_70_TR1 | | | | | LIN19_EN | CAN1_4_RX | | | | | | TRIG_IN[47] |
| P33.0 | | | | | | | | | | | | | ETH0_REF_CLK | | | |
| P33.1 | | | | | | | | | | | | | ETH0_TX_CTL | | | ETH1_TX_ER |
| P33.2 | | | | | | | | | | | | | ETH0_TX_CLK | | | |
| P33.3 | | | | | | | | | | | | | ETH0_TXD_0 | | | ETH1_TXD_4 |
| P33.4 | | | | | | | | | | | | | ETH0_TXD_1 | | | ETH1_TXD_5 |

Table 12-1. Alternate Pin Functions in Active Mode (continued)^[19, 25]

| Pin | Active Mapping | | | | | | | | | | | | | | | |
|-------|------------------------|--------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|----------------------------|---------|---------|------------|
| | HCon#8 ^[23] | HCon#9 | HCon#10 | HCon#11 | HCon#16 | HCon#17 | HCon#18 | HCon#19 | HCon#20 | HCon#21 | HCon#22 | HCon#23 | HCon#24 | HCon#25 | HCon#26 | HCon#27 |
| Name | ACT #0 ^[24] | ACT #1 | ACT #2 | ACT #3 | ACT #4 | ACT #5 | ACT #6 | ACT #7 | ACT #8 | ACT #9 | ACT #10 | ACT #11 | ACT #12 | ACT #13 | ACT #14 | ACT #15 |
| P33.5 | | | | | | | | | | | | | ETH0_TXD_2 | | | ETH1_TXD_6 |
| P33.6 | | | | | | | | | | | | | ETH0_TXD_3 | | | ETH1_TXD_7 |
| P33.7 | | | | | | | | | | | | | ETH0_RXD_0 | | | ETH1_RXD_4 |
| P34.0 | | | | | | | | | | | | | ETH0_RXD_1 | | | ETH1_RXD_5 |
| P34.1 | | | | | | | | | | | | | ETH0_RXD_2 | | | ETH1_RXD_6 |
| P34.2 | | | | | | | | | | | | | ETH0_RXD_3 | | | ETH1_RXD_7 |
| P34.3 | | | | | | | | | | | | | ETH0_RX_CTL | | | ETH1_RX_ER |
| P34.4 | | | | | | | | | | | | | ETH0_RX_CLK | | | |
| P34.5 | | | | | | | | | | | | | ETH0_MDIO | | | |
| P34.6 | | | | | | | | | | | | | ETH0_MDC | | | |
| P34.7 | | | | | | | | | | | | | ETH0_ETH_TSU_TIMER_CMP_VAL | | | |

12.1 Pin Function Description

Table 12-2. Pin Function Description

| Sl. No. | Pin | Module | Description |
|---------|----------------------------|----------|---|
| 1 | PWMx_y | TCPWM | TCPWM 16-bit PWM (no motor control), PWM_DT and PWM_PR line out, x-TCPWM block, y-counter number |
| 2 | PWMx_y_N | TCPWM | TCPWM 16-bit PWM (no motor control), PWM_DT and PWM_PR complementary line out (N), x-TCPWM block, y-counter number |
| 3 | PWMx_M_y | TCPWM | TCPWM 16-bit PWM with motor control line out, x-TCPWM block, y-counter number |
| 4 | PWMx_M_y_N | TCPWM | TCPWM 16-bit PWM with motor control complementary line out (N), x-TCPWM block, y-counter number |
| 5 | PWMx_H_y | TCPWM | TCPWM 32-bit PWM, PWM_DT and PWM_PR line out, x-TCPWM block, y-counter number |
| 6 | PWMx_H_y_N | TCPWM | TCPWM 32-bit PWM, PWM_DT and PWM_PR complementary line out (N), x-TCPWM block, y-counter number |
| 7 | TCx_y_TRz | TCPWM | TCPWM 16-bit dedicated counter input triggers, x-TCPWM block, y-counter number, z-trigger number |
| 8 | TCx_M_y_TRz | TCPWM | TCPWM 16-bit dedicated counter input triggers with motor control, x-TCPWM block, y-counter number, z-trigger number |
| 9 | TCx_H_y_TRz | TCPWM | TCPWM 32-bit dedicated counter input triggers, x-TCPWM block, y-counter number, z-trigger number |
| 10 | SCBx_RX | SCB | UART Receive, x-SCB block |
| 11 | SCBx_TX | SCB | UART Transmit, x-SCB block |
| 12 | SCBx_RTS | SCB | UART Request to Send (Handshake), x-SCB block |
| 13 | SCBx_CTS | SCB | UART Clear to Send (Handshake), x-SCB block |
| 14 | SCBx_SDA | SCB | I2C Data line, x-SCB block |
| 15 | SCBx_SCL | SCB | I2C Clock line, x-SCB block |
| 16 | SCBx_MISO | SCB | SPI Master Input Slave Output, x-SCB block |
| 17 | SCBx_MOSI | SCB | SPI Master Output Slave Input, x-SCB block |
| 18 | SCBx_CLK | SCB | SPI Serial Clock, x-SCB block |
| 19 | SCBx_SELy | SCB | SPI Slave Select, x-SCB block, y-select line |
| 20 | LINx_RX | LIN | LIN Receive line, x-LIN block |
| 21 | LINx_TX | LIN | LIN Transmit line, x-LIN block |
| 22 | LINx_EN | LIN | LIN Enable line, x-LIN block |
| 23 | CANx_y_TX | CANFD | CAN Transmit line, x-CAN block, y-channel number |
| 24 | CANx_y_RX | CANFD | CAN Receive line, x-CAN block, y-channel number |
| 25 | SPIHB_CLK | SMIF | SMIF interface clock |
| 26 | SPIHB_RWDS | SMIF | SMIF (SPI/Hyperbus) read-write-data-strobe line |
| 27 | SPIHB_SELx | SMIF | SMIF (SPI/Hyperbus) memory select line, x-select line number |
| 28 | SPIHB_DATAx | SMIF | SMIF (SPI/Hyperbus) memory data read and write line, x-0 to 7 data lines |
| 29 | ETHx_RX_ER | Ethernet | Ethernet receive error indication line, x-ETH module number |
| 30 | ETHx_ETH_TSU_TIMER_CMP_VAL | Ethernet | Ethernet time stamp unit timer compare indication line, x-ETH module number |
| 31 | ETHx_MDIO | Ethernet | Ethernet management data input/output (MDIO) interface to PHY, x-ETH module number |
| 32 | ETHx_MDC | Ethernet | Ethernet management data clock (MDC) line, x-ETH module number |
| 33 | ETHx_REF_CLK | Ethernet | Ethernet reference clock line, x-ETH module number |
| 34 | ETHx_TX_CTL | Ethernet | Ethernet transmit control line, x-ETH module number |

Table 12-2. Pin Function Description (continued)

| SI. No. | Pin | Module | Description |
|---------|-------------------------------|------------|---|
| 35 | ETHx_TX_ER | Ethernet | Ethernet transmit error indication line, x-ETH module number |
| 36 | ETHx_TX_CLK | Ethernet | Ethernet transmit clock line, x-ETH module number |
| 37 | ETHx_TXD_y | Ethernet | Ethernet transmit data line, , x-ETH module number, y-transmit channel number |
| 38 | ETHx_RXD_y | Ethernet | Ethernet receive data line, , x-ETH module number, y-receive channel number |
| 39 | ETHx_RX_CTL | Ethernet | Ethernet receive control line, x-ETH module number |
| 40 | ETHx_RX_CLK | Ethernet | Ethernet receive clock line, x-ETH module number |
| 41 | SDHC_CARD_MECH_WRIT E_PROT | SDHC | SDHC mechanical write protect |
| 42 | SDHC_CARD_CMD | SDHC | SDHC command line |
| 43 | SDHC_CLK_CARD | SDHC | SDHC clock line |
| 44 | SDHC_CARD_DETECT_N | SDHC | SDHC interface insertion or removal detection line |
| 45 | SDHC_CARD_IF_PWR_EN | SDHC | SDHC interface power cycle line |
| 46 | SDHC_CARD_DAT_3TO0_x | SDHC | SDHC lower 4-bits of the data |
| 47 | SDHC_CARD_DAT_7TO4_x | SDHC | SDHC upper 4-bits of the data in 8-bit mode |
| 48 | AUDIOSSx_MCLK | AUDIOSS | AudioSS master clock out, x-AudioSS block |
| 49 | AUDIOSSx_TX_SCK | AUDIOSS | I ² S serial clock for transmitter, x-AudioSS block |
| 50 | AUDIOSSx_TX_WS | AUDIOSS | I ² S word select for transmitter, x-AudioSS block |
| 51 | AUDIOSSx_TX_SDO | AUDIOSS | I ² S serial data output for transmitter, x-AudioSS block |
| 52 | AUDIOSSx_CLK_I2S_IF | AUDIOSS | I ² S clock supplied from external I2S bus host, x-AudioSS block |
| 53 | AUDIOSSx_RX_SCK | AUDIOSS | I ² S serial clock for receiver, x-AudioSS block |
| 54 | AUDIOSSx_RX_WS | AUDIOSS | I ² S word select for receiver, x-AudioSS block |
| 55 | AUDIOSSx_RX_SDI | AUDIOSS | I ² S serial data input for receiver, x-AudioSS block |
| 56 | FLEXRAY_RXDx | FlexRay | FlexRay data receive line, x-module channel reference A or B |
| 57 | FLEXRAY_TXDx | FlexRay | FlexRay data transmit line, x-module channel reference A or B |
| 58 | FLEXRAY_TXENx_N | FlexRay | FlexRay transmit enable line, x-module channel reference A or B |
| 59 | CAL_SUP_NZ | System | ETAS Calibration support line |
| 60 | FAULT_OUT_x | SRSS | Fault output line x-0 to 3 |
| 61 | TRACE_DATA_x | SRSS | Trace dataout line x-0 to 3 |
| 62 | TRACE_CLOCK | SRSS | Trace clock line |
| 63 | RTC_CAL | SRSS RTC | RTC calibration clock input |
| 64 | SWJ_TRSTN | SRSS | JTAG Test reset line (Active low) |
| 65 | SWJ_SWO_TDO | SRSS | JTAG Test data output/SWO (Serial Wire Output) |
| 66 | SWJ_SWCLK_TCLK | SRSS | JTAG Test clock/SWD clock (Serial Wire Clock) |
| 67 | SWJ_SWDIO_TMS | SRSS | JTAG Test mode select/SWD data (Serial Wire Data Input/Output) |
| 68 | SWJ_SWDOE_TDI | SRSS | JTAG Test data input |
| 69 | HIBERNATE_WAKEUP[x] | SRSS | Hibernate wakeup line x-0 to 3 |
| 70 | EXT_CLK | SRSS | External clock input |
| 71 | EXT_PS_CTL0 | SRSS REGHC | REGHC control line, Transistor mode/Positive terminal of the current sense resistor, PMIC mode/Power good input from PMIC |
| 72 | EXT_PS_CTL1 | SRSS REGHC | REGHC control line, Transistor mode/Negative terminal of the current sense resistor, PMIC mode/Enable output for PMIC |
| 73 | EXT_PS_CTL2 | SRSS REGHC | REGHC control line, Transistor mode/unused, PMIC mode/Reset threshold adjustment for some PMICs |

Table 12-2. Pin Function Description *(continued)*

| SI. No. | Pin | Module | Description |
|---------|---------------|----------|---|
| 74 | ADC[x]_y | PASS SAR | SAR, channel, x-SAR number, y-channel number |
| 75 | ADC[x]_M | PASS SAR | SAR motor control input, x-SAR number |
| 76 | EXT_MUX[x]_y | PASS SAR | External SAR MUX inputs, x-MUX number, y-MUX input 0 to 2 |
| 77 | EXT_MUX[x]_EN | PASS SAR | External SAR MUX enable line |

13. Interrupts and Wake-up Assignments

Table 13-1. Peripheral Interrupt Assignments and Wake-up Sources

| Interrupt | Source | Power Mode | Description |
|-----------|------------------------------------|------------|--|
| 0 | cpuss_interrupts_ipc_0_IRQn | DeepSleep | CPUSS Inter Process Communication Interrupt #0 |
| 1 | cpuss_interrupts_ipc_1_IRQn | DeepSleep | CPUSS Inter Process Communication Interrupt #1 |
| 2 | cpuss_interrupts_ipc_2_IRQn | DeepSleep | CPUSS Inter Process Communication Interrupt #2 |
| 3 | cpuss_interrupts_ipc_3_IRQn | DeepSleep | CPUSS Inter Process Communication Interrupt #3 |
| 4 | cpuss_interrupts_ipc_4_IRQn | DeepSleep | CPUSS Inter Process Communication Interrupt #4 |
| 5 | cpuss_interrupts_ipc_5_IRQn | DeepSleep | CPUSS Inter Process Communication Interrupt #5 |
| 6 | cpuss_interrupts_ipc_6_IRQn | DeepSleep | CPUSS Inter Process Communication Interrupt #6 |
| 7 | cpuss_interrupts_ipc_7_IRQn | DeepSleep | CPUSS Inter Process Communication Interrupt #7 |
| 8 | cpuss_interrupts_fault_0_IRQn | DeepSleep | CPUSS Fault Structure #0 Interrupt |
| 9 | cpuss_interrupts_fault_1_IRQn | DeepSleep | CPUSS Fault Structure #1 Interrupt |
| 10 | cpuss_interrupts_fault_2_IRQn | DeepSleep | CPUSS Fault Structure #2 Interrupt |
| 11 | cpuss_interrupts_fault_3_IRQn | DeepSleep | CPUSS Fault Structure #3 Interrupt |
| 12 | srss_interrupt_backup_IRQn | DeepSleep | BACKUP domain Interrupt |
| 13 | srss_interrupt_mcwtdt_0_IRQn | DeepSleep | Multi Counter Watchdog Timer #0 interrupt |
| 14 | srss_interrupt_mcwtdt_1_IRQn | DeepSleep | Multi Counter Watchdog Timer #1 interrupt |
| 15 | srss_interrupt_mcwtdt_2_IRQn | DeepSleep | Multi Counter Watchdog Timer #2 interrupt |
| 16 | srss_interrupt_wdt_IRQn | DeepSleep | Hardware Watchdog Timer interrupt |
| 17 | srss_interrupt_IRQn | DeepSleep | Other combined Interrupts for SRSS (LVD, CLKCAL) |
| 18 | scb_0_interrupt_IRQn | DeepSleep | SCB0 interrupt (DeepSleep capable) |
| 19 | evtgen_0_interrupt_dpssp_IRQn | DeepSleep | Event gen DeepSleep domain interrupt |
| 20 | ioss_interrupt_vdd_IRQn | DeepSleep | I/O Supply (V _{DDIO} , V _{DDA} , V _{DDD}) state change Interrupt |
| 21 | ioss_interrupt_gpio_dpssp_IRQn | DeepSleep | Consolidated Interrupt for GPIO_STD and GPIO_ENH, All Ports |
| 22 | ioss_interrupts_gpio_dpssp_0_IRQn | DeepSleep | GPIO_ENH Port #0 Interrupt |
| 23 | ioss_interrupts_gpio_dpssp_1_IRQn | DeepSleep | GPIO_STD Port #1 Interrupt |
| 24 | ioss_interrupts_gpio_dpssp_2_IRQn | DeepSleep | GPIO_STD Port #2 Interrupt |
| 25 | ioss_interrupts_gpio_dpssp_3_IRQn | DeepSleep | GPIO_STD Port #3 Interrupt |
| 26 | ioss_interrupts_gpio_dpssp_4_IRQn | DeepSleep | GPIO_STD Port #4 Interrupt |
| 27 | ioss_interrupts_gpio_dpssp_5_IRQn | DeepSleep | GPIO_STD Port #5 Interrupt |
| 28 | ioss_interrupts_gpio_dpssp_6_IRQn | DeepSleep | GPIO_STD Port #6 Interrupt |
| 29 | ioss_interrupts_gpio_dpssp_7_IRQn | DeepSleep | GPIO_STD Port #7 Interrupt |
| 30 | ioss_interrupts_gpio_dpssp_8_IRQn | DeepSleep | GPIO_STD Port #8 Interrupt |
| 31 | ioss_interrupts_gpio_dpssp_9_IRQn | DeepSleep | GPIO_STD Port #9 Interrupt |
| 32 | ioss_interrupts_gpio_dpssp_10_IRQn | DeepSleep | GPIO_STD Port #10 Interrupt |
| 33 | ioss_interrupts_gpio_dpssp_11_IRQn | DeepSleep | GPIO_STD Port #11 Interrupt |
| 34 | ioss_interrupts_gpio_dpssp_12_IRQn | DeepSleep | GPIO_STD Port #12 Interrupt |
| 35 | ioss_interrupts_gpio_dpssp_13_IRQn | DeepSleep | GPIO_STD Port #13 Interrupt |
| 36 | ioss_interrupts_gpio_dpssp_14_IRQn | DeepSleep | GPIO_STD Port #14 Interrupt |
| 37 | ioss_interrupts_gpio_dpssp_15_IRQn | DeepSleep | GPIO_STD Port #15 Interrupt |
| 38 | ioss_interrupts_gpio_dpssp_16_IRQn | DeepSleep | GPIO_STD Port #16 Interrupt |
| 39 | ioss_interrupts_gpio_dpssp_17_IRQn | DeepSleep | GPIO_STD Port #17 Interrupt |

Table 13-1. Peripheral Interrupt Assignments and Wake-up Sources *(continued)*

| Interrupt | Source | Power Mode | Description |
|-----------|------------------------------------|------------|--|
| 40 | ioss_interrupts_gpio_dpslp_18_IRQn | DeepSleep | GPIO_STD Port #18 Interrupt |
| 41 | ioss_interrupts_gpio_dpslp_19_IRQn | DeepSleep | GPIO_STD Port #19 Interrupt |
| 42 | ioss_interrupts_gpio_dpslp_20_IRQn | DeepSleep | GPIO_STD Port #20 Interrupt |
| 43 | ioss_interrupts_gpio_dpslp_21_IRQn | DeepSleep | GPIO_STD Port #21 Interrupt |
| 44 | ioss_interrupts_gpio_dpslp_22_IRQn | DeepSleep | GPIO_STD Port #22 Interrupt |
| 45 | ioss_interrupts_gpio_dpslp_23_IRQn | DeepSleep | GPIO_STD Port #23 Interrupt |
| 46 | ioss_interrupts_gpio_dpslp_28_IRQn | DeepSleep | GPIO_STD Port #28 Interrupt |
| 47 | ioss_interrupts_gpio_dpslp_29_IRQn | DeepSleep | GPIO_STD Port #29 Interrupt |
| 48 | ioss_interrupts_gpio_dpslp_30_IRQn | DeepSleep | GPIO_STD Port #30 Interrupt |
| 49 | ioss_interrupts_gpio_dpslp_31_IRQn | DeepSleep | GPIO_STD Port #31 Interrupt |
| 50 | ioss_interrupts_gpio_dpslp_32_IRQn | DeepSleep | GPIO_STD Port #32 Interrupt |
| 51 | ioss_interrupts_gpio_act_IRQn | Active | Consolidated Interrupt for HSIO_STD, All Ports |
| 52 | ioss_interrupts_gpio_act_24_IRQn | Active | HSIO_STD Port #24 Interrupt |
| 53 | ioss_interrupts_gpio_act_25_IRQn | Active | HSIO_STD Port #25 Interrupt |
| 54 | ioss_interrupts_gpio_act_26_IRQn | Active | HSIO_STD Port #26 Interrupt |
| 55 | ioss_interrupts_gpio_act_27_IRQn | Active | HSIO_STD Port #27 Interrupt |
| 56 | ioss_interrupts_gpio_act_33_IRQn | Active | HSIO_STD Port #33 Interrupt |
| 57 | ioss_interrupts_gpio_act_34_IRQn | Active | HSIO_STD Port #34 Interrupt |
| 58 | cpuss_interrupt_crypto_IRQn | Active | CRYPTO Accelerator Interrupt |
| 59 | cpuss_interrupt_fm_IRQn | Active | Flash Macro Interrupt |
| 60 | cpuss_interrupts_cm7_0_fp_IRQn | Active | CM7_0 Floating Point operation fault |
| 61 | cpuss_interrupts_cm7_1_fp_IRQn | Active | CM7_1 Floating Point operation fault |
| 62 | cpuss_interrupts_cm0_cti_0_IRQn | Active | CM0+ CTI (Cross Trigger Interface) #0 |
| 63 | cpuss_interrupts_cm0_cti_1_IRQn | Active | CM0+ CTI #1 |
| 64 | cpuss_interrupts_cm7_0_cti_0_IRQn | Active | CM7_0 CTI #0 |
| 65 | cpuss_interrupts_cm7_0_cti_1_IRQn | Active | CM7_0 CTI #1 |
| 66 | cpuss_interrupts_cm7_1_cti_0_IRQn | Active | CM7_1 CTI #0 |
| 67 | cpuss_interrupts_cm7_1_cti_1_IRQn | Active | CM7_1 CTI #1 |
| 68 | evtgen_0_interrupt_IRQn | Active | Event gen Active domain Interrupt |
| 69 | canfd_0_interrupt0_IRQn | Active | CAN0, Consolidated Interrupt #0 for all three channels |
| 70 | canfd_0_interrupt1_IRQn | Active | CAN0, Consolidated Interrupt #1 for all three channels |
| 71 | canfd_1_interrupt0_IRQn | Active | CAN1, Consolidated Interrupt #0 for all three channels |
| 72 | canfd_1_interrupt1_IRQn | Active | CAN1, Consolidated Interrupt #1 for all three channels |
| 73 | canfd_0_interrupts0_0_IRQn | Active | CAN0, Interrupt #0, Channel #0 |
| 74 | canfd_0_interrupts0_1_IRQn | Active | CAN0, Interrupt #0, Channel #1 |
| 75 | canfd_0_interrupts0_2_IRQn | Active | CAN0, Interrupt #0, Channel #2 |
| 76 | canfd_0_interrupts0_3_IRQn | Active | CAN0, Interrupt #0, Channel #3 |
| 77 | canfd_0_interrupts0_4_IRQn | Active | CAN0, Interrupt #0, Channel #4 |
| 78 | canfd_0_interrupts1_0_IRQn | Active | CAN0, Interrupt #1, Channel #0 |
| 79 | canfd_0_interrupts1_1_IRQn | Active | CAN0, Interrupt #1, Channel #1 |
| 80 | canfd_0_interrupts1_2_IRQn | Active | CAN0, Interrupt #1, Channel #2 |

Table 13-1. Peripheral Interrupt Assignments and Wake-up Sources (continued)

| Interrupt | Source | Power Mode | Description |
|-----------|----------------------------|------------|--------------------------------|
| 81 | canfd_0_interrupts1_3_IRQn | Active | CAN0, Interrupt #1, Channel #3 |
| 82 | canfd_0_interrupts1_4_IRQn | Active | CAN0, Interrupt #1, Channel #4 |
| 83 | canfd_1_interrupts0_0_IRQn | Active | CAN1, Interrupt #0, Channel #0 |
| 84 | canfd_1_interrupts0_1_IRQn | Active | CAN1, Interrupt #0, Channel #1 |
| 85 | canfd_1_interrupts0_2_IRQn | Active | CAN1, Interrupt #0, Channel #2 |
| 86 | canfd_1_interrupts0_3_IRQn | Active | CAN1, Interrupt #0, Channel #3 |
| 87 | canfd_1_interrupts0_4_IRQn | Active | CAN1, Interrupt #0, Channel #4 |
| 88 | canfd_1_interrupts1_0_IRQn | Active | CAN1, Interrupt #1, Channel #0 |
| 89 | canfd_1_interrupts1_1_IRQn | Active | CAN1, Interrupt #1, Channel #1 |
| 90 | canfd_1_interrupts1_2_IRQn | Active | CAN1, Interrupt #1, Channel #2 |
| 91 | canfd_1_interrupts1_3_IRQn | Active | CAN1, Interrupt #1, Channel #3 |
| 92 | canfd_1_interrupts1_4_IRQn | Active | CAN1, Interrupt #1, Channel #4 |
| 93 | lin_0_interrupts_0_IRQn | Active | LIN0, Channel #0 Interrupt |
| 94 | lin_0_interrupts_1_IRQn | Active | LIN0, Channel #1 Interrupt |
| 95 | lin_0_interrupts_2_IRQn | Active | LIN0, Channel #2 Interrupt |
| 96 | lin_0_interrupts_3_IRQn | Active | LIN0, Channel #3 Interrupt |
| 97 | lin_0_interrupts_4_IRQn | Active | LIN0, Channel #4 Interrupt |
| 98 | lin_0_interrupts_5_IRQn | Active | LIN0, Channel #5 Interrupt |
| 99 | lin_0_interrupts_6_IRQn | Active | LIN0, Channel #6 Interrupt |
| 100 | lin_0_interrupts_7_IRQn | Active | LIN0, Channel #7 Interrupt |
| 101 | lin_0_interrupts_8_IRQn | Active | LIN0, Channel #8 Interrupt |
| 102 | lin_0_interrupts_9_IRQn | Active | LIN0, Channel #9 Interrupt |
| 103 | lin_0_interrupts_10_IRQn | Active | LIN0, Channel #10 Interrupt |
| 104 | lin_0_interrupts_11_IRQn | Active | LIN0, Channel #11 Interrupt |
| 105 | lin_0_interrupts_12_IRQn | Active | LIN0, Channel #12 Interrupt |
| 106 | lin_0_interrupts_13_IRQn | Active | LIN0, Channel #13 Interrupt |
| 107 | lin_0_interrupts_14_IRQn | Active | LIN0, Channel #14 Interrupt |
| 108 | lin_0_interrupts_15_IRQn | Active | LIN0, Channel #15 Interrupt |
| 109 | lin_0_interrupts_16_IRQn | Active | LIN0, Channel #16 Interrupt |
| 110 | lin_0_interrupts_17_IRQn | Active | LIN0, Channel #17 Interrupt |
| 111 | lin_0_interrupts_18_IRQn | Active | LIN0, Channel #18 Interrupt |
| 112 | lin_0_interrupts_19_IRQn | Active | LIN0, Channel #19 Interrupt |
| 113 | scb_1_interrupt_IRQn | Active | SCB1 Interrupt |
| 114 | scb_2_interrupt_IRQn | Active | SCB2 Interrupt |
| 115 | scb_3_interrupt_IRQn | Active | SCB3 Interrupt |
| 116 | scb_4_interrupt_IRQn | Active | SCB4 Interrupt |
| 117 | scb_5_interrupt_IRQn | Active | SCB5 Interrupt |
| 118 | scb_6_interrupt_IRQn | Active | SCB6 Interrupt |
| 119 | scb_7_interrupt_IRQn | Active | SCB7 Interrupt |
| 120 | scb_8_interrupt_IRQn | Active | SCB8 Interrupt |
| 121 | scb_9_interrupt_IRQn | Active | SCB9 Interrupt |

Table 13-1. Peripheral Interrupt Assignments and Wake-up Sources *(continued)*

| Interrupt | Source | Power Mode | Description |
|-----------|-------------------------------|------------|-------------------------------------|
| 122 | scb_10_interrupt_IRQn | Active | SCB10 Interrupt |
| 123 | pass_0_interrupts_sar_0_IRQn | Active | SAR0, Logical Channel #0 Interrupt |
| 124 | pass_0_interrupts_sar_1_IRQn | Active | SAR0, Logical Channel #1 Interrupt |
| 125 | pass_0_interrupts_sar_2_IRQn | Active | SAR0, Logical Channel #2 Interrupt |
| 126 | pass_0_interrupts_sar_3_IRQn | Active | SAR0, Logical Channel #3 Interrupt |
| 127 | pass_0_interrupts_sar_4_IRQn | Active | SAR0, Logical Channel #4 Interrupt |
| 128 | pass_0_interrupts_sar_5_IRQn | Active | SAR0, Logical Channel #5 Interrupt |
| 129 | pass_0_interrupts_sar_6_IRQn | Active | SAR0, Logical Channel #6 Interrupt |
| 130 | pass_0_interrupts_sar_7_IRQn | Active | SAR0, Logical Channel #7 Interrupt |
| 131 | pass_0_interrupts_sar_8_IRQn | Active | SAR0, Logical Channel #8 Interrupt |
| 132 | pass_0_interrupts_sar_9_IRQn | Active | SAR0, Logical Channel #9 Interrupt |
| 133 | pass_0_interrupts_sar_10_IRQn | Active | SAR0, Logical Channel #10 Interrupt |
| 134 | pass_0_interrupts_sar_11_IRQn | Active | SAR0, Logical Channel #11 Interrupt |
| 135 | pass_0_interrupts_sar_12_IRQn | Active | SAR0, Logical Channel #12 Interrupt |
| 136 | pass_0_interrupts_sar_13_IRQn | Active | SAR0, Logical Channel #13 Interrupt |
| 137 | pass_0_interrupts_sar_14_IRQn | Active | SAR0, Logical Channel #14 Interrupt |
| 138 | pass_0_interrupts_sar_15_IRQn | Active | SAR0, Logical Channel #15 Interrupt |
| 139 | pass_0_interrupts_sar_16_IRQn | Active | SAR0, Logical Channel #16 Interrupt |
| 140 | pass_0_interrupts_sar_17_IRQn | Active | SAR0, Logical Channel #17 Interrupt |
| 141 | pass_0_interrupts_sar_18_IRQn | Active | SAR0, Logical Channel #18 Interrupt |
| 142 | pass_0_interrupts_sar_19_IRQn | Active | SAR0, Logical Channel #19 Interrupt |
| 143 | pass_0_interrupts_sar_20_IRQn | Active | SAR0, Logical Channel #20 Interrupt |
| 144 | pass_0_interrupts_sar_21_IRQn | Active | SAR0, Logical Channel #21 Interrupt |
| 145 | pass_0_interrupts_sar_22_IRQn | Active | SAR0, Logical Channel #22 Interrupt |
| 146 | pass_0_interrupts_sar_23_IRQn | Active | SAR0, Logical Channel #23 Interrupt |
| 147 | pass_0_interrupts_sar_24_IRQn | Active | SAR0, Logical Channel #24 Interrupt |
| 148 | pass_0_interrupts_sar_25_IRQn | Active | SAR0, Logical Channel #25 Interrupt |
| 149 | pass_0_interrupts_sar_26_IRQn | Active | SAR0, Logical Channel #26 Interrupt |
| 150 | pass_0_interrupts_sar_27_IRQn | Active | SAR0, Logical Channel #27 Interrupt |
| 151 | pass_0_interrupts_sar_28_IRQn | Active | SAR0, Logical Channel #28 Interrupt |
| 152 | pass_0_interrupts_sar_29_IRQn | Active | SAR0, Logical Channel #29 Interrupt |
| 153 | pass_0_interrupts_sar_30_IRQn | Active | SAR0, Logical Channel #30 Interrupt |
| 154 | pass_0_interrupts_sar_31_IRQn | Active | SAR0, Logical Channel #31 Interrupt |
| 155 | pass_0_interrupts_sar_32_IRQn | Active | SAR1, Logical Channel #0 Interrupt |
| 156 | pass_0_interrupts_sar_33_IRQn | Active | SAR1, Logical Channel #1 Interrupt |
| 157 | pass_0_interrupts_sar_34_IRQn | Active | SAR1, Logical Channel #2 Interrupt |
| 158 | pass_0_interrupts_sar_35_IRQn | Active | SAR1, Logical Channel #3 Interrupt |
| 159 | pass_0_interrupts_sar_36_IRQn | Active | SAR1, Logical Channel #4 Interrupt |
| 160 | pass_0_interrupts_sar_37_IRQn | Active | SAR1, Logical Channel #5 Interrupt |
| 161 | pass_0_interrupts_sar_38_IRQn | Active | SAR1, Logical Channel #6 Interrupt |
| 162 | pass_0_interrupts_sar_39_IRQn | Active | SAR1, Logical Channel #7 Interrupt |

Table 13-1. Peripheral Interrupt Assignments and Wake-up Sources *(continued)*

| Interrupt | Source | Power Mode | Description |
|-----------|-------------------------------|------------|-------------------------------------|
| 163 | pass_0_interrupts_sar_40_IRQn | Active | SAR1, Logical Channel #8 Interrupt |
| 164 | pass_0_interrupts_sar_41_IRQn | Active | SAR1, Logical Channel #9 Interrupt |
| 165 | pass_0_interrupts_sar_42_IRQn | Active | SAR1, Logical Channel #10 Interrupt |
| 166 | pass_0_interrupts_sar_43_IRQn | Active | SAR1, Logical Channel #11 Interrupt |
| 167 | pass_0_interrupts_sar_44_IRQn | Active | SAR1, Logical Channel #12 Interrupt |
| 168 | pass_0_interrupts_sar_45_IRQn | Active | SAR1, Logical Channel #13 Interrupt |
| 169 | pass_0_interrupts_sar_46_IRQn | Active | SAR1, Logical Channel #14 Interrupt |
| 170 | pass_0_interrupts_sar_47_IRQn | Active | SAR1, Logical Channel #15 Interrupt |
| 171 | pass_0_interrupts_sar_48_IRQn | Active | SAR1, Logical Channel #16 Interrupt |
| 172 | pass_0_interrupts_sar_49_IRQn | Active | SAR1, Logical Channel #17 Interrupt |
| 173 | pass_0_interrupts_sar_50_IRQn | Active | SAR1, Logical Channel #18 Interrupt |
| 174 | pass_0_interrupts_sar_51_IRQn | Active | SAR1, Logical Channel #19 Interrupt |
| 175 | pass_0_interrupts_sar_52_IRQn | Active | SAR1, Logical Channel #20 Interrupt |
| 176 | pass_0_interrupts_sar_53_IRQn | Active | SAR1, Logical Channel #21 Interrupt |
| 177 | pass_0_interrupts_sar_54_IRQn | Active | SAR1, Logical Channel #22 Interrupt |
| 178 | pass_0_interrupts_sar_55_IRQn | Active | SAR1, Logical Channel #23 Interrupt |
| 179 | pass_0_interrupts_sar_56_IRQn | Active | SAR1, Logical Channel #24 Interrupt |
| 180 | pass_0_interrupts_sar_57_IRQn | Active | SAR1, Logical Channel #25 Interrupt |
| 181 | pass_0_interrupts_sar_58_IRQn | Active | SAR1, Logical Channel #26 Interrupt |
| 182 | pass_0_interrupts_sar_59_IRQn | Active | SAR1, Logical Channel #27 Interrupt |
| 183 | pass_0_interrupts_sar_60_IRQn | Active | SAR1, Logical Channel #28 Interrupt |
| 184 | pass_0_interrupts_sar_61_IRQn | Active | SAR1, Logical Channel #29 Interrupt |
| 185 | pass_0_interrupts_sar_62_IRQn | Active | SAR1, Logical Channel #30 Interrupt |
| 186 | pass_0_interrupts_sar_63_IRQn | Active | SAR1, Logical Channel #31 Interrupt |
| 187 | pass_0_interrupts_sar_64_IRQn | Active | SAR2, Logical Channel #0 Interrupt |
| 188 | pass_0_interrupts_sar_65_IRQn | Active | SAR2, Logical Channel #1 Interrupt |
| 189 | pass_0_interrupts_sar_66_IRQn | Active | SAR2, Logical Channel #2 Interrupt |
| 190 | pass_0_interrupts_sar_67_IRQn | Active | SAR2, Logical Channel #3 Interrupt |
| 191 | pass_0_interrupts_sar_68_IRQn | Active | SAR2, Logical Channel #4 Interrupt |
| 192 | pass_0_interrupts_sar_69_IRQn | Active | SAR2, Logical Channel #5 Interrupt |
| 193 | pass_0_interrupts_sar_70_IRQn | Active | SAR2, Logical Channel #6 Interrupt |
| 194 | pass_0_interrupts_sar_71_IRQn | Active | SAR2, Logical Channel #7 Interrupt |
| 195 | pass_0_interrupts_sar_72_IRQn | Active | SAR2, Logical Channel #8 Interrupt |
| 196 | pass_0_interrupts_sar_73_IRQn | Active | SAR2, Logical Channel #9 Interrupt |
| 197 | pass_0_interrupts_sar_74_IRQn | Active | SAR2, Logical Channel #10 Interrupt |
| 198 | pass_0_interrupts_sar_75_IRQn | Active | SAR2, Logical Channel #11 Interrupt |
| 199 | pass_0_interrupts_sar_76_IRQn | Active | SAR2, Logical Channel #12 Interrupt |
| 200 | pass_0_interrupts_sar_77_IRQn | Active | SAR2, Logical Channel #13 Interrupt |
| 201 | pass_0_interrupts_sar_78_IRQn | Active | SAR2, Logical Channel #14 Interrupt |
| 202 | pass_0_interrupts_sar_79_IRQn | Active | SAR2, Logical Channel #15 Interrupt |
| 203 | pass_0_interrupts_sar_80_IRQn | Active | SAR2, Logical Channel #16 Interrupt |

Table 13-1. Peripheral Interrupt Assignments and Wake-up Sources *(continued)*

| Interrupt | Source | Power Mode | Description |
|-----------|-------------------------------|------------|-------------------------------------|
| 204 | pass_0_interrupts_sar_81_IRQn | Active | SAR2, Logical Channel #17 Interrupt |
| 205 | pass_0_interrupts_sar_82_IRQn | Active | SAR2, Logical Channel #18 Interrupt |
| 206 | pass_0_interrupts_sar_83_IRQn | Active | SAR2, Logical Channel #19 Interrupt |
| 207 | pass_0_interrupts_sar_84_IRQn | Active | SAR2, Logical Channel #20 Interrupt |
| 208 | pass_0_interrupts_sar_85_IRQn | Active | SAR2, Logical Channel #21 Interrupt |
| 209 | pass_0_interrupts_sar_86_IRQn | Active | SAR2, Logical Channel #22 Interrupt |
| 210 | pass_0_interrupts_sar_87_IRQn | Active | SAR2, Logical Channel #23 Interrupt |
| 211 | pass_0_interrupts_sar_88_IRQn | Active | SAR2, Logical Channel #24 Interrupt |
| 212 | pass_0_interrupts_sar_89_IRQn | Active | SAR2, Logical Channel #25 Interrupt |
| 213 | pass_0_interrupts_sar_90_IRQn | Active | SAR2, Logical Channel #26 Interrupt |
| 214 | pass_0_interrupts_sar_91_IRQn | Active | SAR2, Logical Channel #27 Interrupt |
| 215 | pass_0_interrupts_sar_92_IRQn | Active | SAR2, Logical Channel #28 Interrupt |
| 216 | pass_0_interrupts_sar_93_IRQn | Active | SAR2, Logical Channel #29 Interrupt |
| 217 | pass_0_interrupts_sar_94_IRQn | Active | SAR2, Logical Channel #30 Interrupt |
| 218 | pass_0_interrupts_sar_95_IRQn | Active | SAR2, Logical Channel #31 Interrupt |
| 219 | cpuss_interrupts_dmac_0_IRQn | Active | CPUSS M-DMA0, Channel #0 Interrupt |
| 220 | cpuss_interrupts_dmac_1_IRQn | Active | CPUSS M-DMA0, Channel #1 Interrupt |
| 221 | cpuss_interrupts_dmac_2_IRQn | Active | CPUSS M-DMA0, Channel #2 Interrupt |
| 222 | cpuss_interrupts_dmac_3_IRQn | Active | CPUSS M-DMA0, Channel #3 Interrupt |
| 223 | cpuss_interrupts_dmac_4_IRQn | Active | CPUSS M-DMA0, Channel #4 Interrupt |
| 224 | cpuss_interrupts_dmac_5_IRQn | Active | CPUSS M-DMA0, Channel #5 Interrupt |
| 225 | cpuss_interrupts_dmac_6_IRQn | Active | CPUSS M-DMA0, Channel #6 Interrupt |
| 226 | cpuss_interrupts_dmac_7_IRQn | Active | CPUSS M-DMA0, Channel #7 Interrupt |
| 227 | cpuss_interrupts_dw0_0_IRQn | Active | CPUSS P-DMA0, Channel #0 Interrupt |
| 228 | cpuss_interrupts_dw0_1_IRQn | Active | CPUSS P-DMA0, Channel #1 Interrupt |
| 229 | cpuss_interrupts_dw0_2_IRQn | Active | CPUSS P-DMA0, Channel #2 Interrupt |
| 230 | cpuss_interrupts_dw0_3_IRQn | Active | CPUSS P-DMA0, Channel #3 Interrupt |
| 231 | cpuss_interrupts_dw0_4_IRQn | Active | CPUSS P-DMA0, Channel #4 Interrupt |
| 232 | cpuss_interrupts_dw0_5_IRQn | Active | CPUSS P-DMA0, Channel #5 Interrupt |
| 233 | cpuss_interrupts_dw0_6_IRQn | Active | CPUSS P-DMA0, Channel #6 Interrupt |
| 234 | cpuss_interrupts_dw0_7_IRQn | Active | CPUSS P-DMA0, Channel #7 Interrupt |
| 235 | cpuss_interrupts_dw0_8_IRQn | Active | CPUSS P-DMA0, Channel #8 Interrupt |
| 236 | cpuss_interrupts_dw0_9_IRQn | Active | CPUSS P-DMA0, Channel #9 Interrupt |
| 237 | cpuss_interrupts_dw0_10_IRQn | Active | CPUSS P-DMA0, Channel #10 Interrupt |
| 238 | cpuss_interrupts_dw0_11_IRQn | Active | CPUSS P-DMA0, Channel #11 Interrupt |
| 239 | cpuss_interrupts_dw0_12_IRQn | Active | CPUSS P-DMA0, Channel #12 Interrupt |
| 240 | cpuss_interrupts_dw0_13_IRQn | Active | CPUSS P-DMA0, Channel #13 Interrupt |
| 241 | cpuss_interrupts_dw0_14_IRQn | Active | CPUSS P-DMA0, Channel #14 Interrupt |
| 242 | cpuss_interrupts_dw0_15_IRQn | Active | CPUSS P-DMA0, Channel #15 Interrupt |
| 243 | cpuss_interrupts_dw0_16_IRQn | Active | CPUSS P-DMA0, Channel #16 Interrupt |
| 244 | cpuss_interrupts_dw0_17_IRQn | Active | CPUSS P-DMA0, Channel #17 Interrupt |

Table 13-1. Peripheral Interrupt Assignments and Wake-up Sources (continued)

| Interrupt | Source | Power Mode | Description |
|-----------|------------------------------|------------|-------------------------------------|
| 245 | cpuss_interrupts_dw0_18_IRQn | Active | CPUSS P-DMA0, Channel #18 Interrupt |
| 246 | cpuss_interrupts_dw0_19_IRQn | Active | CPUSS P-DMA0, Channel #19 Interrupt |
| 247 | cpuss_interrupts_dw0_20_IRQn | Active | CPUSS P-DMA0, Channel #20 Interrupt |
| 248 | cpuss_interrupts_dw0_21_IRQn | Active | CPUSS P-DMA0, Channel #21 Interrupt |
| 249 | cpuss_interrupts_dw0_22_IRQn | Active | CPUSS P-DMA0, Channel #22 Interrupt |
| 250 | cpuss_interrupts_dw0_23_IRQn | Active | CPUSS P-DMA0, Channel #23 Interrupt |
| 251 | cpuss_interrupts_dw0_24_IRQn | Active | CPUSS P-DMA0, Channel #24 Interrupt |
| 252 | cpuss_interrupts_dw0_25_IRQn | Active | CPUSS P-DMA0, Channel #25 Interrupt |
| 253 | cpuss_interrupts_dw0_26_IRQn | Active | CPUSS P-DMA0, Channel #26 Interrupt |
| 254 | cpuss_interrupts_dw0_27_IRQn | Active | CPUSS P-DMA0, Channel #27 Interrupt |
| 255 | cpuss_interrupts_dw0_28_IRQn | Active | CPUSS P-DMA0, Channel #28 Interrupt |
| 256 | cpuss_interrupts_dw0_29_IRQn | Active | CPUSS P-DMA0, Channel #29 Interrupt |
| 257 | cpuss_interrupts_dw0_30_IRQn | Active | CPUSS P-DMA0, Channel #30 Interrupt |
| 258 | cpuss_interrupts_dw0_31_IRQn | Active | CPUSS P-DMA0, Channel #31 Interrupt |
| 259 | cpuss_interrupts_dw0_32_IRQn | Active | CPUSS P-DMA0, Channel #32 Interrupt |
| 260 | cpuss_interrupts_dw0_33_IRQn | Active | CPUSS P-DMA0, Channel #33 Interrupt |
| 261 | cpuss_interrupts_dw0_34_IRQn | Active | CPUSS P-DMA0, Channel #34 Interrupt |
| 262 | cpuss_interrupts_dw0_35_IRQn | Active | CPUSS P-DMA0, Channel #35 Interrupt |
| 263 | cpuss_interrupts_dw0_36_IRQn | Active | CPUSS P-DMA0, Channel #36 Interrupt |
| 264 | cpuss_interrupts_dw0_37_IRQn | Active | CPUSS P-DMA0, Channel #37 Interrupt |
| 265 | cpuss_interrupts_dw0_38_IRQn | Active | CPUSS P-DMA0, Channel #38 Interrupt |
| 266 | cpuss_interrupts_dw0_39_IRQn | Active | CPUSS P-DMA0, Channel #39 Interrupt |
| 267 | cpuss_interrupts_dw0_40_IRQn | Active | CPUSS P-DMA0, Channel #40 Interrupt |
| 268 | cpuss_interrupts_dw0_41_IRQn | Active | CPUSS P-DMA0, Channel #41 Interrupt |
| 269 | cpuss_interrupts_dw0_42_IRQn | Active | CPUSS P-DMA0, Channel #42 Interrupt |
| 270 | cpuss_interrupts_dw0_43_IRQn | Active | CPUSS P-DMA0, Channel #43 Interrupt |
| 271 | cpuss_interrupts_dw0_44_IRQn | Active | CPUSS P-DMA0, Channel #44 Interrupt |
| 272 | cpuss_interrupts_dw0_45_IRQn | Active | CPUSS P-DMA0, Channel #45 Interrupt |
| 273 | cpuss_interrupts_dw0_46_IRQn | Active | CPUSS P-DMA0, Channel #46 Interrupt |
| 274 | cpuss_interrupts_dw0_47_IRQn | Active | CPUSS P-DMA0, Channel #47 Interrupt |
| 275 | cpuss_interrupts_dw0_48_IRQn | Active | CPUSS P-DMA0, Channel #48 Interrupt |
| 276 | cpuss_interrupts_dw0_49_IRQn | Active | CPUSS P-DMA0, Channel #49 Interrupt |
| 277 | cpuss_interrupts_dw0_50_IRQn | Active | CPUSS P-DMA0, Channel #50 Interrupt |
| 278 | cpuss_interrupts_dw0_51_IRQn | Active | CPUSS P-DMA0, Channel #51 Interrupt |
| 279 | cpuss_interrupts_dw0_52_IRQn | Active | CPUSS P-DMA0, Channel #52 Interrupt |
| 280 | cpuss_interrupts_dw0_53_IRQn | Active | CPUSS P-DMA0, Channel #53 Interrupt |
| 281 | cpuss_interrupts_dw0_54_IRQn | Active | CPUSS P-DMA0, Channel #54 Interrupt |
| 282 | cpuss_interrupts_dw0_55_IRQn | Active | CPUSS P-DMA0, Channel #55 Interrupt |
| 283 | cpuss_interrupts_dw0_56_IRQn | Active | CPUSS P-DMA0, Channel #56 Interrupt |
| 284 | cpuss_interrupts_dw0_57_IRQn | Active | CPUSS P-DMA0, Channel #57 Interrupt |
| 285 | cpuss_interrupts_dw0_58_IRQn | Active | CPUSS P-DMA0, Channel #58 Interrupt |

Table 13-1. Peripheral Interrupt Assignments and Wake-up Sources (continued)

| Interrupt | Source | Power Mode | Description |
|-----------|------------------------------|------------|-------------------------------------|
| 286 | cpuss_interrupts_dw0_59_IRQn | Active | CPUSS P-DMA0, Channel #59 Interrupt |
| 287 | cpuss_interrupts_dw0_60_IRQn | Active | CPUSS P-DMA0, Channel #60 Interrupt |
| 288 | cpuss_interrupts_dw0_61_IRQn | Active | CPUSS P-DMA0, Channel #61 Interrupt |
| 289 | cpuss_interrupts_dw0_62_IRQn | Active | CPUSS P-DMA0, Channel #62 Interrupt |
| 290 | cpuss_interrupts_dw0_63_IRQn | Active | CPUSS P-DMA0, Channel #63 Interrupt |
| 291 | cpuss_interrupts_dw0_64_IRQn | Active | CPUSS P-DMA0, Channel #64 Interrupt |
| 292 | cpuss_interrupts_dw0_65_IRQn | Active | CPUSS P-DMA0, Channel #65 Interrupt |
| 293 | cpuss_interrupts_dw0_66_IRQn | Active | CPUSS P-DMA0, Channel #66 Interrupt |
| 294 | cpuss_interrupts_dw0_67_IRQn | Active | CPUSS P-DMA0, Channel #67 Interrupt |
| 295 | cpuss_interrupts_dw0_68_IRQn | Active | CPUSS P-DMA0, Channel #68 Interrupt |
| 296 | cpuss_interrupts_dw0_69_IRQn | Active | CPUSS P-DMA0, Channel #69 Interrupt |
| 297 | cpuss_interrupts_dw0_70_IRQn | Active | CPUSS P-DMA0, Channel #70 Interrupt |
| 298 | cpuss_interrupts_dw0_71_IRQn | Active | CPUSS P-DMA0, Channel #71 Interrupt |
| 299 | cpuss_interrupts_dw0_72_IRQn | Active | CPUSS P-DMA0, Channel #72 Interrupt |
| 300 | cpuss_interrupts_dw0_73_IRQn | Active | CPUSS P-DMA0, Channel #73 Interrupt |
| 301 | cpuss_interrupts_dw0_74_IRQn | Active | CPUSS P-DMA0, Channel #74 Interrupt |
| 302 | cpuss_interrupts_dw0_75_IRQn | Active | CPUSS P-DMA0, Channel #75 Interrupt |
| 303 | cpuss_interrupts_dw0_76_IRQn | Active | CPUSS P-DMA0, Channel #76 Interrupt |
| 304 | cpuss_interrupts_dw0_77_IRQn | Active | CPUSS P-DMA0, Channel #77 Interrupt |
| 305 | cpuss_interrupts_dw0_78_IRQn | Active | CPUSS P-DMA0, Channel #78 Interrupt |
| 306 | cpuss_interrupts_dw0_79_IRQn | Active | CPUSS P-DMA0, Channel #79 Interrupt |
| 307 | cpuss_interrupts_dw0_80_IRQn | Active | CPUSS P-DMA0, Channel #80 Interrupt |
| 308 | cpuss_interrupts_dw0_81_IRQn | Active | CPUSS P-DMA0, Channel #81 Interrupt |
| 309 | cpuss_interrupts_dw0_82_IRQn | Active | CPUSS P-DMA0, Channel #82 Interrupt |
| 310 | cpuss_interrupts_dw0_83_IRQn | Active | CPUSS P-DMA0, Channel #83 Interrupt |
| 311 | cpuss_interrupts_dw0_84_IRQn | Active | CPUSS P-DMA0, Channel #84 Interrupt |
| 312 | cpuss_interrupts_dw0_85_IRQn | Active | CPUSS P-DMA0, Channel #85 Interrupt |
| 313 | cpuss_interrupts_dw0_86_IRQn | Active | CPUSS P-DMA0, Channel #86 Interrupt |
| 314 | cpuss_interrupts_dw0_87_IRQn | Active | CPUSS P-DMA0, Channel #87 Interrupt |
| 315 | cpuss_interrupts_dw0_88_IRQn | Active | CPUSS P-DMA0, Channel #88 Interrupt |
| 316 | cpuss_interrupts_dw0_89_IRQn | Active | CPUSS P-DMA0, Channel #89 Interrupt |
| 317 | cpuss_interrupts_dw0_90_IRQn | Active | CPUSS P-DMA0, Channel #90 Interrupt |
| 318 | cpuss_interrupts_dw0_91_IRQn | Active | CPUSS P-DMA0, Channel #91 Interrupt |
| 319 | cpuss_interrupts_dw0_92_IRQn | Active | CPUSS P-DMA0, Channel #92 Interrupt |
| 320 | cpuss_interrupts_dw0_93_IRQn | Active | CPUSS P-DMA0, Channel #93 Interrupt |
| 321 | cpuss_interrupts_dw0_94_IRQn | Active | CPUSS P-DMA0, Channel #94 Interrupt |
| 322 | cpuss_interrupts_dw0_95_IRQn | Active | CPUSS P-DMA0, Channel #95 Interrupt |
| 323 | cpuss_interrupts_dw0_96_IRQn | Active | CPUSS P-DMA0, Channel #96 Interrupt |
| 324 | cpuss_interrupts_dw0_97_IRQn | Active | CPUSS P-DMA0, Channel #97 Interrupt |
| 325 | cpuss_interrupts_dw0_98_IRQn | Active | CPUSS P-DMA0, Channel #98 Interrupt |
| 326 | cpuss_interrupts_dw0_99_IRQn | Active | CPUSS P-DMA0, Channel #99 Interrupt |

Table 13-1. Peripheral Interrupt Assignments and Wake-up Sources *(continued)*

| Interrupt | Source | Power Mode | Description |
|-----------|-------------------------------|------------|--------------------------------------|
| 327 | cpuss_interrupts_dw0_100_IRQn | Active | CPUSS P-DMA0, Channel #100 Interrupt |
| 328 | cpuss_interrupts_dw0_101_IRQn | Active | CPUSS P-DMA0, Channel #101 Interrupt |
| 329 | cpuss_interrupts_dw0_102_IRQn | Active | CPUSS P-DMA0, Channel #102 Interrupt |
| 330 | cpuss_interrupts_dw0_103_IRQn | Active | CPUSS P-DMA0, Channel #103 Interrupt |
| 331 | cpuss_interrupts_dw0_104_IRQn | Active | CPUSS P-DMA0, Channel #104 Interrupt |
| 332 | cpuss_interrupts_dw0_105_IRQn | Active | CPUSS P-DMA0, Channel #105 Interrupt |
| 333 | cpuss_interrupts_dw0_106_IRQn | Active | CPUSS P-DMA0, Channel #106 Interrupt |
| 334 | cpuss_interrupts_dw0_107_IRQn | Active | CPUSS P-DMA0, Channel #107 Interrupt |
| 335 | cpuss_interrupts_dw0_108_IRQn | Active | CPUSS P-DMA0, Channel #108 Interrupt |
| 336 | cpuss_interrupts_dw0_109_IRQn | Active | CPUSS P-DMA0, Channel #109 Interrupt |
| 337 | cpuss_interrupts_dw0_110_IRQn | Active | CPUSS P-DMA0, Channel #110 Interrupt |
| 338 | cpuss_interrupts_dw0_111_IRQn | Active | CPUSS P-DMA0, Channel #111 Interrupt |
| 339 | cpuss_interrupts_dw0_112_IRQn | Active | CPUSS P-DMA0, Channel #112 Interrupt |
| 340 | cpuss_interrupts_dw0_113_IRQn | Active | CPUSS P-DMA0, Channel #113 Interrupt |
| 341 | cpuss_interrupts_dw0_114_IRQn | Active | CPUSS P-DMA0, Channel #114 Interrupt |
| 342 | cpuss_interrupts_dw0_115_IRQn | Active | CPUSS P-DMA0, Channel #115 Interrupt |
| 343 | cpuss_interrupts_dw0_116_IRQn | Active | CPUSS P-DMA0, Channel #116 Interrupt |
| 344 | cpuss_interrupts_dw0_117_IRQn | Active | CPUSS P-DMA0, Channel #117 Interrupt |
| 345 | cpuss_interrupts_dw0_118_IRQn | Active | CPUSS P-DMA0, Channel #118 Interrupt |
| 346 | cpuss_interrupts_dw0_119_IRQn | Active | CPUSS P-DMA0, Channel #119 Interrupt |
| 347 | cpuss_interrupts_dw0_120_IRQn | Active | CPUSS P-DMA0, Channel #120 Interrupt |
| 348 | cpuss_interrupts_dw0_121_IRQn | Active | CPUSS P-DMA0, Channel #121 Interrupt |
| 349 | cpuss_interrupts_dw0_122_IRQn | Active | CPUSS P-DMA0, Channel #122 Interrupt |
| 350 | cpuss_interrupts_dw0_123_IRQn | Active | CPUSS P-DMA0, Channel #123 Interrupt |
| 351 | cpuss_interrupts_dw0_124_IRQn | Active | CPUSS P-DMA0, Channel #124 Interrupt |
| 352 | cpuss_interrupts_dw0_125_IRQn | Active | CPUSS P-DMA0, Channel #125 Interrupt |
| 353 | cpuss_interrupts_dw0_126_IRQn | Active | CPUSS P-DMA0, Channel #126 Interrupt |
| 354 | cpuss_interrupts_dw0_127_IRQn | Active | CPUSS P-DMA0, Channel #127 Interrupt |
| 355 | cpuss_interrupts_dw0_128_IRQn | Active | CPUSS P-DMA0, Channel #128 Interrupt |
| 356 | cpuss_interrupts_dw0_129_IRQn | Active | CPUSS P-DMA0, Channel #129 Interrupt |
| 357 | cpuss_interrupts_dw0_130_IRQn | Active | CPUSS P-DMA0, Channel #130 Interrupt |
| 358 | cpuss_interrupts_dw0_131_IRQn | Active | CPUSS P-DMA0, Channel #131 Interrupt |
| 359 | cpuss_interrupts_dw0_132_IRQn | Active | CPUSS P-DMA0, Channel #132 Interrupt |
| 360 | cpuss_interrupts_dw0_133_IRQn | Active | CPUSS P-DMA0, Channel #133 Interrupt |
| 361 | cpuss_interrupts_dw0_134_IRQn | Active | CPUSS P-DMA0, Channel #134 Interrupt |
| 362 | cpuss_interrupts_dw0_135_IRQn | Active | CPUSS P-DMA0, Channel #135 Interrupt |
| 363 | cpuss_interrupts_dw0_136_IRQn | Active | CPUSS P-DMA0, Channel #136 Interrupt |
| 364 | cpuss_interrupts_dw0_137_IRQn | Active | CPUSS P-DMA0, Channel #137 Interrupt |
| 365 | cpuss_interrupts_dw0_138_IRQn | Active | CPUSS P-DMA0, Channel #138 Interrupt |
| 366 | cpuss_interrupts_dw0_139_IRQn | Active | CPUSS P-DMA0, Channel #139 Interrupt |
| 367 | cpuss_interrupts_dw0_140_IRQn | Active | CPUSS P-DMA0, Channel #140 Interrupt |

Table 13-1. Peripheral Interrupt Assignments and Wake-up Sources *(continued)*

| Interrupt | Source | Power Mode | Description |
|-----------|-------------------------------|------------|--------------------------------------|
| 368 | cpuss_interrupts_dw0_141_IRQn | Active | CPUSS P-DMA0, Channel #141 Interrupt |
| 369 | cpuss_interrupts_dw0_142_IRQn | Active | CPUSS P-DMA0, Channel #142 Interrupt |
| 370 | cpuss_interrupts_dw1_0_IRQn | Active | CPUSS P-DMA1, Channel #0 Interrupt |
| 371 | cpuss_interrupts_dw1_1_IRQn | Active | CPUSS P-DMA1, Channel #1 Interrupt |
| 372 | cpuss_interrupts_dw1_2_IRQn | Active | CPUSS P-DMA1, Channel #2 Interrupt |
| 373 | cpuss_interrupts_dw1_3_IRQn | Active | CPUSS P-DMA1, Channel #3 Interrupt |
| 374 | cpuss_interrupts_dw1_4_IRQn | Active | CPUSS P-DMA1, Channel #4 Interrupt |
| 375 | cpuss_interrupts_dw1_5_IRQn | Active | CPUSS P-DMA1, Channel #5 Interrupt |
| 376 | cpuss_interrupts_dw1_6_IRQn | Active | CPUSS P-DMA1, Channel #6 Interrupt |
| 377 | cpuss_interrupts_dw1_7_IRQn | Active | CPUSS P-DMA1, Channel #7 Interrupt |
| 378 | cpuss_interrupts_dw1_8_IRQn | Active | CPUSS P-DMA1, Channel #8 Interrupt |
| 379 | cpuss_interrupts_dw1_9_IRQn | Active | CPUSS P-DMA1, Channel #9 Interrupt |
| 380 | cpuss_interrupts_dw1_10_IRQn | Active | CPUSS P-DMA1, Channel #10 Interrupt |
| 381 | cpuss_interrupts_dw1_11_IRQn | Active | CPUSS P-DMA1, Channel #11 Interrupt |
| 382 | cpuss_interrupts_dw1_12_IRQn | Active | CPUSS P-DMA1, Channel #12 Interrupt |
| 383 | cpuss_interrupts_dw1_13_IRQn | Active | CPUSS P-DMA1, Channel #13 Interrupt |
| 384 | cpuss_interrupts_dw1_14_IRQn | Active | CPUSS P-DMA1, Channel #14 Interrupt |
| 385 | cpuss_interrupts_dw1_15_IRQn | Active | CPUSS P-DMA1, Channel #15 Interrupt |
| 386 | cpuss_interrupts_dw1_16_IRQn | Active | CPUSS P-DMA1, Channel #16 Interrupt |
| 387 | cpuss_interrupts_dw1_17_IRQn | Active | CPUSS P-DMA1, Channel #17 Interrupt |
| 388 | cpuss_interrupts_dw1_18_IRQn | Active | CPUSS P-DMA1, Channel #18 Interrupt |
| 389 | cpuss_interrupts_dw1_19_IRQn | Active | CPUSS P-DMA1, Channel #19 Interrupt |
| 390 | cpuss_interrupts_dw1_20_IRQn | Active | CPUSS P-DMA1, Channel #20 Interrupt |
| 391 | cpuss_interrupts_dw1_21_IRQn | Active | CPUSS P-DMA1, Channel #21 Interrupt |
| 392 | cpuss_interrupts_dw1_22_IRQn | Active | CPUSS P-DMA1, Channel #22 Interrupt |
| 393 | cpuss_interrupts_dw1_23_IRQn | Active | CPUSS P-DMA1, Channel #23 Interrupt |
| 394 | cpuss_interrupts_dw1_24_IRQn | Active | CPUSS P-DMA1, Channel #24 Interrupt |
| 395 | cpuss_interrupts_dw1_25_IRQn | Active | CPUSS P-DMA1, Channel #25 Interrupt |
| 396 | cpuss_interrupts_dw1_26_IRQn | Active | CPUSS P-DMA1, Channel #26 Interrupt |
| 397 | cpuss_interrupts_dw1_27_IRQn | Active | CPUSS P-DMA1, Channel #27 Interrupt |
| 398 | cpuss_interrupts_dw1_28_IRQn | Active | CPUSS P-DMA1, Channel #28 Interrupt |
| 399 | cpuss_interrupts_dw1_29_IRQn | Active | CPUSS P-DMA1, Channel #29 Interrupt |
| 400 | cpuss_interrupts_dw1_30_IRQn | Active | CPUSS P-DMA1, Channel #30 Interrupt |
| 401 | cpuss_interrupts_dw1_31_IRQn | Active | CPUSS P-DMA1, Channel #31 Interrupt |
| 402 | cpuss_interrupts_dw1_32_IRQn | Active | CPUSS P-DMA1, Channel #32 Interrupt |
| 403 | cpuss_interrupts_dw1_33_IRQn | Active | CPUSS P-DMA1, Channel #33 Interrupt |
| 404 | cpuss_interrupts_dw1_34_IRQn | Active | CPUSS P-DMA1, Channel #34 Interrupt |
| 405 | cpuss_interrupts_dw1_35_IRQn | Active | CPUSS P-DMA1, Channel #35 Interrupt |
| 406 | cpuss_interrupts_dw1_36_IRQn | Active | CPUSS P-DMA1, Channel #36 Interrupt |
| 407 | cpuss_interrupts_dw1_37_IRQn | Active | CPUSS P-DMA1, Channel #37 Interrupt |
| 408 | cpuss_interrupts_dw1_38_IRQn | Active | CPUSS P-DMA1, Channel #38 Interrupt |

Table 13-1. Peripheral Interrupt Assignments and Wake-up Sources *(continued)*

| Interrupt | Source | Power Mode | Description |
|-----------|------------------------------|------------|--|
| 409 | cpuss_interrupts_dw1_39_IRQn | Active | CPUSS P-DMA1, Channel #39 Interrupt |
| 410 | cpuss_interrupts_dw1_40_IRQn | Active | CPUSS P-DMA1, Channel #40 Interrupt |
| 411 | cpuss_interrupts_dw1_41_IRQn | Active | CPUSS P-DMA1, Channel #41 Interrupt |
| 412 | cpuss_interrupts_dw1_42_IRQn | Active | CPUSS P-DMA1, Channel #42 Interrupt |
| 413 | cpuss_interrupts_dw1_43_IRQn | Active | CPUSS P-DMA1, Channel #43 Interrupt |
| 414 | cpuss_interrupts_dw1_44_IRQn | Active | CPUSS P-DMA1, Channel #44 Interrupt |
| 415 | cpuss_interrupts_dw1_45_IRQn | Active | CPUSS P-DMA1, Channel #45 Interrupt |
| 416 | cpuss_interrupts_dw1_46_IRQn | Active | CPUSS P-DMA1, Channel #46 Interrupt |
| 417 | cpuss_interrupts_dw1_47_IRQn | Active | CPUSS P-DMA1, Channel #47 Interrupt |
| 418 | cpuss_interrupts_dw1_48_IRQn | Active | CPUSS P-DMA1, Channel #48 Interrupt |
| 419 | cpuss_interrupts_dw1_49_IRQn | Active | CPUSS P-DMA1, Channel #49 Interrupt |
| 420 | cpuss_interrupts_dw1_50_IRQn | Active | CPUSS P-DMA1, Channel #50 Interrupt |
| 421 | cpuss_interrupts_dw1_51_IRQn | Active | CPUSS P-DMA1, Channel #51 Interrupt |
| 422 | cpuss_interrupts_dw1_52_IRQn | Active | CPUSS P-DMA1, Channel #52 Interrupt |
| 423 | cpuss_interrupts_dw1_53_IRQn | Active | CPUSS P-DMA1, Channel #53 Interrupt |
| 424 | cpuss_interrupts_dw1_54_IRQn | Active | CPUSS P-DMA1, Channel #54 Interrupt |
| 425 | cpuss_interrupts_dw1_55_IRQn | Active | CPUSS P-DMA1, Channel #55 Interrupt |
| 426 | cpuss_interrupts_dw1_56_IRQn | Active | CPUSS P-DMA1, Channel #56 Interrupt |
| 427 | cpuss_interrupts_dw1_57_IRQn | Active | CPUSS P-DMA1, Channel #57 Interrupt |
| 428 | cpuss_interrupts_dw1_58_IRQn | Active | CPUSS P-DMA1, Channel #58 Interrupt |
| 429 | cpuss_interrupts_dw1_59_IRQn | Active | CPUSS P-DMA1, Channel #59 Interrupt |
| 430 | cpuss_interrupts_dw1_60_IRQn | Active | CPUSS P-DMA1, Channel #60 Interrupt |
| 431 | cpuss_interrupts_dw1_61_IRQn | Active | CPUSS P-DMA1, Channel #61 Interrupt |
| 432 | cpuss_interrupts_dw1_62_IRQn | Active | CPUSS P-DMA1, Channel #62 Interrupt |
| 433 | cpuss_interrupts_dw1_63_IRQn | Active | CPUSS P-DMA1, Channel #63 Interrupt |
| 434 | cpuss_interrupts_dw1_64_IRQn | Active | CPUSS P-DMA1, Channel #64 Interrupt |
| 435 | tcpwm_1_interrupts_0_IRQn | Active | TCPWM1 Group #0, Counter #0 Interrupt |
| 436 | tcpwm_1_interrupts_1_IRQn | Active | TCPWM1 Group #0, Counter #1 Interrupt |
| 437 | tcpwm_1_interrupts_2_IRQn | Active | TCPWM1 Group #0, Counter #2 Interrupt |
| 438 | tcpwm_1_interrupts_3_IRQn | Active | TCPWM1 Group #0, Counter #3 Interrupt |
| 439 | tcpwm_1_interrupts_4_IRQn | Active | TCPWM1 Group #0, Counter #4 Interrupt |
| 440 | tcpwm_1_interrupts_5_IRQn | Active | TCPWM1 Group #0, Counter #5 Interrupt |
| 441 | tcpwm_1_interrupts_6_IRQn | Active | TCPWM1 Group #0, Counter #6 Interrupt |
| 442 | tcpwm_1_interrupts_7_IRQn | Active | TCPWM1 Group #0, Counter #7 Interrupt |
| 443 | tcpwm_1_interrupts_8_IRQn | Active | TCPWM1 Group #0, Counter #8 Interrupt |
| 444 | tcpwm_1_interrupts_9_IRQn | Active | TCPWM1 Group #0, Counter #9 Interrupt |
| 445 | tcpwm_1_interrupts_10_IRQn | Active | TCPWM1 Group #0, Counter #10 Interrupt |
| 446 | tcpwm_1_interrupts_11_IRQn | Active | TCPWM1 Group #0, Counter #11 Interrupt |
| 447 | tcpwm_1_interrupts_12_IRQn | Active | TCPWM1 Group #0, Counter #12 Interrupt |
| 448 | tcpwm_1_interrupts_13_IRQn | Active | TCPWM1 Group #0, Counter #13 Interrupt |
| 449 | tcpwm_1_interrupts_14_IRQn | Active | TCPWM1 Group #0, Counter #14 Interrupt |

Table 13-1. Peripheral Interrupt Assignments and Wake-up Sources *(continued)*

| Interrupt | Source | Power Mode | Description |
|-----------|----------------------------|------------|--|
| 450 | tcpwm_1_interrupts_15_IRQn | Active | TCPWM1 Group #0, Counter #15 Interrupt |
| 451 | tcpwm_1_interrupts_16_IRQn | Active | TCPWM1 Group #0, Counter #16 Interrupt |
| 452 | tcpwm_1_interrupts_17_IRQn | Active | TCPWM1 Group #0, Counter #17 Interrupt |
| 453 | tcpwm_1_interrupts_18_IRQn | Active | TCPWM1 Group #0, Counter #18 Interrupt |
| 454 | tcpwm_1_interrupts_19_IRQn | Active | TCPWM1 Group #0, Counter #19 Interrupt |
| 455 | tcpwm_1_interrupts_20_IRQn | Active | TCPWM1 Group #0, Counter #20 Interrupt |
| 456 | tcpwm_1_interrupts_21_IRQn | Active | TCPWM1 Group #0, Counter #21 Interrupt |
| 457 | tcpwm_1_interrupts_22_IRQn | Active | TCPWM1 Group #0, Counter #22 Interrupt |
| 458 | tcpwm_1_interrupts_23_IRQn | Active | TCPWM1 Group #0, Counter #23 Interrupt |
| 459 | tcpwm_1_interrupts_24_IRQn | Active | TCPWM1 Group #0, Counter #24 Interrupt |
| 460 | tcpwm_1_interrupts_25_IRQn | Active | TCPWM1 Group #0, Counter #25 Interrupt |
| 461 | tcpwm_1_interrupts_26_IRQn | Active | TCPWM1 Group #0, Counter #26 Interrupt |
| 462 | tcpwm_1_interrupts_27_IRQn | Active | TCPWM1 Group #0, Counter #27 Interrupt |
| 463 | tcpwm_1_interrupts_28_IRQn | Active | TCPWM1 Group #0, Counter #28 Interrupt |
| 464 | tcpwm_1_interrupts_29_IRQn | Active | TCPWM1 Group #0, Counter #29 Interrupt |
| 465 | tcpwm_1_interrupts_30_IRQn | Active | TCPWM1 Group #0, Counter #30 Interrupt |
| 466 | tcpwm_1_interrupts_31_IRQn | Active | TCPWM1 Group #0, Counter #31 Interrupt |
| 467 | tcpwm_1_interrupts_32_IRQn | Active | TCPWM1 Group #0, Counter #32 Interrupt |
| 468 | tcpwm_1_interrupts_33_IRQn | Active | TCPWM1 Group #0, Counter #33 Interrupt |
| 469 | tcpwm_1_interrupts_34_IRQn | Active | TCPWM1 Group #0, Counter #34 Interrupt |
| 470 | tcpwm_1_interrupts_35_IRQn | Active | TCPWM1 Group #0, Counter #35 Interrupt |
| 471 | tcpwm_1_interrupts_36_IRQn | Active | TCPWM1 Group #0, Counter #36 Interrupt |
| 472 | tcpwm_1_interrupts_37_IRQn | Active | TCPWM1 Group #0, Counter #37 Interrupt |
| 473 | tcpwm_1_interrupts_38_IRQn | Active | TCPWM1 Group #0, Counter #38 Interrupt |
| 474 | tcpwm_1_interrupts_39_IRQn | Active | TCPWM1 Group #0, Counter #39 Interrupt |
| 475 | tcpwm_1_interrupts_40_IRQn | Active | TCPWM1 Group #0, Counter #40 Interrupt |
| 476 | tcpwm_1_interrupts_41_IRQn | Active | TCPWM1 Group #0, Counter #41 Interrupt |
| 477 | tcpwm_1_interrupts_42_IRQn | Active | TCPWM1 Group #0, Counter #42 Interrupt |
| 478 | tcpwm_1_interrupts_43_IRQn | Active | TCPWM1 Group #0, Counter #43 Interrupt |
| 479 | tcpwm_1_interrupts_44_IRQn | Active | TCPWM1 Group #0, Counter #44 Interrupt |
| 480 | tcpwm_1_interrupts_45_IRQn | Active | TCPWM1 Group #0, Counter #45 Interrupt |
| 481 | tcpwm_1_interrupts_46_IRQn | Active | TCPWM1 Group #0, Counter #46 Interrupt |
| 482 | tcpwm_1_interrupts_47_IRQn | Active | TCPWM1 Group #0, Counter #47 Interrupt |
| 483 | tcpwm_1_interrupts_48_IRQn | Active | TCPWM1 Group #0, Counter #48 Interrupt |
| 484 | tcpwm_1_interrupts_49_IRQn | Active | TCPWM1 Group #0, Counter #49 Interrupt |
| 485 | tcpwm_1_interrupts_50_IRQn | Active | TCPWM1 Group #0, Counter #50 Interrupt |
| 486 | tcpwm_1_interrupts_51_IRQn | Active | TCPWM1 Group #0, Counter #51 Interrupt |
| 487 | tcpwm_1_interrupts_52_IRQn | Active | TCPWM1 Group #0, Counter #52 Interrupt |
| 488 | tcpwm_1_interrupts_53_IRQn | Active | TCPWM1 Group #0, Counter #53 Interrupt |
| 489 | tcpwm_1_interrupts_54_IRQn | Active | TCPWM1 Group #0, Counter #54 Interrupt |
| 490 | tcpwm_1_interrupts_55_IRQn | Active | TCPWM1 Group #0, Counter #55 Interrupt |

Table 13-1. Peripheral Interrupt Assignments and Wake-up Sources (continued)

| Interrupt | Source | Power Mode | Description |
|-----------|-----------------------------|------------|--|
| 491 | tcpwm_1_interrupts_56_IRQn | Active | TCPWM1 Group #0, Counter #56 Interrupt |
| 492 | tcpwm_1_interrupts_57_IRQn | Active | TCPWM1 Group #0, Counter #57 Interrupt |
| 493 | tcpwm_1_interrupts_58_IRQn | Active | TCPWM1 Group #0, Counter #58 Interrupt |
| 494 | tcpwm_1_interrupts_59_IRQn | Active | TCPWM1 Group #0, Counter #59 Interrupt |
| 495 | tcpwm_1_interrupts_60_IRQn | Active | TCPWM1 Group #0, Counter #60 Interrupt |
| 496 | tcpwm_1_interrupts_61_IRQn | Active | TCPWM1 Group #0, Counter #61 Interrupt |
| 497 | tcpwm_1_interrupts_62_IRQn | Active | TCPWM1 Group #0, Counter #62 Interrupt |
| 498 | tcpwm_1_interrupts_63_IRQn | Active | TCPWM1 Group #0, Counter #63 Interrupt |
| 499 | tcpwm_1_interrupts_64_IRQn | Active | TCPWM1 Group #0, Counter #64 Interrupt |
| 500 | tcpwm_1_interrupts_65_IRQn | Active | TCPWM1 Group #0, Counter #65 Interrupt |
| 501 | tcpwm_1_interrupts_66_IRQn | Active | TCPWM1 Group #0, Counter #66 Interrupt |
| 502 | tcpwm_1_interrupts_67_IRQn | Active | TCPWM1 Group #0, Counter #67 Interrupt |
| 503 | tcpwm_1_interrupts_68_IRQn | Active | TCPWM1 Group #0, Counter #68 Interrupt |
| 504 | tcpwm_1_interrupts_69_IRQn | Active | TCPWM1 Group #0, Counter #69 Interrupt |
| 505 | tcpwm_1_interrupts_70_IRQn | Active | TCPWM1 Group #0, Counter #70 Interrupt |
| 506 | tcpwm_1_interrupts_71_IRQn | Active | TCPWM1 Group #0, Counter #71 Interrupt |
| 507 | tcpwm_1_interrupts_72_IRQn | Active | TCPWM1 Group #0, Counter #72 Interrupt |
| 508 | tcpwm_1_interrupts_73_IRQn | Active | TCPWM1 Group #0, Counter #73 Interrupt |
| 509 | tcpwm_1_interrupts_74_IRQn | Active | TCPWM1 Group #0, Counter #74 Interrupt |
| 510 | tcpwm_1_interrupts_75_IRQn | Active | TCPWM1 Group #0, Counter #75 Interrupt |
| 511 | tcpwm_1_interrupts_76_IRQn | Active | TCPWM1 Group #0, Counter #76 Interrupt |
| 512 | tcpwm_1_interrupts_77_IRQn | Active | TCPWM1 Group #0, Counter #77 Interrupt |
| 513 | tcpwm_1_interrupts_78_IRQn | Active | TCPWM1 Group #0, Counter #78 Interrupt |
| 514 | tcpwm_1_interrupts_79_IRQn | Active | TCPWM1 Group #0, Counter #79 Interrupt |
| 515 | tcpwm_1_interrupts_80_IRQn | Active | TCPWM1 Group #0, Counter #80 Interrupt |
| 516 | tcpwm_1_interrupts_81_IRQn | Active | TCPWM1 Group #0, Counter #81 Interrupt |
| 517 | tcpwm_1_interrupts_82_IRQn | Active | TCPWM1 Group #0, Counter #82 Interrupt |
| 518 | tcpwm_1_interrupts_83_IRQn | Active | TCPWM1 Group #0, Counter #83 Interrupt |
| 519 | tcpwm_0_interrupts_0_IRQn | Active | TCPWM0 Group #0, Counter #0 Interrupt |
| 520 | tcpwm_0_interrupts_1_IRQn | Active | TCPWM0 Group #0, Counter #1 Interrupt |
| 521 | tcpwm_0_interrupts_2_IRQn | Active | TCPWM0 Group #0, Counter #2 Interrupt |
| 522 | tcpwm_1_interrupts_256_IRQn | Active | TCPWM1 Group #1, Counter #0 Interrupt |
| 523 | tcpwm_1_interrupts_257_IRQn | Active | TCPWM1 Group #1, Counter #1 Interrupt |
| 524 | tcpwm_1_interrupts_258_IRQn | Active | TCPWM1 Group #1, Counter #2 Interrupt |
| 525 | tcpwm_1_interrupts_259_IRQn | Active | TCPWM1 Group #1, Counter #3 Interrupt |
| 526 | tcpwm_1_interrupts_260_IRQn | Active | TCPWM1 Group #1, Counter #4 Interrupt |
| 527 | tcpwm_1_interrupts_261_IRQn | Active | TCPWM1 Group #1, Counter #5 Interrupt |
| 528 | tcpwm_1_interrupts_262_IRQn | Active | TCPWM1 Group #1, Counter #6 Interrupt |
| 529 | tcpwm_1_interrupts_263_IRQn | Active | TCPWM1 Group #1, Counter #7 Interrupt |
| 530 | tcpwm_1_interrupts_264_IRQn | Active | TCPWM1 Group #1, Counter #8 Interrupt |
| 531 | tcpwm_1_interrupts_265_IRQn | Active | TCPWM1 Group #1, Counter #9 Interrupt |

Table 13-1. Peripheral Interrupt Assignments and Wake-up Sources (continued)

| Interrupt | Source | Power Mode | Description |
|-----------|-------------------------------|------------|---|
| 532 | tcpwm_1_interrupts_266_IRQn | Active | TCPWM1 Group #1, Counter #10 Interrupt |
| 533 | tcpwm_1_interrupts_267_IRQn | Active | TCPWM1 Group #1, Counter #11 Interrupt |
| 534 | tcpwm_0_interrupts_256_IRQn | Active | TCPWM0 Group #1, Counter #0 Interrupt |
| 535 | tcpwm_0_interrupts_257_IRQn | Active | TCPWM0 Group #1, Counter #1 Interrupt |
| 536 | tcpwm_0_interrupts_258_IRQn | Active | TCPWM0 Group #1, Counter #2 Interrupt |
| 537 | tcpwm_1_interrupts_512_IRQn | Active | TCPWM1 Group #2, Counter #0 Interrupt |
| 538 | tcpwm_1_interrupts_513_IRQn | Active | TCPWM1 Group #2, Counter #1 Interrupt |
| 539 | tcpwm_1_interrupts_514_IRQn | Active | TCPWM1 Group #2, Counter #2 Interrupt |
| 540 | tcpwm_1_interrupts_515_IRQn | Active | TCPWM1 Group #2, Counter #3 Interrupt |
| 541 | tcpwm_1_interrupts_516_IRQn | Active | TCPWM1 Group #2, Counter #4 Interrupt |
| 542 | tcpwm_1_interrupts_517_IRQn | Active | TCPWM1 Group #2, Counter #5 Interrupt |
| 543 | tcpwm_1_interrupts_518_IRQn | Active | TCPWM1 Group #2, Counter #6 Interrupt |
| 544 | tcpwm_1_interrupts_519_IRQn | Active | TCPWM1 Group #2, Counter #7 Interrupt |
| 545 | tcpwm_1_interrupts_520_IRQn | Active | TCPWM1 Group #2, Counter #8 Interrupt |
| 546 | tcpwm_1_interrupts_521_IRQn | Active | TCPWM1 Group #2, Counter #9 Interrupt |
| 547 | tcpwm_1_interrupts_522_IRQn | Active | TCPWM1 Group #2, Counter #10 Interrupt |
| 548 | tcpwm_1_interrupts_523_IRQn | Active | TCPWM1 Group #2, Counter #11 Interrupt |
| 549 | tcpwm_1_interrupts_524_IRQn | Active | TCPWM1 Group #2, Counter #12 Interrupt |
| 550 | tcpwm_0_interrupts_512_IRQn | Active | TCPWM0 Group #2, Counter #0 Interrupt |
| 551 | tcpwm_0_interrupts_513_IRQn | Active | TCPWM0 Group #2, Counter #1 Interrupt |
| 552 | tcpwm_0_interrupts_514_IRQn | Active | TCPWM0 Group #2, Counter #2 Interrupt |
| 553 | flexray_0_interrupt0_IRQn | Active | FlexRay0 interrupt #0 |
| 554 | flexray_0_interrupt1_IRQn | Active | FlexRay0 interrupt #1 |
| 555 | smif_0_interrupt_IRQn | Active | SMIF0 (QSPI) interrupt |
| 556 | eth_0_interrupt_eth_IRQn | Active | Ethernet0 interrupt |
| 557 | eth_0_interrupt_eth_q2_IRQn | Active | Ethernet0 interrupt for dma_priority_queue2 |
| 558 | eth_0_interrupt_eth_q1_IRQn | Active | Ethernet0 interrupt for dma_priority_queue1 |
| 559 | eth_1_interrupt_eth_IRQn | Active | Ethernet1 interrupt |
| 560 | eth_1_interrupt_eth_q2_IRQn | Active | Ethernet1 interrupt for dma_priority_queue2 |
| 561 | eth_1_interrupt_eth_q1_IRQn | Active | Ethernet1 interrupt for dma_priority_queue1 |
| 562 | sdhc_0_interrupt_general_IRQn | Active | SDHC0 general interrupt |
| 563 | sdhc_0_interrupt_wakeup_IRQn | Active | SDHC0 wakeup interrupt |
| 564 | audioss_0_interrupt_i2s_IRQn | Active | AUDIOSS I ² S0 interrupt |
| 565 | audioss_1_interrupt_i2s_IRQn | Active | AUDIOSS I ² S1 interrupt |
| 566 | audioss_2_interrupt_i2s_IRQn | Active | AUDIOSS I ² S2 interrupt |

14. Core Interrupt Types

Table 14-1. Core Interrupt Types

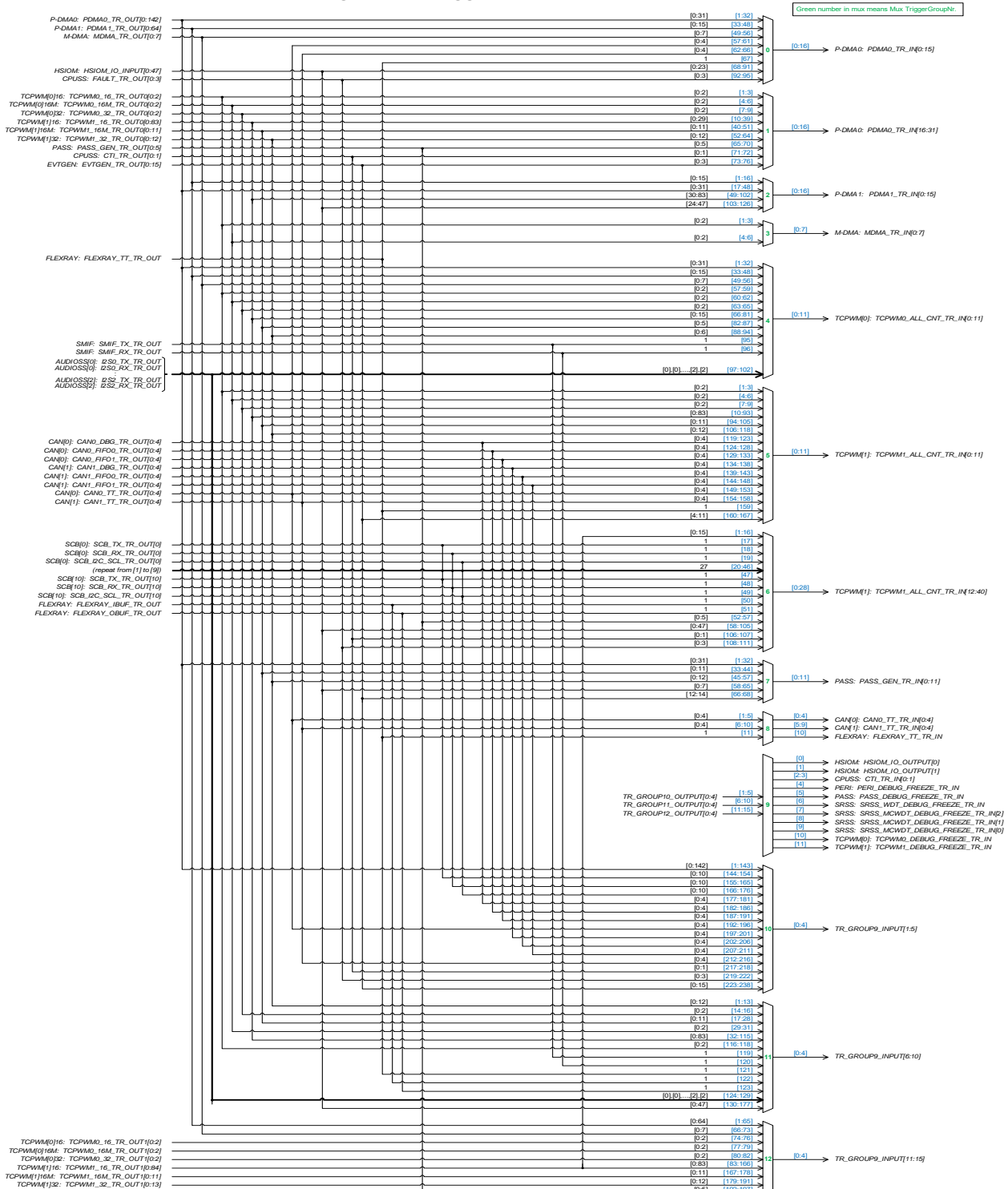
| Interrupt | Source | Power Mode | Description |
|-----------|---------------------------------|------------|--------------------------------|
| 0 | CPUIntIdx0_IRQn ^[26] | DeepSleep | CPU User Interrupt #0 |
| 1 | CPUIntIdx1_IRQn ^[26] | DeepSleep | CPU User Interrupt #1 |
| 2 | CPUIntIdx2_IRQn | DeepSleep | CPU User Interrupt #2 |
| 3 | CPUIntIdx3_IRQn | DeepSleep | CPU User Interrupt #3 |
| 4 | CPUIntIdx4_IRQn | DeepSleep | CPU User Interrupt #4 |
| 5 | CPUIntIdx5_IRQn | DeepSleep | CPU User Interrupt #5 |
| 6 | CPUIntIdx6_IRQn | DeepSleep | CPU User Interrupt #6 |
| 7 | CPUIntIdx7_IRQn | DeepSleep | CPU User Interrupt #7 |
| 8 | Internal0_IRQn | Active | Internal Software Interrupt #0 |
| 9 | Internal1_IRQn | Active | Internal Software Interrupt #1 |
| 10 | Internal2_IRQn | Active | Internal Software Interrupt #2 |
| 11 | Internal3_IRQn | Active | Internal Software Interrupt #3 |
| 12 | Internal4_IRQn | Active | Internal Software Interrupt #4 |
| 13 | Internal5_IRQn | Active | Internal Software Interrupt #5 |
| 14 | Internal6_IRQn | Active | Internal Software Interrupt #6 |
| 15 | Internal7_IRQn | Active | Internal Software Interrupt #7 |

Note

26. User interrupt cannot be used for CM0+ application, as it is used internally by system calls. Note, this does not impact CM7 application.

15. Trigger Multiplexer

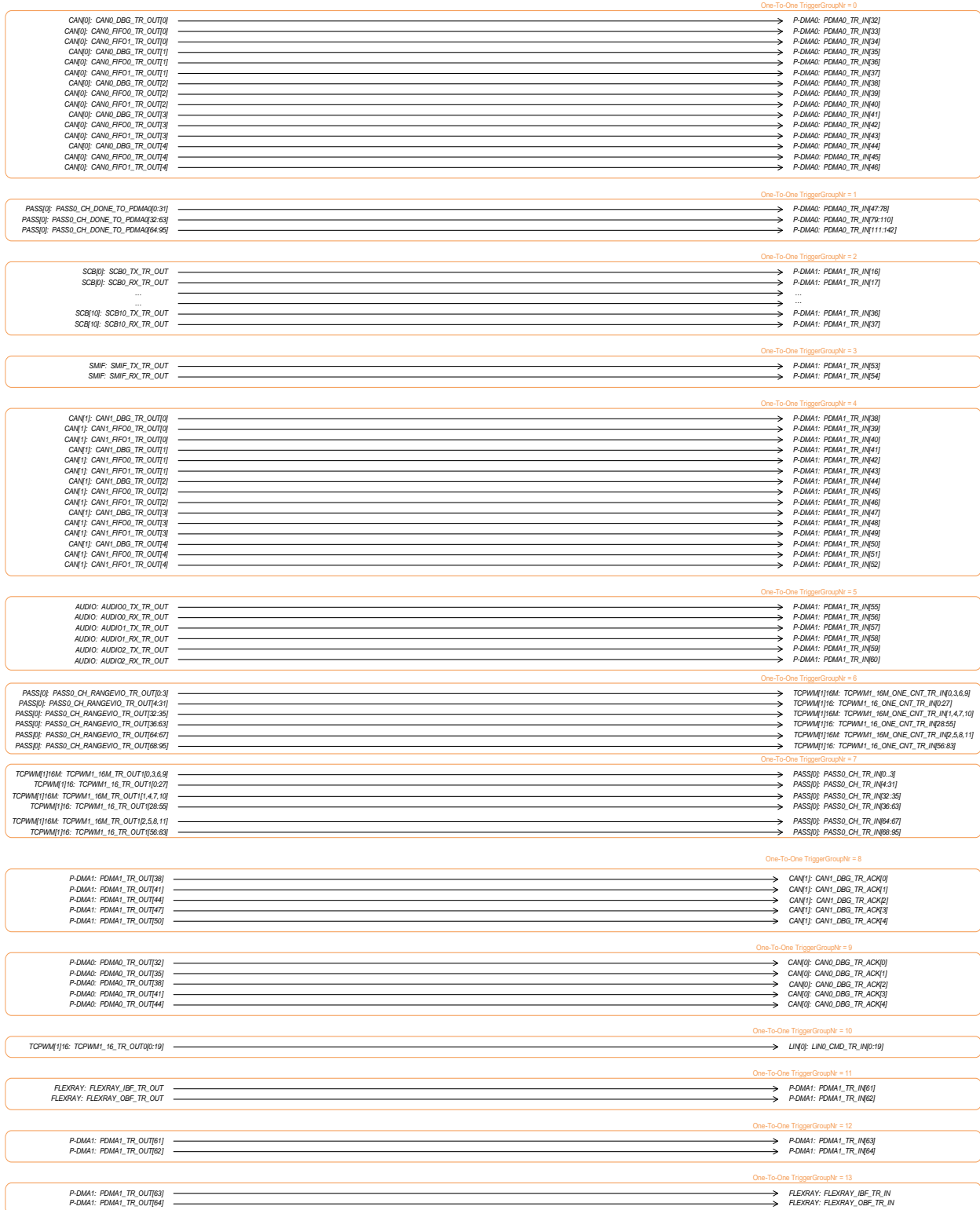
Figure 15-1. Trigger Multiplexer Group^[27]



Note

27. The diagram shows only the TRIG_LABEL; the final trigger formation is based on the formula TRIG_{PREFIX(IN/OUT)}_{MUX_x}_{TRIG_LABEL} and the information provided in Table 16-1 on page 67, and Table 17-1 on page 71.

Figure 15-2.Triggers One-to-One^[28]



Note

28. The diagram shows only the TRIG_LABEL; the final trigger formation is based on the formula TRIG_{PREFIX(IN_1TO1/OUT_1TO1)}_{x}_{TRIG_LABEL} and the information provided in Table 18-1 on page 72.

16. Triggers Group Inputs

Table 16-1. Trigger Inputs

| Input | Trigger | Description |
|--|--------------------------|---|
| MUX Group 0: P-DMA0 trigger multiplexer | | |
| 1:32 ^[29] | PDMA0_TR_OUT[0:31] | Allow P-DMA0 to chain to itself. Channels 0 - 31 are dedicated for chaining |
| 33:48 | PDMA1_TR_OUT[0:15] | Cross connections from P-DMA1 to P-DMA0, Channels 0-15 are used |
| 49:56 | MDMA_TR_OUT[0:7] | Cross connections from M-DMA0 to P-DMA0 |
| 57:61 | CAN0_TT_TR_OUT[0:4] | CAN0 Time Trigger Sync Outputs |
| 62:66 | CAN1_TT_TR_OUT[0:4] | CAN1 Time Trigger Sync Outputs |
| 67 | FLEXRAY_TT_TR_OUT | FlexRay0 timer trigger |
| 68:91 | HSIOM_IO_INPUT[0:23] | I/O Inputs |
| 92:95 | FAULT_TR_OUT[0:3] | Fault events |
| MUX Group 1: TCPWM to P-DMA0 trigger multiplexer | | |
| 1:3 | TCPWM0_16_TR_OUT0[0:2] | 16-bit TCPWM0 counters |
| 4:6 | TCPWM0_16M_TR_OUT0[0:2] | 16-bit Motor enhanced TCPWM0 counters |
| 7:9 | TCPWM0_32_TR_OUT0[0:2] | 32-bit TCPWM0 counters |
| 10:39 | TCPWM1_16_TR_OUT0[0:29] | 16-bit TCPWM1 counters |
| 40:51 | TCPWM1_16M_TR_OUT0[0:11] | 16-bit Motor enhanced TCPWM1 counters |
| 52:64 | TCPWM1_32_TR_OUT0[0:12] | 32-bit TCPWM1 counters |
| 65:70 | PASS_GEN_TR_OUT[0:5] | PASS SAR events |
| 71:72 | CTI_TR_OUT[0:1] | Trace events |
| 73:76 | EVTGEN_TR_OUT[0:3] | Event generator triggers |
| MUX Group 2: P-DMA1 trigger multiplexer | | |
| 1:16 | PDMA1_TR_OUT[0:15] | Allow P-DMA1 to chain to itself. Channels 0–15 are dedicated for chaining |
| 17:48 | PDMA0_TR_OUT[0:31] | Cross connections from P-DMA0 to P-DMA1, channels 0–31 are used. |
| 49:102 | TCPWM1_16_TR_OUT0[30:83] | 16-bit TCPWM1 counters |
| 103:126 | HSIOM_IO_INPUT[24:47] | I/O Inputs |
| MUX Group 3: M-DMA0 trigger multiplexer | | |
| 1:3 | TCPWM0_16_TR_OUT0[0:2] | 16-bit TCPWM0 counters |
| 4:6 | TCPWM0_16M_TR_OUT0[0:2] | 16-bit Motor enhanced TCPWM0 counters |
| MUX Group 4: TCPWM0 Loop back trigger multiplexer | | |
| 1:32 | PDMA0_TR_OUT[0:31] | General-purpose P-DMA0 triggers |
| 33:48 | PDMA1_TR_OUT[0:15] | General-purpose P-DMA1 triggers |
| 49:56 | MDMA_TR_OUT[0:7] | M-DMA0 triggers |
| 57:59 | TCPWM0_16_TR_OUT0[0:2] | 16-bit TCPWM0 counters |
| 60:62 | TCPWM0_16M_TR_OUT0[0:2] | 16-bit Motor enhanced TCPWM0 counters |
| 63:65 | TCPWM0_32_TR_OUT0[0:2] | 32-bit TCPWM0 counters |
| 66:81 | TCPWM1_16_TR_OUT0[0:15] | 16-bit TCPWM1 counters |
| 82:87 | TCPWM1_16M_TR_OUT0[0:5] | 16-bit Motor enhanced TCPWM1 counters |
| 88:94 | TCPWM1_32_TR_OUT0[0:6] | 32-bit TCPWM1 counters |
| 95 | SMIF_TX_TR_OUT | SMIF0 TX trigger |
| 96 | SMIF_RX_TR_OUT | SMIF0 RX trigger |

Note

29. "x:y" depicts a range starting from 'x' through 'y'.

Table 16-1. Trigger Inputs (continued)

| Input | Trigger | Description |
|--|--------------------------|---------------------------------------|
| 97 | I2S0_TX_TR_OUT | I ² S0 TX trigger |
| 98 | I2S0_RX_TR_OUT | I ² S0 RX trigger |
| 99 | I2S1_TX_TR_OUT | I ² S1 TX trigger |
| 100 | I2S1_RX_TR_OUT | I ² S1 RX trigger |
| 101 | I2S2_TX_TR_OUT | I ² S2 TX trigger |
| 102 | I2S2_RX_TR_OUT | I ² S2 RX trigger |
| MUX Group 5: TCPWM1 Loop back trigger multiplexer | | |
| 1:3 | TCPWM0_16_TR_OUT0[0:2] | 16-bit TCPWM0 counters |
| 4:6 | TCPWM0_16M_TR_OUT0[0:2] | 16-bit Motor enhanced TCPWM0 counters |
| 7:9 | TCPWM0_32_TR_OUT0[0:2] | 32-bit TCPWM0 counters |
| 10:93 | TCPWM1_16_TR_OUT0[0:83] | 16-bit TCPWM1 counters |
| 94:105 | TCPWM1_16M_TR_OUT0[0:11] | 16-bit Motor enhanced TCPWM1 counters |
| 106:118 | TCPWM1_32_TR_OUT0[0:12] | 32-bit TCPWM1 counters |
| 119:123 | CAN0_DBG_TR_OUT[0:4] | CAN0 M-DMA0 events |
| 124:128 | CAN0_FIFO0_TR_OUT[0:4] | CAN0 FIFO0 events |
| 129:133 | CAN0_FIFO1_TR_OUT[0:4] | CAN0 FIFO1 events |
| 134:138 | CAN1_DBG_TR_OUT[0:4] | CAN1 M-DMA0 events |
| 139:143 | CAN1_FIFO0_TR_OUT[0:4] | CAN1 FIFO0 events |
| 144:148 | CAN1_FIFO1_TR_OUT[0:4] | CAN1 FIFO1 events |
| 149:153 | CAN0_TT_TR_OUT[0:4] | CAN0 TT Sync Outputs |
| 154:158 | CAN1_TT_TR_OUT[0:4] | CAN1 TT Sync Outputs |
| 159 | FLEXRAY_TT_TR_OUT | FlexRay0 timer trigger |
| 160:167 | EVTGEN_TR_OUT[4:11] | Event generator triggers |
| MUX Group 6: TCPWM1 trigger Multiplexer | | |
| 1:16 | TCPWM1_16_TR_OUT1[0:15] | 16-bit TCPWM1 counters |
| 17 | SCB_TX_TR_OUT[0] | SCB0 TX trigger |
| 18 | SCB_RX_TR_OUT[0] | SCB0 RX trigger |
| 19 | SCB_I2C_SCL_TR_OUT[0] | SCB0 I ² C trigger |
| 20 | SCB_TX_TR_OUT[1] | SCB1 TX trigger |
| 21 | SCB_RX_TR_OUT[1] | SCB1 RX trigger |
| 22 | SCB_I2C_SCL_TR_OUT[1] | SCB1 I ² C trigger |
| 23 | SCB_TX_TR_OUT[2] | SCB2 TX trigger |
| 24 | SCB_RX_TR_OUT[2] | SCB2 RX trigger |
| 25 | SCB_I2C_SCL_TR_OUT[2] | SCB2 I ² C trigger |
| 26 | SCB_TX_TR_OUT[3] | SCB3 TX trigger |
| 27 | SCB_RX_TR_OUT[3] | SCB3 RX trigger |
| 28 | SCB_I2C_SCL_TR_OUT[3] | SCB3 I ² C trigger |
| 29 | SCB_TX_TR_OUT[4] | SCB4 TX trigger |
| 30 | SCB_RX_TR_OUT[4] | SCB4 RX trigger |
| 31 | SCB_I2C_SCL_TR_OUT[4] | SCB4 I ² C trigger |
| 32 | SCB_TX_TR_OUT[5] | SCB5 TX trigger |
| 33 | SCB_RX_TR_OUT[5] | SCB5 RX trigger |
| 34 | SCB_I2C_SCL_TR_OUT[5] | SCB5 I ² C trigger |

Table 16-1. Trigger Inputs (continued)

| Input | Trigger | Description |
|--|--------------------------|--|
| 35 | SCB_TX_TR_OUT[6] | SCB6 TX trigger |
| 36 | SCB_RX_TR_OUT[6] | SCB6 RX trigger |
| 37 | SCB_I2C_SCL_TR_OUT[6] | SCB6 I ² C trigger |
| 38 | SCB_TX_TR_OUT[7] | SCB7 TX trigger |
| 39 | SCB_RX_TR_OUT[7] | SCB7 RX trigger |
| 40 | SCB_I2C_SCL_TR_OUT[7] | SCB7 I ² C trigger |
| 41 | SCB_TX_TR_OUT[8] | SCB8 TX trigger |
| 42 | SCB_RX_TR_OUT[8] | SCB8 RX trigger |
| 43 | SCB_I2C_SCL_TR_OUT[8] | SCB8 I ² C trigger |
| 44 | SCB_TX_TR_OUT[9] | SCB9 TX trigger |
| 45 | SCB_RX_TR_OUT[9] | SCB9 RX trigger |
| 46 | SCB_I2C_SCL_TR_OUT[9] | SCB9 I ² C trigger |
| 47 | SCB_TX_TR_OUT[10] | SCB10 TX trigger |
| 48 | SCB_RX_TR_OUT[10] | SCB10 RX trigger |
| 49 | SCB_I2C_SCL_TR_OUT[10] | SCB10 I ² C trigger |
| 50 | FLEXRAY_IBUF_TR_OUT | FlexRay IBUF trigger |
| 51 | FLEXRAY_OBUF_TR_OUT | FlexRay OBUF trigger |
| 52:57 | PASS_GEN_TR_OUT[0:5] | PASS SAR ADC events |
| 58:105 | HSIOM_IO_INPUT[0:47] | I/O Inputs |
| 106:107 | CTI_TR_IN[0:1] | CPUSS CTI Trace events |
| 108:111 | FAULT_TR_OUT[0:3] | Fault events |
| MUX Group 7: PASS trigger multiplexer | | |
| 1:31 | PDMA0_TR_OUT[0:31] | General purpose P-DMA0 triggers |
| 32:44 | TCPWM1_16M_TR_OUT0[0:11] | 16-bit Motor enhanced TCPWM1 counters |
| 45:57 | TCPWM1_32_TR_OUT0[0:12] | 32-bit TCPWM1 counters |
| 58:65 | HSIOM_IO_INPUT[0:7] | I/O Inputs |
| 66:68 | EVTGEN_TR_OUT[12:14] | Event generator triggers |
| MUX Group 8: CAN and FLEXRAY TT Sync | | |
| 1:5 | CAN0_TT_TR_OUT[0:4] | CAN0 TT Sync Outputs |
| 6:10 | CAN1_TT_TR_OUT[0:4] | CAN1 TT Sync Outputs |
| 11 | FLEXRAY_TT_TR_OUT | FlexRay timer trigger |
| MUX Group 9: Debug multiplexer | | |
| 1:5 | TR_GROUP10_OUTPUT[0:4] | Output from debug reduction multiplexer #1 |
| 6:10 | TR_GROUP11_OUTPUT[0:4] | Output from debug reduction multiplexer #2 |
| 11:15 | TR_GROUP12_OUTPUT[0:4] | Output from debug reduction multiplexer #3 |
| MUX Group 10: Debug Reduction #1 | | |
| 1:143 | PDMA0_TR_OUT[0:142] | General purpose P-DMA0 triggers |
| 144:154 | SCB_TX_TR_OUT[0:10] | SCB TX triggers |
| 155:165 | SCB_RX_TR_OUT[0:10] | SCB RX triggers |
| 166:176 | SCB_I2C_SCL_TR_OUT[0:10] | SCB I ² C triggers |
| 177:181 | CAN0_DBG_TR_OUT[0:4] | CAN0 M-DMA0 |
| 182:186 | CAN0_FIFO0_TR_OUT[0:4] | CAN0 FIFO0 |

Table 16-1. Trigger Inputs (continued)

| Input | Trigger | Description |
|---|--------------------------|---------------------------------------|
| 187:191 | CAN0_FIFO1_TR_OUT[0:4] | CAN0 FIFO1 |
| 192:196 | CAN0_TT_TR_OUT[0:4] | CAN0 TT Sync Outputs |
| 197:201 | CAN1_DBG_TR_OUT[0:4] | CAN1 M-DMA0 |
| 202:206 | CAN1_FIFO0_TR_OUT[0:4] | CAN1 FIFO0 |
| 207:211 | CAN1_FIFO1_TR_OUT[0:4] | CAN1 FIFO1 |
| 212:216 | CAN1_TT_TR_OUT[0:4] | CAN1 TT Sync Outputs |
| 217:218 | CTI_TR_OUT[0:1] | CPUSS CTI Trace events |
| 219:222 | FAULT_TR_OUT[0:3] | Fault events |
| 223:238 | EVTGEN_TR_OUT[0:15] | EVTGEN Triggers |
| MUX Group 11: Debug Reduction #2 | | |
| 1:13 | TCPWM1_32_TR_OUT0[0:12] | 32-bit TCPWM1 counters |
| 14:16 | TCPWM0_32_TR_OUT0[0:2] | 32-bit TCPWM0 counters |
| 17:28 | TCPWM1_16M_TR_OUT0[0:11] | 16-bit Motor enhanced TCPWM1 counters |
| 29:31 | TCPWM0_16M_TR_OUT0[0:2] | 16-bit Motor enhanced TCPWM0 counters |
| 32:115 | TCPWM1_16_TR_OUT0[0:83] | 16-bit TCPWM1 counters |
| 116:118 | TCPWM0_16_TR_OUT0[0:2] | 16-bit TCPWM0 counters |
| 119 | SMIF_TX_TR_OUT | SMIF TX trigger |
| 120 | SMIF_RX_TR_OUT | SMIF RX trigger |
| 121 | FLEXRAY_TT_TR_OUT | FlexRay Time Trigger output |
| 122 | FLEXRAY_IBUF_TR_OUT | FlexRay M-DMA0 trans request |
| 123 | FLEXRAY_OBUF_TR_OUT | FlexRay M-DMA0 trans request |
| 124 | I2S0_TX_TR_OUT | I ² S0 TX trigger |
| 125 | I2S0_RX_TR_OUT | I ² S0 RX trigger |
| 126 | I2S1_TX_TR_OUT | I ² S1 TX trigger |
| 127 | I2S1_RX_TR_OUT | I ² S1 RX trigger |
| 128 | I2S2_TX_TR_OUT | I ² S2 TX trigger |
| 129 | I2S2_RX_TR_OUT | I ² S2 RX trigger |
| 130:177 | HSIOM_IO_INPUT[0:47] | I/O inputs |
| MUX Group 12: Debug Reduction #3 | | |
| 1:65 | PDMA1_TR_OUT[0:64] | General purpose P-DMA1 triggers |
| 66:73 | MDMA_TR_OUT[0:7] | M-DMA0 triggers |
| 74:76 | TCPWM0_16_TR_OUT1[0:2] | 16-bit TCPWM0 counters |
| 77:79 | TCPWM0_16M_TR_OUT1[0:2] | 16-bit Motor enhanced TCPWM0 counters |
| 80:82 | TCPWM0_32_TR_OUT1[0:2] | 32-bit TCPWM0 counters |
| 83:166 | TCPWM1_16_TR_OUT1[0:83] | 16-bit TCPWM1 counters |
| 167:178 | TCPWM1_16M_TR_OUT1[0:11] | 16-bit Motor enhanced TCPWM1 counters |
| 179:191 | TCPWM1_32_TR_OUT1[0:12] | 32-bit TCPWM1 counters |
| 192:197 | PASS_GEN_TR_OUT[0:5] | PASS SAR ADC events |

17. Triggers Group Outputs

Table 17-1. Trigger Outputs

| Output | Trigger | Description |
|--|----------------------------------|------------------------------------|
| MUX Group 0: P-DMA0 trigger multiplexer | | |
| 0:15 | PDMA0_TR_IN[0:15] | Triggers to P-DMA0[0:15] |
| MUX Group 1: TCPWM to P-DMA0 trigger multiplexer | | |
| 0:15 | PDMA0_TR_IN[16:31] | Triggers to P-DMA0[16:31] |
| MUX Group 2: P-DMA1 trigger multiplexer | | |
| 0:15 | PDMA1_TR_IN[0:15] | Triggers to P-DMA1 |
| MUX Group 3: M-DMA0 trigger multiplexer | | |
| 0:7 | M-DMA_TR_IN[0:7] | Triggers to M-DMA0 |
| MUX Group 4: TCPWM0 Loop back trigger multiplexer | | |
| 0:11 | TCPWM0_ALL_CNT_TR_IN[0:11] | Triggers to TCPWM0 |
| MUX Group 5: TCPWM1 Loop back trigger multiplexer | | |
| 0:11 | TCPWM1_ALL_CNT_TR_IN[0:11] | Triggers to TCPWM1 |
| MUX Group 6: TCPWM1 trigger Multiplexer | | |
| 0:28 | TCPWM1_ALL_CNT_TR_IN[12:40] | Triggers to TCPWM1 |
| MUX Group 7: PASS trigger multiplexer | | |
| 0:11 | PASS_GEN_TR_IN[0:11] | Triggers to PASS SAR ADCs |
| MUX Group 8: CAN and FLEXRAY TT Sync | | |
| 0:4 | CAN0_TT_TR_IN[0:4] | CAN0 TT Sync Inputs |
| 5:9 | CAN1_TT_TR_IN[0:4] | CAN1 TT Sync Inputs |
| 10 | FLEXRAY_TT_TR_IN | FlexRay TT Inputs |
| MUX Group 9: Debug multiplexer | | |
| 0 | HSIOM_IO_OUTPUT[0] | To HSIOM as an output |
| 1 | HSIOM_IO_OUTPUT[1] | To HSIOM as an output |
| 2:3 | CTI_TR_IN[0:1] | To the Cross Trigger system |
| 4 | PERI_DEBUG_FREEZE_TR_IN | Signal to Freeze PERI operation |
| 5 | PASS_DEBUG_FREEZE_TR_IN | Signal to Freeze SAR ADC operation |
| 6 | SRSS_WDT_DEBUG_FREEZE_TR_IN | Signal to Freeze WDT operation |
| 7 | SRSS_MCWDT_DEBUG_FREEZE_TR_IN[2] | Signal to Freeze MCWDT2 operation |
| 8 | SRSS_MCWDT_DEBUG_FREEZE_TR_IN[1] | Signal to Freeze MCWDT1 operation |
| 9 | SRSS_MCWDT_DEBUG_FREEZE_TR_IN[0] | Signal to Freeze MCWDT0 operation |
| 10 | TCPWM0_DEBUG_FREEZE_TR_IN | Signal to Freeze TCPWM0 operation |
| 11 | TCPWM1_DEBUG_FREEZE_TR_IN | Signal to Freeze TCPWM1 operation |
| MUX Group 10: Debug Reduction #1 | | |
| 0:4 | TR_GROUP9_INPUT[1:5] | To main debug multiplexer |
| MUX Group 11: Debug Reduction #2 | | |
| 0:4 | TR_GROUP9_INPUT[6:10] | To main debug multiplexer |
| MUX Group 12: Debug Reduction #3 | | |
| 0:4 | TR_GROUP9_INPUT[11:15] | To main debug multiplexer |

18. Triggers One-to-one

Table 18-1. Triggers 1:1

| Input | Trigger In | Trigger Out | Description |
|--|-----------------------------|----------------------|---|
| MUX Group 0: CAN0 to P-DMA0 Triggers | | | |
| 0 | CAN0_DBG_TR_OUT[0] | PDMA0_TR_IN[32] | CAN0, Channel #0 P-DMA0 trigger |
| 1 | CAN0_FIFO0_TR_OUT[0] | PDMA0_TR_IN[33] | CAN0, Channel #0 FIFO0 trigger |
| 2 | CAN0_FIFO1_TR_OUT[0] | PDMA0_TR_IN[34] | CAN0, Channel #0 FIFO1 trigger |
| 3 | CAN0_DBG_TR_OUT[1] | PDMA0_TR_IN[35] | CAN0, Channel #1 P-DMA0 trigger |
| 4 | CAN0_FIFO0_TR_OUT[1] | PDMA0_TR_IN[36] | CAN0, Channel #1 FIFO0 trigger |
| 5 | CAN0_FIFO1_TR_OUT[1] | PDMA0_TR_IN[37] | CAN0, Channel #1 FIFO1 trigger |
| 6 | CAN0_DBG_TR_OUT[2] | PDMA0_TR_IN[38] | CAN0, Channel #2 P-DMA0 trigger |
| 7 | CAN0_FIFO0_TR_OUT[2] | PDMA0_TR_IN[39] | CAN0, Channel #2 FIFO0 trigger |
| 8 | CAN0_FIFO1_TR_OUT[2] | PDMA0_TR_IN[40] | CAN0, Channel #2 FIFO1 trigger |
| 9 | CAN0_DBG_TR_OUT[3] | PDMA0_TR_IN[41] | CAN0, Channel #3 P-DMA0 trigger |
| 10 | CAN0_FIFO0_TR_OUT[3] | PDMA0_TR_IN[42] | CAN0, Channel #3 FIFO0 trigger |
| 11 | CAN0_FIFO1_TR_OUT[3] | PDMA0_TR_IN[43] | CAN0, Channel #3 FIFO1 trigger |
| 12 | CAN0_DBG_TR_OUT[4] | PDMA0_TR_IN[44] | CAN0, Channel #4 P-DMA0 trigger |
| 13 | CAN0_FIFO0_TR_OUT[4] | PDMA0_TR_IN[45] | CAN0, Channel #4 FIFO0 trigger |
| 14 | CAN0_FIFO1_TR_OUT[4] | PDMA0_TR_IN[46] | CAN0, Channel #4 FIFO1 trigger |
| MUX Group 1: PASS SARx to P-DMA0 direct connect | | | |
| 0:31 | PASS0_CH_DONE_TR_OUT[0:31] | PDMA0_TR_IN[47:78] | PASS SAR0 [0:31] to P-DMA0 direct connect |
| 32:63 | PASS0_CH_DONE_TR_OUT[32:63] | PDMA0_TR_IN[79:110] | PASS SAR1 [0:31] to P-DMA0 direct connect |
| 64:95 | PASS0_CH_DONE_TR_OUT[64:95] | PDMA0_TR_IN[111:142] | PASS SAR2 [0:31] to P-DMA0 direct connect |
| MUX Group 2: SCBx to P-DMA1 Triggers | | | |
| 0 | SCB0_TX_TR_OUT | PDMA1_TR_IN[16] | SCB0 to P-DMA1 Trigger |
| 1 | SCB0_RX_TR_OUT | PDMA1_TR_IN[17] | SCB0 to P-DMA1 Trigger |
| 2 | SCB1_TX_TR_OUT | PDMA1_TR_IN[18] | SCB1 to P-DMA1 Trigger |
| 3 | SCB1_RX_TR_OUT | PDMA1_TR_IN[19] | SCB1 to P-DMA1 Trigger |
| 4 | SCB2_TX_TR_OUT | PDMA1_TR_IN[20] | SCB2 to P-DMA1 Trigger |
| 5 | SCB2_RX_TR_OUT | PDMA1_TR_IN[21] | SCB2 to P-DMA1 Trigger |
| 6 | SCB3_TX_TR_OUT | PDMA1_TR_IN[22] | SCB3 to P-DMA1 Trigger |
| 7 | SCB3_RX_TR_OUT | PDMA1_TR_IN[23] | SCB3 to P-DMA1 Trigger |
| 8 | SCB4_TX_TR_OUT | PDMA1_TR_IN[24] | SCB4 to P-DMA1 Trigger |
| 9 | SCB4_RX_TR_OUT | PDMA1_TR_IN[25] | SCB4 to P-DMA1 Trigger |
| 10 | SCB5_TX_TR_OUT | PDMA1_TR_IN[26] | SCB5 to P-DMA1 Trigger |
| 11 | SCB5_RX_TR_OUT | PDMA1_TR_IN[27] | SCB5 to P-DMA1 Trigger |
| 12 | SCB6_TX_TR_OUT | PDMA1_TR_IN[28] | SCB6 to P-DMA1 Trigger |
| 13 | SCB6_RX_TR_OUT | PDMA1_TR_IN[29] | SCB6 to P-DMA1 Trigger |
| 14 | SCB7_TX_TR_OUT | PDMA1_TR_IN[30] | SCB7 to P-DMA1 Trigger |
| 15 | SCB7_RX_TR_OUT | PDMA1_TR_IN[31] | SCB7 to P-DMA1 Trigger |
| 16 | SCB8_TX_TR_OUT | PDMA1_TR_IN[32] | SCB8 to P-DMA1 Trigger |
| 17 | SCB8_RX_TR_OUT | PDMA1_TR_IN[33] | SCB8 to P-DMA1 Trigger |
| 18 | SCB9_TX_TR_OUT | PDMA1_TR_IN[34] | SCB9 to P-DMA1 Trigger |

Table 18-1. Triggers 1:1 (continued)

| Input | Trigger In | Trigger Out | Description |
|--|-----------------------------|-----------------------------|---|
| 19 | SCB9_RX_TR_OUT | PDMA1_TR_IN[35] | SCB9 to P-DMA1 Trigger |
| 20 | SCB10_TX_TR_OUT | PDMA1_TR_IN[36] | SCB10 to P-DMA1 Trigger |
| 21 | SCB10_RX_TR_OUT | PDMA1_TR_IN[37] | SCB10 to P-DMA1 Trigger |
| MUX Group 3: SMIF0 to P-DMA1 Triggers | | | |
| 0 | SMIF_TX_TR_OUT | PDMA1_TR_IN[53] | SMIF0 to P-DMA1 Trigger |
| 1 | SMIF_RX_TR_OUT | PDMA1_TR_IN[54] | SMIF0 to P-DMA1 Trigger |
| MUX Group 4: CAN1 to P-DMA1 triggers | | | |
| 0 | CAN1_DBG_TR_OUT[0] | PDMA1_TR_IN[38] | CAN1 Channel #0 P-DMA1 trigger |
| 1 | CAN1_FIFO0_TR_OUT[0] | PDMA1_TR_IN[39] | CAN1 Channel #0 FIFO0 trigger |
| 2 | CAN1_FIFO1_TR_OUT[0] | PDMA1_TR_IN[40] | CAN1 Channel #0 FIFO1 trigger |
| 3 | CAN1_DBG_TR_OUT[1] | PDMA1_TR_IN[41] | CAN1 Channel #1 P-DMA1 trigger |
| 4 | CAN1_FIFO0_TR_OUT[1] | PDMA1_TR_IN[42] | CAN1 Channel #1 FIFO0 trigger |
| 5 | CAN1_FIFO1_TR_OUT[1] | PDMA1_TR_IN[43] | CAN1 Channel #1 FIFO1 trigger |
| 6 | CAN1_DBG_TR_OUT[2] | PDMA1_TR_IN[44] | CAN1 Channel #2 P-DMA1 trigger |
| 7 | CAN1_FIFO0_TR_OUT[2] | PDMA1_TR_IN[45] | CAN1 Channel #2 FIFO0 trigger |
| 8 | CAN1_FIFO1_TR_OUT[2] | PDMA1_TR_IN[46] | CAN1 Channel #2 FIFO1 trigger |
| 9 | CAN1_DBG_TR_OUT[3] | PDMA1_TR_IN[47] | CAN1 Channel #3 P-DMA1 trigger |
| 10 | CAN1_FIFO0_TR_OUT[3] | PDMA1_TR_IN[48] | CAN1 Channel #3 FIFO0 trigger |
| 11 | CAN1_FIFO1_TR_OUT[3] | PDMA1_TR_IN[49] | CAN1 Channel #3 FIFO1 trigger |
| 12 | CAN1_DBG_TR_OUT[4] | PDMA1_TR_IN[50] | CAN1 Channel #4 P-DMA1 trigger |
| 13 | CAN1_FIFO0_TR_OUT[4] | PDMA1_TR_IN[51] | CAN1 Channel #4 FIFO0 trigger |
| 14 | CAN1_FIFO1_TR_OUT[4] | PDMA1_TR_IN[52] | CAN1 Channel #4 FIFO1 trigger |
| MUX Group 5: I²Sx to P-DMA1 Triggers | | | |
| 0 | AUDIO0_TX_TR_OUT | PDMA1_TR_IN[55] | I ² S0 TX to P-DMA1 trigger |
| 1 | AUDIO0_RX_TR_OUT | PDMA1_TR_IN[56] | I ² S0 RX to P-DMA1 trigger |
| 2 | AUDIO1_TX_TR_OUT | PDMA1_TR_IN[57] | I ² S1 TX to P-DMA1 trigger |
| 3 | AUDIO1_RX_TR_OUT | PDMA1_TR_IN[58] | I ² S1 RX to P-DMA1 trigger |
| 4 | AUDIO2_TX_TR_OUT | PDMA1_TR_IN[59] | I ² S2 TX to P-DMA1 trigger |
| 5 | AUDIO2_RX_TR_OUT | PDMA1_TR_IN[60] | I ² S2 RX to P-DMA1 trigger |
| MUX Group 6: PASS SARx to TCPWM1 direct connect | | | |
| 0 | PASS0_CH_RANGEVIO_TR_OUT[0] | TCPWM1_16M_ONE_CNT_TR_IN[0] | SAR0 ch#0 ^[30] , range violation to TCPWM1 Group #1 Counter #00 trig = 2 |
| 1 | PASS0_CH_RANGEVIO_TR_OUT[1] | TCPWM1_16M_ONE_CNT_TR_IN[3] | SAR0 ch#1, range violation to TCPWM1 Group #1 Counter #03 trig = 2 |
| 2 | PASS0_CH_RANGEVIO_TR_OUT[2] | TCPWM1_16M_ONE_CNT_TR_IN[6] | SAR0 ch#2, range violation to TCPWM1 Group #1 Counter #06 trig = 2 |
| 3 | PASS0_CH_RANGEVIO_TR_OUT[3] | TCPWM1_16M_ONE_CNT_TR_IN[9] | SAR0 ch#3, range violation to TCPWM1 Group #1 Counter #09 trig = 2 |
| 4 | PASS0_CH_RANGEVIO_TR_OUT[4] | TCPWM1_16M_ONE_CNT_TR_IN[0] | SAR0 ch#4, range violation to TCPWM1 Group #0 Counter #00 trig = 2 |
| 5 | PASS0_CH_RANGEVIO_TR_OUT[5] | TCPWM1_16M_ONE_CNT_TR_IN[1] | SAR0 ch#5, range violation to TCPWM1 Group #0 Counter #01 trig = 2 |
| 6 | PASS0_CH_RANGEVIO_TR_OUT[6] | TCPWM1_16M_ONE_CNT_TR_IN[2] | SAR0 ch#6, range violation to TCPWM1 Group #0 Counter #02 trig = 2 |
| 7 | PASS0_CH_RANGEVIO_TR_OUT[7] | TCPWM1_16M_ONE_CNT_TR_IN[3] | SAR0 ch#7, range violation to TCPWM1 Group #0 Counter #03 trig = 2 |
| 8 | PASS0_CH_RANGEVIO_TR_OUT[8] | TCPWM1_16M_ONE_CNT_TR_IN[4] | SAR0 ch#8, range violation to TCPWM1 Group #0 Counter #04 trig = 2 |

Note

30. Each logical channel of SAR ADC[x] can be connected to any of the SAR ADC[x]_y external pin. (x = 0, or 1, or 2 and y=0 to max 31)

Table 18-1. Triggers 1:1 (continued)

| Input | Trigger In | Trigger Out | Description |
|-------|------------------------------|------------------------------|---|
| 9 | PASS0_CH_RANGEVIO_TR_OUT[9] | TCPWM1_16_ONE_CNT_TR_IN[5] | SAR0 ch#9, range violation to TCPWM1 Group #0 Counter #05 trig = 2 |
| 10 | PASS0_CH_RANGEVIO_TR_OUT[10] | TCPWM1_16_ONE_CNT_TR_IN[6] | SAR0 ch#10, range violation to TCPWM1 Group #0 Counter #06 trig = 2 |
| 11 | PASS0_CH_RANGEVIO_TR_OUT[11] | TCPWM1_16_ONE_CNT_TR_IN[7] | SAR0 ch#11, range violation to TCPWM1 Group #0 Counter #07 trig = 2 |
| 12 | PASS0_CH_RANGEVIO_TR_OUT[12] | TCPWM1_16_ONE_CNT_TR_IN[8] | SAR0 ch#12, range violation to TCPWM1 Group #0 Counter #08 trig = 2 |
| 13 | PASS0_CH_RANGEVIO_TR_OUT[13] | TCPWM1_16_ONE_CNT_TR_IN[9] | SAR0 ch#13, range violation to TCPWM1 Group #0 Counter #09 trig = 2 |
| 14 | PASS0_CH_RANGEVIO_TR_OUT[14] | TCPWM1_16_ONE_CNT_TR_IN[10] | SAR0 ch#14, range violation to TCPWM1 Group #0 Counter #10 trig = 2 |
| 15 | PASS0_CH_RANGEVIO_TR_OUT[15] | TCPWM1_16_ONE_CNT_TR_IN[11] | SAR0 ch#15, range violation to TCPWM1 Group #0 Counter #11 trig = 2 |
| 16 | PASS0_CH_RANGEVIO_TR_OUT[16] | TCPWM1_16_ONE_CNT_TR_IN[12] | SAR0 ch#16, range violation to TCPWM1 Group #0 Counter #12 trig = 2 |
| 17 | PASS0_CH_RANGEVIO_TR_OUT[17] | TCPWM1_16_ONE_CNT_TR_IN[13] | SAR0 ch#17, range violation to TCPWM1 Group #0 Counter #13 trig = 2 |
| 18 | PASS0_CH_RANGEVIO_TR_OUT[18] | TCPWM1_16_ONE_CNT_TR_IN[14] | SAR0 ch#18, range violation to TCPWM1 Group #0 Counter #14 trig = 2 |
| 19 | PASS0_CH_RANGEVIO_TR_OUT[19] | TCPWM1_16_ONE_CNT_TR_IN[15] | SAR0 ch#19, range violation to TCPWM1 Group #0 Counter #15 trig = 2 |
| 20 | PASS0_CH_RANGEVIO_TR_OUT[20] | TCPWM1_16_ONE_CNT_TR_IN[16] | SAR0 ch#20, range violation to TCPWM1 Group #0 Counter #16 trig = 2 |
| 21 | PASS0_CH_RANGEVIO_TR_OUT[21] | TCPWM1_16_ONE_CNT_TR_IN[17] | SAR0 ch#21, range violation to TCPWM1 Group #0 Counter #17 trig = 2 |
| 22 | PASS0_CH_RANGEVIO_TR_OUT[22] | TCPWM1_16_ONE_CNT_TR_IN[18] | SAR0 ch#22, range violation to TCPWM1 Group #0 Counter #18 trig = 2 |
| 23 | PASS0_CH_RANGEVIO_TR_OUT[23] | TCPWM1_16_ONE_CNT_TR_IN[19] | SAR0 ch#23, range violation to TCPWM1 Group #0 Counter #19 trig = 2 |
| 24 | PASS0_CH_RANGEVIO_TR_OUT[24] | TCPWM1_16_ONE_CNT_TR_IN[20] | SAR0 ch#24, range violation to TCPWM1 Group #0 Counter #20 trig = 2 |
| 25 | PASS0_CH_RANGEVIO_TR_OUT[25] | TCPWM1_16_ONE_CNT_TR_IN[21] | SAR0 ch#25, range violation to TCPWM1 Group #0 Counter #21 trig = 2 |
| 26 | PASS0_CH_RANGEVIO_TR_OUT[26] | TCPWM1_16_ONE_CNT_TR_IN[22] | SAR0 ch#26, range violation to TCPWM1 Group #0 Counter #22 trig = 2 |
| 27 | PASS0_CH_RANGEVIO_TR_OUT[27] | TCPWM1_16_ONE_CNT_TR_IN[23] | SAR0 ch#27, range violation to TCPWM1 Group #0 Counter #23 trig = 2 |
| 28 | PASS0_CH_RANGEVIO_TR_OUT[28] | TCPWM1_16_ONE_CNT_TR_IN[24] | SAR0 ch#28, range violation to TCPWM1 Group #0 Counter #24 trig = 2 |
| 29 | PASS0_CH_RANGEVIO_TR_OUT[29] | TCPWM1_16_ONE_CNT_TR_IN[25] | SAR0 ch#29, range violation to TCPWM1 Group #0 Counter #25 trig = 2 |
| 30 | PASS0_CH_RANGEVIO_TR_OUT[30] | TCPWM1_16_ONE_CNT_TR_IN[26] | SAR0 ch#30, range violation to TCPWM1 Group #0 Counter #26 trig = 2 |
| 31 | PASS0_CH_RANGEVIO_TR_OUT[31] | TCPWM1_16_ONE_CNT_TR_IN[27] | SAR0 ch#31, range violation to TCPWM1 Group #0 Counter #27 trig = 2 |
| 32 | PASS0_CH_RANGEVIO_TR_OUT[32] | TCPWM1_16M_ONE_CNT_TR_IN[1] | SAR1 ch#0, range violation to TCPWM1 Group #1 Counter #01 trig = 2 |
| 33 | PASS0_CH_RANGEVIO_TR_OUT[33] | TCPWM1_16M_ONE_CNT_TR_IN[4] | SAR1 ch#1, range violation to TCPWM1 Group #1 Counter #04 trig = 2 |
| 34 | PASS0_CH_RANGEVIO_TR_OUT[34] | TCPWM1_16M_ONE_CNT_TR_IN[7] | SAR1 ch#2, range violation to TCPWM1 Group #1 Counter #07 trig = 2 |
| 35 | PASS0_CH_RANGEVIO_TR_OUT[35] | TCPWM1_16M_ONE_CNT_TR_IN[10] | SAR1 ch#3, range violation to TCPWM1 Group #1 Counter #10 trig = 2 |
| 36 | PASS0_CH_RANGEVIO_TR_OUT[36] | TCPWM1_16_ONE_CNT_TR_IN[28] | SAR1 ch#4, range violation to TCPWM1 Group #0 Counter #28 trig = 2 |
| 37 | PASS0_CH_RANGEVIO_TR_OUT[37] | TCPWM1_16_ONE_CNT_TR_IN[29] | SAR1 ch#5, range violation to TCPWM1 Group #0 Counter #29 trig = 2 |
| 38 | PASS0_CH_RANGEVIO_TR_OUT[38] | TCPWM1_16_ONE_CNT_TR_IN[30] | SAR1 ch#6, range violation to TCPWM1 Group #0 Counter #30 trig = 2 |
| 39 | PASS0_CH_RANGEVIO_TR_OUT[39] | TCPWM1_16_ONE_CNT_TR_IN[31] | SAR1 ch#7, range violation to TCPWM1 Group #0 Counter #31 trig = 2 |
| 40 | PASS0_CH_RANGEVIO_TR_OUT[40] | TCPWM1_16_ONE_CNT_TR_IN[32] | SAR1 ch#8, range violation to TCPWM1 Group #0 Counter #32 trig = 2 |
| 41 | PASS0_CH_RANGEVIO_TR_OUT[41] | TCPWM1_16_ONE_CNT_TR_IN[33] | SAR1 ch#9, range violation to TCPWM1 Group #0 Counter #33 trig = 2 |
| 42 | PASS0_CH_RANGEVIO_TR_OUT[42] | TCPWM1_16_ONE_CNT_TR_IN[34] | SAR1 ch#10, range violation to TCPWM1 Group #0 Counter #34 trig = 2 |
| 43 | PASS0_CH_RANGEVIO_TR_OUT[43] | TCPWM1_16_ONE_CNT_TR_IN[35] | SAR1 ch#11, range violation to TCPWM1 Group #0 Counter #35 trig = 2 |
| 44 | PASS0_CH_RANGEVIO_TR_OUT[44] | TCPWM1_16_ONE_CNT_TR_IN[36] | SAR1 ch#12, range violation to TCPWM1 Group #0 Counter #36 trig = 2 |
| 45 | PASS0_CH_RANGEVIO_TR_OUT[45] | TCPWM1_16_ONE_CNT_TR_IN[37] | SAR1 ch#13, range violation to TCPWM1 Group #0 Counter #37 trig = 2 |
| 46 | PASS0_CH_RANGEVIO_TR_OUT[46] | TCPWM1_16_ONE_CNT_TR_IN[38] | SAR1 ch#14, range violation to TCPWM1 Group #0 Counter #38 trig = 2 |
| 47 | PASS0_CH_RANGEVIO_TR_OUT[47] | TCPWM1_16_ONE_CNT_TR_IN[39] | SAR1 ch#15, range violation to TCPWM1 Group #0 Counter #39 trig = 2 |
| 48 | PASS0_CH_RANGEVIO_TR_OUT[48] | TCPWM1_16_ONE_CNT_TR_IN[40] | SAR1 ch#16, range violation to TCPWM1 Group #0 Counter #40 trig = 2 |
| 49 | PASS0_CH_RANGEVIO_TR_OUT[49] | TCPWM1_16_ONE_CNT_TR_IN[41] | SAR1 ch#17, range violation to TCPWM1 Group #0 Counter #41 trig = 2 |

Table 18-1. Triggers 1:1 (continued)

| Input | Trigger In | Trigger Out | Description |
|-------|------------------------------|------------------------------|---|
| 50 | PASS0_CH_RANGEVIO_TR_OUT[50] | TCPWM1_16_ONE_CNT_TR_IN[42] | SAR1 ch#18, range violation to TCPWM1 Group #0 Counter #42 trig = 2 |
| 51 | PASS0_CH_RANGEVIO_TR_OUT[51] | TCPWM1_16_ONE_CNT_TR_IN[43] | SAR1 ch#19, range violation to TCPWM1 Group #0 Counter #43 trig = 2 |
| 52 | PASS0_CH_RANGEVIO_TR_OUT[52] | TCPWM1_16_ONE_CNT_TR_IN[44] | SAR1 ch#20, range violation to TCPWM1 Group #0 Counter #44 trig = 2 |
| 53 | PASS0_CH_RANGEVIO_TR_OUT[53] | TCPWM1_16_ONE_CNT_TR_IN[45] | SAR1 ch#21, range violation to TCPWM1 Group #0 Counter #45 trig = 2 |
| 54 | PASS0_CH_RANGEVIO_TR_OUT[54] | TCPWM1_16_ONE_CNT_TR_IN[46] | SAR1 ch#22, range violation to TCPWM1 Group #0 Counter #46 trig = 2 |
| 55 | PASS0_CH_RANGEVIO_TR_OUT[55] | TCPWM1_16_ONE_CNT_TR_IN[47] | SAR1 ch#23, range violation to TCPWM1 Group #0 Counter #47 trig = 2 |
| 56 | PASS0_CH_RANGEVIO_TR_OUT[56] | TCPWM1_16_ONE_CNT_TR_IN[48] | SAR1 ch#24, range violation to TCPWM1 Group #0 Counter #48 trig = 2 |
| 57 | PASS0_CH_RANGEVIO_TR_OUT[57] | TCPWM1_16_ONE_CNT_TR_IN[49] | SAR1 ch#25, range violation to TCPWM1 Group #0 Counter #49 trig = 2 |
| 58 | PASS0_CH_RANGEVIO_TR_OUT[58] | TCPWM1_16_ONE_CNT_TR_IN[50] | SAR1 ch#26, range violation to TCPWM1 Group #0 Counter #50 trig = 2 |
| 59 | PASS0_CH_RANGEVIO_TR_OUT[59] | TCPWM1_16_ONE_CNT_TR_IN[51] | SAR1 ch#27, range violation to TCPWM1 Group #0 Counter #51 trig = 2 |
| 60 | PASS0_CH_RANGEVIO_TR_OUT[60] | TCPWM1_16_ONE_CNT_TR_IN[52] | SAR1 ch#28, range violation to TCPWM1 Group #0 Counter #52 trig = 2 |
| 61 | PASS0_CH_RANGEVIO_TR_OUT[61] | TCPWM1_16_ONE_CNT_TR_IN[53] | SAR1 ch#29, range violation to TCPWM1 Group #0 Counter #53 trig = 2 |
| 62 | PASS0_CH_RANGEVIO_TR_OUT[62] | TCPWM1_16_ONE_CNT_TR_IN[54] | SAR1 ch#30, range violation to TCPWM1 Group #0 Counter #54 trig = 2 |
| 63 | PASS0_CH_RANGEVIO_TR_OUT[63] | TCPWM1_16_ONE_CNT_TR_IN[55] | SAR1 ch#31, range violation to TCPWM1 Group #0 Counter #55 trig = 2 |
| 64 | PASS0_CH_RANGEVIO_TR_OUT[64] | TCPWM1_16M_ONE_CNT_TR_IN[2] | SAR2 ch#0, range violation to TCPWM1 Group #1 Counter #02 trig = 2 |
| 65 | PASS0_CH_RANGEVIO_TR_OUT[65] | TCPWM1_16M_ONE_CNT_TR_IN[5] | SAR2 ch#1, range violation to TCPWM1 Group #1 Counter #05 trig = 2 |
| 66 | PASS0_CH_RANGEVIO_TR_OUT[66] | TCPWM1_16M_ONE_CNT_TR_IN[8] | SAR2 ch#2, range violation to TCPWM1 Group #1 Counter #08 trig = 2 |
| 67 | PASS0_CH_RANGEVIO_TR_OUT[67] | TCPWM1_16M_ONE_CNT_TR_IN[11] | SAR2 ch#3, range violation to TCPWM1 Group #1 Counter #11 trig = 2 |
| 68 | PASS0_CH_RANGEVIO_TR_OUT[68] | TCPWM1_16_ONE_CNT_TR_IN[56] | SAR2 ch#4, range violation to TCPWM1 Group #0 Counter #56 trig = 2 |
| 69 | PASS0_CH_RANGEVIO_TR_OUT[69] | TCPWM1_16_ONE_CNT_TR_IN[57] | SAR2 ch#5, range violation to TCPWM1 Group #0 Counter #57 trig = 2 |
| 70 | PASS0_CH_RANGEVIO_TR_OUT[70] | TCPWM1_16_ONE_CNT_TR_IN[58] | SAR2 ch#6, range violation to TCPWM1 Group #0 Counter #58 trig = 2 |
| 71 | PASS0_CH_RANGEVIO_TR_OUT[71] | TCPWM1_16_ONE_CNT_TR_IN[59] | SAR2 ch#7, range violation to TCPWM1 Group #0 Counter #59 trig = 2 |
| 72 | PASS0_CH_RANGEVIO_TR_OUT[72] | TCPWM1_16_ONE_CNT_TR_IN[60] | SAR2 ch#8, range violation to TCPWM1 Group #0 Counter #60 trig = 2 |
| 73 | PASS0_CH_RANGEVIO_TR_OUT[73] | TCPWM1_16_ONE_CNT_TR_IN[61] | SAR2 ch#9, range violation to TCPWM1 Group #0 Counter #61 trig = 2 |
| 74 | PASS0_CH_RANGEVIO_TR_OUT[74] | TCPWM1_16_ONE_CNT_TR_IN[62] | SAR2 ch#10, range violation to TCPWM1 Group #0 Counter #62 trig = 2 |
| 75 | PASS0_CH_RANGEVIO_TR_OUT[75] | TCPWM1_16_ONE_CNT_TR_IN[63] | SAR2 ch#11, range violation to TCPWM1 Group #0 Counter #63 trig = 2 |
| 76 | PASS0_CH_RANGEVIO_TR_OUT[76] | TCPWM1_16_ONE_CNT_TR_IN[64] | SAR2 ch#12, range violation to TCPWM1 Group #0 Counter #64 trig = 2 |
| 77 | PASS0_CH_RANGEVIO_TR_OUT[77] | TCPWM1_16_ONE_CNT_TR_IN[65] | SAR2 ch#13, range violation to TCPWM1 Group #0 Counter #65 trig = 2 |
| 78 | PASS0_CH_RANGEVIO_TR_OUT[78] | TCPWM1_16_ONE_CNT_TR_IN[66] | SAR2 ch#14, range violation to TCPWM1 Group #0 Counter #66 trig = 2 |
| 79 | PASS0_CH_RANGEVIO_TR_OUT[79] | TCPWM1_16_ONE_CNT_TR_IN[67] | SAR2 ch#15, range violation to TCPWM1 Group #0 Counter #67 trig = 2 |
| 80 | PASS0_CH_RANGEVIO_TR_OUT[80] | TCPWM1_16_ONE_CNT_TR_IN[68] | SAR2 ch#16, range violation to TCPWM1 Group #0 Counter #68 trig = 2 |
| 81 | PASS0_CH_RANGEVIO_TR_OUT[81] | TCPWM1_16_ONE_CNT_TR_IN[69] | SAR2 ch#17, range violation to TCPWM1 Group #0 Counter #69 trig = 2 |
| 82 | PASS0_CH_RANGEVIO_TR_OUT[82] | TCPWM1_16_ONE_CNT_TR_IN[70] | SAR2 ch#18, range violation to TCPWM1 Group #0 Counter #70 trig = 2 |
| 83 | PASS0_CH_RANGEVIO_TR_OUT[83] | TCPWM1_16_ONE_CNT_TR_IN[71] | SAR2 ch#19, range violation to TCPWM1 Group #0 Counter #71 trig = 2 |
| 84 | PASS0_CH_RANGEVIO_TR_OUT[84] | TCPWM1_16_ONE_CNT_TR_IN[72] | SAR2 ch#20, range violation to TCPWM1 Group #0 Counter #72 trig = 2 |
| 85 | PASS0_CH_RANGEVIO_TR_OUT[85] | TCPWM1_16_ONE_CNT_TR_IN[73] | SAR2 ch#21, range violation to TCPWM1 Group #0 Counter #73 trig = 2 |
| 86 | PASS0_CH_RANGEVIO_TR_OUT[86] | TCPWM1_16_ONE_CNT_TR_IN[74] | SAR2 ch#22, range violation to TCPWM1 Group #0 Counter #74 trig = 2 |
| 87 | PASS0_CH_RANGEVIO_TR_OUT[87] | TCPWM1_16_ONE_CNT_TR_IN[75] | SAR2 ch#23, range violation to TCPWM1 Group #0 Counter #75 trig = 2 |
| 88 | PASS0_CH_RANGEVIO_TR_OUT[88] | TCPWM1_16_ONE_CNT_TR_IN[76] | SAR2 ch#24, range violation to TCPWM1 Group #0 Counter #76 trig = 2 |
| 89 | PASS0_CH_RANGEVIO_TR_OUT[89] | TCPWM1_16_ONE_CNT_TR_IN[77] | SAR2 ch#25, range violation to TCPWM1 Group #0 Counter #77 trig = 2 |
| 90 | PASS0_CH_RANGEVIO_TR_OUT[90] | TCPWM1_16_ONE_CNT_TR_IN[78] | SAR2 ch#26, range violation to TCPWM1 Group #0 Counter #78 trig = 2 |

Table 18-1. Triggers 1:1 (continued)

| Input | Trigger In | Trigger Out | Description |
|--|------------------------------|-----------------------------|---|
| 91 | PASS0_CH_RANGEVIO_TR_OUT[91] | TCPWM1_16_ONE_CNT_TR_IN[79] | SAR2 ch#27, range violation to TCPWM1 Group #0 Counter #79 trig = 2 |
| 92 | PASS0_CH_RANGEVIO_TR_OUT[92] | TCPWM1_16_ONE_CNT_TR_IN[80] | SAR2 ch#28, range violation to TCPWM1 Group #0 Counter #80 trig = 2 |
| 93 | PASS0_CH_RANGEVIO_TR_OUT[93] | TCPWM1_16_ONE_CNT_TR_IN[81] | SAR2 ch#29, range violation to TCPWM1 Group #0 Counter #81 trig = 2 |
| 94 | PASS0_CH_RANGEVIO_TR_OUT[94] | TCPWM1_16_ONE_CNT_TR_IN[82] | SAR2 ch#30, range violation to TCPWM1 Group #0 Counter #82 trig = 2 |
| 95 | PASS0_CH_RANGEVIO_TR_OUT[95] | TCPWM1_16_ONE_CNT_TR_IN[83] | SAR2 ch#31, range violation to TCPWM1 Group #0 Counter #83 trig = 2 |
| MUX Group 7: TCPWM1 to PASS SARx | | | |
| 0 | TCPWM1_16M_TR_OUT1[0] | PASS0_CH_TR_IN[0] | TCPWM1 Group #1 Counter #00 (PWM1_M_0) to SAR0 ch#0 |
| 1 | TCPWM1_16M_TR_OUT1[3] | PASS0_CH_TR_IN[1] | TCPWM1 Group #1 Counter #03 (PWM1_M_3) to SAR0 ch#1 |
| 2 | TCPWM1_16M_TR_OUT1[6] | PASS0_CH_TR_IN[2] | TCPWM1 Group #1 Counter #06 (PWM1_M_6) to SAR0 ch#2 |
| 3 | TCPWM1_16M_TR_OUT1[9] | PASS0_CH_TR_IN[3] | TCPWM1 Group #1 Counter #09 (PWM1_M_9) to SAR0 ch#3 |
| 4:31 | TCPWM1_16_TR_OUT1[0:27] | PASS0_CH_TR_IN[4:31] | TCPWM1 Group #0 Counter #00 through 27 (PWM1_0 to PWM1_27) to SAR0 ch#4 through SAR0 ch#31 |
| 32 | TCPWM1_16M_TR_OUT1[1] | PASS0_CH_TR_IN[32] | TCPWM1 Group #1 Counter #01 (PWM1_M_1) to SAR1 ch#0 |
| 33 | TCPWM1_16M_TR_OUT1[4] | PASS0_CH_TR_IN[33] | TCPWM1 Group #1 Counter #04 (PWM1_M_4) to SAR1 ch#1 |
| 34 | TCPWM1_16M_TR_OUT1[7] | PASS0_CH_TR_IN[34] | TCPWM1 Group #1 Counter #07 (PWM1_M_7) to SAR1 ch#2 |
| 35 | TCPWM1_16M_TR_OUT1[10] | PASS0_CH_TR_IN[35] | TCPWM1 Group #1 Counter #10 (PWM1_M_10) to SAR1 ch#3 |
| 36:63 | TCPWM1_16_TR_OUT1[28:55] | PASS0_CH_TR_IN[36:63] | TCPWM1 Group #0 Counter #28 through 55 (PWM1_28 to PWM1_55) to SAR1 ch#4 through SAR1 ch#31 |
| 64 | TCPWM1_16M_TR_OUT1[2] | PASS0_CH_TR_IN[64] | TCPWM1 Group #1 Counter #02 (PWM1_M_2) to SAR2 ch#0 |
| 65 | TCPWM1_16M_TR_OUT1[5] | PASS0_CH_TR_IN[65] | TCPWM1 Group #1 Counter #05 (PWM1_M_5) to SAR2 ch#1 |
| 66 | TCPWM1_16M_TR_OUT1[8] | PASS0_CH_TR_IN[66] | TCPWM1 Group #1 Counter #08 (PWM1_M_8) to SAR2 ch#2 |
| 67 | TCPWM1_16M_TR_OUT1[11] | PASS0_CH_TR_IN[67] | TCPWM1 Group #1 Counter #11 (PWM1_M_11) to SAR2 ch#3 |
| 68:95 | TCPWM1_16_TR_OUT1[56:83] | PASS0_CH_TR_IN[68:95] | TCPWM1 Group #1 Counter #56 through 83 (PWM1_56 to PWM1_83) to SAR2 ch#4 through SAR2 ch#31 |
| MUX Group 8: Acknowledge triggers from P-DMA1 to CAN1 | | | |
| 0 | PDMA1_TR_OUT[38] | CAN1_DBG_TR_ACK[0] | CAN1 Channel#0 P-DMA1 acknowledge |
| 1 | PDMA1_TR_OUT[41] | CAN1_DBG_TR_ACK[1] | CAN1 Channel#1 P-DMA1 acknowledge |
| 2 | PDMA1_TR_OUT[44] | CAN1_DBG_TR_ACK[2] | CAN1 Channel#2 P-DMA1 acknowledge |
| 3 | PDMA1_TR_OUT[47] | CAN1_DBG_TR_ACK[3] | CAN1 Channel#3 P-DMA1 acknowledge |
| 4 | PDMA1_TR_OUT[50] | CAN1_DBG_TR_ACK[4] | CAN1 Channel#4 P-DMA1 acknowledge |
| MUX Group 9: Acknowledge triggers from P-DMA0 to CAN0 | | | |
| 0 | PDMA0_TR_OUT[32] | CAN0_DBG_TR_ACK[0] | CAN0 Channel#0 P-DMA0 acknowledge |
| 1 | PDMA0_TR_OUT[35] | CAN0_DBG_TR_ACK[1] | CAN0 Channel#1 P-DMA0 acknowledge |
| 2 | PDMA0_TR_OUT[38] | CAN0_DBG_TR_ACK[2] | CAN0 Channel#2 P-DMA0 acknowledge |
| 3 | PDMA0_TR_OUT[41] | CAN0_DBG_TR_ACK[3] | CAN0 Channel#3 P-DMA0 acknowledge |
| 4 | PDMA0_TR_OUT[44] | CAN0_DBG_TR_ACK[4] | CAN0 Channel#4 P-DMA0 acknowledge |
| MUX Group 10: TCPWM1 to LIN0 triggers | | | |
| 0:19 | TCPWM1_16_TR_OUT0[0:19] | LIN0_CMD_TR_IN[0:19] | TCPWM1 (Group #0 Counter #00 to #19) to LIN0 |
| MUX Group 11: FLEXRAY to P-DMA1 triggers | | | |
| 0 | FLEXRAY_IBF_TR_OUT | PDMA1_TR_IN[61] | FlexRay to P-DMA1 |
| 1 | FLEXRAY_OBF_TR_OUT | PDMA1_TR_IN[62] | FlexRay to P-DMA1 |
| MUX Group 12: P-DMA1 TO P-DMA1 triggers | | | |
| 0 | PDMA1_TR_OUT[61] | PDMA1_TR_IN[63] | P-DMA1 to P-DMA1 |

Table 18-1. Triggers 1:1 (continued)

| Input | Trigger In | Trigger Out | Description |
|---|------------------|-------------------|-------------------|
| 1 | PDMA1_TR_OUT[62] | PDMA1_TR_IN[64] | P-DMA1 to P-DMA1 |
| MUX Group 13: P-DMA1 TO FLEXRAY triggers | | | |
| 0 | PDMA1_TR_OUT[63] | FLEXRAY_IBF_TR_IN | P-DMA1 to FlexRay |
| 1 | PDMA1_TR_OUT[64] | FLEXRAY_OBF_TR_IN | P-DMA1 to FlexRay |

19. Peripheral Clocks

Table 19-1. Peripheral Clock Assignments

| Output | Destination | Description |
|------------------------------------|---------------------------|-----------------------------|
| CPUSS Root Clocks (Group 0) | | |
| 0 | PCLK_CPUSS_CLOCK_TRACE_IN | Trace clock |
| 1 | PCLK_SMARTIO12_CLOCK | Smart I/O #12 |
| 2 | PCLK_SMARTIO13_CLOCK | Smart I/O #13 |
| 3 | PCLK_SMARTIO14_CLOCK | Smart I/O #14 |
| 4 | PCLK_SMARTIO15_CLOCK | Smart I/O #15 |
| 5 | PCLK_SMARTIO17_CLOCK | Smart I/O #17 |
| 6 | PCLK_TCPWM0_CLOCKS0 | TCPWM0 Group #0, Counter #0 |
| 7 | PCLK_TCPWM0_CLOCKS1 | TCPWM0 Group #0, Counter #1 |
| 8 | PCLK_TCPWM0_CLOCKS2 | TCPWM0 Group #0, Counter #2 |
| 9 | PCLK_TCPWM0_CLOCKS256 | TCPWM0 Group #1, Counter #0 |
| 10 | PCLK_TCPWM0_CLOCKS257 | TCPWM0 Group #1, Counter #1 |
| 11 | PCLK_TCPWM0_CLOCKS258 | TCPWM0 Group #1, Counter #2 |
| 12 | PCLK_TCPWM0_CLOCKS512 | TCPWM0 Group #2, Counter #0 |
| 13 | PCLK_TCPWM0_CLOCKS513 | TCPWM0 Group #2, Counter #1 |
| 14 | PCLK_TCPWM0_CLOCKS514 | TCPWM0 Group #2, Counter #2 |
| COMM Root Clocks (Group 1) | | |
| 0 | PCLK_CANFD0_CLOCK_CAN0 | CAN0, Channel #0 |
| 1 | PCLK_CANFD0_CLOCK_CAN1 | CAN0, Channel #1 |
| 2 | PCLK_CANFD0_CLOCK_CAN2 | CAN0, Channel #2 |
| 3 | PCLK_CANFD0_CLOCK_CAN3 | CAN0, Channel #3 |
| 4 | PCLK_CANFD0_CLOCK_CAN4 | CAN0, Channel #4 |
| 5 | PCLK_CANFD1_CLOCK_CAN0 | CAN1, Channel #0 |
| 6 | PCLK_CANFD1_CLOCK_CAN1 | CAN1, Channel #1 |
| 7 | PCLK_CANFD1_CLOCK_CAN2 | CAN1, Channel #2 |
| 8 | PCLK_CANFD1_CLOCK_CAN3 | CAN1, Channel #3 |
| 9 | PCLK_CANFD1_CLOCK_CAN4 | CAN1, Channel #4 |
| 10 | PCLK_LIN0_CLOCK_CH_EN0 | LIN0, Channel #0 |
| 11 | PCLK_LIN0_CLOCK_CH_EN1 | LIN0, Channel #1 |
| 12 | PCLK_LIN0_CLOCK_CH_EN2 | LIN0, Channel #2 |
| 13 | PCLK_LIN0_CLOCK_CH_EN3 | LIN0, Channel #3 |
| 14 | PCLK_LIN0_CLOCK_CH_EN4 | LIN0, Channel #4 |
| 15 | PCLK_LIN0_CLOCK_CH_EN5 | LIN0, Channel #5 |
| 16 | PCLK_LIN0_CLOCK_CH_EN6 | LIN0, Channel #6 |
| 17 | PCLK_LIN0_CLOCK_CH_EN7 | LIN0, Channel #7 |
| 18 | PCLK_LIN0_CLOCK_CH_EN8 | LIN0, Channel #8 |
| 19 | PCLK_LIN0_CLOCK_CH_EN9 | LIN0, Channel #9 |
| 20 | PCLK_LIN0_CLOCK_CH_EN10 | LIN0, Channel #10 |
| 21 | PCLK_LIN0_CLOCK_CH_EN11 | LIN0, Channel #11 |
| 22 | PCLK_LIN0_CLOCK_CH_EN12 | LIN0, Channel #12 |

Table 19-1. Peripheral Clock Assignments (continued)

| Output | Destination | Description |
|--------|---------------------------|------------------------------|
| 23 | PCLK_LIN0_CLOCK_CH_EN13 | LIN0, Channel #13 |
| 24 | PCLK_LIN0_CLOCK_CH_EN14 | LIN0, Channel #14 |
| 25 | PCLK_LIN0_CLOCK_CH_EN15 | LIN0, Channel #15 |
| 26 | PCLK_LIN0_CLOCK_CH_EN16 | LIN0, Channel #16 |
| 27 | PCLK_LIN0_CLOCK_CH_EN17 | LIN0, Channel #17 |
| 28 | PCLK_LIN0_CLOCK_CH_EN18 | LIN0, Channel #18 |
| 29 | PCLK_LIN0_CLOCK_CH_EN19 | LIN0, Channel #19 |
| 30 | PCLK_SCB0_CLOCK | SCB0 |
| 31 | PCLK_SCB1_CLOCK | SCB1 |
| 32 | PCLK_SCB2_CLOCK | SCB2 |
| 33 | PCLK_SCB3_CLOCK | SCB3 |
| 34 | PCLK_SCB4_CLOCK | SCB4 |
| 35 | PCLK_SCB5_CLOCK | SCB5 |
| 36 | PCLK_SCB6_CLOCK | SCB6 |
| 37 | PCLK_SCB7_CLOCK | SCB7 |
| 38 | PCLK_SCB8_CLOCK | SCB8 |
| 39 | PCLK_SCB9_CLOCK | SCB9 |
| 40 | PCLK_SCB10_CLOCK | SCB10 |
| 41 | PCLK_FLEXRAY0_CLK_FLEXRAY | FlexRay0 clock |
| 42 | PCLK_PASS0_CLOCK_SAR0 | SAR0 |
| 43 | PCLK_PASS0_CLOCK_SAR1 | SAR1 |
| 44 | PCLK_PASS0_CLOCK_SAR2 | SAR2 |
| 45 | PCLK_TCPWM1_CLOCKS0 | TCPWM1 Group #0, Counter #0 |
| 46 | PCLK_TCPWM1_CLOCKS1 | TCPWM1 Group #0, Counter #1 |
| 47 | PCLK_TCPWM1_CLOCKS2 | TCPWM1 Group #0, Counter #2 |
| 48 | PCLK_TCPWM1_CLOCKS3 | TCPWM1 Group #0, Counter #3 |
| 49 | PCLK_TCPWM1_CLOCKS4 | TCPWM1 Group #0, Counter #4 |
| 50 | PCLK_TCPWM1_CLOCKS5 | TCPWM1 Group #0, Counter #5 |
| 51 | PCLK_TCPWM1_CLOCKS6 | TCPWM1 Group #0, Counter #6 |
| 52 | PCLK_TCPWM1_CLOCKS7 | TCPWM1 Group #0, Counter #7 |
| 53 | PCLK_TCPWM1_CLOCKS8 | TCPWM1 Group #0, Counter #8 |
| 54 | PCLK_TCPWM1_CLOCKS9 | TCPWM1 Group #0, Counter #9 |
| 55 | PCLK_TCPWM1_CLOCKS10 | TCPWM1 Group #0, Counter #10 |
| 56 | PCLK_TCPWM1_CLOCKS11 | TCPWM1 Group #0, Counter #11 |
| 57 | PCLK_TCPWM1_CLOCKS12 | TCPWM1 Group #0, Counter #12 |
| 58 | PCLK_TCPWM1_CLOCKS13 | TCPWM1 Group #0, Counter #13 |
| 59 | PCLK_TCPWM1_CLOCKS14 | TCPWM1 Group #0, Counter #14 |
| 60 | PCLK_TCPWM1_CLOCKS15 | TCPWM1 Group #0, Counter #15 |
| 61 | PCLK_TCPWM1_CLOCKS16 | TCPWM1 Group #0, Counter #16 |
| 62 | PCLK_TCPWM1_CLOCKS17 | TCPWM1 Group #0, Counter #17 |
| 63 | PCLK_TCPWM1_CLOCKS18 | TCPWM1 Group #0, Counter #18 |

Table 19-1. Peripheral Clock Assignments (continued)

| Output | Destination | Description |
|--------|----------------------|------------------------------|
| 64 | PCLK_TCPWM1_CLOCKS19 | TCPWM1 Group #0, Counter #19 |
| 65 | PCLK_TCPWM1_CLOCKS20 | TCPWM1 Group #0, Counter #20 |
| 66 | PCLK_TCPWM1_CLOCKS21 | TCPWM1 Group #0, Counter #21 |
| 67 | PCLK_TCPWM1_CLOCKS22 | TCPWM1 Group #0, Counter #22 |
| 68 | PCLK_TCPWM1_CLOCKS23 | TCPWM1 Group #0, Counter #23 |
| 69 | PCLK_TCPWM1_CLOCKS24 | TCPWM1 Group #0, Counter #24 |
| 70 | PCLK_TCPWM1_CLOCKS25 | TCPWM1 Group #0, Counter #25 |
| 71 | PCLK_TCPWM1_CLOCKS26 | TCPWM1 Group #0, Counter #26 |
| 72 | PCLK_TCPWM1_CLOCKS27 | TCPWM1 Group #0, Counter #27 |
| 73 | PCLK_TCPWM1_CLOCKS28 | TCPWM1 Group #0, Counter #28 |
| 74 | PCLK_TCPWM1_CLOCKS29 | TCPWM1 Group #0, Counter #29 |
| 75 | PCLK_TCPWM1_CLOCKS30 | TCPWM1 Group #0, Counter #30 |
| 76 | PCLK_TCPWM1_CLOCKS31 | TCPWM1 Group #0, Counter #31 |
| 77 | PCLK_TCPWM1_CLOCKS32 | TCPWM1 Group #0, Counter #32 |
| 78 | PCLK_TCPWM1_CLOCKS33 | TCPWM1 Group #0, Counter #33 |
| 79 | PCLK_TCPWM1_CLOCKS34 | TCPWM1 Group #0, Counter #34 |
| 80 | PCLK_TCPWM1_CLOCKS35 | TCPWM1 Group #0, Counter #35 |
| 81 | PCLK_TCPWM1_CLOCKS36 | TCPWM1 Group #0, Counter #36 |
| 82 | PCLK_TCPWM1_CLOCKS37 | TCPWM1 Group #0, Counter #37 |
| 83 | PCLK_TCPWM1_CLOCKS38 | TCPWM1 Group #0, Counter #38 |
| 84 | PCLK_TCPWM1_CLOCKS39 | TCPWM1 Group #0, Counter #39 |
| 85 | PCLK_TCPWM1_CLOCKS40 | TCPWM1 Group #0, Counter #40 |
| 86 | PCLK_TCPWM1_CLOCKS41 | TCPWM1 Group #0, Counter #41 |
| 87 | PCLK_TCPWM1_CLOCKS42 | TCPWM1 Group #0, Counter #42 |
| 88 | PCLK_TCPWM1_CLOCKS43 | TCPWM1 Group #0, Counter #43 |
| 89 | PCLK_TCPWM1_CLOCKS44 | TCPWM1 Group #0, Counter #44 |
| 90 | PCLK_TCPWM1_CLOCKS45 | TCPWM1 Group #0, Counter #45 |
| 91 | PCLK_TCPWM1_CLOCKS46 | TCPWM1 Group #0, Counter #46 |
| 92 | PCLK_TCPWM1_CLOCKS47 | TCPWM1 Group #0, Counter #47 |
| 93 | PCLK_TCPWM1_CLOCKS48 | TCPWM1 Group #0, Counter #48 |
| 94 | PCLK_TCPWM1_CLOCKS49 | TCPWM1 Group #0, Counter #49 |
| 95 | PCLK_TCPWM1_CLOCKS50 | TCPWM1 Group #0, Counter #50 |
| 96 | PCLK_TCPWM1_CLOCKS51 | TCPWM1 Group #0, Counter #51 |
| 97 | PCLK_TCPWM1_CLOCKS52 | TCPWM1 Group #0, Counter #52 |
| 98 | PCLK_TCPWM1_CLOCKS53 | TCPWM1 Group #0, Counter #53 |
| 99 | PCLK_TCPWM1_CLOCKS54 | TCPWM1 Group #0, Counter #54 |
| 100 | PCLK_TCPWM1_CLOCKS55 | TCPWM1 Group #0, Counter #55 |
| 101 | PCLK_TCPWM1_CLOCKS56 | TCPWM1 Group #0, Counter #56 |
| 102 | PCLK_TCPWM1_CLOCKS57 | TCPWM1 Group #0, Counter #57 |
| 103 | PCLK_TCPWM1_CLOCKS58 | TCPWM1 Group #0, Counter #58 |
| 104 | PCLK_TCPWM1_CLOCKS59 | TCPWM1 Group #0, Counter #59 |

Table 19-1. Peripheral Clock Assignments *(continued)*

| Output | Destination | Description |
|--------|-----------------------|------------------------------|
| 105 | PCLK_TCPWM1_CLOCKS60 | TCPWM1 Group #0, Counter #60 |
| 106 | PCLK_TCPWM1_CLOCKS61 | TCPWM1 Group #0, Counter #61 |
| 107 | PCLK_TCPWM1_CLOCKS62 | TCPWM1 Group #0, Counter #62 |
| 108 | PCLK_TCPWM1_CLOCKS63 | TCPWM1 Group #0, Counter #63 |
| 109 | PCLK_TCPWM1_CLOCKS64 | TCPWM1 Group #0, Counter #64 |
| 110 | PCLK_TCPWM1_CLOCKS65 | TCPWM1 Group #0, Counter #65 |
| 111 | PCLK_TCPWM1_CLOCKS66 | TCPWM1 Group #0, Counter #66 |
| 112 | PCLK_TCPWM1_CLOCKS67 | TCPWM1 Group #0, Counter #67 |
| 113 | PCLK_TCPWM1_CLOCKS68 | TCPWM1 Group #0, Counter #68 |
| 114 | PCLK_TCPWM1_CLOCKS69 | TCPWM1 Group #0, Counter #69 |
| 115 | PCLK_TCPWM1_CLOCKS70 | TCPWM1 Group #0, Counter #70 |
| 116 | PCLK_TCPWM1_CLOCKS71 | TCPWM1 Group #0, Counter #71 |
| 117 | PCLK_TCPWM1_CLOCKS72 | TCPWM1 Group #0, Counter #72 |
| 118 | PCLK_TCPWM1_CLOCKS73 | TCPWM1 Group #0, Counter #73 |
| 119 | PCLK_TCPWM1_CLOCKS74 | TCPWM1 Group #0, Counter #74 |
| 120 | PCLK_TCPWM1_CLOCKS75 | TCPWM1 Group #0, Counter #75 |
| 121 | PCLK_TCPWM1_CLOCKS76 | TCPWM1 Group #0, Counter #76 |
| 122 | PCLK_TCPWM1_CLOCKS77 | TCPWM1 Group #0, Counter #77 |
| 123 | PCLK_TCPWM1_CLOCKS78 | TCPWM1 Group #0, Counter #78 |
| 124 | PCLK_TCPWM1_CLOCKS79 | TCPWM1 Group #0, Counter #79 |
| 125 | PCLK_TCPWM1_CLOCKS80 | TCPWM1 Group #0, Counter #80 |
| 126 | PCLK_TCPWM1_CLOCKS81 | TCPWM1 Group #0, Counter #81 |
| 127 | PCLK_TCPWM1_CLOCKS82 | TCPWM1 Group #0, Counter #82 |
| 128 | PCLK_TCPWM1_CLOCKS83 | TCPWM1 Group #0, Counter #83 |
| 129 | PCLK_TCPWM1_CLOCKS256 | TCPWM1 Group #1, Counter #0 |
| 130 | PCLK_TCPWM1_CLOCKS257 | TCPWM1 Group #1, Counter #1 |
| 131 | PCLK_TCPWM1_CLOCKS258 | TCPWM1 Group #1, Counter #2 |
| 132 | PCLK_TCPWM1_CLOCKS259 | TCPWM1 Group #1, Counter #3 |
| 133 | PCLK_TCPWM1_CLOCKS260 | TCPWM1 Group #1, Counter #4 |
| 134 | PCLK_TCPWM1_CLOCKS261 | TCPWM1 Group #1, Counter #5 |
| 135 | PCLK_TCPWM1_CLOCKS262 | TCPWM1 Group #1, Counter #6 |
| 136 | PCLK_TCPWM1_CLOCKS263 | TCPWM1 Group #1, Counter #7 |
| 137 | PCLK_TCPWM1_CLOCKS264 | TCPWM1 Group #1, Counter #8 |
| 138 | PCLK_TCPWM1_CLOCKS265 | TCPWM1 Group #1, Counter #9 |
| 139 | PCLK_TCPWM1_CLOCKS266 | TCPWM1 Group #1, Counter #10 |
| 140 | PCLK_TCPWM1_CLOCKS267 | TCPWM1 Group #1, Counter #11 |
| 141 | PCLK_TCPWM1_CLOCKS512 | TCPWM1 Group #2, Counter #0 |
| 142 | PCLK_TCPWM1_CLOCKS513 | TCPWM1 Group #2, Counter #1 |
| 143 | PCLK_TCPWM1_CLOCKS514 | TCPWM1 Group #2, Counter #2 |
| 144 | PCLK_TCPWM1_CLOCKS515 | TCPWM1 Group #2, Counter #3 |
| 145 | PCLK_TCPWM1_CLOCKS516 | TCPWM1 Group #2, Counter #4 |

Table 19-1. Peripheral Clock Assignments *(continued)*

| Output | Destination | Description |
|---------------|-----------------------|------------------------------|
| 146 | PCLK_TCPWM1_CLOCKS517 | TCPWM1 Group #2, Counter #5 |
| 147 | PCLK_TCPWM1_CLOCKS518 | TCPWM1 Group #2, Counter #6 |
| 148 | PCLK_TCPWM1_CLOCKS519 | TCPWM1 Group #2, Counter #7 |
| 149 | PCLK_TCPWM1_CLOCKS520 | TCPWM1 Group #2, Counter #8 |
| 150 | PCLK_TCPWM1_CLOCKS521 | TCPWM1 Group #2, Counter #9 |
| 151 | PCLK_TCPWM1_CLOCKS522 | TCPWM1 Group #2, Counter #10 |
| 152 | PCLK_TCPWM1_CLOCKS523 | TCPWM1 Group #2, Counter #11 |
| 153 | PCLK_TCPWM1_CLOCKS524 | TCPWM1 Group #2, Counter #12 |

20. Faults

Table 20-1. Fault Assignments

| Fault | Source | Description |
|-------|--------------------------|---|
| 0 | CPUSS_MPU_VIO_0 | CM0+ SMPU violation DATA0[31:0]: Violating address. DATA1[0]: User read. DATA1[1]: User write. DATA1[2]: User execute. DATA1[3]: Privileged read. DATA1[4]: Privileged write. DATA1[5]: Privileged execute. DATA1[6]: Non-secure. DATA1[11:8]: Master identifier. DATA1[15:12]: Protection context identifier. DATA1[31]: '0' MPU violation; '1': SMPU violation. |
| 1 | CPUSS_MPU_VIO_1 | CRYPTO SMPU violation. See CPUSS_MPU_VIO_0 description. |
| 2 | CPUSS_MPU_VIO_2 | P-DMA0 MPU/SMPU violation. See CPUSS_MPU_VIO_0 description. |
| 3 | CPUSS_MPU_VIO_3 | P-DMA1 MPU/SMPU violation. See CPUSS_MPU_VIO_0 description. |
| 4 | CPUSS_MPU_VIO_4 | M-DMA0 MPU/SMPU violation. See CPUSS_MPU_VIO_0 description. |
| 5 | CPUSS_MPU_VIO_5 | SDHC MPU/SMPU violation. See CPUSS_MPU_VIO_0 description. |
| 9 | CPUSS_MPU_VIO_9 | Ethernet0 MPU/SMPU violation. See CPUSS_MPU_VIO_0 description. |
| 10 | CPUSS_MPU_VIO_10 | Ethernet1 MPU/SMPU violation. See CPUSS_MPU_VIO_0 description. |
| 13 | CPUSS_MPU_VIO_13 | CM7_1 MPU/SMPU violation. See CPUSS_MPU_VIO_0 description. |
| 14 | CPUSS_MPU_VIO_14 | CM7_0 MPU/SMPU violation. See CPUSS_MPU_VIO_0 description. |
| 15 | CPUSS_MPU_VIO_15 | Test Controller MPU/SMPU violation. See CPUSS_MPU_VIO_0 description. |
| 16 | CPUSS_CM7_1_TCM_C_ECC | Correctable ECC error in CM7_1 TCM memory DATA0[23:2]: Violating address. DATA1[7:0]: Syndrome of code word (at address offset 0x0). DATA1[31:30]: 0=ITCM, 2=DOTCM, 3=D1TCM |
| 17 | CPUSS_CM7_1_TCM_NC_ECC | Non Correctable ECC error in CM7_1 TCM memory. See CPUSS_CM7_1_TCM_C_ECC description. |
| 18 | CPUSS_CM7_0_CACHE_C_ECC | Correctable ECC error in CM7_0 Cache memories DATA0[16:2]: location information: Tag/Data SRAM, Way, Index and line Offset, see CM7 UGRM IEBR0/DEBR0 description for details. DATA0[31]: 0=Instruction cache, 1= Data cache |
| 19 | CPUSS_CM7_0_CACHE_NC_ECC | Non Correctable ECC error in CM7_0 Cache memories. See CPUSS_CM7_0_CACHE_C_ECC description. |
| 20 | CPUSS_CM7_1_CACHE_C_ECC | Correctable ECC error in CM7_1 Cache memories. See CPUSS_CM7_0_CACHE_C_ECC description. |
| 21 | CPUSS_CM7_1_CACHE_NC_ECC | Non Correctable ECC error in CM7_1 Cache memories. See CPUSS_CM7_0_CACHE_C_ECC description. |
| 25 | PERI_MS_VIO_4 | P-DMA1 Peripheral Master Interface PPU violation. See PERI_MS_VIO_0 description. |
| 26 | PERI_PERI_C_ECC | Peripheral protection SRAM correctable ECC violation DATA0[10:0]: Violating address. DATA1[7:0]: Syndrome of SRAM word. |
| 27 | PERI_PERI_NC_ECC | Peripheral protection SRAM non-correctable ECC violation |
| 28 | PERI_MS_VIO_0 | CM0+ Peripheral Master Interface PPU violation DATA0[31:0]: Violating address. DATA1[0]: User read. DATA1[1]: User write. DATA1[2]: User execute. DATA1[3]: Privileged read. DATA1[4]: Privileged write. DATA1[5]: Privileged execute. DATA1[6]: Non-secure. DATA1[11:8]: Master identifier. DATA1[15:12]: Protection context identifier. DATA1[31:28]: "0": master interface, PPU violation, "1": timeout detected, "2": bus error, other: undefined. |

Table 20-1. Fault Assignments (continued)

| Fault | Source | Description |
|-------|----------------------------|--|
| 29 | PERI_MS_VIO_1 | CM7_0 Peripheral Master Interface PPU violation. See PERI_MS_VIO_0 description. |
| 30 | PERI_MS_VIO_2 | CM7_1 Peripheral Master Interface PPU violation. See PERI_MS_VIO_0 description. |
| 31 | PERI_MS_VIO_3 | P-DMA0 Peripheral Master Interface PPU_3 violation. See PERI_MS_VIO_0 description. |
| 32 | PERI_GROUP_VIO_0 | Peripheral Group #0 PPU violation. DATA0[31:0]: Violating address. DATA1[0]: User read. DATA1[1]: User write. DATA1[2]: User execute. DATA1[3]: Privileged read. DATA1[4]: Privileged write. DATA1[5]: Privileged execute. DATA1[6]: Non-secure. DATA1[11:8]: Master identifier. DATA1[15:12]: Protection context identifier. DATA1[31:28]: "0": decoder or peripheral bus error, other: undefined. |
| 33 | PERI_GROUP_VIO_1 | Peripheral Group #1 PPU violation. See PERI_GROUP_VIO_0 description. |
| 34 | PERI_GROUP_VIO_2 | Peripheral Group #2 PPU violation. See PERI_GROUP_VIO_0 description. |
| 35 | PERI_GROUP_VIO_3 | Peripheral Group #3 PPU violation. See PERI_GROUP_VIO_0 description. |
| 36 | PERI_GROUP_VIO_4 | Peripheral Group #4 PPU violation. See PERI_GROUP_VIO_0 description. |
| 37 | PERI_GROUP_VIO_5 | Peripheral Group #5 PPU violation. See PERI_GROUP_VIO_0 description. |
| 38 | PERI_GROUP_VIO_6 | Peripheral Group #6 PPU violation. See PERI_GROUP_VIO_0 description. |
| 40 | PERI_GROUP_VIO_8 | Peripheral Group #8 PPU violation. See PERI_GROUP_VIO_0 description. |
| 41 | PERI_GROUP_VIO_9 | Peripheral Group #9 PPU violation. See PERI_GROUP_VIO_0 description. |
| 48 | CPUSS_FLASHC_MAIN_BUS_ERR | Flash controller main flash bus error FAULT_DATA0[26:0]: Violating address. Append 5'b00010 as most significant bits to derive 32-bit system address. FAULT_DATA1[11:8]: Master identifier. |
| 49 | CPUSS_FLASHC_MAIN_C_ECC | Flash controller main flash cache correctable ECC violation DATA[26:0]: Violating address. Append 5'b00010 as most significant bits to derive 32-bit system address. DATA1[7:0]: Syndrome of 64-bit word (at address offset 0x00). DATA1[15:8]: Syndrome of 64-bit word (at address offset 0x08). DATA1[23:16]: Syndrome of 64-bit word (at address offset 0x10). DATA1[31:24]: Syndrome of 64-bit word (at address offset 0x18). |
| 50 | CPUSS_FLASHC_MAIN_NC_ECC | Flash controller main flash cache non-correctable ECC violation. See CPUSS_FLASHC_MAIN_C_ECC description. |
| 51 | CPUSS_FLASHC_WORK_BUS_ERR | Flash controller work-flash bus error. See CPUSS_FLASHC_MAIN_BUS_ERR description. |
| 52 | CPUSS_FLASHC_WORK_C_ECC | Flash controller work flash cache correctable ECC violation. DATA0[26:0]: Violating address. Append 5'b00010 as most significant bits to derive 32-bit system address. DATA1[6:0]: Syndrome of 32-bit word. |
| 53 | CPUSS_FLASHC_WORK_NC_ECC | Flash controller work-flash cache non-correctable ECC violation. See CPUSS_FLASHC_WORK_C_ECC description. |
| 54 | CPUSS_FLASHC_CM0_CA_C_ECC | Flash controller CM0+ cache correctable ECC violation. DATA0[26:0]: Violating address. DATA1[6:0]: Syndrome of 32-bit SRAM word (at address offset 0x0). DATA1[14:8]: Syndrome of 32-bit SRAM word (at address offset 0x4). DATA1[22:16]: Syndrome of 32-bit SRAM word (at address offset 0x8). DATA1[30:24]: Syndrome of 32-bit SRAM word (at address offset 0xc). |
| 55 | CPUSS_FLASHC_CM0_CA_NC_ECC | Flash controller CM0+ cache non-correctable ECC violation. See CPUSS_FLASHC_CM0_CA_C_ECC description. |
| 56 | CPUSS_CM7_0_TCM_C_ECC | CPU CM7_0 TCM memory correctable ECC violation. See CPUSS_CM7_1_TCM_C_ECC description. |
| 57 | CPUSS_CM7_0_TCM_NC_ECC | CPU CM7_0 TCM memory non-correctable ECC violation. See CPUSS_CM7_1_TCM_C_ECC description. |

Table 20-1. Fault Assignments (continued)

| Fault | Source | Description |
|-------|----------------------|--|
| 58 | CPUSS_RAMC0_C_ECC | System memory controller 0 correctable ECC violation: DATA0[31:0]: Violating address. DATA1[6:0]: Syndrome of 32-bit SRAM code word. |
| 59 | CPUSS_RAMC0_NC_ECC | System memory controller 0 non-correctable ECC violation. See CPUSS_RAMC0_C_ECC description. |
| 60 | CPUSS_RAMC1_C_ECC | System memory controller 1 correctable ECC violation. See CPUSS_RAMC0_C_ECC description. |
| 61 | CPUSS_RAMC1_NC_ECC | System memory controller 1 non-correctable ECC violation. See CPUSS_RAMC0_C_ECC description. |
| 62 | CPUSS_RAMC2_C_ECC | System memory controller 2 correctable ECC violation. See CPUSS_RAMC0_C_ECC description. |
| 63 | CPUSS_RAMC2_NC_ECC | System memory controller 2 non-correctable ECC violation. See CPUSS_RAMC0_C_ECC description. |
| 64 | CPUSS_CRYPT0_C_ECC | Crypto memory correctable ECC violation. DATA0[31:0]: Violating address. DATA1[6:0]: Syndrome of Least Significant 32-bit SRAM. DATA1[14:8]: Syndrome of Most Significant 32-bit SRAM. |
| 65 | CPUSS_CRYPT0_NC_ECC | CRYPTO memory non-correctable ECC violation. See CPUSS_CRYPT0_C_ECC description. |
| 70 | CPUSS_DW0_C_ECC | P-DMA0 memory correctable ECC violation: DATA0[11:0]: Violating DW SRAM address (word address, assuming byte addressable). DATA1[6:0]: Syndrome of 32-bit SRAM code word. |
| 71 | CPUSS_DW0_NC_ECC | P-DMA0 memory non-correctable ECC violation. See CPUSS_DW0_C_ECC description. |
| 72 | CPUSS_DW1_C_ECC | P-DMA1 memory correctable ECC violation. See CPUSS_DW0_C_ECC description. |
| 73 | CPUSS_DW1_NC_ECC | P-DMA1 memory non-correctable ECC violation. See CPUSS_DW0_C_ECC description. |
| 74 | CPUSS_FM_SRAM_C_ECC | Flash code storage SRAM memory correctable ECC violation: DATA0[15:0]: Address location in the eCT Flash SRAM. DATA1[6:0]: Syndrome of 32-bit SRAM word. |
| 75 | CPUSS_FM_SRAM_NC_ECC | Flash code storage SRAM memory non-correctable ECC violation: See CPUSS_FM_SRAMC_C_ECC description. |
| 80 | CANFD_0_CAN_C_ECC | CAN0 message buffer correctable ECC violation: DATA0[15:0]: Violating address. DATA0[22:16]: ECC violating data[38:32] from MRAM. DATA0[27:24]: Master ID: 0-7 = CAN channel ID within mxttcanfd cluster, 8 = AHB I/F DATA1[31:0]: ECC violating data[31:0] from MRAM. |
| 81 | CANFD_0_CAN_NC_ECC | CAN0 message buffer non-correctable ECC violation: DATA0[15:0]: Violating address. DATA0[22:16]: ECC violating data[38:32] from MRAM (not for Address Error). DATA0[27:24]: Master ID: 0-7 = CAN channel ID within mxttcanfd cluster, 8 = AHB I/F DATA0[30]: Write access, only possible for Address Error DATA0[31]: Address Error: a CAN channel did an MRAM access above MRAM_SIZE DATA1[31:0]: ECC violating data[31:0] from MRAM (not for Address Error). |
| 82 | CANFD_1_CAN_C_ECC | CAN1 message buffer correctable ECC violation. See CANFD_0_CAN_C_ECC description. |
| 83 | CANFD_1_CAN_NC_ECC | CAN1 message buffer non-correctable ECC violation. See CANFD_0_CAN_NC_ECC description. |
| 90 | SRSS_FAULT_CSV | Consolidated fault output for clock supervisors. Multiple CSV can detect a violation at the same time. DATA0[15:0]: CLK_HF* root CSV violation flags. DATA0[24]: CLK_REF CSV violation flag (reference clock for CLK_HF CSVs) DATA0[25]: CLK_LF CSV violation flag DATA0[26]: CLK_HVILO CSV violation flag |
| 91 | SRSS_FAULT_SSV | Consolidated fault output for supply supervisors. Multiple CSV can detect a violation at the same time. DATA0[0]: BOD on VDDA DATA[1]: OVD on VDDA DATA[16]: LVD/HVD #1 DATA0[17]: LVD/HVD #2 |

Table 20-1. Fault Assignments *(continued)*

| Fault | Source | Description |
|-------|-------------------|---|
| 92 | SRSS_FAULT_MCWDT0 | Fault output for MCWDT0 (all sub-counters) Multiple counters can detect a violation at the same time. DATA0[0]: MCWDT sub counter 0 LOWER_LIMIT DATA0[1]: MCWDT sub counter 0 UPPER_LIMIT DATA0[2]: MCWDT sub counter 1 LOWER_LIMIT DATA0[3]: MCWDT sub counter 1 UPPER_LIMIT |
| 93 | SRSS_FAULT_MCWDT1 | Fault output for MCWDT1 (all sub-counters). See SRSS_FAULT_MCWDT0 description. |
| 94 | SRSS_FAULT_MCWDT2 | Fault output for MCWDT2 (all sub-counters). See SRSS_FAULT_MCWDT0 description. |

21. Peripheral Protection Unit Fixed Structure Pairs

Protection pair is a pair PPU structures, a master, and a slave structure. The master structure protects the slave structure, and the slave structure protects resources such as peripheral registers, or the peripheral itself.

Table 21-1. PPU Fixed Structure Pairs

| Pair No. | PPU Fixed Structure Pair | Address | Size | Description |
|----------|---|------------|------------|---------------------------------|
| 0 | PERI_MS_PPU_FX_PERI_MAIN | 0x40000200 | 0x00000040 | Peripheral Interconnect main |
| 1 | PERI_MS_PPU_FX_PERI_SECURE | 0x40002000 | 0x00000004 | Peripheral interconnect secure |
| 2 | PERI_MS_PPU_FX_PERI_GR0_GROUP | 0x40004010 | 0x00000004 | Peripheral Group #0 main |
| 3 | PERI_MS_PPU_FX_PERI_GR1_GROUP | 0x40004050 | 0x00000004 | Peripheral Group #1 main |
| 4 | PERI_MS_PPU_FX_PERI_GR2_GROUP | 0x40004090 | 0x00000004 | Peripheral Group #2 main |
| 5 | PERI_MS_PPU_FX_PERI_GR3_GROUP | 0x400040C0 | 0x00000020 | Peripheral Group #3 main |
| 6 | PERI_MS_PPU_FX_PERI_GR4_GROUP | 0x40004100 | 0x00000020 | Peripheral Group #4 main |
| 7 | PERI_MS_PPU_FX_PERI_GR5_GROUP | 0x40004140 | 0x00000020 | Peripheral Group #5 main |
| 8 | PERI_MS_PPU_FX_PERI_GR6_GROUP | 0x40004180 | 0x00000020 | Peripheral Group #6 main |
| 9 | PERI_MS_PPU_FX_PERI_GR8_GROUP | 0x40004200 | 0x00000020 | Peripheral Group #8 main |
| 10 | PERI_MS_PPU_FX_PERI_GR9_GROUP | 0x40004240 | 0x00000020 | Peripheral Group #9 main |
| 11 | PERI_MS_PPU_FX_PERI_GR0_BOOT | 0x40004020 | 0x00000004 | Peripheral Group #0 boot |
| 12 | PERI_MS_PPU_FX_PERI_GR1_BOOT | 0x40004060 | 0x00000004 | Peripheral Group #1 boot |
| 13 | PERI_MS_PPU_FX_PERI_GR2_BOOT | 0x400040A0 | 0x00000004 | Peripheral Group #2 boot |
| 14 | PERI_MS_PPU_FX_PERI_GR3_BOOT | 0x400040E0 | 0x00000004 | Peripheral Group #3 boot |
| 15 | PERI_MS_PPU_FX_PERI_GR4_BOOT | 0x40004120 | 0x00000004 | Peripheral Group #4 boot |
| 16 | PERI_MS_PPU_FX_PERI_GR5_BOOT | 0x40004160 | 0x00000004 | Peripheral Group #5 boot |
| 17 | PERI_MS_PPU_FX_PERI_GR6_BOOT | 0x400041A0 | 0x00000004 | Peripheral Group #6 boot |
| 18 | PERI_MS_PPU_FX_PERI_GR8_BOOT | 0x40004220 | 0x00000004 | Peripheral Group #8 boot |
| 19 | PERI_MS_PPU_FX_PERI_GR9_BOOT | 0x40004260 | 0x00000004 | Peripheral Group #9 boot |
| 20 | PERI_MS_PPU_FX_PERI_TR | 0x40008000 | 0x00008000 | Peripheral trigger multiplexer |
| 21 | PERI_MS_PPU_FX_PERI_MS_BOOT | 0x40030000 | 0x00001000 | Peripheral master slave boot |
| 22 | PERI_MS_PPU_FX_PERI_PCLK_MAIN | 0x40040000 | 0x00004000 | Peripheral clock main |
| 23 | PERI_MS_PPU_FX_CRYPT0_MAIN | 0x40100000 | 0x00000400 | Crypto main |
| 24 | PERI_MS_PPU_FX_CRYPT0_CRYPT0 | 0x40101000 | 0x00000800 | Crypto MMIO (Memory Mapped I/O) |
| 25 | PERI_MS_PPU_FX_CRYPT0_BOOT | 0x40102000 | 0x00000100 | Crypto boot |
| 26 | PERI_MS_PPU_FX_CRYPT0_KEY0 | 0x40102100 | 0x00000004 | Crypto Key #0 |
| 27 | PERI_MS_PPU_FX_CRYPT0_KEY1 | 0x40102120 | 0x00000004 | Crypto Key #1 |
| 28 | PERI_MS_PPU_FX_CRYPT0_BUF | 0x40108000 | 0x00002000 | Crypto buffer |
| 29 | PERI_MS_PPU_FX_CPUSS_CM7_0 | 0x40200000 | 0x00000400 | CM7_0 CPU core |
| 30 | PERI_MS_PPU_FX_CPUSS_CM7_1 | 0x40200400 | 0x00000400 | CM7_1 CPU core |
| 31 | PERI_MS_PPU_FX_CPUSS_CM0 | 0x40201000 | 0x00001000 | CM0+ CPU core |
| 32 | PERI_MS_PPU_FX_CPUSS_BOOT ^[31] | 0x40202000 | 0x00000200 | CPUSS boot |
| 33 | PERI_MS_PPU_FX_CPUSS_CM0_INT | 0x40208000 | 0x00001000 | CPUSS CM0+ interrupts |
| 34 | PERI_MS_PPU_FX_CPUSS_CM7_0_INT | 0x4020A000 | 0x00001000 | CPUSS CM7_0 interrupts |
| 35 | PERI_MS_PPU_FX_CPUSS_CM7_1_INT | 0x4020C000 | 0x00001000 | CPUSS CM7_1 interrupts |
| 36 | PERI_MS_PPU_FX_FAULT_STRUCTURE0_MAIN | 0x40210000 | 0x00000100 | CPUSS Fault Structure #0 main |
| 37 | PERI_MS_PPU_FX_FAULT_STRUCTURE1_MAIN | 0x40210100 | 0x00000100 | CPUSS Fault Structure #1 main |

Table 21-1. PPU Fixed Structure Pairs (continued)

| Pair No. | PPU Fixed Structure Pair | Address | Size | Description |
|----------|---|------------|------------|------------------------------------|
| 38 | PERI_MS_PPU_FX_FAULT_STRUCT2_MAIN | 0x40210200 | 0x00000100 | CPUSS Fault Structure #2 main |
| 39 | PERI_MS_PPU_FX_FAULT_STRUCT3_MAIN | 0x40210300 | 0x00000100 | CPUSS Fault Structure #3 main |
| 40 | PERI_MS_PPU_FX_IPC_STRUCT0_IPC | 0x40220000 | 0x00000020 | CPUSS IPC Structure #0 |
| 41 | PERI_MS_PPU_FX_IPC_STRUCT1_IPC | 0x40220020 | 0x00000020 | CPUSS IPC Structure #1 |
| 42 | PERI_MS_PPU_FX_IPC_STRUCT2_IPC | 0x40220040 | 0x00000020 | CPUSS IPC Structure #2 |
| 43 | PERI_MS_PPU_FX_IPC_STRUCT3_IPC | 0x40220060 | 0x00000020 | CPUSS IPC Structure #3 |
| 44 | PERI_MS_PPU_FX_IPC_STRUCT4_IPC | 0x40220080 | 0x00000020 | CPUSS IPC Structure #4 |
| 45 | PERI_MS_PPU_FX_IPC_STRUCT5_IPC | 0x402200A0 | 0x00000020 | CPUSS IPC Structure #5 |
| 46 | PERI_MS_PPU_FX_IPC_STRUCT6_IPC | 0x402200C0 | 0x00000020 | CPUSS IPC Structure #6 |
| 47 | PERI_MS_PPU_FX_IPC_STRUCT7_IPC | 0x402200E0 | 0x00000020 | CPUSS IPC Structure #7 |
| 48 | PERI_MS_PPU_FX_IPC_INTR_STRUCT0_INTR | 0x40221000 | 0x00000010 | CPUSS IPC Interrupt Structure #0 |
| 49 | PERI_MS_PPU_FX_IPC_INTR_STRUCT1_INTR | 0x40221020 | 0x00000010 | CPUSS IPC Interrupt Structure #1 |
| 50 | PERI_MS_PPU_FX_IPC_INTR_STRUCT2_INTR | 0x40221040 | 0x00000010 | CPUSS IPC Interrupt Structure #2 |
| 51 | PERI_MS_PPU_FX_IPC_INTR_STRUCT3_INTR | 0x40221060 | 0x00000010 | CPUSS IPC Interrupt Structure #3 |
| 52 | PERI_MS_PPU_FX_IPC_INTR_STRUCT4_INTR | 0x40221080 | 0x00000010 | CPUSS IPC Interrupt Structure #4 |
| 53 | PERI_MS_PPU_FX_IPC_INTR_STRUCT5_INTR | 0x402210A0 | 0x00000010 | CPUSS IPC Interrupt Structure #5 |
| 54 | PERI_MS_PPU_FX_IPC_INTR_STRUCT6_INTR | 0x402210C0 | 0x00000010 | CPUSS IPC Interrupt Structure #6 |
| 55 | PERI_MS_PPU_FX_IPC_INTR_STRUCT7_INTR | 0x402210E0 | 0x00000010 | CPUSS IPC Interrupt Structure #7 |
| 56 | PERI_MS_PPU_FX_PROT_SMPU_MAIN | 0x40230000 | 0x00000040 | Peripheral protection SMPU main |
| 57 | PERI_MS_PPU_FX_PROT_MPU0_MAIN | 0x40234000 | 0x00000004 | Peripheral protection MPU #0 main |
| 58 | PERI_MS_PPU_FX_PROT_MPU5_MAIN | 0x40235400 | 0x00000400 | Peripheral protection MPU #5 main |
| 59 | PERI_MS_PPU_FX_PROT_MPU9_MAIN | 0x40236400 | 0x00000400 | Peripheral protection MPU #9 main |
| 60 | PERI_MS_PPU_FX_PROT_MPU10_MAIN | 0x40236800 | 0x00000400 | Peripheral protection MPU #10 main |
| 61 | PERI_MS_PPU_FX_PROT_MPU13_MAIN | 0x40237400 | 0x00000004 | Peripheral protection MPU #13 main |
| 62 | PERI_MS_PPU_FX_PROT_MPU14_MAIN | 0x40237800 | 0x00000004 | Peripheral protection MPU #14 main |
| 63 | PERI_MS_PPU_FX_PROT_MPU15_MAIN | 0x40237C00 | 0x00000400 | Peripheral protection MPU #15 main |
| 64 | PERI_MS_PPU_FX_FLASHC_MAIN | 0x40240000 | 0x00000008 | Flash controller main |
| 65 | PERI_MS_PPU_FX_FLASHC_CMD | 0x40240008 | 0x00000004 | Flash controller command |
| 66 | PERI_MS_PPU_FX_FLASHC_DFT | 0x40240200 | 0x00000100 | Flash controller tests |
| 67 | PERI_MS_PPU_FX_FLASHC_CM0 | 0x40240400 | 0x00000080 | Flash controller CM0+ |
| 68 | PERI_MS_PPU_FX_FLASHC_CM7_0 | 0x402404E0 | 0x00000004 | Flash controller CM7_0 |
| 69 | PERI_MS_PPU_FX_FLASHC_CM7_1 | 0x40240560 | 0x00000004 | Flash controller CM7_1 |
| 70 | PERI_MS_PPU_FX_FLASHC_CRYPT0 | 0x40240580 | 0x00000004 | Flash controller Crypto |
| 71 | PERI_MS_PPU_FX_FLASHC_DW0 | 0x40240600 | 0x00000004 | Flash controller P-DMA0 |
| 72 | PERI_MS_PPU_FX_FLASHC_DW1 | 0x40240680 | 0x00000004 | Flash controller P-DMA1 |
| 73 | PERI_MS_PPU_FX_FLASHC_DMAC | 0x40240700 | 0x00000004 | Flash controller M-DMA0 |
| 74 | PERI_MS_PPU_FX_FLASHC_SLOW0 | 0x40240780 | 0x00000004 | Flash External AHB-Lite Master 0 |
| 75 | PERI_MS_PPU_FX_FLASHC_FlashMgmt ^[31] | 0x4024F000 | 0x00000080 | Flash management |
| 76 | PERI_MS_PPU_FX_FLASHC_MainSafety | 0x4024F400 | 0x00000008 | Flash controller code-flash safety |

Note

31. Fixed PPU is configured inside the Boot and user is not allowed to change the attributes of this PPU.

Table 21-1. PPU Fixed Structure Pairs (continued)

| Pair No. | PPU Fixed Structure Pair | Address | Size | Description |
|----------|-----------------------------------|------------|------------|------------------------------------|
| 77 | PERI_MS_PPU_FX_FLASHC_WorkSafety | 0x4024F500 | 0x00000004 | Flash controller work-flash safety |
| 78 | PERI_MS_PPU_FX_SRSS_GENERAL | 0x40260000 | 0x00000400 | SRSS General |
| 79 | PERI_MS_PPU_FX_SRSS_MAIN | 0x40261000 | 0x00001000 | SRSS main |
| 80 | PERI_MS_PPU_FX_SRSS_SECURE | 0x40262000 | 0x00002000 | SRSS secure |
| 81 | PERI_MS_PPU_FX_MCWDT0_CONFIG | 0x40268000 | 0x00000080 | MCWDT #0 configuration |
| 82 | PERI_MS_PPU_FX_MCWDT1_CONFIG | 0x40268100 | 0x00000080 | MCWDT #1 configuration |
| 83 | PERI_MS_PPU_FX_MCWDT2_CONFIG | 0x40268200 | 0x00000080 | MCWDT #2 configuration |
| 84 | PERI_MS_PPU_FX_MCWDT0_MAIN | 0x40268080 | 0x00000040 | MCWDT #0 main |
| 85 | PERI_MS_PPU_FX_MCWDT1_MAIN | 0x40268180 | 0x00000040 | MCWDT #1 main |
| 86 | PERI_MS_PPU_FX_MCWDT2_MAIN | 0x40268280 | 0x00000040 | MCWDT #2 main |
| 87 | PERI_MS_PPU_FX_WDT_CONFIG | 0x4026C000 | 0x00000020 | System WDT configuration |
| 88 | PERI_MS_PPU_FX_WDT_MAIN | 0x4026C040 | 0x00000020 | System WDT main |
| 89 | PERI_MS_PPU_FX_BACKUP_BACKUP | 0x40270000 | 0x00010000 | SRSS backup |
| 90 | PERI_MS_PPU_FX_DW0_DW | 0x40280000 | 0x00000100 | P-DMA0 main |
| 91 | PERI_MS_PPU_FX_DW1_DW | 0x40290000 | 0x00000100 | P-DMA1 main |
| 92 | PERI_MS_PPU_FX_DW0_DW_CRC | 0x40280100 | 0x00000080 | P-DMA0 CRC |
| 93 | PERI_MS_PPU_FX_DW1_DW_CRC | 0x40290100 | 0x00000080 | P-DMA1 CRC |
| 94 | PERI_MS_PPU_FX_DW0_CH_STRUCT0_CH | 0x40288000 | 0x00000040 | P-DMA0 Channel #0 |
| 95 | PERI_MS_PPU_FX_DW0_CH_STRUCT1_CH | 0x40288040 | 0x00000040 | P-DMA0 Channel #1 |
| 96 | PERI_MS_PPU_FX_DW0_CH_STRUCT2_CH | 0x40288080 | 0x00000040 | P-DMA0 Channel #2 |
| 97 | PERI_MS_PPU_FX_DW0_CH_STRUCT3_CH | 0x402880C0 | 0x00000040 | P-DMA0 Channel #3 |
| 98 | PERI_MS_PPU_FX_DW0_CH_STRUCT4_CH | 0x40288100 | 0x00000040 | P-DMA0 Channel #4 |
| 99 | PERI_MS_PPU_FX_DW0_CH_STRUCT5_CH | 0x40288140 | 0x00000040 | P-DMA0 Channel #5 |
| 100 | PERI_MS_PPU_FX_DW0_CH_STRUCT6_CH | 0x40288180 | 0x00000040 | P-DMA0 Channel #6 |
| 101 | PERI_MS_PPU_FX_DW0_CH_STRUCT7_CH | 0x402881C0 | 0x00000040 | P-DMA0 Channel #7 |
| 102 | PERI_MS_PPU_FX_DW0_CH_STRUCT8_CH | 0x40288200 | 0x00000040 | P-DMA0 Channel #8 |
| 103 | PERI_MS_PPU_FX_DW0_CH_STRUCT9_CH | 0x40288240 | 0x00000040 | P-DMA0 Channel #9 |
| 104 | PERI_MS_PPU_FX_DW0_CH_STRUCT10_CH | 0x40288280 | 0x00000040 | P-DMA0 Channel #10 |
| 105 | PERI_MS_PPU_FX_DW0_CH_STRUCT11_CH | 0x402882C0 | 0x00000040 | P-DMA0 Channel #11 |
| 106 | PERI_MS_PPU_FX_DW0_CH_STRUCT12_CH | 0x40288300 | 0x00000040 | P-DMA0 Channel #12 |
| 107 | PERI_MS_PPU_FX_DW0_CH_STRUCT13_CH | 0x40288340 | 0x00000040 | P-DMA0 Channel #13 |
| 108 | PERI_MS_PPU_FX_DW0_CH_STRUCT14_CH | 0x40288380 | 0x00000040 | P-DMA0 Channel #14 |
| 109 | PERI_MS_PPU_FX_DW0_CH_STRUCT15_CH | 0x402883C0 | 0x00000040 | P-DMA0 Channel #15 |
| 110 | PERI_MS_PPU_FX_DW0_CH_STRUCT16_CH | 0x40288400 | 0x00000040 | P-DMA0 Channel #16 |
| 111 | PERI_MS_PPU_FX_DW0_CH_STRUCT17_CH | 0x40288440 | 0x00000040 | P-DMA0 Channel #17 |
| 112 | PERI_MS_PPU_FX_DW0_CH_STRUCT18_CH | 0x40288480 | 0x00000040 | P-DMA0 Channel #18 |
| 113 | PERI_MS_PPU_FX_DW0_CH_STRUCT19_CH | 0x402884C0 | 0x00000040 | P-DMA0 Channel #19 |
| 114 | PERI_MS_PPU_FX_DW0_CH_STRUCT20_CH | 0x40288500 | 0x00000040 | P-DMA0 Channel #20 |
| 115 | PERI_MS_PPU_FX_DW0_CH_STRUCT21_CH | 0x40288540 | 0x00000040 | P-DMA0 Channel #21 |
| 116 | PERI_MS_PPU_FX_DW0_CH_STRUCT22_CH | 0x40288580 | 0x00000040 | P-DMA0 Channel #22 |
| 117 | PERI_MS_PPU_FX_DW0_CH_STRUCT23_CH | 0x402885C0 | 0x00000040 | P-DMA0 Channel #23 |

Table 21-1. PPU Fixed Structure Pairs (continued)

| Pair No. | PPU Fixed Structure Pair | Address | Size | Description |
|----------|-----------------------------------|------------|------------|--------------------|
| 118 | PERI_MS_PPU_FX_DW0_CH_STRUCT24_CH | 0x40288600 | 0x00000040 | P-DMA0 Channel #24 |
| 119 | PERI_MS_PPU_FX_DW0_CH_STRUCT25_CH | 0x40288640 | 0x00000040 | P-DMA0 Channel #25 |
| 120 | PERI_MS_PPU_FX_DW0_CH_STRUCT26_CH | 0x40288680 | 0x00000040 | P-DMA0 Channel #26 |
| 121 | PERI_MS_PPU_FX_DW0_CH_STRUCT27_CH | 0x402886C0 | 0x00000040 | P-DMA0 Channel #27 |
| 122 | PERI_MS_PPU_FX_DW0_CH_STRUCT28_CH | 0x40288700 | 0x00000040 | P-DMA0 Channel #28 |
| 123 | PERI_MS_PPU_FX_DW0_CH_STRUCT29_CH | 0x40288740 | 0x00000040 | P-DMA0 Channel #29 |
| 124 | PERI_MS_PPU_FX_DW0_CH_STRUCT30_CH | 0x40288780 | 0x00000040 | P-DMA0 Channel #30 |
| 125 | PERI_MS_PPU_FX_DW0_CH_STRUCT31_CH | 0x402887C0 | 0x00000040 | P-DMA0 Channel #31 |
| 126 | PERI_MS_PPU_FX_DW0_CH_STRUCT32_CH | 0x40288800 | 0x00000040 | P-DMA0 Channel #32 |
| 127 | PERI_MS_PPU_FX_DW0_CH_STRUCT33_CH | 0x40288840 | 0x00000040 | P-DMA0 Channel #33 |
| 128 | PERI_MS_PPU_FX_DW0_CH_STRUCT34_CH | 0x40288880 | 0x00000040 | P-DMA0 Channel #34 |
| 129 | PERI_MS_PPU_FX_DW0_CH_STRUCT35_CH | 0x402888C0 | 0x00000040 | P-DMA0 Channel #35 |
| 130 | PERI_MS_PPU_FX_DW0_CH_STRUCT36_CH | 0x40288900 | 0x00000040 | P-DMA0 Channel #36 |
| 131 | PERI_MS_PPU_FX_DW0_CH_STRUCT37_CH | 0x40288940 | 0x00000040 | P-DMA0 Channel #37 |
| 132 | PERI_MS_PPU_FX_DW0_CH_STRUCT38_CH | 0x40288980 | 0x00000040 | P-DMA0 Channel #38 |
| 133 | PERI_MS_PPU_FX_DW0_CH_STRUCT39_CH | 0x402889C0 | 0x00000040 | P-DMA0 Channel #39 |
| 134 | PERI_MS_PPU_FX_DW0_CH_STRUCT40_CH | 0x40288A00 | 0x00000040 | P-DMA0 Channel #40 |
| 135 | PERI_MS_PPU_FX_DW0_CH_STRUCT41_CH | 0x40288A40 | 0x00000040 | P-DMA0 Channel #41 |
| 136 | PERI_MS_PPU_FX_DW0_CH_STRUCT42_CH | 0x40288A80 | 0x00000040 | P-DMA0 Channel #42 |
| 137 | PERI_MS_PPU_FX_DW0_CH_STRUCT43_CH | 0x40288AC0 | 0x00000040 | P-DMA0 Channel #43 |
| 138 | PERI_MS_PPU_FX_DW0_CH_STRUCT44_CH | 0x40288B00 | 0x00000040 | P-DMA0 Channel #44 |
| 139 | PERI_MS_PPU_FX_DW0_CH_STRUCT45_CH | 0x40288B40 | 0x00000040 | P-DMA0 Channel #45 |
| 140 | PERI_MS_PPU_FX_DW0_CH_STRUCT46_CH | 0x40288B80 | 0x00000040 | P-DMA0 Channel #46 |
| 141 | PERI_MS_PPU_FX_DW0_CH_STRUCT47_CH | 0x40288BC0 | 0x00000040 | P-DMA0 Channel #47 |
| 142 | PERI_MS_PPU_FX_DW0_CH_STRUCT48_CH | 0x40288C00 | 0x00000040 | P-DMA0 Channel #48 |
| 143 | PERI_MS_PPU_FX_DW0_CH_STRUCT49_CH | 0x40288C40 | 0x00000040 | P-DMA0 Channel #49 |
| 144 | PERI_MS_PPU_FX_DW0_CH_STRUCT50_CH | 0x40288C80 | 0x00000040 | P-DMA0 Channel #50 |
| 145 | PERI_MS_PPU_FX_DW0_CH_STRUCT51_CH | 0x40288CC0 | 0x00000040 | P-DMA0 Channel #51 |
| 146 | PERI_MS_PPU_FX_DW0_CH_STRUCT52_CH | 0x40288D00 | 0x00000040 | P-DMA0 Channel #52 |
| 147 | PERI_MS_PPU_FX_DW0_CH_STRUCT53_CH | 0x40288D40 | 0x00000040 | P-DMA0 Channel #53 |
| 148 | PERI_MS_PPU_FX_DW0_CH_STRUCT54_CH | 0x40288D80 | 0x00000040 | P-DMA0 Channel #54 |
| 149 | PERI_MS_PPU_FX_DW0_CH_STRUCT55_CH | 0x40288DC0 | 0x00000040 | P-DMA0 Channel #55 |
| 150 | PERI_MS_PPU_FX_DW0_CH_STRUCT56_CH | 0x40288E00 | 0x00000040 | P-DMA0 Channel #56 |
| 151 | PERI_MS_PPU_FX_DW0_CH_STRUCT57_CH | 0x40288E40 | 0x00000040 | P-DMA0 Channel #57 |
| 152 | PERI_MS_PPU_FX_DW0_CH_STRUCT58_CH | 0x40288E80 | 0x00000040 | P-DMA0 Channel #58 |
| 153 | PERI_MS_PPU_FX_DW0_CH_STRUCT59_CH | 0x40288EC0 | 0x00000040 | P-DMA0 Channel #59 |
| 154 | PERI_MS_PPU_FX_DW0_CH_STRUCT60_CH | 0x40288F00 | 0x00000040 | P-DMA0 Channel #60 |
| 155 | PERI_MS_PPU_FX_DW0_CH_STRUCT61_CH | 0x40288F40 | 0x00000040 | P-DMA0 Channel #61 |
| 156 | PERI_MS_PPU_FX_DW0_CH_STRUCT62_CH | 0x40288F80 | 0x00000040 | P-DMA0 Channel #62 |
| 157 | PERI_MS_PPU_FX_DW0_CH_STRUCT63_CH | 0x40288FC0 | 0x00000040 | P-DMA0 Channel #63 |
| 158 | PERI_MS_PPU_FX_DW0_CH_STRUCT64_CH | 0x40289000 | 0x00000040 | P-DMA0 Channel #64 |

Table 21-1. PPU Fixed Structure Pairs (continued)

| Pair No. | PPU Fixed Structure Pair | Address | Size | Description |
|----------|------------------------------------|------------|------------|---------------------|
| 159 | PERI_MS_PPU_FX_DW0_CH_STRUCT65_CH | 0x40289040 | 0x00000040 | P-DMA0 Channel #65 |
| 160 | PERI_MS_PPU_FX_DW0_CH_STRUCT66_CH | 0x40289080 | 0x00000040 | P-DMA0 Channel #66 |
| 161 | PERI_MS_PPU_FX_DW0_CH_STRUCT67_CH | 0x402890C0 | 0x00000040 | P-DMA0 Channel #67 |
| 162 | PERI_MS_PPU_FX_DW0_CH_STRUCT68_CH | 0x40289100 | 0x00000040 | P-DMA0 Channel #68 |
| 163 | PERI_MS_PPU_FX_DW0_CH_STRUCT69_CH | 0x40289140 | 0x00000040 | P-DMA0 Channel #69 |
| 164 | PERI_MS_PPU_FX_DW0_CH_STRUCT70_CH | 0x40289180 | 0x00000040 | P-DMA0 Channel #70 |
| 165 | PERI_MS_PPU_FX_DW0_CH_STRUCT71_CH | 0x402891C0 | 0x00000040 | P-DMA0 Channel #71 |
| 166 | PERI_MS_PPU_FX_DW0_CH_STRUCT72_CH | 0x40289200 | 0x00000040 | P-DMA0 Channel #72 |
| 167 | PERI_MS_PPU_FX_DW0_CH_STRUCT73_CH | 0x40289240 | 0x00000040 | P-DMA0 Channel #73 |
| 168 | PERI_MS_PPU_FX_DW0_CH_STRUCT74_CH | 0x40289280 | 0x00000040 | P-DMA0 Channel #74 |
| 169 | PERI_MS_PPU_FX_DW0_CH_STRUCT75_CH | 0x402892C0 | 0x00000040 | P-DMA0 Channel #75 |
| 170 | PERI_MS_PPU_FX_DW0_CH_STRUCT76_CH | 0x40289300 | 0x00000040 | P-DMA0 Channel #76 |
| 171 | PERI_MS_PPU_FX_DW0_CH_STRUCT77_CH | 0x40289340 | 0x00000040 | P-DMA0 Channel #77 |
| 172 | PERI_MS_PPU_FX_DW0_CH_STRUCT78_CH | 0x40289380 | 0x00000040 | P-DMA0 Channel #78 |
| 173 | PERI_MS_PPU_FX_DW0_CH_STRUCT79_CH | 0x402893C0 | 0x00000040 | P-DMA0 Channel #79 |
| 174 | PERI_MS_PPU_FX_DW0_CH_STRUCT80_CH | 0x40289400 | 0x00000040 | P-DMA0 Channel #80 |
| 175 | PERI_MS_PPU_FX_DW0_CH_STRUCT81_CH | 0x40289440 | 0x00000040 | P-DMA0 Channel #81 |
| 176 | PERI_MS_PPU_FX_DW0_CH_STRUCT82_CH | 0x40289480 | 0x00000040 | P-DMA0 Channel #82 |
| 177 | PERI_MS_PPU_FX_DW0_CH_STRUCT83_CH | 0x402894C0 | 0x00000040 | P-DMA0 Channel #83 |
| 178 | PERI_MS_PPU_FX_DW0_CH_STRUCT84_CH | 0x40289500 | 0x00000040 | P-DMA0 Channel #84 |
| 179 | PERI_MS_PPU_FX_DW0_CH_STRUCT85_CH | 0x40289540 | 0x00000040 | P-DMA0 Channel #85 |
| 180 | PERI_MS_PPU_FX_DW0_CH_STRUCT86_CH | 0x40289580 | 0x00000040 | P-DMA0 Channel #86 |
| 181 | PERI_MS_PPU_FX_DW0_CH_STRUCT87_CH | 0x402895C0 | 0x00000040 | P-DMA0 Channel #87 |
| 182 | PERI_MS_PPU_FX_DW0_CH_STRUCT88_CH | 0x40289600 | 0x00000040 | P-DMA0 Channel #88 |
| 183 | PERI_MS_PPU_FX_DW0_CH_STRUCT89_CH | 0x40289640 | 0x00000040 | P-DMA0 Channel #89 |
| 184 | PERI_MS_PPU_FX_DW0_CH_STRUCT90_CH | 0x40289680 | 0x00000040 | P-DMA0 Channel #90 |
| 185 | PERI_MS_PPU_FX_DW0_CH_STRUCT91_CH | 0x402896C0 | 0x00000040 | P-DMA0 Channel #91 |
| 186 | PERI_MS_PPU_FX_DW0_CH_STRUCT92_CH | 0x40289700 | 0x00000040 | P-DMA0 Channel #92 |
| 187 | PERI_MS_PPU_FX_DW0_CH_STRUCT93_CH | 0x40289740 | 0x00000040 | P-DMA0 Channel #93 |
| 188 | PERI_MS_PPU_FX_DW0_CH_STRUCT94_CH | 0x40289780 | 0x00000040 | P-DMA0 Channel #94 |
| 189 | PERI_MS_PPU_FX_DW0_CH_STRUCT95_CH | 0x402897C0 | 0x00000040 | P-DMA0 Channel #95 |
| 190 | PERI_MS_PPU_FX_DW0_CH_STRUCT96_CH | 0x40289800 | 0x00000040 | P-DMA0 Channel #96 |
| 191 | PERI_MS_PPU_FX_DW0_CH_STRUCT97_CH | 0x40289840 | 0x00000040 | P-DMA0 Channel #97 |
| 192 | PERI_MS_PPU_FX_DW0_CH_STRUCT98_CH | 0x40289880 | 0x00000040 | P-DMA0 Channel #98 |
| 193 | PERI_MS_PPU_FX_DW0_CH_STRUCT99_CH | 0x402898C0 | 0x00000040 | P-DMA0 Channel #99 |
| 194 | PERI_MS_PPU_FX_DW0_CH_STRUCT100_CH | 0x40289900 | 0x00000040 | P-DMA0 Channel #100 |
| 195 | PERI_MS_PPU_FX_DW0_CH_STRUCT101_CH | 0x40289940 | 0x00000040 | P-DMA0 Channel #101 |
| 196 | PERI_MS_PPU_FX_DW0_CH_STRUCT102_CH | 0x40289980 | 0x00000040 | P-DMA0 Channel #102 |
| 197 | PERI_MS_PPU_FX_DW0_CH_STRUCT103_CH | 0x402899C0 | 0x00000040 | P-DMA0 Channel #103 |
| 198 | PERI_MS_PPU_FX_DW0_CH_STRUCT104_CH | 0x40289A00 | 0x00000040 | P-DMA0 Channel #104 |
| 199 | PERI_MS_PPU_FX_DW0_CH_STRUCT105_CH | 0x40289A40 | 0x00000040 | P-DMA0 Channel #105 |

Table 21-1. PPU Fixed Structure Pairs (continued)

| Pair No. | PPU Fixed Structure Pair | Address | Size | Description |
|----------|------------------------------------|------------|------------|---------------------|
| 200 | PERI_MS_PPU_FX_DW0_CH_STRUCT106_CH | 0x40289A80 | 0x00000040 | P-DMA0 Channel #106 |
| 201 | PERI_MS_PPU_FX_DW0_CH_STRUCT107_CH | 0x40289AC0 | 0x00000040 | P-DMA0 Channel #107 |
| 202 | PERI_MS_PPU_FX_DW0_CH_STRUCT108_CH | 0x40289B00 | 0x00000040 | P-DMA0 Channel #108 |
| 203 | PERI_MS_PPU_FX_DW0_CH_STRUCT109_CH | 0x40289B40 | 0x00000040 | P-DMA0 Channel #109 |
| 204 | PERI_MS_PPU_FX_DW0_CH_STRUCT110_CH | 0x40289B80 | 0x00000040 | P-DMA0 Channel #110 |
| 205 | PERI_MS_PPU_FX_DW0_CH_STRUCT111_CH | 0x40289BC0 | 0x00000040 | P-DMA0 Channel #111 |
| 206 | PERI_MS_PPU_FX_DW0_CH_STRUCT112_CH | 0x40289C00 | 0x00000040 | P-DMA0 Channel #112 |
| 207 | PERI_MS_PPU_FX_DW0_CH_STRUCT113_CH | 0x40289C40 | 0x00000040 | P-DMA0 Channel #113 |
| 208 | PERI_MS_PPU_FX_DW0_CH_STRUCT114_CH | 0x40289C80 | 0x00000040 | P-DMA0 Channel #114 |
| 209 | PERI_MS_PPU_FX_DW0_CH_STRUCT115_CH | 0x40289CC0 | 0x00000040 | P-DMA0 Channel #115 |
| 210 | PERI_MS_PPU_FX_DW0_CH_STRUCT116_CH | 0x40289D00 | 0x00000040 | P-DMA0 Channel #116 |
| 211 | PERI_MS_PPU_FX_DW0_CH_STRUCT117_CH | 0x40289D40 | 0x00000040 | P-DMA0 Channel #117 |
| 212 | PERI_MS_PPU_FX_DW0_CH_STRUCT118_CH | 0x40289D80 | 0x00000040 | P-DMA0 Channel #118 |
| 213 | PERI_MS_PPU_FX_DW0_CH_STRUCT119_CH | 0x40289DC0 | 0x00000040 | P-DMA0 Channel #119 |
| 214 | PERI_MS_PPU_FX_DW0_CH_STRUCT120_CH | 0x40289E00 | 0x00000040 | P-DMA0 Channel #120 |
| 215 | PERI_MS_PPU_FX_DW0_CH_STRUCT121_CH | 0x40289E40 | 0x00000040 | P-DMA0 Channel #121 |
| 216 | PERI_MS_PPU_FX_DW0_CH_STRUCT122_CH | 0x40289E80 | 0x00000040 | P-DMA0 Channel #122 |
| 217 | PERI_MS_PPU_FX_DW0_CH_STRUCT123_CH | 0x40289EC0 | 0x00000040 | P-DMA0 Channel #123 |
| 218 | PERI_MS_PPU_FX_DW0_CH_STRUCT124_CH | 0x40289F00 | 0x00000040 | P-DMA0 Channel #124 |
| 219 | PERI_MS_PPU_FX_DW0_CH_STRUCT125_CH | 0x40289F40 | 0x00000040 | P-DMA0 Channel #125 |
| 220 | PERI_MS_PPU_FX_DW0_CH_STRUCT126_CH | 0x40289F80 | 0x00000040 | P-DMA0 Channel #126 |
| 221 | PERI_MS_PPU_FX_DW0_CH_STRUCT127_CH | 0x40289FC0 | 0x00000040 | P-DMA0 Channel #127 |
| 222 | PERI_MS_PPU_FX_DW0_CH_STRUCT128_CH | 0x4028A000 | 0x00000040 | P-DMA0 Channel #128 |
| 223 | PERI_MS_PPU_FX_DW0_CH_STRUCT129_CH | 0x4028A040 | 0x00000040 | P-DMA0 Channel #129 |
| 224 | PERI_MS_PPU_FX_DW0_CH_STRUCT130_CH | 0x4028A080 | 0x00000040 | P-DMA0 Channel #130 |
| 225 | PERI_MS_PPU_FX_DW0_CH_STRUCT131_CH | 0x4028A0C0 | 0x00000040 | P-DMA0 Channel #131 |
| 226 | PERI_MS_PPU_FX_DW0_CH_STRUCT132_CH | 0x4028A100 | 0x00000040 | P-DMA0 Channel #132 |
| 227 | PERI_MS_PPU_FX_DW0_CH_STRUCT133_CH | 0x4028A140 | 0x00000040 | P-DMA0 Channel #133 |
| 228 | PERI_MS_PPU_FX_DW0_CH_STRUCT134_CH | 0x4028A180 | 0x00000040 | P-DMA0 Channel #134 |
| 229 | PERI_MS_PPU_FX_DW0_CH_STRUCT135_CH | 0x4028A1C0 | 0x00000040 | P-DMA0 Channel #135 |
| 230 | PERI_MS_PPU_FX_DW0_CH_STRUCT136_CH | 0x4028A200 | 0x00000040 | P-DMA0 Channel #136 |
| 231 | PERI_MS_PPU_FX_DW0_CH_STRUCT137_CH | 0x4028A240 | 0x00000040 | P-DMA0 Channel #137 |
| 232 | PERI_MS_PPU_FX_DW0_CH_STRUCT138_CH | 0x4028A280 | 0x00000040 | P-DMA0 Channel #138 |
| 233 | PERI_MS_PPU_FX_DW0_CH_STRUCT139_CH | 0x4028A2C0 | 0x00000040 | P-DMA0 Channel #139 |
| 234 | PERI_MS_PPU_FX_DW0_CH_STRUCT140_CH | 0x4028A300 | 0x00000040 | P-DMA0 Channel #140 |
| 235 | PERI_MS_PPU_FX_DW0_CH_STRUCT141_CH | 0x4028A340 | 0x00000040 | P-DMA0 Channel #141 |
| 236 | PERI_MS_PPU_FX_DW0_CH_STRUCT142_CH | 0x4028A380 | 0x00000040 | P-DMA0 Channel #142 |
| 237 | PERI_MS_PPU_FX_DW1_CH_STRUCT0_CH | 0x40298000 | 0x00000040 | P-DMA1 Channel #0 |
| 238 | PERI_MS_PPU_FX_DW1_CH_STRUCT1_CH | 0x40298040 | 0x00000040 | P-DMA1 Channel #1 |
| 239 | PERI_MS_PPU_FX_DW1_CH_STRUCT2_CH | 0x40298080 | 0x00000040 | P-DMA1 Channel #2 |
| 240 | PERI_MS_PPU_FX_DW1_CH_STRUCT3_CH | 0x402980C0 | 0x00000040 | P-DMA1 Channel #3 |

Table 21-1. PPU Fixed Structure Pairs (continued)

| Pair No. | PPU Fixed Structure Pair | Address | Size | Description |
|----------|-----------------------------------|------------|------------|--------------------|
| 241 | PERI_MS_PPU_FX_DW1_CH_STRUCT4_CH | 0x40298100 | 0x00000040 | P-DMA1 Channel #4 |
| 242 | PERI_MS_PPU_FX_DW1_CH_STRUCT5_CH | 0x40298140 | 0x00000040 | P-DMA1 Channel #5 |
| 243 | PERI_MS_PPU_FX_DW1_CH_STRUCT6_CH | 0x40298180 | 0x00000040 | P-DMA1 Channel #6 |
| 244 | PERI_MS_PPU_FX_DW1_CH_STRUCT7_CH | 0x402981C0 | 0x00000040 | P-DMA1 Channel #7 |
| 245 | PERI_MS_PPU_FX_DW1_CH_STRUCT8_CH | 0x40298200 | 0x00000040 | P-DMA1 Channel #8 |
| 246 | PERI_MS_PPU_FX_DW1_CH_STRUCT9_CH | 0x40298240 | 0x00000040 | P-DMA1 Channel #9 |
| 247 | PERI_MS_PPU_FX_DW1_CH_STRUCT10_CH | 0x40298280 | 0x00000040 | P-DMA1 Channel #10 |
| 248 | PERI_MS_PPU_FX_DW1_CH_STRUCT11_CH | 0x402982C0 | 0x00000040 | P-DMA1 Channel #11 |
| 249 | PERI_MS_PPU_FX_DW1_CH_STRUCT12_CH | 0x40298300 | 0x00000040 | P-DMA1 Channel #12 |
| 250 | PERI_MS_PPU_FX_DW1_CH_STRUCT13_CH | 0x40298340 | 0x00000040 | P-DMA1 Channel #13 |
| 251 | PERI_MS_PPU_FX_DW1_CH_STRUCT14_CH | 0x40298380 | 0x00000040 | P-DMA1 Channel #14 |
| 252 | PERI_MS_PPU_FX_DW1_CH_STRUCT15_CH | 0x402983C0 | 0x00000040 | P-DMA1 Channel #15 |
| 253 | PERI_MS_PPU_FX_DW1_CH_STRUCT16_CH | 0x40298400 | 0x00000040 | P-DMA1 Channel #16 |
| 254 | PERI_MS_PPU_FX_DW1_CH_STRUCT17_CH | 0x40298440 | 0x00000040 | P-DMA1 Channel #17 |
| 255 | PERI_MS_PPU_FX_DW1_CH_STRUCT18_CH | 0x40298480 | 0x00000040 | P-DMA1 Channel #18 |
| 256 | PERI_MS_PPU_FX_DW1_CH_STRUCT19_CH | 0x402984C0 | 0x00000040 | P-DMA1 Channel #19 |
| 257 | PERI_MS_PPU_FX_DW1_CH_STRUCT20_CH | 0x40298500 | 0x00000040 | P-DMA1 Channel #20 |
| 258 | PERI_MS_PPU_FX_DW1_CH_STRUCT21_CH | 0x40298540 | 0x00000040 | P-DMA1 Channel #21 |
| 259 | PERI_MS_PPU_FX_DW1_CH_STRUCT22_CH | 0x40298580 | 0x00000040 | P-DMA1 Channel #22 |
| 260 | PERI_MS_PPU_FX_DW1_CH_STRUCT23_CH | 0x402985C0 | 0x00000040 | P-DMA1 Channel #23 |
| 261 | PERI_MS_PPU_FX_DW1_CH_STRUCT24_CH | 0x40298600 | 0x00000040 | P-DMA1 Channel #24 |
| 262 | PERI_MS_PPU_FX_DW1_CH_STRUCT25_CH | 0x40298640 | 0x00000040 | P-DMA1 Channel #25 |
| 263 | PERI_MS_PPU_FX_DW1_CH_STRUCT26_CH | 0x40298680 | 0x00000040 | P-DMA1 Channel #26 |
| 264 | PERI_MS_PPU_FX_DW1_CH_STRUCT27_CH | 0x402986C0 | 0x00000040 | P-DMA1 Channel #27 |
| 265 | PERI_MS_PPU_FX_DW1_CH_STRUCT28_CH | 0x40298700 | 0x00000040 | P-DMA1 Channel #28 |
| 266 | PERI_MS_PPU_FX_DW1_CH_STRUCT29_CH | 0x40298740 | 0x00000040 | P-DMA1 Channel #29 |
| 267 | PERI_MS_PPU_FX_DW1_CH_STRUCT30_CH | 0x40298780 | 0x00000040 | P-DMA1 Channel #30 |
| 268 | PERI_MS_PPU_FX_DW1_CH_STRUCT31_CH | 0x402987C0 | 0x00000040 | P-DMA1 Channel #31 |
| 269 | PERI_MS_PPU_FX_DW1_CH_STRUCT32_CH | 0x40298800 | 0x00000040 | P-DMA1 Channel #32 |
| 270 | PERI_MS_PPU_FX_DW1_CH_STRUCT33_CH | 0x40298840 | 0x00000040 | P-DMA1 Channel #33 |
| 271 | PERI_MS_PPU_FX_DW1_CH_STRUCT34_CH | 0x40298880 | 0x00000040 | P-DMA1 Channel #34 |
| 272 | PERI_MS_PPU_FX_DW1_CH_STRUCT35_CH | 0x402988C0 | 0x00000040 | P-DMA1 Channel #35 |
| 273 | PERI_MS_PPU_FX_DW1_CH_STRUCT36_CH | 0x40298900 | 0x00000040 | P-DMA1 Channel #36 |
| 274 | PERI_MS_PPU_FX_DW1_CH_STRUCT37_CH | 0x40298940 | 0x00000040 | P-DMA1 Channel #37 |
| 275 | PERI_MS_PPU_FX_DW1_CH_STRUCT38_CH | 0x40298980 | 0x00000040 | P-DMA1 Channel #38 |
| 276 | PERI_MS_PPU_FX_DW1_CH_STRUCT39_CH | 0x402989C0 | 0x00000040 | P-DMA1 Channel #39 |
| 277 | PERI_MS_PPU_FX_DW1_CH_STRUCT40_CH | 0x40298A00 | 0x00000040 | P-DMA1 Channel #40 |
| 278 | PERI_MS_PPU_FX_DW1_CH_STRUCT41_CH | 0x40298A40 | 0x00000040 | P-DMA1 Channel #41 |
| 279 | PERI_MS_PPU_FX_DW1_CH_STRUCT42_CH | 0x40298A80 | 0x00000040 | P-DMA1 Channel #42 |
| 280 | PERI_MS_PPU_FX_DW1_CH_STRUCT43_CH | 0x40298AC0 | 0x00000040 | P-DMA1 Channel #43 |
| 281 | PERI_MS_PPU_FX_DW1_CH_STRUCT44_CH | 0x40298B00 | 0x00000040 | P-DMA1 Channel #44 |

Table 21-1. PPU Fixed Structure Pairs (continued)

| Pair No. | PPU Fixed Structure Pair | Address | Size | Description |
|----------|-----------------------------------|------------|------------|--------------------|
| 282 | PERI_MS_PPU_FX_DW1_CH_STRUCT45_CH | 0x40298B40 | 0x00000040 | P-DMA1 Channel #45 |
| 283 | PERI_MS_PPU_FX_DW1_CH_STRUCT46_CH | 0x40298B80 | 0x00000040 | P-DMA1 Channel #46 |
| 284 | PERI_MS_PPU_FX_DW1_CH_STRUCT47_CH | 0x40298BC0 | 0x00000040 | P-DMA1 Channel #47 |
| 285 | PERI_MS_PPU_FX_DW1_CH_STRUCT48_CH | 0x40298C00 | 0x00000040 | P-DMA1 Channel #48 |
| 286 | PERI_MS_PPU_FX_DW1_CH_STRUCT49_CH | 0x40298C40 | 0x00000040 | P-DMA1 Channel #49 |
| 287 | PERI_MS_PPU_FX_DW1_CH_STRUCT50_CH | 0x40298C80 | 0x00000040 | P-DMA1 Channel #50 |
| 288 | PERI_MS_PPU_FX_DW1_CH_STRUCT51_CH | 0x40298CC0 | 0x00000040 | P-DMA1 Channel #51 |
| 289 | PERI_MS_PPU_FX_DW1_CH_STRUCT52_CH | 0x40298D00 | 0x00000040 | P-DMA1 Channel #52 |
| 290 | PERI_MS_PPU_FX_DW1_CH_STRUCT53_CH | 0x40298D40 | 0x00000040 | P-DMA1 Channel #53 |
| 291 | PERI_MS_PPU_FX_DW1_CH_STRUCT54_CH | 0x40298D80 | 0x00000040 | P-DMA1 Channel #54 |
| 292 | PERI_MS_PPU_FX_DW1_CH_STRUCT55_CH | 0x40298DC0 | 0x00000040 | P-DMA1 Channel #55 |
| 293 | PERI_MS_PPU_FX_DW1_CH_STRUCT56_CH | 0x40298E00 | 0x00000040 | P-DMA1 Channel #56 |
| 294 | PERI_MS_PPU_FX_DW1_CH_STRUCT57_CH | 0x40298E40 | 0x00000040 | P-DMA1 Channel #57 |
| 295 | PERI_MS_PPU_FX_DW1_CH_STRUCT58_CH | 0x40298E80 | 0x00000040 | P-DMA1 Channel #58 |
| 296 | PERI_MS_PPU_FX_DW1_CH_STRUCT59_CH | 0x40298EC0 | 0x00000040 | P-DMA1 Channel #59 |
| 297 | PERI_MS_PPU_FX_DW1_CH_STRUCT60_CH | 0x40298F00 | 0x00000040 | P-DMA1 Channel #60 |
| 298 | PERI_MS_PPU_FX_DW1_CH_STRUCT61_CH | 0x40298F40 | 0x00000040 | P-DMA1 Channel #61 |
| 299 | PERI_MS_PPU_FX_DW1_CH_STRUCT62_CH | 0x40298F80 | 0x00000040 | P-DMA1 Channel #62 |
| 300 | PERI_MS_PPU_FX_DW1_CH_STRUCT63_CH | 0x40298FC0 | 0x00000040 | P-DMA1 Channel #63 |
| 301 | PERI_MS_PPU_FX_DW1_CH_STRUCT64_CH | 0x40299000 | 0x00000040 | P-DMA1 Channel #64 |
| 302 | PERI_MS_PPU_FX_DMACH_TOP | 0x402A0000 | 0x00000010 | M-DMA0 main |
| 303 | PERI_MS_PPU_FX_DMACH_CH0_CH | 0x402A1000 | 0x00000100 | M-DMA0 Channel #0 |
| 304 | PERI_MS_PPU_FX_DMACH_CH1_CH | 0x402A1100 | 0x00000100 | M-DMA0 Channel #1 |
| 305 | PERI_MS_PPU_FX_DMACH_CH2_CH | 0x402A1200 | 0x00000100 | M-DMA0 Channel #2 |
| 306 | PERI_MS_PPU_FX_DMACH_CH3_CH | 0x402A1300 | 0x00000100 | M-DMA0 Channel #3 |
| 307 | PERI_MS_PPU_FX_DMACH_CH4_CH | 0x402A1400 | 0x00000100 | M-DMA0 Channel #4 |
| 308 | PERI_MS_PPU_FX_DMACH_CH5_CH | 0x402A1500 | 0x00000100 | M-DMA0 Channel #5 |
| 309 | PERI_MS_PPU_FX_DMACH_CH6_CH | 0x402A1600 | 0x00000100 | M-DMA0 Channel #6 |
| 310 | PERI_MS_PPU_FX_DMACH_CH7_CH | 0x402A1700 | 0x00000100 | M-DMA0 Channel #7 |
| 311 | PERI_MS_PPU_FX_EFUSE_CTL | 0x402C0000 | 0x00000200 | EFUSE control |
| 312 | PERI_MS_PPU_FX_EFUSE_DATA | 0x402C0800 | 0x00000200 | EFUSE data |
| 313 | PERI_MS_PPU_FX_BIST | 0x402F0000 | 0x00001000 | Built-in self test |
| 314 | PERI_MS_PPU_FX_HSIOM_PRT0_PRT | 0x40300000 | 0x00000008 | HSIOm Port #0 |
| 315 | PERI_MS_PPU_FX_HSIOM_PRT1_PRT | 0x40300010 | 0x00000008 | HSIOm Port #1 |
| 316 | PERI_MS_PPU_FX_HSIOM_PRT2_PRT | 0x40300020 | 0x00000008 | HSIOm Port #2 |
| 317 | PERI_MS_PPU_FX_HSIOM_PRT3_PRT | 0x40300030 | 0x00000008 | HSIOm Port #3 |
| 318 | PERI_MS_PPU_FX_HSIOM_PRT4_PRT | 0x40300040 | 0x00000008 | HSIOm Port #4 |
| 319 | PERI_MS_PPU_FX_HSIOM_PRT5_PRT | 0x40300050 | 0x00000008 | HSIOm Port #5 |
| 320 | PERI_MS_PPU_FX_HSIOM_PRT6_PRT | 0x40300060 | 0x00000008 | HSIOm Port #6 |
| 321 | PERI_MS_PPU_FX_HSIOM_PRT7_PRT | 0x40300070 | 0x00000008 | HSIOm Port #7 |
| 322 | PERI_MS_PPU_FX_HSIOM_PRT8_PRT | 0x40300080 | 0x00000008 | HSIOm Port #8 |

Table 21-1. PPU Fixed Structure Pairs (continued)

| Pair No. | PPU Fixed Structure Pair | Address | Size | Description |
|----------|--------------------------------|------------|------------|--------------------------|
| 323 | PERI_MS_PPU_FX_HSIOM_PRT9_PRT | 0x40300090 | 0x00000008 | HSIOm Port #9 |
| 324 | PERI_MS_PPU_FX_HSIOM_PRT10_PRT | 0x403000A0 | 0x00000008 | HSIOm Port #10 |
| 325 | PERI_MS_PPU_FX_HSIOM_PRT11_PRT | 0x403000B0 | 0x00000008 | HSIOm Port #11 |
| 326 | PERI_MS_PPU_FX_HSIOM_PRT12_PRT | 0x403000C0 | 0x00000008 | HSIOm Port #12 |
| 327 | PERI_MS_PPU_FX_HSIOM_PRT13_PRT | 0x403000D0 | 0x00000008 | HSIOm Port #13 |
| 328 | PERI_MS_PPU_FX_HSIOM_PRT14_PRT | 0x403000E0 | 0x00000008 | HSIOm Port #14 |
| 329 | PERI_MS_PPU_FX_HSIOM_PRT15_PRT | 0x403000F0 | 0x00000008 | HSIOm Port #15 |
| 330 | PERI_MS_PPU_FX_HSIOM_PRT16_PRT | 0x40300100 | 0x00000008 | HSIOm Port #16 |
| 331 | PERI_MS_PPU_FX_HSIOM_PRT17_PRT | 0x40300110 | 0x00000008 | HSIOm Port #17 |
| 332 | PERI_MS_PPU_FX_HSIOM_PRT18_PRT | 0x40300120 | 0x00000008 | HSIOm Port #18 |
| 333 | PERI_MS_PPU_FX_HSIOM_PRT19_PRT | 0x40300130 | 0x00000008 | HSIOm Port #19 |
| 334 | PERI_MS_PPU_FX_HSIOM_PRT20_PRT | 0x40300140 | 0x00000008 | HSIOm Port #20 |
| 335 | PERI_MS_PPU_FX_HSIOM_PRT21_PRT | 0x40300150 | 0x00000008 | HSIOm Port #21 |
| 336 | PERI_MS_PPU_FX_HSIOM_PRT22_PRT | 0x40300160 | 0x00000008 | HSIOm Port #22 |
| 337 | PERI_MS_PPU_FX_HSIOM_PRT23_PRT | 0x40300170 | 0x00000008 | HSIOm Port #23 |
| 338 | PERI_MS_PPU_FX_HSIOM_PRT24_PRT | 0x40300180 | 0x00000008 | HSIOm Port #24 |
| 339 | PERI_MS_PPU_FX_HSIOM_PRT25_PRT | 0x40300190 | 0x00000008 | HSIOm Port #25 |
| 340 | PERI_MS_PPU_FX_HSIOM_PRT26_PRT | 0x403001A0 | 0x00000008 | HSIOm Port #26 |
| 341 | PERI_MS_PPU_FX_HSIOM_PRT27_PRT | 0x403001B0 | 0x00000008 | HSIOm Port #27 |
| 342 | PERI_MS_PPU_FX_HSIOM_PRT28_PRT | 0x403001C0 | 0x00000008 | HSIOm Port #28 |
| 343 | PERI_MS_PPU_FX_HSIOM_PRT29_PRT | 0x403001D0 | 0x00000008 | HSIOm Port #29 |
| 344 | PERI_MS_PPU_FX_HSIOM_PRT30_PRT | 0x403001E0 | 0x00000008 | HSIOm Port #30 |
| 345 | PERI_MS_PPU_FX_HSIOM_PRT31_PRT | 0x403001F0 | 0x00000008 | HSIOm Port #31 |
| 346 | PERI_MS_PPU_FX_HSIOM_PRT32_PRT | 0x40300200 | 0x00000008 | HSIOm Port #32 |
| 347 | PERI_MS_PPU_FX_HSIOM_PRT33_PRT | 0x40300210 | 0x00000008 | HSIOm Port #33 |
| 348 | PERI_MS_PPU_FX_HSIOM_PRT34_PRT | 0x40300220 | 0x00000008 | HSIOm Port #34 |
| 349 | PERI_MS_PPU_FX_HSIOM_AMUX | 0x40302000 | 0x00000010 | HSIOm Analog multiplexer |
| 350 | PERI_MS_PPU_FX_HSIOM_MON | 0x40302200 | 0x00000010 | HSIOm monitor |
| 351 | PERI_MS_PPU_FX_HSIOM_ALTJTAG | 0x40302240 | 0x00000004 | HSIOm Alternate JTAG |
| 352 | PERI_MS_PPU_FX_GPIO_PRT0_PRT | 0x40310000 | 0x00000040 | GPIO_ENH Port #0 |
| 353 | PERI_MS_PPU_FX_GPIO_PRT1_PRT | 0x40310080 | 0x00000040 | GPIO_STD Port #1 |
| 354 | PERI_MS_PPU_FX_GPIO_PRT2_PRT | 0x40310100 | 0x00000040 | GPIO_STD Port #2 |
| 355 | PERI_MS_PPU_FX_GPIO_PRT3_PRT | 0x40310180 | 0x00000040 | GPIO_STD Port #3 |
| 356 | PERI_MS_PPU_FX_GPIO_PRT4_PRT | 0x40310200 | 0x00000040 | GPIO_STD Port #4 |
| 357 | PERI_MS_PPU_FX_GPIO_PRT5_PRT | 0x40310280 | 0x00000040 | GPIO_STD Port #5 |
| 358 | PERI_MS_PPU_FX_GPIO_PRT6_PRT | 0x40310300 | 0x00000040 | GPIO_STD Port #6 |
| 359 | PERI_MS_PPU_FX_GPIO_PRT7_PRT | 0x40310380 | 0x00000040 | GPIO_STD Port #7 |
| 360 | PERI_MS_PPU_FX_GPIO_PRT8_PRT | 0x40310400 | 0x00000040 | GPIO_STD Port #8 |
| 361 | PERI_MS_PPU_FX_GPIO_PRT9_PRT | 0x40310480 | 0x00000040 | GPIO_STD Port #9 |
| 362 | PERI_MS_PPU_FX_GPIO_PRT10_PRT | 0x40310500 | 0x00000040 | GPIO_STD Port #10 |
| 363 | PERI_MS_PPU_FX_GPIO_PRT11_PRT | 0x40310580 | 0x00000040 | GPIO_STD Port #11 |

Table 21-1. PPU Fixed Structure Pairs (continued)

| Pair No. | PPU Fixed Structure Pair | Address | Size | Description |
|----------|-------------------------------|------------|------------|---------------------------------|
| 364 | PERI_MS_PPU_FX_GPIO_PRT12_PRT | 0x40310600 | 0x00000040 | GPIO_STD Port #12 |
| 365 | PERI_MS_PPU_FX_GPIO_PRT13_PRT | 0x40310680 | 0x00000040 | GPIO_STD Port #13 |
| 366 | PERI_MS_PPU_FX_GPIO_PRT14_PRT | 0x40310700 | 0x00000040 | GPIO_STD Port #14 |
| 367 | PERI_MS_PPU_FX_GPIO_PRT15_PRT | 0x40310780 | 0x00000040 | GPIO_STD Port #15 |
| 368 | PERI_MS_PPU_FX_GPIO_PRT16_PRT | 0x40310800 | 0x00000040 | GPIO_STD Port #16 |
| 369 | PERI_MS_PPU_FX_GPIO_PRT17_PRT | 0x40310880 | 0x00000040 | GPIO_STD Port #17 |
| 370 | PERI_MS_PPU_FX_GPIO_PRT18_PRT | 0x40310900 | 0x00000040 | GPIO_STD Port #18 |
| 371 | PERI_MS_PPU_FX_GPIO_PRT19_PRT | 0x40310980 | 0x00000040 | GPIO_STD Port #19 |
| 372 | PERI_MS_PPU_FX_GPIO_PRT20_PRT | 0x40310A00 | 0x00000040 | GPIO_STD Port #20 |
| 373 | PERI_MS_PPU_FX_GPIO_PRT21_PRT | 0x40310A80 | 0x00000040 | GPIO_STD Port #21 |
| 374 | PERI_MS_PPU_FX_GPIO_PRT22_PRT | 0x40310B00 | 0x00000040 | GPIO_STD Port #22 |
| 375 | PERI_MS_PPU_FX_GPIO_PRT23_PRT | 0x40310B80 | 0x00000040 | GPIO_STD Port #23 |
| 376 | PERI_MS_PPU_FX_GPIO_PRT24_PRT | 0x40310C00 | 0x00000040 | HSIO_STD Port #24 |
| 377 | PERI_MS_PPU_FX_GPIO_PRT25_PRT | 0x40310C80 | 0x00000040 | HSIO_STD Port #25 |
| 378 | PERI_MS_PPU_FX_GPIO_PRT26_PRT | 0x40310D00 | 0x00000040 | HSIO_STD Port #26 |
| 379 | PERI_MS_PPU_FX_GPIO_PRT27_PRT | 0x40310D80 | 0x00000040 | HSIO_STD Port #27 |
| 380 | PERI_MS_PPU_FX_GPIO_PRT28_PRT | 0x40310E00 | 0x00000040 | GPIO_STD Port #28 |
| 381 | PERI_MS_PPU_FX_GPIO_PRT29_PRT | 0x40310E80 | 0x00000040 | GPIO_STD Port #29 |
| 382 | PERI_MS_PPU_FX_GPIO_PRT30_PRT | 0x40310F00 | 0x00000040 | GPIO_STD Port #30 |
| 383 | PERI_MS_PPU_FX_GPIO_PRT31_PRT | 0x40310F80 | 0x00000040 | GPIO_STD Port #31 |
| 384 | PERI_MS_PPU_FX_GPIO_PRT32_PRT | 0x40311000 | 0x00000040 | GPIO_STD Port #32 |
| 385 | PERI_MS_PPU_FX_GPIO_PRT33_PRT | 0x40311080 | 0x00000040 | HSIO_STD Port #33 |
| 386 | PERI_MS_PPU_FX_GPIO_PRT34_PRT | 0x40311100 | 0x00000040 | HSIO_STD Port #34 |
| 387 | PERI_MS_PPU_FX_GPIO_PRT0_CFG | 0x40310040 | 0x00000020 | GPIO_ENH Port #0 configuration |
| 388 | PERI_MS_PPU_FX_GPIO_PRT1_CFG | 0x403100C0 | 0x00000020 | GPIO_STD Port #1 configuration |
| 389 | PERI_MS_PPU_FX_GPIO_PRT2_CFG | 0x40310140 | 0x00000020 | GPIO_STD Port #2 configuration |
| 390 | PERI_MS_PPU_FX_GPIO_PRT3_CFG | 0x403101C0 | 0x00000020 | GPIO_STD Port #3 configuration |
| 391 | PERI_MS_PPU_FX_GPIO_PRT4_CFG | 0x40310240 | 0x00000020 | GPIO_STD Port #4 configuration |
| 392 | PERI_MS_PPU_FX_GPIO_PRT5_CFG | 0x403102C0 | 0x00000020 | GPIO_STD Port #5 configuration |
| 393 | PERI_MS_PPU_FX_GPIO_PRT6_CFG | 0x40310340 | 0x00000020 | GPIO_STD Port #6 configuration |
| 394 | PERI_MS_PPU_FX_GPIO_PRT7_CFG | 0x403103C0 | 0x00000020 | GPIO_STD Port #7 configuration |
| 395 | PERI_MS_PPU_FX_GPIO_PRT8_CFG | 0x40310440 | 0x00000020 | GPIO_STD Port #8 configuration |
| 396 | PERI_MS_PPU_FX_GPIO_PRT9_CFG | 0x403104C0 | 0x00000020 | GPIO_STD Port #9 configuration |
| 397 | PERI_MS_PPU_FX_GPIO_PRT10_CFG | 0x40310540 | 0x00000020 | GPIO_STD Port #10 configuration |
| 398 | PERI_MS_PPU_FX_GPIO_PRT11_CFG | 0x403105C0 | 0x00000020 | GPIO_STD Port #11 configuration |
| 399 | PERI_MS_PPU_FX_GPIO_PRT12_CFG | 0x40310640 | 0x00000020 | GPIO_STD Port #12 configuration |
| 400 | PERI_MS_PPU_FX_GPIO_PRT13_CFG | 0x403106C0 | 0x00000020 | GPIO_STD Port #13 configuration |
| 401 | PERI_MS_PPU_FX_GPIO_PRT14_CFG | 0x40310740 | 0x00000020 | GPIO_STD Port #14 configuration |
| 402 | PERI_MS_PPU_FX_GPIO_PRT15_CFG | 0x403107C0 | 0x00000020 | GPIO_STD Port #15 configuration |
| 403 | PERI_MS_PPU_FX_GPIO_PRT16_CFG | 0x40310840 | 0x00000020 | GPIO_STD Port #16 configuration |
| 404 | PERI_MS_PPU_FX_GPIO_PRT17_CFG | 0x403108C0 | 0x00000020 | GPIO_STD Port #17 configuration |

Table 21-1. PPU Fixed Structure Pairs (continued)

| Pair No. | PPU Fixed Structure Pair | Address | Size | Description |
|----------|-------------------------------------|------------|------------|---------------------------------|
| 405 | PERI_MS_PPU_FX_GPIO_PRT18_CFG | 0x40310940 | 0x00000020 | GPIO_STD Port #18 configuration |
| 406 | PERI_MS_PPU_FX_GPIO_PRT19_CFG | 0x403109C0 | 0x00000020 | GPIO_STD Port #19 configuration |
| 407 | PERI_MS_PPU_FX_GPIO_PRT20_CFG | 0x40310A40 | 0x00000020 | GPIO_STD Port #20 configuration |
| 408 | PERI_MS_PPU_FX_GPIO_PRT21_CFG | 0x40310AC0 | 0x00000020 | GPIO_STD Port #21 configuration |
| 409 | PERI_MS_PPU_FX_GPIO_PRT22_CFG | 0x40310B40 | 0x00000020 | GPIO_STD Port #22 configuration |
| 410 | PERI_MS_PPU_FX_GPIO_PRT23_CFG | 0x40310BC0 | 0x00000020 | GPIO_STD Port #23 configuration |
| 411 | PERI_MS_PPU_FX_GPIO_PRT24_CFG | 0x40310C40 | 0x00000020 | HSIO_STD Port #24 configuration |
| 412 | PERI_MS_PPU_FX_GPIO_PRT25_CFG | 0x40310CC0 | 0x00000020 | HSIO_STD Port #25 configuration |
| 413 | PERI_MS_PPU_FX_GPIO_PRT26_CFG | 0x40310D40 | 0x00000020 | HSIO_STD Port #26 configuration |
| 414 | PERI_MS_PPU_FX_GPIO_PRT27_CFG | 0x40310DC0 | 0x00000020 | HSIO_STD Port #27 configuration |
| 415 | PERI_MS_PPU_FX_GPIO_PRT28_CFG | 0x40310E40 | 0x00000020 | GPIO_STD Port #28 configuration |
| 416 | PERI_MS_PPU_FX_GPIO_PRT29_CFG | 0x40310EC0 | 0x00000020 | GPIO_STD Port #29 configuration |
| 417 | PERI_MS_PPU_FX_GPIO_PRT30_CFG | 0x40310F40 | 0x00000020 | GPIO_STD Port #30 configuration |
| 418 | PERI_MS_PPU_FX_GPIO_PRT31_CFG | 0x40310FC0 | 0x00000020 | GPIO_STD Port #31 configuration |
| 419 | PERI_MS_PPU_FX_GPIO_PRT32_CFG | 0x40311040 | 0x00000020 | GPIO_STD Port #32 configuration |
| 420 | PERI_MS_PPU_FX_GPIO_PRT33_CFG | 0x403110C0 | 0x00000020 | HSIO_STD Port #33 configuration |
| 421 | PERI_MS_PPU_FX_GPIO_PRT34_CFG | 0x40311140 | 0x00000020 | HSIO_STD Port #34 configuration |
| 422 | PERI_MS_PPU_FX_GPIO_GPIO | 0x40314000 | 0x00000040 | GPIO main |
| 423 | PERI_MS_PPU_FX_GPIO_TEST | 0x40315000 | 0x00000008 | GPIO test |
| 424 | PERI_MS_PPU_FX_SMARTIO_PRT12_PRT | 0x40320C00 | 0x00000100 | SMART I/O #12 |
| 425 | PERI_MS_PPU_FX_SMARTIO_PRT13_PRT | 0x40320D00 | 0x00000100 | SMART I/O #13 |
| 426 | PERI_MS_PPU_FX_SMARTIO_PRT14_PRT | 0x40320E00 | 0x00000100 | SMART I/O #14 |
| 427 | PERI_MS_PPU_FX_SMARTIO_PRT15_PRT | 0x40320F00 | 0x00000100 | SMART I/O #15 |
| 428 | PERI_MS_PPU_FX_SMARTIO_PRT17_PRT | 0x40321100 | 0x00000100 | SMART I/O #17 |
| 429 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT0_CNT | 0x40380000 | 0x00000080 | TCPWM0 Group #0, Counter #0 |
| 430 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT1_CNT | 0x40380080 | 0x00000080 | TCPWM0 Group #0, Counter #1 |
| 431 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT2_CNT | 0x40380100 | 0x00000080 | TCPWM0 Group #0, Counter #2 |
| 432 | PERI_MS_PPU_FX_TCPWM0_GRP1_CNT0_CNT | 0x40388000 | 0x00000080 | TCPWM0 Group #1, Counter #0 |
| 433 | PERI_MS_PPU_FX_TCPWM0_GRP1_CNT1_CNT | 0x40388080 | 0x00000080 | TCPWM0 Group #1, Counter #1 |
| 434 | PERI_MS_PPU_FX_TCPWM0_GRP1_CNT2_CNT | 0x40388100 | 0x00000080 | TCPWM0 Group #1, Counter #2 |
| 435 | PERI_MS_PPU_FX_TCPWM0_GRP2_CNT0_CNT | 0x40390000 | 0x00000080 | TCPWM0 Group #2, Counter #0 |
| 436 | PERI_MS_PPU_FX_TCPWM0_GRP2_CNT1_CNT | 0x40390080 | 0x00000080 | TCPWM0 Group #2, Counter #1 |
| 437 | PERI_MS_PPU_FX_TCPWM0_GRP2_CNT2_CNT | 0x40390100 | 0x00000080 | TCPWM0 Group #2, Counter #2 |
| 438 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT0_CNT | 0x40580000 | 0x00000080 | TCPWM1 Group #0, Counter #0 |
| 439 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT1_CNT | 0x40580080 | 0x00000080 | TCPWM1 Group #0, Counter #1 |
| 440 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT2_CNT | 0x40580100 | 0x00000080 | TCPWM1 Group #0, Counter #2 |
| 441 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT3_CNT | 0x40580180 | 0x00000080 | TCPWM1 Group #0, Counter #3 |
| 442 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT4_CNT | 0x40580200 | 0x00000080 | TCPWM1 Group #0, Counter #4 |
| 443 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT5_CNT | 0x40580280 | 0x00000080 | TCPWM1 Group #0, Counter #5 |
| 444 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT6_CNT | 0x40580300 | 0x00000080 | TCPWM1 Group #0, Counter #6 |
| 445 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT7_CNT | 0x40580380 | 0x00000080 | TCPWM1 Group #0, Counter #7 |

Table 21-1. PPU Fixed Structure Pairs (continued)

| Pair No. | PPU Fixed Structure Pair | Address | Size | Description |
|----------|--------------------------------------|------------|------------|------------------------------|
| 446 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT8_CNT | 0x40580400 | 0x00000080 | TCPWM1 Group #0, Counter #8 |
| 447 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT9_CNT | 0x40580480 | 0x00000080 | TCPWM1 Group #0, Counter #9 |
| 448 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT10_CNT | 0x40580500 | 0x00000080 | TCPWM1 Group #0, Counter #10 |
| 449 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT11_CNT | 0x40580580 | 0x00000080 | TCPWM1 Group #0, Counter #11 |
| 450 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT12_CNT | 0x40580600 | 0x00000080 | TCPWM1 Group #0, Counter #12 |
| 451 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT13_CNT | 0x40580680 | 0x00000080 | TCPWM1 Group #0, Counter #13 |
| 452 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT14_CNT | 0x40580700 | 0x00000080 | TCPWM1 Group #0, Counter #14 |
| 453 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT15_CNT | 0x40580780 | 0x00000080 | TCPWM1 Group #0, Counter #15 |
| 454 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT16_CNT | 0x40580800 | 0x00000080 | TCPWM1 Group #0, Counter #16 |
| 455 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT17_CNT | 0x40580880 | 0x00000080 | TCPWM1 Group #0, Counter #17 |
| 456 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT18_CNT | 0x40580900 | 0x00000080 | TCPWM1 Group #0, Counter #18 |
| 457 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT19_CNT | 0x40580980 | 0x00000080 | TCPWM1 Group #0, Counter #19 |
| 458 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT20_CNT | 0x40580A00 | 0x00000080 | TCPWM1 Group #0, Counter #20 |
| 459 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT21_CNT | 0x40580A80 | 0x00000080 | TCPWM1 Group #0, Counter #21 |
| 460 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT22_CNT | 0x40580B00 | 0x00000080 | TCPWM1 Group #0, Counter #22 |
| 461 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT23_CNT | 0x40580B80 | 0x00000080 | TCPWM1 Group #0, Counter #23 |
| 462 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT24_CNT | 0x40580C00 | 0x00000080 | TCPWM1 Group #0, Counter #24 |
| 463 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT25_CNT | 0x40580C80 | 0x00000080 | TCPWM1 Group #0, Counter #25 |
| 464 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT26_CNT | 0x40580D00 | 0x00000080 | TCPWM1 Group #0, Counter #26 |
| 465 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT27_CNT | 0x40580D80 | 0x00000080 | TCPWM1 Group #0, Counter #27 |
| 466 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT28_CNT | 0x40580E00 | 0x00000080 | TCPWM1 Group #0, Counter #28 |
| 467 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT29_CNT | 0x40580E80 | 0x00000080 | TCPWM1 Group #0, Counter #29 |
| 468 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT30_CNT | 0x40580F00 | 0x00000080 | TCPWM1 Group #0, Counter #30 |
| 469 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT31_CNT | 0x40580F80 | 0x00000080 | TCPWM1 Group #0, Counter #31 |
| 470 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT32_CNT | 0x40581000 | 0x00000080 | TCPWM1 Group #0, Counter #32 |
| 471 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT33_CNT | 0x40581080 | 0x00000080 | TCPWM1 Group #0, Counter #33 |
| 472 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT34_CNT | 0x40581100 | 0x00000080 | TCPWM1 Group #0, Counter #34 |
| 473 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT35_CNT | 0x40581180 | 0x00000080 | TCPWM1 Group #0, Counter #35 |
| 474 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT36_CNT | 0x40581200 | 0x00000080 | TCPWM1 Group #0, Counter #36 |
| 475 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT37_CNT | 0x40581280 | 0x00000080 | TCPWM1 Group #0, Counter #37 |
| 476 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT38_CNT | 0x40581300 | 0x00000080 | TCPWM1 Group #0, Counter #38 |
| 477 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT39_CNT | 0x40581380 | 0x00000080 | TCPWM1 Group #0, Counter #39 |
| 478 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT40_CNT | 0x40581400 | 0x00000080 | TCPWM1 Group #0, Counter #40 |
| 479 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT41_CNT | 0x40581480 | 0x00000080 | TCPWM1 Group #0, Counter #41 |
| 480 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT42_CNT | 0x40581500 | 0x00000080 | TCPWM1 Group #0, Counter #42 |
| 481 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT43_CNT | 0x40581580 | 0x00000080 | TCPWM1 Group #0, Counter #43 |
| 482 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT44_CNT | 0x40581600 | 0x00000080 | TCPWM1 Group #0, Counter #44 |
| 483 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT45_CNT | 0x40581680 | 0x00000080 | TCPWM1 Group #0, Counter #45 |
| 484 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT46_CNT | 0x40581700 | 0x00000080 | TCPWM1 Group #0, Counter #46 |
| 485 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT47_CNT | 0x40581780 | 0x00000080 | TCPWM1 Group #0, Counter #47 |
| 486 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT48_CNT | 0x40581800 | 0x00000080 | TCPWM1 Group #0, Counter #48 |

Table 21-1. PPU Fixed Structure Pairs (continued)

| Pair No. | PPU Fixed Structure Pair | Address | Size | Description |
|----------|--------------------------------------|------------|------------|------------------------------|
| 487 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT49_CNT | 0x40581880 | 0x00000080 | TCPWM1 Group #0, Counter #49 |
| 488 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT50_CNT | 0x40581900 | 0x00000080 | TCPWM1 Group #0, Counter #50 |
| 489 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT51_CNT | 0x40581980 | 0x00000080 | TCPWM1 Group #0, Counter #51 |
| 490 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT52_CNT | 0x40581A00 | 0x00000080 | TCPWM1 Group #0, Counter #52 |
| 491 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT53_CNT | 0x40581A80 | 0x00000080 | TCPWM1 Group #0, Counter #53 |
| 492 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT54_CNT | 0x40581B00 | 0x00000080 | TCPWM1 Group #0, Counter #54 |
| 493 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT55_CNT | 0x40581B80 | 0x00000080 | TCPWM1 Group #0, Counter #55 |
| 494 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT56_CNT | 0x40581C00 | 0x00000080 | TCPWM1 Group #0, Counter #56 |
| 495 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT57_CNT | 0x40581C80 | 0x00000080 | TCPWM1 Group #0, Counter #57 |
| 496 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT58_CNT | 0x40581D00 | 0x00000080 | TCPWM1 Group #0, Counter #58 |
| 497 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT59_CNT | 0x40581D80 | 0x00000080 | TCPWM1 Group #0, Counter #59 |
| 498 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT60_CNT | 0x40581E00 | 0x00000080 | TCPWM1 Group #0, Counter #60 |
| 499 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT61_CNT | 0x40581E80 | 0x00000080 | TCPWM1 Group #0, Counter #61 |
| 500 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT62_CNT | 0x40581F00 | 0x00000080 | TCPWM1 Group #0, Counter #62 |
| 501 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT63_CNT | 0x40581F80 | 0x00000080 | TCPWM1 Group #0, Counter #63 |
| 502 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT64_CNT | 0x40582000 | 0x00000080 | TCPWM1 Group #0, Counter #64 |
| 503 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT65_CNT | 0x40582080 | 0x00000080 | TCPWM1 Group #0, Counter #65 |
| 504 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT66_CNT | 0x40582100 | 0x00000080 | TCPWM1 Group #0, Counter #66 |
| 505 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT67_CNT | 0x40582180 | 0x00000080 | TCPWM1 Group #0, Counter #67 |
| 506 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT68_CNT | 0x40582200 | 0x00000080 | TCPWM1 Group #0, Counter #68 |
| 507 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT69_CNT | 0x40582280 | 0x00000080 | TCPWM1 Group #0, Counter #69 |
| 508 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT70_CNT | 0x40582300 | 0x00000080 | TCPWM1 Group #0, Counter #70 |
| 509 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT71_CNT | 0x40582380 | 0x00000080 | TCPWM1 Group #0, Counter #71 |
| 510 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT72_CNT | 0x40582400 | 0x00000080 | TCPWM1 Group #0, Counter #72 |
| 511 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT73_CNT | 0x40582480 | 0x00000080 | TCPWM1 Group #0, Counter #73 |
| 512 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT74_CNT | 0x40582500 | 0x00000080 | TCPWM1 Group #0, Counter #74 |
| 513 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT75_CNT | 0x40582580 | 0x00000080 | TCPWM1 Group #0, Counter #75 |
| 514 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT76_CNT | 0x40582600 | 0x00000080 | TCPWM1 Group #0, Counter #76 |
| 515 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT77_CNT | 0x40582680 | 0x00000080 | TCPWM1 Group #0, Counter #77 |
| 516 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT78_CNT | 0x40582700 | 0x00000080 | TCPWM1 Group #0, Counter #78 |
| 517 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT79_CNT | 0x40582780 | 0x00000080 | TCPWM1 Group #0, Counter #79 |
| 518 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT80_CNT | 0x40582800 | 0x00000080 | TCPWM1 Group #0, Counter #80 |
| 519 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT81_CNT | 0x40582880 | 0x00000080 | TCPWM1 Group #0, Counter #81 |
| 520 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT82_CNT | 0x40582900 | 0x00000080 | TCPWM1 Group #0, Counter #82 |
| 521 | PERI_MS_PPU_FX_TCPWM1_GRP0_CNT83_CNT | 0x40582980 | 0x00000080 | TCPWM1 Group #0, Counter #83 |
| 522 | PERI_MS_PPU_FX_TCPWM1_GRP1_CNT0_CNT | 0x40588000 | 0x00000080 | TCPWM1 Group #1, Counter #0 |
| 523 | PERI_MS_PPU_FX_TCPWM1_GRP1_CNT1_CNT | 0x40588080 | 0x00000080 | TCPWM1 Group #1, Counter #1 |
| 524 | PERI_MS_PPU_FX_TCPWM1_GRP1_CNT2_CNT | 0x40588100 | 0x00000080 | TCPWM1 Group #1, Counter #2 |
| 525 | PERI_MS_PPU_FX_TCPWM1_GRP1_CNT3_CNT | 0x40588180 | 0x00000080 | TCPWM1 Group #1, Counter #3 |
| 526 | PERI_MS_PPU_FX_TCPWM1_GRP1_CNT4_CNT | 0x40588200 | 0x00000080 | TCPWM1 Group #1, Counter #4 |
| 527 | PERI_MS_PPU_FX_TCPWM1_GRP1_CNT5_CNT | 0x40588280 | 0x00000080 | TCPWM1 Group #1, Counter #5 |

Table 21-1. PPU Fixed Structure Pairs (continued)

| Pair No. | PPU Fixed Structure Pair | Address | Size | Description |
|----------|--------------------------------------|------------|------------|---------------------------------|
| 528 | PERI_MS_PPU_FX_TCPWM1_GRP1_CNT6_CNT | 0x40588300 | 0x00000080 | TCPWM1 Group #1, Counter #6 |
| 529 | PERI_MS_PPU_FX_TCPWM1_GRP1_CNT7_CNT | 0x40588380 | 0x00000080 | TCPWM1 Group #1, Counter #7 |
| 530 | PERI_MS_PPU_FX_TCPWM1_GRP1_CNT8_CNT | 0x40588400 | 0x00000080 | TCPWM1 Group #1, Counter #8 |
| 531 | PERI_MS_PPU_FX_TCPWM1_GRP1_CNT9_CNT | 0x40588480 | 0x00000080 | TCPWM1 Group #1, Counter #9 |
| 532 | PERI_MS_PPU_FX_TCPWM1_GRP1_CNT10_CNT | 0x40588500 | 0x00000080 | TCPWM1 Group #1, Counter #10 |
| 533 | PERI_MS_PPU_FX_TCPWM1_GRP1_CNT11_CNT | 0x40588580 | 0x00000080 | TCPWM1 Group #1, Counter #11 |
| 534 | PERI_MS_PPU_FX_TCPWM1_GRP2_CNT0_CNT | 0x40590000 | 0x00000080 | TCPWM1 Group #2, Counter #0 |
| 535 | PERI_MS_PPU_FX_TCPWM1_GRP2_CNT1_CNT | 0x40590080 | 0x00000080 | TCPWM1 Group #2, Counter #1 |
| 536 | PERI_MS_PPU_FX_TCPWM1_GRP2_CNT2_CNT | 0x40590100 | 0x00000080 | TCPWM1 Group #2, Counter #2 |
| 537 | PERI_MS_PPU_FX_TCPWM1_GRP2_CNT3_CNT | 0x40590180 | 0x00000080 | TCPWM1 Group #2, Counter #3 |
| 538 | PERI_MS_PPU_FX_TCPWM1_GRP2_CNT4_CNT | 0x40590200 | 0x00000080 | TCPWM1 Group #2, Counter #4 |
| 539 | PERI_MS_PPU_FX_TCPWM1_GRP2_CNT5_CNT | 0x40590280 | 0x00000080 | TCPWM1 Group #2, Counter #5 |
| 540 | PERI_MS_PPU_FX_TCPWM1_GRP2_CNT6_CNT | 0x40590300 | 0x00000080 | TCPWM1 Group #2, Counter #6 |
| 541 | PERI_MS_PPU_FX_TCPWM1_GRP2_CNT7_CNT | 0x40590380 | 0x00000080 | TCPWM1 Group #2, Counter #7 |
| 542 | PERI_MS_PPU_FX_TCPWM1_GRP2_CNT8_CNT | 0x40590400 | 0x00000080 | TCPWM1 Group #2, Counter #8 |
| 543 | PERI_MS_PPU_FX_TCPWM1_GRP2_CNT9_CNT | 0x40590480 | 0x00000080 | TCPWM1 Group #2, Counter #9 |
| 544 | PERI_MS_PPU_FX_TCPWM1_GRP2_CNT10_CNT | 0x40590500 | 0x00000080 | TCPWM1 Group #2, Counter #10 |
| 545 | PERI_MS_PPU_FX_TCPWM1_GRP2_CNT11_CNT | 0x40590580 | 0x00000080 | TCPWM1 Group #2, Counter #11 |
| 546 | PERI_MS_PPU_FX_TCPWM1_GRP2_CNT12_CNT | 0x40590600 | 0x00000080 | TCPWM1 Group #2, Counter #12 |
| 547 | PERI_MS_PPU_FX_EVTGEN0 | 0x403F0000 | 0x00001000 | Event generator #0 |
| 548 | PERI_MS_PPU_FX_SMIF0 | 0x40420000 | 0x00010000 | Serial Memory Interface #0 |
| 549 | PERI_MS_PPU_FX_SDHC0 | 0x40460000 | 0x00010000 | Secure Digital High Capacity #0 |
| 550 | PERI_MS_PPU_FX_ETH0 | 0x40480000 | 0x00010000 | Ethernet0 |
| 551 | PERI_MS_PPU_FX_ETH1 | 0x40490000 | 0x00010000 | Ethernet1 |
| 552 | PERI_MS_PPU_FX_LIN0_MAIN | 0x40500000 | 0x00000008 | LIN0, main |
| 553 | PERI_MS_PPU_FX_LIN0_CH0_CH | 0x40508000 | 0x00000100 | LIN0, Channel #0 |
| 554 | PERI_MS_PPU_FX_LIN0_CH1_CH | 0x40508100 | 0x00000100 | LIN0, Channel #1 |
| 555 | PERI_MS_PPU_FX_LIN0_CH2_CH | 0x40508200 | 0x00000100 | LIN0, Channel #2 |
| 556 | PERI_MS_PPU_FX_LIN0_CH3_CH | 0x40508300 | 0x00000100 | LIN0, Channel #3 |
| 557 | PERI_MS_PPU_FX_LIN0_CH4_CH | 0x40508400 | 0x00000100 | LIN0, Channel #4 |
| 558 | PERI_MS_PPU_FX_LIN0_CH5_CH | 0x40508500 | 0x00000100 | LIN0, Channel #5 |
| 559 | PERI_MS_PPU_FX_LIN0_CH6_CH | 0x40508600 | 0x00000100 | LIN0, Channel #6 |
| 560 | PERI_MS_PPU_FX_LIN0_CH7_CH | 0x40508700 | 0x00000100 | LIN0, Channel #7 |
| 561 | PERI_MS_PPU_FX_LIN0_CH8_CH | 0x40508800 | 0x00000100 | LIN0, Channel #8 |
| 562 | PERI_MS_PPU_FX_LIN0_CH9_CH | 0x40508900 | 0x00000100 | LIN0, Channel #9 |
| 563 | PERI_MS_PPU_FX_LIN0_CH10_CH | 0x40508A00 | 0x00000100 | LIN0, Channel #10 |
| 564 | PERI_MS_PPU_FX_LIN0_CH11_CH | 0x40508B00 | 0x00000100 | LIN0, Channel #11 |
| 565 | PERI_MS_PPU_FX_LIN0_CH12_CH | 0x40508C00 | 0x00000100 | LIN0, Channel #12 |
| 566 | PERI_MS_PPU_FX_LIN0_CH13_CH | 0x40508D00 | 0x00000100 | LIN0, Channel #13 |
| 567 | PERI_MS_PPU_FX_LIN0_CH14_CH | 0x40508E00 | 0x00000100 | LIN0, Channel #14 |
| 568 | PERI_MS_PPU_FX_LIN0_CH15_CH | 0x40508F00 | 0x00000100 | LIN0, Channel #15 |

Table 21-1. PPU Fixed Structure Pairs (continued)

| Pair No. | PPU Fixed Structure Pair | Address | Size | Description |
|----------|----------------------------------|------------|------------|----------------------|
| 569 | PERI_MS_PPU_FX_LIN0_CH16_CH | 0x40509000 | 0x00000100 | LIN0, Channel #16 |
| 570 | PERI_MS_PPU_FX_LIN0_CH17_CH | 0x40509100 | 0x00000100 | LIN0, Channel #17 |
| 571 | PERI_MS_PPU_FX_LIN0_CH18_CH | 0x40509200 | 0x00000100 | LIN0, Channel #18 |
| 572 | PERI_MS_PPU_FX_LIN0_CH19_CH | 0x40509300 | 0x00000100 | LIN0, Channel #19 |
| 573 | PERI_MS_PPU_FX_CANFD0_CH0_CH | 0x40520000 | 0x00000200 | CAN0, Channel #0 |
| 574 | PERI_MS_PPU_FX_CANFD0_CH1_CH | 0x40520200 | 0x00000200 | CAN0, Channel #1 |
| 575 | PERI_MS_PPU_FX_CANFD0_CH2_CH | 0x40520400 | 0x00000200 | CAN0, Channel #2 |
| 576 | PERI_MS_PPU_FX_CANFD0_CH3_CH | 0x40520600 | 0x00000200 | CAN0, Channel #3 |
| 577 | PERI_MS_PPU_FX_CANFD0_CH4_CH | 0x40520800 | 0x00000200 | CAN0, Channel #4 |
| 578 | PERI_MS_PPU_FX_CANFD1_CH0_CH | 0x40540000 | 0x00000200 | CAN1, Channel #0 |
| 579 | PERI_MS_PPU_FX_CANFD1_CH1_CH | 0x40540200 | 0x00000200 | CAN1, Channel #1 |
| 580 | PERI_MS_PPU_FX_CANFD1_CH2_CH | 0x40540400 | 0x00000200 | CAN1, Channel #2 |
| 581 | PERI_MS_PPU_FX_CANFD1_CH3_CH | 0x40540600 | 0x00000200 | CAN1, Channel #3 |
| 582 | PERI_MS_PPU_FX_CANFD1_CH4_CH | 0x40540800 | 0x00000200 | CAN1, Channel #4 |
| 583 | PERI_MS_PPU_FX_CANFD0_MAIN | 0x40521000 | 0x00000100 | CAN0 main |
| 584 | PERI_MS_PPU_FX_CANFD1_MAIN | 0x40541000 | 0x00000100 | CAN1 main |
| 585 | PERI_MS_PPU_FX_CANFD0_BUF | 0x40530000 | 0x00010000 | CAN0 buffer |
| 586 | PERI_MS_PPU_FX_CANFD1_BUF | 0x40550000 | 0x00010000 | CAN1 buffer |
| 587 | PERI_MS_PPU_FX_FLEXRAY0 | 0x40560000 | 0x00001000 | FlexRay Interface #0 |
| 588 | PERI_MS_PPU_FX_SCB0 | 0x40600000 | 0x00010000 | SCB0 |
| 589 | PERI_MS_PPU_FX_SCB1 | 0x40610000 | 0x00010000 | SCB1 |
| 590 | PERI_MS_PPU_FX_SCB2 | 0x40620000 | 0x00010000 | SCB2 |
| 591 | PERI_MS_PPU_FX_SCB3 | 0x40630000 | 0x00010000 | SCB3 |
| 592 | PERI_MS_PPU_FX_SCB4 | 0x40640000 | 0x00010000 | SCB4 |
| 593 | PERI_MS_PPU_FX_SCB5 | 0x40650000 | 0x00010000 | SCB5 |
| 594 | PERI_MS_PPU_FX_SCB6 | 0x40660000 | 0x00010000 | SCB6 |
| 595 | PERI_MS_PPU_FX_SCB7 | 0x40670000 | 0x00010000 | SCB7 |
| 596 | PERI_MS_PPU_FX_SCB8 | 0x40680000 | 0x00010000 | SCB8 |
| 597 | PERI_MS_PPU_FX_SCB9 | 0x40690000 | 0x00010000 | SCB9 |
| 598 | PERI_MS_PPU_FX_SCB10 | 0x406A0000 | 0x00010000 | SCB10 |
| 599 | PERI_MS_PPU_FX_I2S0 | 0x40800000 | 0x00001000 | AUDIOSS I2S0 |
| 600 | PERI_MS_PPU_FX_I2S1 | 0x40801000 | 0x00001000 | AUDIOSS I2S1 |
| 601 | PERI_MS_PPU_FX_I2S2 | 0x40802000 | 0x00001000 | AUDIOSS I2S2 |
| 602 | PERI_MS_PPU_FX_PASS0_SAR0_SAR | 0x40900000 | 0x00000400 | PASS SAR0 |
| 603 | PERI_MS_PPU_FX_PASS0_SAR1_SAR | 0x40901000 | 0x00000400 | PASS SAR1 |
| 604 | PERI_MS_PPU_FX_PASS0_SAR2_SAR | 0x40902000 | 0x00000400 | PASS SAR2 |
| 605 | PERI_MS_PPU_FX_PASS0_SAR0_CH0_CH | 0x40900800 | 0x00000040 | SAR0, Channel #0 |
| 606 | PERI_MS_PPU_FX_PASS0_SAR0_CH1_CH | 0x40900840 | 0x00000040 | SAR0, Channel #1 |
| 607 | PERI_MS_PPU_FX_PASS0_SAR0_CH2_CH | 0x40900880 | 0x00000040 | SAR0, Channel #2 |
| 608 | PERI_MS_PPU_FX_PASS0_SAR0_CH3_CH | 0x409008C0 | 0x00000040 | SAR0, Channel #3 |
| 609 | PERI_MS_PPU_FX_PASS0_SAR0_CH4_CH | 0x40900900 | 0x00000040 | SAR0, Channel #4 |

Table 21-1. PPU Fixed Structure Pairs (continued)

| Pair No. | PPU Fixed Structure Pair | Address | Size | Description |
|----------|-----------------------------------|------------|------------|-------------------|
| 610 | PERI_MS_PPU_FX_PASS0_SAR0_CH5_CH | 0x40900940 | 0x00000040 | SAR0, Channel #5 |
| 611 | PERI_MS_PPU_FX_PASS0_SAR0_CH6_CH | 0x40900980 | 0x00000040 | SAR0, Channel #6 |
| 612 | PERI_MS_PPU_FX_PASS0_SAR0_CH7_CH | 0x409009C0 | 0x00000040 | SAR0, Channel #7 |
| 613 | PERI_MS_PPU_FX_PASS0_SAR0_CH8_CH | 0x40900A00 | 0x00000040 | SAR0, Channel #8 |
| 614 | PERI_MS_PPU_FX_PASS0_SAR0_CH9_CH | 0x40900A40 | 0x00000040 | SAR0, Channel #9 |
| 615 | PERI_MS_PPU_FX_PASS0_SAR0_CH10_CH | 0x40900A80 | 0x00000040 | SAR0, Channel #10 |
| 616 | PERI_MS_PPU_FX_PASS0_SAR0_CH11_CH | 0x40900AC0 | 0x00000040 | SAR0, Channel #11 |
| 617 | PERI_MS_PPU_FX_PASS0_SAR0_CH12_CH | 0x40900B00 | 0x00000040 | SAR0, Channel #12 |
| 618 | PERI_MS_PPU_FX_PASS0_SAR0_CH13_CH | 0x40900B40 | 0x00000040 | SAR0, Channel #13 |
| 619 | PERI_MS_PPU_FX_PASS0_SAR0_CH14_CH | 0x40900B80 | 0x00000040 | SAR0, Channel #14 |
| 620 | PERI_MS_PPU_FX_PASS0_SAR0_CH15_CH | 0x40900BC0 | 0x00000040 | SAR0, Channel #15 |
| 621 | PERI_MS_PPU_FX_PASS0_SAR0_CH16_CH | 0x40900C00 | 0x00000040 | SAR0, Channel #16 |
| 622 | PERI_MS_PPU_FX_PASS0_SAR0_CH17_CH | 0x40900C40 | 0x00000040 | SAR0, Channel #17 |
| 623 | PERI_MS_PPU_FX_PASS0_SAR0_CH18_CH | 0x40900C80 | 0x00000040 | SAR0, Channel #18 |
| 624 | PERI_MS_PPU_FX_PASS0_SAR0_CH19_CH | 0x40900CC0 | 0x00000040 | SAR0, Channel #19 |
| 625 | PERI_MS_PPU_FX_PASS0_SAR0_CH20_CH | 0x40900D00 | 0x00000040 | SAR0, Channel #20 |
| 626 | PERI_MS_PPU_FX_PASS0_SAR0_CH21_CH | 0x40900D40 | 0x00000040 | SAR0, Channel #21 |
| 627 | PERI_MS_PPU_FX_PASS0_SAR0_CH22_CH | 0x40900D80 | 0x00000040 | SAR0, Channel #22 |
| 628 | PERI_MS_PPU_FX_PASS0_SAR0_CH23_CH | 0x40900DC0 | 0x00000040 | SAR0, Channel #23 |
| 629 | PERI_MS_PPU_FX_PASS0_SAR0_CH24_CH | 0x40900E00 | 0x00000040 | SAR0, Channel #24 |
| 630 | PERI_MS_PPU_FX_PASS0_SAR0_CH25_CH | 0x40900E40 | 0x00000040 | SAR0, Channel #25 |
| 631 | PERI_MS_PPU_FX_PASS0_SAR0_CH26_CH | 0x40900E80 | 0x00000040 | SAR0, Channel #26 |
| 632 | PERI_MS_PPU_FX_PASS0_SAR0_CH27_CH | 0x40900EC0 | 0x00000040 | SAR0, Channel #27 |
| 633 | PERI_MS_PPU_FX_PASS0_SAR0_CH28_CH | 0x40900F00 | 0x00000040 | SAR0, Channel #28 |
| 634 | PERI_MS_PPU_FX_PASS0_SAR0_CH29_CH | 0x40900F40 | 0x00000040 | SAR0, Channel #29 |
| 635 | PERI_MS_PPU_FX_PASS0_SAR0_CH30_CH | 0x40900F80 | 0x00000040 | SAR0, Channel #30 |
| 636 | PERI_MS_PPU_FX_PASS0_SAR0_CH31_CH | 0x40900FC0 | 0x00000040 | SAR0, Channel #31 |
| 637 | PERI_MS_PPU_FX_PASS0_SAR1_CH0_CH | 0x40901800 | 0x00000040 | SAR1, Channel #0 |
| 638 | PERI_MS_PPU_FX_PASS0_SAR1_CH1_CH | 0x40901840 | 0x00000040 | SAR1, Channel #1 |
| 639 | PERI_MS_PPU_FX_PASS0_SAR1_CH2_CH | 0x40901880 | 0x00000040 | SAR1, Channel #2 |
| 640 | PERI_MS_PPU_FX_PASS0_SAR1_CH3_CH | 0x409018C0 | 0x00000040 | SAR1, Channel #3 |
| 641 | PERI_MS_PPU_FX_PASS0_SAR1_CH4_CH | 0x40901900 | 0x00000040 | SAR1, Channel #4 |
| 642 | PERI_MS_PPU_FX_PASS0_SAR1_CH5_CH | 0x40901940 | 0x00000040 | SAR1, Channel #5 |
| 643 | PERI_MS_PPU_FX_PASS0_SAR1_CH6_CH | 0x40901980 | 0x00000040 | SAR1, Channel #6 |
| 644 | PERI_MS_PPU_FX_PASS0_SAR1_CH7_CH | 0x409019C0 | 0x00000040 | SAR1, Channel #7 |
| 645 | PERI_MS_PPU_FX_PASS0_SAR1_CH8_CH | 0x40901A00 | 0x00000040 | SAR1, Channel #8 |
| 646 | PERI_MS_PPU_FX_PASS0_SAR1_CH9_CH | 0x40901A40 | 0x00000040 | SAR1, Channel #9 |
| 647 | PERI_MS_PPU_FX_PASS0_SAR1_CH10_CH | 0x40901A80 | 0x00000040 | SAR1, Channel #10 |
| 648 | PERI_MS_PPU_FX_PASS0_SAR1_CH11_CH | 0x40901AC0 | 0x00000040 | SAR1, Channel #11 |
| 649 | PERI_MS_PPU_FX_PASS0_SAR1_CH12_CH | 0x40901B00 | 0x00000040 | SAR1, Channel #12 |
| 650 | PERI_MS_PPU_FX_PASS0_SAR1_CH13_CH | 0x40901B40 | 0x00000040 | SAR1, Channel #13 |

Table 21-1. PPU Fixed Structure Pairs (continued)

| Pair No. | PPU Fixed Structure Pair | Address | Size | Description |
|----------|-----------------------------------|------------|------------|-------------------|
| 651 | PERI_MS_PPU_FX_PASS0_SAR1_CH14_CH | 0x40901B80 | 0x00000040 | SAR1, Channel #14 |
| 652 | PERI_MS_PPU_FX_PASS0_SAR1_CH15_CH | 0x40901BC0 | 0x00000040 | SAR1, Channel #15 |
| 653 | PERI_MS_PPU_FX_PASS0_SAR1_CH16_CH | 0x40901C00 | 0x00000040 | SAR1, Channel #16 |
| 654 | PERI_MS_PPU_FX_PASS0_SAR1_CH17_CH | 0x40901C40 | 0x00000040 | SAR1, Channel #17 |
| 655 | PERI_MS_PPU_FX_PASS0_SAR1_CH18_CH | 0x40901C80 | 0x00000040 | SAR1, Channel #18 |
| 656 | PERI_MS_PPU_FX_PASS0_SAR1_CH19_CH | 0x40901CC0 | 0x00000040 | SAR1, Channel #19 |
| 657 | PERI_MS_PPU_FX_PASS0_SAR1_CH20_CH | 0x40901D00 | 0x00000040 | SAR1, Channel #20 |
| 658 | PERI_MS_PPU_FX_PASS0_SAR1_CH21_CH | 0x40901D40 | 0x00000040 | SAR1, Channel #21 |
| 659 | PERI_MS_PPU_FX_PASS0_SAR1_CH22_CH | 0x40901D80 | 0x00000040 | SAR1, Channel #22 |
| 660 | PERI_MS_PPU_FX_PASS0_SAR1_CH23_CH | 0x40901DC0 | 0x00000040 | SAR1, Channel #23 |
| 661 | PERI_MS_PPU_FX_PASS0_SAR1_CH24_CH | 0x40901E00 | 0x00000040 | SAR1, Channel #24 |
| 662 | PERI_MS_PPU_FX_PASS0_SAR1_CH25_CH | 0x40901E40 | 0x00000040 | SAR1, Channel #25 |
| 663 | PERI_MS_PPU_FX_PASS0_SAR1_CH26_CH | 0x40901E80 | 0x00000040 | SAR1, Channel #26 |
| 664 | PERI_MS_PPU_FX_PASS0_SAR1_CH27_CH | 0x40901EC0 | 0x00000040 | SAR1, Channel #27 |
| 665 | PERI_MS_PPU_FX_PASS0_SAR1_CH28_CH | 0x40901F00 | 0x00000040 | SAR1, Channel #28 |
| 666 | PERI_MS_PPU_FX_PASS0_SAR1_CH29_CH | 0x40901F40 | 0x00000040 | SAR1, Channel #29 |
| 667 | PERI_MS_PPU_FX_PASS0_SAR1_CH30_CH | 0x40901F80 | 0x00000040 | SAR1, Channel #30 |
| 668 | PERI_MS_PPU_FX_PASS0_SAR1_CH31_CH | 0x40901FC0 | 0x00000040 | SAR1, Channel #31 |
| 669 | PERI_MS_PPU_FX_PASS0_SAR2_CH0_CH | 0x40902800 | 0x00000040 | SAR2, Channel #0 |
| 670 | PERI_MS_PPU_FX_PASS0_SAR2_CH1_CH | 0x40902840 | 0x00000040 | SAR2, Channel #1 |
| 671 | PERI_MS_PPU_FX_PASS0_SAR2_CH2_CH | 0x40902880 | 0x00000040 | SAR2, Channel #2 |
| 672 | PERI_MS_PPU_FX_PASS0_SAR2_CH3_CH | 0x409028C0 | 0x00000040 | SAR2, Channel #3 |
| 673 | PERI_MS_PPU_FX_PASS0_SAR2_CH4_CH | 0x40902900 | 0x00000040 | SAR2, Channel #4 |
| 674 | PERI_MS_PPU_FX_PASS0_SAR2_CH5_CH | 0x40902940 | 0x00000040 | SAR2, Channel #5 |
| 675 | PERI_MS_PPU_FX_PASS0_SAR2_CH6_CH | 0x40902980 | 0x00000040 | SAR2, Channel #6 |
| 676 | PERI_MS_PPU_FX_PASS0_SAR2_CH7_CH | 0x409029C0 | 0x00000040 | SAR2, Channel #7 |
| 677 | PERI_MS_PPU_FX_PASS0_SAR2_CH8_CH | 0x40902A00 | 0x00000040 | SAR2, Channel #8 |
| 678 | PERI_MS_PPU_FX_PASS0_SAR2_CH9_CH | 0x40902A40 | 0x00000040 | SAR2, Channel #9 |
| 679 | PERI_MS_PPU_FX_PASS0_SAR2_CH10_CH | 0x40902A80 | 0x00000040 | SAR2, Channel #10 |
| 680 | PERI_MS_PPU_FX_PASS0_SAR2_CH11_CH | 0x40902AC0 | 0x00000040 | SAR2, Channel #11 |
| 681 | PERI_MS_PPU_FX_PASS0_SAR2_CH12_CH | 0x40902B00 | 0x00000040 | SAR2, Channel #12 |
| 682 | PERI_MS_PPU_FX_PASS0_SAR2_CH13_CH | 0x40902B40 | 0x00000040 | SAR2, Channel #13 |
| 683 | PERI_MS_PPU_FX_PASS0_SAR2_CH14_CH | 0x40902B80 | 0x00000040 | SAR2, Channel #14 |
| 684 | PERI_MS_PPU_FX_PASS0_SAR2_CH15_CH | 0x40902BC0 | 0x00000040 | SAR2, Channel #15 |
| 685 | PERI_MS_PPU_FX_PASS0_SAR2_CH16_CH | 0x40902C00 | 0x00000040 | SAR2, Channel #16 |
| 686 | PERI_MS_PPU_FX_PASS0_SAR2_CH17_CH | 0x40902C40 | 0x00000040 | SAR2, Channel #17 |
| 687 | PERI_MS_PPU_FX_PASS0_SAR2_CH18_CH | 0x40902C80 | 0x00000040 | SAR2, Channel #18 |
| 688 | PERI_MS_PPU_FX_PASS0_SAR2_CH19_CH | 0x40902CC0 | 0x00000040 | SAR2, Channel #19 |
| 689 | PERI_MS_PPU_FX_PASS0_SAR2_CH20_CH | 0x40902D00 | 0x00000040 | SAR2, Channel #20 |
| 690 | PERI_MS_PPU_FX_PASS0_SAR2_CH21_CH | 0x40902D40 | 0x00000040 | SAR2, Channel #21 |
| 691 | PERI_MS_PPU_FX_PASS0_SAR2_CH22_CH | 0x40902D80 | 0x00000040 | SAR2, Channel #22 |

Table 21-1. PPU Fixed Structure Pairs *(continued)*

| Pair No. | PPU Fixed Structure Pair | Address | Size | Description |
|----------|-----------------------------------|------------|------------|-------------------|
| 692 | PERI_MS_PPU_FX_PASS0_SAR2_CH23_CH | 0x40902DC0 | 0x00000040 | SAR2, Channel #23 |
| 693 | PERI_MS_PPU_FX_PASS0_SAR2_CH24_CH | 0x40902E00 | 0x00000040 | SAR2, Channel #24 |
| 694 | PERI_MS_PPU_FX_PASS0_SAR2_CH25_CH | 0x40902E40 | 0x00000040 | SAR2, Channel #25 |
| 695 | PERI_MS_PPU_FX_PASS0_SAR2_CH26_CH | 0x40902E80 | 0x00000040 | SAR2, Channel #26 |
| 696 | PERI_MS_PPU_FX_PASS0_SAR2_CH27_CH | 0x40902EC0 | 0x00000040 | SAR2, Channel #27 |
| 697 | PERI_MS_PPU_FX_PASS0_SAR2_CH28_CH | 0x40902F00 | 0x00000040 | SAR2, Channel #28 |
| 698 | PERI_MS_PPU_FX_PASS0_SAR2_CH29_CH | 0x40902F40 | 0x00000040 | SAR2, Channel #29 |
| 699 | PERI_MS_PPU_FX_PASS0_SAR2_CH30_CH | 0x40902F80 | 0x00000040 | SAR2, Channel #30 |
| 700 | PERI_MS_PPU_FX_PASS0_SAR2_CH31_CH | 0x40902FC0 | 0x00000040 | SAR2, Channel #31 |
| 701 | PERI_MS_PPU_FX_PASS0_TOP | 0x409F0000 | 0x00001000 | PASS0 SAR main |

22. Bus Masters

The Arbiter (part of flash controller) performs priority-based arbitration based on the master identifier. Each bus master has a dedicated 4-bit master identifier. This master identifier is used for bus arbitration and IPC functionality.

Table 22-1. Bus Masters for Access and Protection Control

| ID No. | Master ID | Description |
|--------|--------------------|---|
| 0 | CPUSS_MS_ID_CM0 | Master ID for CM0+ |
| 1 | CPUSS_MS_ID_CRYPT0 | Master ID for Crypto |
| 2 | CPUSS_MS_ID_DW0 | Master ID for P-DMA0 |
| 3 | CPUSS_MS_ID_DW1 | Master ID for P-DMA1 |
| 4 | CPUSS_MS_ID_DMAC | Master ID for M-DMA0 |
| 5 | CPUSS_MS_ID_SLOW0 | Master ID for External AHB-Lite Master 0 (SDHC) |
| 9 | CPUSS_MS_ID_FAST0 | Master ID for External AXI Master 0 (ETH0) |
| 10 | CPUSS_MS_ID_FAST1 | Master ID for External AXI Master 1 (ETH1) |
| 13 | CPUSS_MS_ID_CM7_1 | Master ID for CM7_1 |
| 14 | CPUSS_MS_ID_CM7_0 | Master ID for CM7_0 |
| 15 | CPUSS_MS_ID_TC | Master ID for DAP Tap Controller |

23. Miscellaneous Configuration

Table 23-1. Miscellaneous Configuration for CYT4BF Devices

| Sl. No. | Configuration | Number/Instances | Description |
|---------|--|------------------|--|
| 0 | SRSS_NUM_CLKPATH | 7 | Number of clock paths. One for each of FLL, PLL, Direct and CSV |
| 1 | SRSS_NUM_HFROOT | 8 | Number of CLK_HFs present |
| 2 | PERI_PC_NR | 8 | Number of protection contexts |
| 3 | PERI_PERI_PCLK_PCLK_GROUP_NR | 2 | Number of asynchronous PCLK groups |
| 4 | PERI_PERI_PCLK_PCLK_GROUP_NR0_GR_DIV_8_VECT | 4 | Group 0, Number of divide-by-8 clock dividers |
| 5 | PERI_PERI_PCLK_PCLK_GROUP_NR0_GR_DIV_16_VECT | 3 | Group 0, Number of divide-by-16 clock dividers |
| 6 | PERI_PERI_PCLK_PCLK_GROUP_NR0_GR_DIV_24_5_VECT | 1 | Group 0, Number of divide-by-24.5 clock dividers |
| 7 | PERI_PERI_PCLK_PCLK_GROUP_NR0_GR_CLOCK_VECT | 15 | Group 0, Number of programmable clocks [1, 256] |
| 8 | PERI_PERI_PCLK_PCLK_GROUP_NR1_GR_DIV_8_VECT | 19 | Group 1, Number of divide-by-8 clock dividers |
| 9 | PERI_PERI_PCLK_PCLK_GROUP_NR1_GR_DIV_16_VECT | 20 | Group 1, Number of divide-by-16 clock dividers |
| 10 | PERI_PERI_PCLK_PCLK_GROUP_NR1_GR_DIV_24_5_VECT | 21 | Group 1, Number of divide-by-24.5 clock dividers |
| 11 | PERI_PERI_PCLK_PCLK_GROUP_NR1_GR_CLOCK_VECT | 154 | Group 1, Number of programmable clocks [1, 256] |
| 12 | CPUSS_CM0P_MPU_NR | 8 | Number of MPU regions in CM0+ |
| 13 | CPUSS_CM7_0_FPU_LVL | 2 | CM7_0 Floating point unit configuration. 0 - No FPU 1 - Single precision FPU 2 - Single and Double precision FPU |
| 14 | CPUSS_CM7_0_MPU_NR | 16 | Number of MPU regions in CM7_0 |
| 15 | CPUSS_CM7_0_ICACHE_SIZE | 16 | CM7_0 Instruction cache (ICACHE) size in KB |
| 16 | CPUSS_CM7_0_DCACHE_SIZE | 16 | CM7_0 Data cache size (DCACHE) in KB |
| 17 | CPUSS_CM7_0_ITCM_SIZE | 16 | CM7_0 Instruction TCM (ITCM) size in KB |
| 18 | CPUSS_CM7_0_DTCM_SIZE | 16 | CM7_0 Data TCM (DTCM) size in KB |
| 19 | CPUSS_CM7_1_FPU_LVL | 2 | CM7_1 Floating point unit configuration. 0 - No FPU 1 - Single precision FPU 2 - Single and Double precision FPU |
| 20 | CPUSS_CM7_1_MPU_NR | 16 | Number of MPU regions in CM7_1 |
| 21 | CPUSS_CM7_1_ICACHE_SIZE | 16 | CM7_1 Instruction cache (ICACHE) size in KB |
| 22 | CPUSS_CM7_1_DCACHE_SIZE | 16 | CM7_1 Data cache size (DCACHE) in KB |
| 23 | CPUSS_CM7_1_ITCM_SIZE | 16 | CM7_1 Instruction TCM (ITCM) size in KB |
| 24 | CPUSS_CM7_1_DTCM_SIZE | 16 | CM7_1 Data TCM (DTCM) size in KB |
| 25 | CPUSS_DW0_CH_NR | 143 | Number of P-DMA0 channels |
| 26 | CPUSS_DW1_CH_NR | 65 | Number of P-DMA1 channels |
| 27 | CPUSS_DMACH_CH_NR | 8 | Number of M-DMA0 controller channels |
| 28 | CPUSS_CRYPTOBUFF_SIZE | 2048 | Number of 32-bit words in the IP internal memory buffer (to allow for a 256-B, 512-B, 1-KB, 2-KB, 4-KB, 8-KB, 16-KB, and 32-KB memory buffer) |
| 29 | CPUSS_FAULT_FAULT_NR | 4 | Number of fault structures |
| 30 | CPUSS_IPC_IPC_NR | 8 | Number of IPC structures 0 - Reserved for CM0+ access 1 - Reserved for CM7_0 access 2 - Reserved for CM7_1 access 3 - Reserved for DAP access Remaining for user purposes |
| 31 | CPUSS_PROT_SMPU_STRUCT_NR | 16 | Number of S MPU protection structures |
| 32 | SCB0_EZ_DATA_NR | 256 | Number of EZ memory bytes. This memory is used in EZ mode, CMD_RESP mode and FIFO mode. Note: Only SCB0 supports EZ mode |

Table 23-1. Miscellaneous Configuration for CYT4BF Devices (continued)

| Sl. No. | Configuration | Number/Instances | Description |
|---------|-------------------------------------|------------------|---|
| 33 | TCPWM0_TR_ONE_CNT_NR | 3 | Number of input triggers per counter, routed to one counter |
| 34 | TCPWM0_TR_ALL_CNT_NR | 12 | Number of input triggers routed to all counters, based on the pin package |
| 35 | TCPWM0_GRP_NR | 3 | Number of TCPWM0 counter groups |
| 36 | TCPWM0_GRP_NR0_GRP_GRP_CNT_NR | 3 | Number of counters per TCPWM0 Group #0 |
| 37 | TCPWM0_GRP_NR0_CNT_GRP_CNT_WIDTH | 16 | Counter width in number of bits per TCPWM0 Group #0 |
| 38 | TCPWM0_GRP_NR1_GRP_GRP_CNT_NR | 3 | Number of counters per TCPWM0 Group #1 |
| 39 | TCPWM0_GRP_NR1_CNT_GRP_CNT_WIDTH | 16 | Counter width in number of bits per TCPWM0 Group #1 |
| 40 | TCPWM0_GRP_NR2_GRP_GRP_CNT_NR | 3 | Number of counters per TCPWM0 Group #2 |
| 41 | TCPWM0_GRP_NR2_CNT_GRP_CNT_WIDTH | 32 | Counter width in number of bits per TCPWM0 Group #2 |
| 42 | TCPWM1_GRP_NR | 3 | Number of TCPWM1 counter groups |
| 43 | TCPWM1_GRP_NR0_GRP_GRP_CNT_NR | 84 | Number of counters per TCPWM1 Group #0 |
| 44 | TCPWM1_GRP_NR0_CNT_GRP_CNT_WIDTH | 16 | Counter width in number of bits per TCPWM1 Group #0 |
| 45 | TCPWM1_GRP_NR1_GRP_GRP_CNT_NR | 12 | Number of counters per TCPWM1 Group #1 |
| 46 | TCPWM1_GRP_NR1_CNT_GRP_CNT_WIDTH | 16 | Counter width in number of bits per TCPWM1 Group #1 |
| 47 | TCPWM1_GRP_NR2_GRP_GRP_CNT_NR | 13 | Number of counters per TCPWM1 Group #2 |
| 48 | TCPWM1_GRP_NR2_CNT_GRP_CNT_WIDTH | 32 | Counter width in number of bits per TCPWM1 Group #2 |
| 49 | CANFD0_MRAM_SIZE / CANFD1_MRAM_SIZE | 40 | Message RAM size in KB shared by all the channels |
| 50 | EVTGEN_COMP_STRUCT_NR | 16 | Number of Event Generator comparator structures |

24. Development Support

CYT4BF has a rich set of documentation, programming tools, and online resources to assist during the development process. Visit www.cypress.com to find out more.

24.1 Documentation

A suite of documentation supports CYT4BF to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

24.1.1 *Software User Guide*

A step-by-step guide for using the sample driver library along with third-party IDEs such as IAR EWARM and GHS Multi.

24.1.2 *Technical Reference Manual*

The Technical Reference Manual (TRM) contains all the technical detail needed to use a CYT4BF device, including a complete description of all registers. The TRM is available in the documentation section at www.cypress.com.

24.2 Tools

CYT4BF is supported on third-party development tool ecosystems such as IAR and GHS. CYT4BF is also supported by Cypress programming utilities for programming, erasing, or reading using Cypress' MiniProg4 or Segger J-link. More details are available in the documentation section at www.cypress.com.

25. Electrical Specifications

The specifications listed here are Preliminary.

25.1 Absolute Maximum Ratings

Use of this device under conditions outside the Min and Max limits listed in [Table 25-1](#) may cause permanent damage to the device. Exposure to conditions within the limits of [Table 25-1](#) but beyond those of normal operation for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When operated under conditions within the limits of [Table 25-1](#) but beyond those of normal operation, the device may not operate to specification.

Power considerations

The average chip-junction temperature, T_J , in °C, may be calculated using Equation 1:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \text{Equation. 1}$$

Where:

T_A is the ambient temperature in °C.

θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W.

P_D is the sum of P_{INT} and P_{IO} ($P_D = P_{INT} + P_{IO}$).

P_{INT} is the chip internal power. ($P_{INT} = V_{DD} \times I_{DD} + V_{DDA} \times I_A$)

P_{IO} represents the power dissipation on input and output pins; user determined.

For most applications, $P_{IO} < P_{INT}$ and may be neglected.

On the other hand, P_{IO} may be significant if the device is configured to continuously drive external modules and/or memories.

WARNING:

- The recommended operating conditions are required to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are guaranteed when the device is operated under these conditions.
- Operation under any conditions other than those mentioned in the respective "Details/Conditions" may adversely affect reliability of the device and can result in device failure.
- No guarantee is made with respect to any use, operating conditions, or combinations not represented in this datasheet. If you want to operate the device under any condition other than those listed herein, contact the sales representatives.

Table 25-1. Absolute Maximum Ratings

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---------|-------------------------|--|---------------------------|-----|---------------------------|-------|--|
| SID10 | V _{DDD_ABS} | V _{DDD} power supply voltage ^[41] | V _{SSD} - 0.3 | - | V _{SSD} + 6.0 | V | For ports 0, 1, 2, 3, 4, 5, 16, 17, 18, 19, 20, 21, 22, 23, 28, 29, 30, 31 |
| SID10B | V _{DDIO_1_ABS} | V _{DDIO_1} power supply voltage ^[41] | V _{SSD} - 0.3 | - | V _{SSD} + 6.0 | V | For ports 6, 7, 8, 9, 32 |
| SID10C | V _{DDIO_2_ABS} | V _{DDIO_2} power supply voltage ^[41] | V _{SSD} - 0.3 | - | V _{SSD} + 6.0 | V | For ports 10, 11, 12, 13, 14, 15 |
| SID10D | V _{DDIO_3_ABS} | V _{DDIO_3} power supply voltage ^[41] | V _{SSIO_3} - 0.3 | - | V _{SSIO_3} + 4.0 | V | For ports 24, 25 |
| SID10E | V _{DDIO_4_ABS} | V _{DDIO_4} power supply voltage ^[41] | V _{SSIO_4} - 0.3 | - | V _{SSIO_4} + 4.0 | V | For ports 26, 27, 33, 34 |
| SID11 | V _{DDA_ABS} | V _{DDA} analog power supply voltage ^[41] | V _{SSA} - 0.3 | - | V _{SSA} + 6.0 | V | V _{DDIO_2} = V _{DDA} |
| SID12 | V _{REFH_ABS} | Analog reference voltage, HIGH ^[41] | V _{SSA} - 0.3 | - | V _{SSA} + 6.0 | V | V _{REFH} ≤ (V _{DDA} + 0.3 V) |
| SID12A | V _{REFL_ABS} | Analog reference voltage, LOW ^[41] | V _{SSA} - 0.3 | - | V _{SSA} + 0.3 | V | |
| SID13 | V _{CCD_ABS} | V _{CCD} Power supply voltage ^[41] | V _{SSD} - 0.3 | - | V _{SSD} + 1.21 | V | |
| SID15A | V _{I0_ABS} | Input voltage ^[41] | V _{SSD} - 0.5 | - | V _{DDD} + 0.5 | V | For ports 0, 1, 2, 3, 4, 5, 16, 17, 18, 19, 20, 21, 22, 23, 28, 29, 30, 31 |
| SID15B | V _{I1_ABS} | Input voltage ^[41] | V _{SSD} - 0.5 | - | V _{DDIO_1} + 0.5 | V | For ports 6, 7, 8, 9, 32 |
| SID15C | V _{I2_ABS} | Input voltage ^[41] | V _{SSD} - 0.5 | - | V _{DDIO_2} + 0.5 | V | For ports 10, 11, 12, 13, 14, 15 |
| SID15D | V _{I3_ABS} | Input voltage ^[41] | V _{SSIO_3} - 0.5 | - | V _{DDIO_3} + 0.5 | V | For ports 24, 25 |
| SID15E | V _{I4_ABS} | Input voltage ^[41] | V _{SSIO_4} - 0.5 | - | V _{DDIO_4} + 0.5 | V | For ports 26, 27, 33, 34 |
| SID15F | V _{I5_ABS} | Input voltage ^[41] | V _{SSD} - 0.5 | - | V _{DDD} + 0.5 | V | For EXT_PS_CTL0 in external PMIC/transistor mode, EXT_PS_CTL1 in external transistor mode. |
| SID16 | V _{IA_ABS} | Analog input voltage ^[41] | V _{SSA} - 0.3 | - | V _{DDA} + 0.3 | V | |
| SID17A | V _{O0_ABS} | Output voltage ^[41] | V _{SSD} - 0.3 | - | V _{DDD} + 0.3 | V | For ports 0, 1, 2, 3, 4, 5, 16, 17, 18, 19, 20, 21, 22, 23, 28, 29, 30, 31 |
| SID17B | V _{O1_ABS} | Output voltage ^[41] | V _{SSD} - 0.3 | - | V _{DDIO_1} + 0.3 | V | For ports 6, 7, 8, 9, 32 |
| SID17C | V _{O2_ABS} | Output voltage ^[41] | V _{SSD} - 0.3 | - | V _{DDIO_2} + 0.3 | V | For ports 10, 11, 12, 13, 14, 15 |
| SID17D | V _{O3_ABS} | Output voltage ^[41] | V _{SSIO_3} - 0.3 | - | V _{DDIO_3} + 0.3 | V | For ports 24, 25 |
| SID17E | V _{O5_ABS} | Output voltage ^[41] | V _{SSIO_4} - 0.3 | - | V _{DDIO_4} + 0.3 | V | For ports 26, 27, 33, 34 |
| SID17F | V _{O4_ABS} | Output voltage ^[41] | V _{SSD} - 0.3 | - | V _{DDD} + 0.3 | V | For EXT_PS_CTL1/2 in external PMIC mode, DRV_VOUT in external transistor mode |
| SID18 | I _{CLAMP_ABS} | Maximum clamp current ^[42, 43, 44] | -5 | - | 5 | mA | |

Notes

41. These parameters are based on the condition that V_{SSD} = V_{SSA} = V_{SSIO_3} = V_{SSIO_4} = 0.0 V.

42. A current-limiting resistor must be provided such that the current at the I/O pin does not exceed rated values at any time, including during power transients. Refer to Figure 25-1. for more information on the recommended circuit.

43. V_{DDD} and V_{DDIO} must be sufficiently loaded or protected to prevent them from being pulled out of the recommended operating range by the clamp current.

44. When the conditions of [42], [43] and SID18A/B/C/D are met, |I_{CLAMP_ABS}| supersedes V_{IA_ABS} and V_{I_ABS}.

Table 25-1. Absolute Maximum Ratings (continued)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---------|-----------------------------------|---|-----|-----|-----|-------|---|
| SID18A | I _{CLAMP_SUPPLY_POS_ABS} | Maximum positive clamp current per I/O supply pin. Limit applies to I/O supply pin closest to the B+ injected current ^[45] | – | – | 10 | mA | +B injected DC current is not allowed for Ports 11 and 21. |
| SID18B | I _{CLAMP_SUPPLY_NEG_ABS} | Maximum negative clamp current per I/O ground pin. Limit applies to I/O supply pin closest to the B+ injected current ^[45] | – | – | 10 | mA | +B injected DC current is not allowed for Ports 11 and 21. |
| SID18C | I _{CLAMP_TOTAL_POS_ABS} | Maximum positive clamp current per I/O supply, if not limited by the per supply pin (based on SID18A). | – | – | 50 | mA | |
| SID18D | I _{CLAMP_TOTAL_NEG_ABS} | Maximum negative clamp current per I/O ground, if not limited by the per supply pin (based on SID18B). | – | – | 50 | mA | |
| SID20A | I _{OL1A_ABS} | LOW-level maximum output current ^[46] | – | – | 6 | mA | GPIO_STD, configured for drive_sel<1:0>= 0b0X |
| SID20B | I _{OL1B_ABS} | LOW-level maximum output current ^[46] | – | – | 2 | mA | GPIO_STD, configured for drive_sel<1:0>= 0b10 |
| SID20C | I _{OL1C_ABS} | LOW-level maximum output current ^[46] | – | – | 1 | mA | GPIO_STD, configured for drive_sel<1:0>= 0b11 |
| SID21A | I _{OL2A_ABS} | LOW-level maximum output current ^[46] | – | – | 6 | mA | GPIO_ENH, configured for drive_sel<1:0>= 0b0X |
| SID21B | I _{OL2B_ABS} | LOW-level maximum output current ^[46] | – | – | 2 | mA | GPIO_ENH, configured for drive_sel<1:0>= 0b10 |
| SID21C | I _{OL2C_ABS} | LOW-level maximum output current ^[46] | – | – | 1 | mA | GPIO_ENH, configured for drive_sel<1:0>= 0b11 |
| SID22A | I _{OL3A_ABS} | LOW-level maximum output current ^[46] | – | – | 10 | mA | HSIO, configured for drive_sel<1:0>= 0b00 |
| SID22B | I _{OL3B_ABS} | LOW-level maximum output current ^[46] | – | – | 2 | mA | HSIO, configured for drive_sel<1:0>= 0b01 |
| SID22C | I _{OL3C_ABS} | LOW-level maximum output current ^[46] | – | – | 1 | mA | HSIO, configured for drive_sel<1:0>= 0b10 |
| SID22D | I _{OL3D_ABS} | LOW-level maximum output current ^[46] | – | – | 0.5 | mA | HSIO, configured for drive_sel<1:0>= 0b11 |
| SID23A | I _{OL4A_ABS} | Sink maximum current ^[46] | – | – | 4 | mA | For pin EXT_PS_CTL1 in external PMIC mode and internal regulator mode and pin EXT_PS_CTL2 in external PMIC mode |
| SID23B | I _{OL4B_ABS} | Sink average current ^[47] | – | – | 1 | mA | For pin EXT_PS_CTL1 in external PMIC mode and internal regulator mode and pin EXT_PS_CTL2 in external PMIC mode |
| SID23C | I _{OL4C_ABS} | Sink maximum current ^[46] | – | – | 25 | mA | For pin DRV_VOUT in external transistor mode |
| SID26A | ∑I _{OL_ABS_GPIO} | LOW-level total output current ^[48] | – | – | 50 | mA | |
| SID26B | ∑I _{OL_ABS_HSIO} | LOW-level total output current ^[49] | – | – | 85 | mA | |
| SID27A | I _{OH1A_ABS} | HIGH-level maximum output current ^[46] | – | – | –5 | mA | GPIO_STD, configured for drive_sel<1:0>= 0b0X |

Notes

45. The definition of “closer” depends on the package. In TEQFP packaging, “closest” is determined by counting pins. For example, in a 176-TEQFP package, P17.4 (pin 120) is closer to the V_{DD} on pin 110 than on pin 132. Ports 11 and 21 should not be used for injection currents. The impact of injection currents is only defined for GPIO_STD/GPIO_ENH type I/Os. In BGA packaging, the following IO port groups are treated as having separate supply pins: Ports 0, 1, 2, 22, 23, and 28; Ports 3, 4, 5, 29, 30, and 31; Ports 6, 7, 8, 9, and 32; Ports 10, 12, 13, 14, 15, 26, and 27; Ports 16 and 17; Ports 18, 19, and 20.

46. The maximum output current is the peak current flowing through any one I/O.

47. The average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 10 ms period. The average value is the operation current × the operation ratio. The operation current period over the average current spec should be less than 100 ns.

Table 25-1. Absolute Maximum Ratings (continued)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---------|--------------------------|--|------|-----|------|-------|--|
| SID27B | I _{OH1B_ABS} | HIGH-level maximum output current ^[46] | – | – | –2 | mA | GPIO_STD, configured for drive_sel<1:0>= 0b10 |
| SID27C | I _{OH1C_ABS} | HIGH-level maximum output current ^[46] | – | – | –1 | mA | GPIO_STD, configured for drive_sel<1:0>= 0b11 |
| SID28A | I _{OH2A_ABS} | HIGH-level maximum output current ^[46] | – | – | –5 | mA | GPIO_ENH, configured for drive_sel<1:0>= 0b0X |
| SID28B | I _{OH2B_ABS} | HIGH-level maximum output current ^[46] | – | – | –2 | mA | GPIO_ENH, configured for drive_sel<1:0>= 0b10 |
| SID28C | I _{OH2C_ABS} | HIGH-level maximum output current ^[46] | – | – | –1 | mA | GPIO_ENH, configured for drive_sel<1:0>= 0b11 |
| SID29A | I _{OH3A_ABS} | HIGH-level maximum output current ^[46] | – | – | –10 | mA | HSIO, configured for drive_sel<1:0>= 0b00 |
| SID29B | I _{OH3B_ABS} | HIGH-level maximum output current ^[46] | – | – | –2 | mA | HSIO, configured for drive_sel<1:0>= 0b01 |
| SID29C | I _{OH3C_ABS} | HIGH-level maximum output current ^[46] | – | – | –1 | mA | HSIO, configured for drive_sel<1:0>= 0b10 |
| SID29D | I _{OH3D_ABS} | HIGH-level maximum output current ^[46] | – | – | –0.5 | mA | HSIO, configured for drive_sel<1:0>= 0b11 |
| SID30A | I _{OH4A_ABS} | Source maximum current ^[46] | – | – | –4 | mA | For pin EXT_PS_CTL1 in external PMIC mode and internal regulator mode and pin EXT_PS_CTL2 in external PMIC mode. |
| SID30B | I _{OH4B_ABS} | Source maximum current ^[46] | – | – | –25 | mA | For pin DRV_VOUT in external transistor mode. |
| SID30C | I _{OH4C_ABS} | Source average current ^[47] | – | – | –1 | mA | For pin EXT_PS_CTL1 in external PMIC mode and internal regulator mode and pin EXT_PS_CTL2 in external PMIC mode. |
| SID30D | I _{OH4D_ABS} | Source average current ^[47] | – | – | –12 | mA | For pin DRV_VOUT in external transistor mode. |
| SID33A | $\sum I_{OH_ABS_GPIO}$ | HIGH-level total output current ^[48] | – | – | –50 | mA | |
| SID33B | $\sum I_{OH_ABS_HSIO}$ | HIGH-level total output current ^[49] | – | – | –85 | mA | |
| SID33D | PIO | Total output power dissipation ^[50] | – | – | 307 | mW | |
| SID34 | P _D | Power dissipation for external PMIC/transistor mode | – | – | 1000 | mW | T _J should not exceed 150 °C |
| SID34A | P _D | Power dissipation for internal regulator mode | – | – | 2000 | mW | T _J should not exceed 150 °C |
| SID35 | T _A | Ambient temperature | –40 | – | 105 | °C | For S-grade devices |
| SID36 | T _A | Ambient temperature | –40 | – | 125 | °C | For E-grade devices |
| SID37 | T _{STG} | Storage temperature | –55 | – | 150 | °C | |
| SID38 | T _J | Operating Junction temperature | –40 | – | 150 | °C | |
| SID39A | V _{ESD_HBM} | Electrostatic discharge human body model | 2000 | – | – | V | |
| SID39B1 | V _{ESD_CDM1} | Electrostatic discharge charged device model for corner pins | 750 | – | – | V | |
| SID39B2 | V _{ESD_CDM2} | Electrostatic discharge charged device model for all other pins | 500 | – | – | V | |
| SID39C | I _{LU} | The maximum pin current the device can tolerate before triggering a latch-up | –100 | – | 100 | mA | |

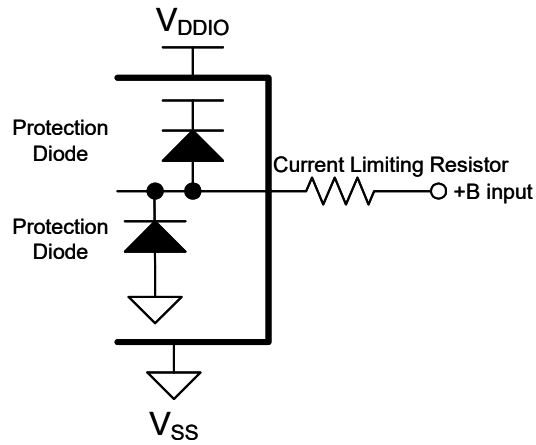
Notes

48. The total output current is the maximum current flowing through all GPIO_STD and GPIO_ENH I/Os.

49. The total output current is the maximum current flowing through all HSIO_STD I/Os.

50. The total output power dissipation is the maximum power dissipation flowing through all I/Os. $PIO = (V_{DD} \cdot V_{DDIO_1} \cdot V_{DDIO_2}) \times (|\sum I_{OH_ABS_GPIO}| + |\sum I_{OL_ABS_GPIO}|) + (V_{DDIO_3} \cdot V_{DDIO_4}) \times (|\sum I_{OH_ABS_HSIO}| + |\sum I_{OL_ABS_HSIO}|)$

Figure 25-1.Example of a Recommended Circuit^[50]



WARNING:

Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current, or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

Note

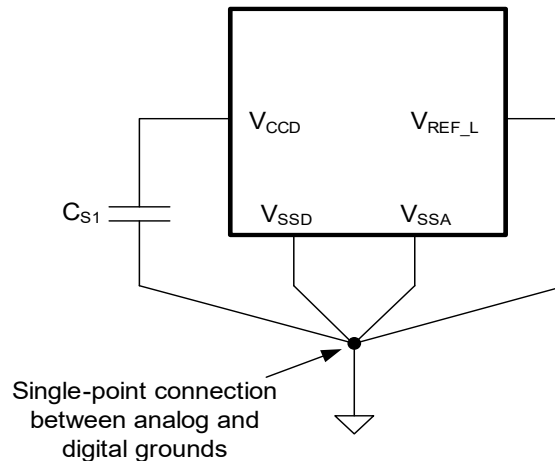
50. +B is the positive battery voltage around 45 V.

25.2 Device-Level Specifications

Table 25-2. Recommended Operating Conditions

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|--|---------------------|------|---------------------|---------|---|
| Recommended Operating Conditions | | | | | | | |
| SID40 | V_{DDDD} , V_{DDDA} , V_{DDIO_1} , V_{DDIO_2} , | Power supply voltage ^[51] | 2.7 ^[52] | – | 5.5 ^[53] | V | |
| SID40A | $V_{DDIO_1_EFP}$ | Power supply voltage for eFuse programming ^[54] | 3 | – | 5.5 | V | |
| SID40B | V_{DDIO_3} , V_{DDIO_4} | Power supply voltage | 2.7 | – | 3.6 | V | |
| SID40C | V_{CCD} | External V_{CCD} power supply | 1.10 | 1.15 | 1.20 | V | External V_{CCD} power supply range when externally supplying V_{CCD} |
| SID41 | C_{S1} | Smoothing capacitor ^[55, 56] | 6.79 | – | 22 | μ F | |

Figure 25-2.Smoothing Capacitor



Smoothing capacitor should be placed as close as possible to the V_{CCD} pin.

Notes

- 51. V_{DDDD} , V_{DDIO_1} , V_{DDIO_2} , V_{DDIO_3} , V_{DDIO_4} , and V_{DDA} do not have any sequencing limitation and can establish in any order. These supplies (except V_{DDA} and V_{DDIO_2}) are independent in voltage level. See 12-Bit SAR ADC DC Specifications when using ADC units.
- 52. 3.0 V \pm 10% is supported with a lower BOD setting option for V_{DDDD} and V_{DDA} . This setting provides robust protection for internal timing but BOD reset occurs at a voltage below the specified operating conditions. A higher BOD setting option is available (consistent with down to 3.0 V) and guarantees that all operating conditions are met.
- 53. 5.0 V \pm 10% is supported with a higher OVD setting option for V_{DDDD} and V_{DDA} . This setting provides robust protection for internal and interface timing, but OVD reset occurs at a voltage above the specified operating conditions. A lower OVD setting option is available (consistent with up to 5.0 V) and guarantees that all operating conditions are met.
- 54. eFuse programming must be executed with the part in a “quiet” state, with minimal activity (preferably only JTAG or a single LIN/CAN channel on V_{DDDD} domain, no activity on V_{DDIO_1}).
- 55. Smoothing capacitor, C_{S1} is required per chip (not per V_{CCD} pin). The V_{CCD} pins must be connected together to ensure a low-impedance connection (see the requirement in Figure 25-2. and Table 25-3).
- 56. Capacitors used for power supply decoupling or filtering are operated under a continuous DC-bias. Many capacitors used with DC power across them provide less than their target capacitance, and their capacitance is not constant across their working voltage range. When selecting capacitors for use with this device, ensure that the selected components provide the required capacitance under the specific operating conditions of temperature and voltage used in your design. While the temperature coefficient is normally found within a part’s catalog (such as, X7R, C0G, Y5V), the matching voltage coefficient may only be available on the component datasheet or direct from the manufacturer. Use of components that do not provide the required capacitance under the actual operating conditions may cause the device to operate to less than datasheet specifications.

25.3 Smoothing Capacitor Recommendations

Table 25-3. Smoothing Capacitor Connections

| Package | C _{S1} @ Pin Pair |
|-----------|--|
| 176-TEQFP | V _{CCD} : 156, V _{SSD} : 155 |
| 272-BGA | V _{CCD} : F13, V _{SSD} : G12 |
| 320-BGA | V _{CCD} : F15, V _{SSD} : H13 |

25.4 DC Specifications

Table 25-4. DC Specifications, CPU Current, and Transition Time Specifications

All specifications are valid for $-40\text{ }^{\circ}\text{C} \leq T_A \leq 125\text{ }^{\circ}\text{C}$ and for 2.7 V to 5.5 V except where noted.

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|--------------------------|--------------------------------|--|-----|-----|-----|-------|--|
| Active/Sleep Mode | | | | | | | |
| SID49C1 | I _{DD_VDDD_CM0_7_8_1} | V _{DDD} current in internal regulator mode, LPACTIVE mode (CM0+ and CM7_0 at 8 MHz, all peripherals are disabled) | – | 16 | 24 | mA | CM0+ and CM7_0 clocked at 8 MHz with IMO. CM7_1 powered off. All peripherals are disabled. No IO toggling. CPUs CM7_0 and CM0+ executing Dhrystone from flash with cache enabled. Typ: T _A = 25 °C, V _{DDD} = 5.0 V, process typ (TT) Max: T _A = 25 °C, V _{DDD} = 5.5 V, process worst (FF) |
| SID49C | I _{DD_VDDD_CM0_7_8} | V _{DDD} current in internal regulator mode, LPACTIVE mode (CM0+ and CM7_0 at 8 MHz, all peripherals are enabled) | – | 18 | 226 | mA | CM0+ and CM7_0 clocked at 8 MHz with IMO. CM7_1 powered off. All peripherals are enabled. No IO toggling. M-DMA transferring data from code + work flash, P-DMA chains with maximum trigger activity. CPUs CM7_0 and CM0+ executing Dhrystone from flash with cache enabled. Typ: T _A = 25 °C, V _{DDD} = 5.0 V, process typ (TT) Max: T _A = 105 °C, V _{DDD} = 5.5 V, process worst (FF) |

Table 25-4. DC Specifications, CPU Current, and Transition Time Specifications (continued)

 All specifications are valid for $-40\text{ }^{\circ}\text{C} \leq T_A \leq 125\text{ }^{\circ}\text{C}$ and for 2.7 V to 5.5 V except where noted.

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|---------------------------|---|-----|-----|-----|-------|---|
| SID49E1 | $I_{DD1_VCCD_CM7_350}$ | V_{CCD} current in external PMIC/transistor mode, Active mode (CM7_0 at 350 MHz, CM0+ at 100 MHz, all peripherals are enabled) | – | 155 | 431 | mA | PLL enabled at 350 MHz with ECO reference. All peripherals are enabled. No IO toggling. CM7_1 powered off. M-DMA transferring data from code + work flash, P-DMA chains with maximum trigger activity. CPUs CM7_0 and CM0+ executing Dhrystone from flash with cache enabled. Typ: $T_A = 25\text{ }^{\circ}\text{C}$, $V_{DD} = 5.0\text{ V}$, process typ (TT) Max: $T_A = 125\text{ }^{\circ}\text{C}$, $V_{DD} = 5.5\text{ V}$, process worst (FF) |
| SID49E2 | $I_{DD1_VDDD_CM7_350}$ | V_{DDD} current in external PMIC/transistor mode, Active mode (CM7_0 at 350 MHz, CM0+ at 100 MHz, all peripherals are enabled) | – | 7 | 9 | mA | PLL enabled at 350 MHz with ECO reference. All peripherals are enabled. No IO toggling. CM7_1 powered off. M-DMA transferring data from code + work flash, P-DMA chains with maximum trigger activity. CPUs CM7_0 and CM0+ executing Dhrystone from flash with cache enabled. Typ: $T_A = 25\text{ }^{\circ}\text{C}$, $V_{DD} = 5.0\text{ V}$, process typ (TT) Max: $T_A = 125\text{ }^{\circ}\text{C}$, $V_{DD} = 5.5\text{ V}$, process worst (FF) |
| SID50A1 | $I_{DD1_VCCD_F}$ | V_{CCD} current in external PMIC/transistor mode, Active mode (CM7 CPUs at 350 MHz, CM0+ at 100 MHz, all peripherals are enabled) | – | 209 | 543 | mA | PLL enabled at 350 MHz with ECO reference. All peripherals are enabled. No IO toggling. M-DMA transferring data from code + work flash, P-DMA chains with maximum trigger activity. CM7 CPUs and CM0+ executing Dhrystone from flash with cache enabled. Typ: $T_A = 25\text{ }^{\circ}\text{C}$, $V_{DD} = 5.0\text{ V}$, process typ (TT) Max: $T_A = 125\text{ }^{\circ}\text{C}$, $V_{DD} = 5.5\text{ V}$, process worst (FF) |

Table 25-4. DC Specifications, CPU Current, and Transition Time Specifications (continued)

 All specifications are valid for $-40\text{ }^{\circ}\text{C} \leq T_A \leq 125\text{ }^{\circ}\text{C}$ and for 2.7 V to 5.5 V except where noted.

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|--------------------|--|-----|-----|-----|-------|---|
| SID50A2 | $I_{DD1_VDDD_F}$ | VDDD current in external PMIC/transistor mode, Active mode (CM7 CPUs at 350 MHz, CM0+ at 100 MHz, all peripherals are enabled) | – | 7 | 9.3 | mA | PLL enabled at 350 MHz with ECO reference. All peripherals are enabled. No IO toggling. M-DMA transferring data from code + work flash, P-DMA chains with maximum trigger activity. CM7 CPUs and CM0+ executing Dhrystone from flash with cache enabled. Typ: $T_A = 25\text{ }^{\circ}\text{C}$, $V_{DDD} = 5.0\text{ V}$, process typ (TT) Max: $T_A = 125\text{ }^{\circ}\text{C}$, $V_{DDD} = 5.5\text{ V}$, process worst (FF) |
| SID53A | $I_{DD2_8_VDDD}$ | V_{DDD} current in internal regulator mode. CM7_1=OFF, Other CPUs in Sleep. | – | 13 | 218 | mA | IMO clocked at 8 MHz. All peripherals, PLL, FLL, peripheral clocks, interrupts, CSV, DMA are disabled. No IO toggling. Typ: $T_A = 25\text{ }^{\circ}\text{C}$, $V_{DDD} = 5.0\text{ V}$, process typ (TT) Max: $T_A = 105\text{ }^{\circ}\text{C}$, $V_{DDD} = 5.5\text{ V}$, process worst (FF) |

Table 25-4. DC Specifications, CPU Current, and Transition Time Specifications (continued)

 All specifications are valid for $-40\text{ }^{\circ}\text{C} \leq T_A \leq 125\text{ }^{\circ}\text{C}$ and for 2.7 V to 5.5 V except where noted.

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|-----------------------|-----------------------|---|-----|-----|-----|-------|--|
| SID58A | I _{DD_CWU2} | Average current for cyclic wake-up operation. This is the average current for the specified LPACTIVE mode and DeepSleep mode (RTC, WDT, and Event Generator operating). | – | 60 | 198 | μA | <p>$T_A = 25\text{ }^{\circ}\text{C}$, 64-KB SRAM retention, Event generator operates with ILO0 in DeepSleep and LP Active, Smart I/O operates with ILO0, CM0+, CM7_0: Retained, CM7_1: OFF.</p> <p>Typ: $V_{DD} = 5.0\text{ V}$, process typ (TT)</p> <p>Max: $V_{DD} = 5.5\text{ V}$, process worst (FF)</p> <p>This average current is achieved under the following conditions.</p> <ol style="list-style-type: none"> 1. MCU repetitively goes from DeepSleep to LP Active with a period of 32 ms. 2. One of the I/Os is toggled using Smart I/O to activate an external sensor connected to an analog input of A/D in DeepSleep 3. After 200 μs delay, the CM7_0 wakes up by Event generator trigger to LP Active mode with IMO and A/D conversion is triggered by software. 4. Group A/D conversion is performed on 5 channels with the sampling time of 1 μs each. 5. Once the group A/D conversion is finished, and the results fit in the window of the range comparator, the I/O is toggled back by software to de-activate the sensor and the CM7_0 goes back to DeepSleep. |
| DeepSleep Mode | | | | | | | |
| SID64A | I _{DD_DS64A} | 64-KB SRAM retention, ILO0 operation | – | 50 | 176 | μA | <p>DeepSleep Mode (RTC, WDT, and event generator operating, all other peripherals are off except for retention registers), CM0+, CM7_0: Retained</p> <p>$T_A = 25\text{ }^{\circ}\text{C}$</p> <p>Typ: $V_{DD} = 5.0\text{ V}$, process typ (TT)</p> <p>Max: $V_{DD} = 5.5\text{ V}$, process worst (FF)</p> |
| SID64C | I _{DD_DS64C} | 64 KB SRAM retention, ILO0 operation | – | 1.4 | 5.5 | mA | <p>DeepSleep Mode steady state at $T_A = 125\text{ }^{\circ}\text{C}$ (RTC, WDT, and event generator operating, all other peripherals are off except for retention registers), CM0+, CM7_0: Retained</p> <p>Typ: $V_{DD} = 5.0\text{ V}$ process worst (TT)</p> <p>Max: $V_{DD} = 5.5\text{ V}$ process worst (FF)</p> |
| Hibernate Mode | | | | | | | |

Table 25-4. DC Specifications, CPU Current, and Transition Time Specifications (continued)

 All specifications are valid for $-40\text{ }^{\circ}\text{C} \leq T_A \leq 125\text{ }^{\circ}\text{C}$ and for 2.7 V to 5.5 V except where noted.

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|------------------------------------|--------------------------|---|-----|-----|------|-------|---|
| SID66 | I _{DD_HIB1} | Hibernate Mode | – | 8 | – | μA | T _A = 25 °C, V _{DDD} = 5.0 V, Process typ (TT) |
| SID66A | I _{DD_HIB2} | Hibernate Mode | – | – | 248 | μA | T _A = 125 °C, V _{DDD} = 5.5 V, Process worst (FF) |
| Power Mode Transition Times | | | | | | | |
| SID69 | t _{ACT_DS} | Power down time from Active to DeepSleep | – | – | 2.5 | μs | When the IMO is already running and all HFCLK roots are at least 8 MHz. HFCLK roots that are slower than this will require additional time to turn off. |
| SID67 | t _{DS_ACT} | DeepSleep to Active transition time (IMO clock) | – | – | 10 | μs | When using the 8-MHz IMO. Measured from wakeup interrupt during DeepSleep until wakeup. |
| SID67C | t _{DS_ACT1} | DeepSleep to Active transition time (IMO clock, flash execution) | – | – | 26 | μs | When using the 8-MHz IMO. Measured from wakeup interrupt during DeepSleep until flash execution. |
| SID67A | t _{DS_ACT_FLL} | DeepSleep to Active transition time (FLL clock) | – | – | 15 | μs | When using the FLL to generate 96 MHz from the 8-MHz IMO. Measured from wakeup interrupt during DeepSleep until the FLL locks. |
| SID67D | t _{DS_ACT_FLL1} | DeepSleep to Active transition time (FLL clock, flash execution) | – | – | 26 | μs | When using the FLL to generate 96 MHz from the 8-MHz IMO. Measured from wakeup interrupt during DeepSleep until flash execution. |
| SID67B | t _{DS_ACT_PLL} | DeepSleep to Active transition time (PLL clock) | – | – | 60 | μs | When using the PLL to generate 96 MHz from the 8-MHz IMO. Measured from wakeup interrupt during DeepSleep until the PLL locks. |
| SID68 | t _{HVR_ACT} | Release time from HV reset (POR, BOD, OVD, OCD, WDT, Hibernate wakeup, or XRES_L) release until CM0+ begins executing ROM boot | – | – | 265 | μs | Without boot runtime, guaranteed by design |
| SID68A | t _{LVR_ACT} | Release time from LV reset (Fault, Internal system reset, MCWDT, or CSV) during Active/Sleep until CM0+ begins executing ROM boot | – | – | 10 | μs | Without boot runtime. Guaranteed by design |
| SID68B | t _{LVR_DS} | Release time from LV reset (Fault, or MCWDT) during DeepSleep until CM0+ begins executing ROM boot | – | – | 15 | μs | Without boot runtime. Guaranteed by design |
| SID80A | t _{RB_N} | ROM boot startup time or wakeup time from hibernate in NORMAL protection state | – | – | 1300 | μs | Guaranteed by Design, CM0+ clocked at 100 MHz |
| SID80B | t _{RB_S} | ROM boot startup time or wakeup time from hibernate in SECURE protection state | – | – | 2150 | μs | Guaranteed by Design, TOC2_FLAGS = 0x2CF, CM0+ clocked at 100 MHz |
| SID81A | t _{FB} | Flash boot startup time or wakeup time from hibernate in NORMAL/SECURE protection state | – | – | 80 | μs | Guaranteed by Design, TOC2_FLAGS = 0x2CF, CM0+ clocked at 100 MHz, Listen window = 0 ms |

Table 25-4. DC Specifications, CPU Current, and Transition Time Specifications (continued)

 All specifications are valid for $-40\text{ }^{\circ}\text{C} \leq T_A \leq 125\text{ }^{\circ}\text{C}$ and for 2.7 V to 5.5 V except where noted.

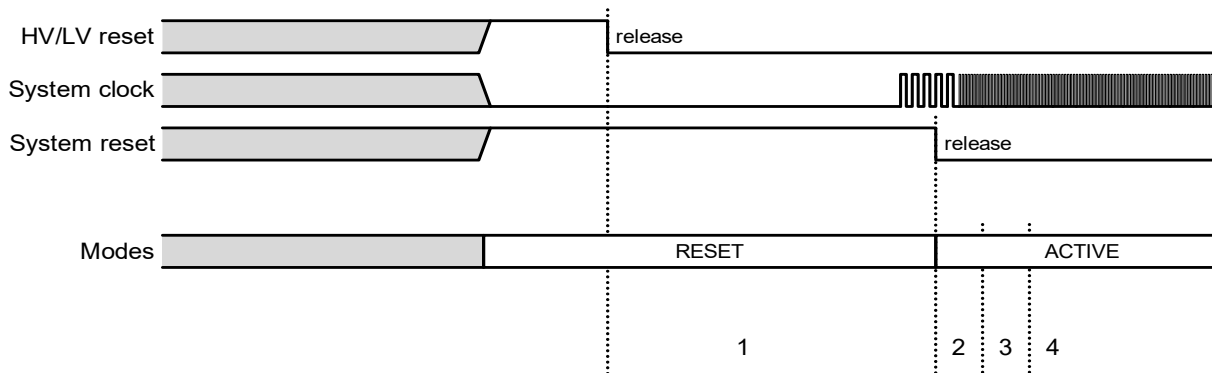
| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------------------------------|------------------|---|-----------------------|-----|----------------------|---------------|---|
| SID81B | t_{FB_A} | Flash boot with app authentication time in NORMAL/SECURE protection state | – | – | 4070 | μs | Guaranteed by Design, TOC2_FLAGS = 0x2CF, CM0+ clocked at 100 MHz, Listen window = 0 ms, App size is 64 KB with the last 256 bytes being a digital signature in RSASSA-PKCS1-v1.5 |
| Regulator Specifications | | | | | | | |
| SID600 | V_{CCD} | Core supply voltage | 1.05 | 1.1 | 1.15 | V | Static variation: $\pm 25\text{ mV}$ Static + Transient variation: $\pm 50\text{ mV}$ |
| SID601 | I_{DDD_ACT} | Regulator operating current in Active/Sleep mode | – | 900 | 1500 | μA | Guaranteed by design |
| SID602 | I_{DDD_DPSLP} | Regulator operating current in DeepSleep mode | – | 1.5 | 20 | μA | Guaranteed by design |
| SID603 | I_{RUSH} | In-rush current | – | – | 850 | mA | Average V_{DDD} current until C_{s1} (connected to V_{CCD} pin) is charged after Active regulator is turned on |
| SID604 | I_{ILDOUT} | Internal regulator output current for operation | – | – | 300 | mA | |
| SID605 | I_{HCR0UT} | High current regulator output current for operation | – | – | 600 | mA | Using an external pass transistor |
| SID606 | V_{OL_HCR} | Output voltage LOW level for external PMIC enable output (EXT_PS_CTL1) | – | – | 0.5 | V | $I_{OL} = 1\text{ mA}$ |
| SID606A | V_{OH_HCR} | Output voltage HIGH level for external PMIC enable output (EXT_PS_CTL1) | $V_{DDD} - 0.5$ | – | – | V | $I_{OH} = -1\text{ mA}$ |
| SID607 | V_{IH_HCR} | Input voltage HIGH threshold for external PMIC power OK input (EXT_PS_CTL0) | $0.7 \times V_{DDD}$ | – | – | V | |
| SID607A | V_{IL_HCR} | Input voltage LOW threshold for external PMIC power OK input (EXT_PS_CTL0) | – | – | $0.3 \times V_{DDD}$ | V | |
| SID607B | V_{HYS_HCR} | Hysteresis for external PMIC power OK input (EXT_PS_CTL0) | $0.05 \times V_{DDD}$ | – | – | V | |
| SID608 | I_{DRV_VOUT} | DRV_VOUT pin output current to external NPN base current | – | – | 9 | mA | See Architecture TRM for external NPN transistor selection |

25.5 Reset Specifications

Table 25-5. XRES_L Reset

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------------------------------|-----------------------|---|-------------------------|-----|------------------------|-------|---|
| XRES_L DC Specifications | | | | | | | |
| SID73 | I _{IDD_XRES} | I _{DD} when XRES_L asserted | – | – | 2.5 | mA | MAX: T _A = 125 °C, V _{DDD} = 5.5 V, V _{CCD} = 1.15 V, process worst (FF) |
| SID74 | V _{IH} | Input voltage HIGH threshold | 0.7 × V _{DDD} | – | – | V | CMOS Input |
| SID75 | V _{IL} | Input voltage LOW threshold | – | – | 0.3 × V _{DDD} | V | CMOS Input |
| SID76 | R _{PULLUP} | Pull-up resistor | 7 | – | 20 | kΩ | |
| SID77 | C _{IN} | Input capacitance | – | – | 5 | pF | |
| SID78 | V _{HYSXRES} | Input voltage hysteresis | 0.05 × V _{DDD} | – | – | V | |
| XRES_L AC Specifications | | | | | | | |
| SID70 | t _{XRES_ACT} | XRES_L deasserted to Active transition time | – | – | 265 | μs | Without boot runtime, guaranteed by design |
| SID71 | t _{XRES_PW} | XRES_L pulse width | 5 | – | – | μs | |
| SID72 | t _{XRES_FT} | Pulse suppression width | 100 | – | – | ns | |

Figure 25-3.Reset Sequence



- | | |
|----|---|
| 1: | SID68/68A/68B: Time from HV/LV reset release until CM 0+ begins executing ROM boot |
| 2: | SID80A/80B: ROM boot code operation |
| 3: | SID81A/81B: Flash boot code operation |
| 4: | User code operation |

25.6 I/O
Table 25-6. I/O Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|-------------------------------|---|--|-----|-----|-------|---|
| GPIO_STD Specifications for ports P1 through P23, P28 to P32 | | | | | | | |
| SID650 | V _{OL1_GPIO_STD} | Output voltage LOW level | – | – | 0.6 | V | I _{OL} = 6 mA drive_sel<1:0> = 0b0X, 4.5 V ≤ V _{DD} or V _{DDIO_1} or V _{DDIO_2} ≤ 5.5 V |
| SID650C | V _{OL1C_GPIO_STD} | Output voltage LOW level | – | – | 0.4 | V | I _{OL} = 5 mA drive_sel<1:0> = 0b0X, 4.5 V ≤ V _{DD} or V _{DDIO_1} or V _{DDIO_2} ≤ 5.5 V |
| SID651 | V _{OL2_GPIO_STD} | Output voltage LOW level | – | – | 0.4 | V | I _{OL} = 2 mA drive_sel<1:0> = 0b0X, 2.7 V ≤ V _{DD} or V _{DDIO_1} or V _{DDIO_2} < 4.5 V |
| SID652 | V _{OL3_GPIO_STD} | Output voltage LOW level | – | – | 0.4 | V | I _{OL} = 1 mA drive_sel<1:0> = 0b10, 2.7 V ≤ V _{DD} or V _{DDIO_1} or V _{DDIO_2} < 4.5 V |
| SID652C | V _{OL3C_GPIO_STD} | Output voltage LOW level | – | – | 0.4 | V | I _{OL} = 2 mA drive_sel<1:0> = 0b10, 4.5 V ≤ V _{DD} or V _{DDIO_1} or V _{DDIO_2} ≤ 5.5 V |
| SID653 | V _{OL4_GPIO_STD} | Output voltage LOW level | – | – | 0.4 | V | I _{OL} = 0.5 mA drive_sel<1:0> = 0b11, 2.7 V ≤ V _{DD} or V _{DDIO_1} or V _{DDIO_2} < 4.5 V |
| SID653C | V _{OL4C_GPIO_STD} | Output voltage LOW level | – | – | 0.4 | V | I _{OL} = 1 mA drive_sel<1:0> = 0b11, 4.5 V ≤ V _{DD} or V _{DDIO_1} or V _{DDIO_2} ≤ 5.5 V |
| SID654 | V _{OH1_GPIO_STD} | Output voltage HIGH level | (V _{DD} , V _{DDIO_1} , or V _{DDIO_2}) – 0.5 | – | – | V | I _{OH} = –2 mA drive_sel<1:0> = 0b0X, 2.7 V ≤ V _{DD} or V _{DDIO_1} or V _{DDIO_2} < 4.5 V |
| SID655 | V _{OH2_GPIO_STD} | Output voltage HIGH level | (V _{DD} , V _{DDIO_1} , or V _{DDIO_2}) – 0.5 | – | – | V | I _{OH} = –5 mA drive_sel<1:0> = 0b0X, 4.5 V ≤ V _{DD} or V _{DDIO_1} or V _{DDIO_2} ≤ 5.5 V |
| SID656 | V _{OH3_GPIO_STD} | Output voltage HIGH level | (V _{DD} , V _{DDIO_1} , or V _{DDIO_2}) – 0.5 | – | – | V | I _{OH} = –1 mA drive_sel<1:0> = 0b10, 2.7 V ≤ (V _{DD} , V _{DDIO_1} , or V _{DDIO_2}) < 4.5 V |
| SID656C | V _{OH3C_GPIO_STD} | Output voltage HIGH level | (V _{DD} , V _{DDIO_1} , or V _{DDIO_2}) – 0.5 | – | – | V | I _{OH} = –2 mA drive_sel<1:0> = 0b10, 4.5 V ≤ (V _{DD} , V _{DDIO_1} , or V _{DDIO_2}) ≤ 5.5 V |
| SID657 | V _{OH4_GPIO_STD} | Output voltage HIGH level | (V _{DD} , V _{DDIO_1} , or V _{DDIO_2}) – 0.5 | – | – | V | I _{OH} = –0.5 mA drive_sel<1:0> = 0b11, 2.7 V ≤ (V _{DD} , V _{DDIO_1} , or V _{DDIO_2}) < 4.5 V |
| SID657C | V _{OH4C_GPIO_STD} | Output voltage HIGH level | (V _{DD} , V _{DDIO_1} , or V _{DDIO_2}) – 0.5 | – | – | V | I _{OH} = –1 mA drive_sel<1:0> = 0b11, 4.5 V ≤ (V _{DD} , V _{DDIO_1} , or V _{DDIO_2}) ≤ 5.5 V |
| SID658 | R _{PD_GPIO_STD} | Pull-down resistance | 25 | 50 | 100 | kΩ | |
| SID659 | R _{PU_GPIO_STD} | Pull-up resistance | 25 | 50 | 100 | kΩ | |
| SID660 | V _{IH_CMOS_GPIO_STD} | Input voltage HIGH threshold in CMOS mode | 0.7 × (V _{DD} , V _{DDIO_1} , or V _{DDIO_2}) | – | – | V | |

Table 25-6. I/O Specifications (continued)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|--|---|---|------|--|-------|---|
| SID661 | V _{IH_TTL_GPIO_STD} | Input voltage HIGH threshold in TTL mode | 2.0 | – | – | V | |
| SID662 | V _{IH_AUTO_GPIO_STD} | Input voltage HIGH threshold in AUTO mode | 0.8 × (V _{DDD} , V _{DDIO_1} , or V _{DDIO_2}) | – | – | V | |
| SID663 | V _{IL_CMOS_GPIO_STD} | Input voltage LOW threshold in CMOS mode | – | – | 0.3 × (V _{DDD} , V _{DDIO_1} , or V _{DDIO_2}) | V | |
| SID664 | V _{IL_TTL_GPIO_STD} | Input voltage LOW threshold in TTL mode | – | – | 0.8 | V | |
| SID665 | V _{IL_AUTO_GPIO_STD} | Input voltage LOW threshold in AUTO mode | – | – | 0.5 × (V _{DDD} , V _{DDIO_1} , or V _{DDIO_2}) | V | |
| SID666 | V _{HYST_CMOS_GPIO_STD} | Hysteresis in CMOS mode | 0.05 × (V _{DDD} , V _{DDIO_1} , or V _{DDIO_2}) | – | – | V | |
| SID668 | V _{HYST_AUTO_GPIO_STD} | Hysteresis in AUTO mode | 0.05 × (V _{DDD} , V _{DDIO_1} , or V _{DDIO_2}) | – | – | V | |
| SID669 | C _{in_GPIO_STD} | Input pin capacitance | – | – | 5 | pF | For 10 MHz and 100 MHz |
| SID670 | I _{IL_GPIO_STD} | Input leakage current | –250 | 0.02 | 250 | nA | For GPIO_STD except P21.0, P21.1, P21.2, P21.3, P21.4, P22.1, P22.2, P22.3, P23.3, P23.4. V _{DDIO_1} = V _{DDIO_2} = V _{DDD} = V _{DDA} = 5.5 V, V _{SSD} < V _I < V _{DDD} , V _{DDIO_1} , V _{DDIO_2} –40 °C ≤ T _A ≤ 125 °C Typ: T _A = 25 °C, V _{DDIO_1} = V _{DDIO_2} = V _{DDD} = V _{DDA} = 5.0 V |
| SID670C | I _{IL_GPIO_STD_B} | Input leakage current | –700 | 0.02 | 700 | nA | Only for P21.0, P21.1, P21.2, P21.3, P21.4, P22.1, P22.2, P22.3, P23.3, P23.4. V _{DDIO_1} = V _{DDIO_2} = V _{DDD} = V _{DDA} = 5.5 V, V _{SSD} < V _I < V _{DDD} , V _{DDIO_1} , V _{DDIO_2} –40 °C ≤ T _A ≤ 125 °C Typ: T _A = 25 °C, V _{DDIO_1} = V _{DDIO_2} = V _{DDD} = V _{DDA} = 5.0 V |
| SID671 | t _R or t _F (fast) _{20_0_GPIO_STD} | Rise time or fall time (10% to 90% of V _{DDIO}) | 1 | – | 10 | ns | 20-pF load, drive_sel<1:0> = 0b00 |
| SID672 | t _R or t _F (fast) _{50_0_GPIO_STD} | Rise time or fall time (10% to 90% of V _{DDIO}) | 1 | – | 20 | ns | 50-pF load, drive_sel<1:0> = 0b00 |
| SID673 | t _R or t _F (fast) _{20_1_GPIO_STD} | Rise time or fall time (10% to 90% of V _{DDIO}) | 1 | – | 20 | ns | 20-pF load, drive_sel<1:0> = 0b01 |
| SID674 | t _R or t _F (fast) _{10_2_GPIO_STD} | Rise time or fall time (10% to 90% of V _{DDIO}) | 1 | – | 20 | ns | 10-pF load, drive_sel<1:0> = 0b10 |

Table 25-6. I/O Specifications (continued)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------------------------------------|---|--|------|-----|-----|-------|---|
| SID675 | t_R or t_F (fast) _{6_3_GPIO_STD} | Rise time or fall time (10% to 90% of V_{DDIO}) | 1 | – | 20 | ns | 6-pF load, drive_sel<1:0> = 0b11 |
| SID676 | t_F (fast) _{100_GPIO_STD} | Fall time (30% to 70% of V_{DDIO}) | 0.35 | – | 250 | ns | 10-pF to 400-pF load, RPU = 767 Ω , drive_sel<1:0> = 0b00, Freq = 100 kHz |
| SID677 | t_F (fast) _{400_GPIO_STD} | Fall time (30% to 70% of V_{DDIO}) | 0.35 | – | 250 | ns | 10-pF to 400-pF load, RPU = 350 Ω , drive_sel<1:0> = 0b00, Freq = 400 kHz |
| SID678 | $f_{IN_GPIO_STD}$ | Input frequency | – | – | 100 | MHz | |
| SID679 | $f_{OUT_GPIO_STD0H}$ | Output frequency | – | – | 50 | MHz | 20 pF load, drive_sel<1:0> = 00, $4.5\text{ V} \leq V_{DDDD}$ or V_{DDIO_1} or $V_{DDIO_2} \leq 5.5\text{ V}$ |
| SID680 | $f_{OUT_GPIO_STD0L}$ | Output frequency | – | – | 32 | MHz | 20 pF load, drive_sel<1:0> = 00, $2.7\text{ V} \leq V_{DDDD}$ or V_{DDIO_1} or $V_{DDIO_2} < 4.5\text{ V}$ |
| SID681 | $f_{OUT_GPIO_STD1H}$ | Output frequency | – | – | 25 | MHz | 20 pF load, drive_sel<1:0> = 01, $4.5\text{ V} \leq V_{DDDD}$ or V_{DDIO_1} or $V_{DDIO_2} \leq 5.5\text{ V}$ |
| SID682 | $f_{OUT_GPIO_STD1L}$ | Output frequency | – | – | 15 | MHz | 20 pF load, drive_sel<1:0> = 01, $2.7\text{ V} \leq V_{DDDD}$ or V_{DDIO_1} or $V_{DDIO_2} < 4.5\text{ V}$ |
| SID683 | $f_{OUT_GPIO_STD2H}$ | Output frequency | – | – | 25 | MHz | 10 pF load, drive_sel<1:0> = 10, $4.5\text{ V} \leq V_{DDDD}$ or V_{DDIO_1} or $V_{DDIO_2} \leq 5.5\text{ V}$ |
| SID684 | $f_{OUT_GPIO_STD2L}$ | Output frequency | – | – | 15 | MHz | 10 pF load, drive_sel<1:0> = 10, $2.7\text{ V} \leq V_{DDDD}$ or V_{DDIO_1} or $V_{DDIO_2} < 4.5\text{ V}$ |
| SID685 | $f_{OUT_GPIO_STD3H}$ | Output frequency | – | – | 15 | MHz | 6 pF load, drive_sel<1:0> = 11, $4.5\text{ V} \leq V_{DDDD}$ or V_{DDIO_1} or $V_{DDIO_2} \leq 5.5\text{ V}$ |
| SID686 | $f_{OUT_GPIO_STD3L}$ | Output frequency | – | – | 10 | MHz | 6 pF load, drive_sel<1:0> = 11, $2.7\text{ V} \leq V_{DDDD}$ or V_{DDIO_1} or $V_{DDIO_2} < 4.5\text{ V}$ |
| GPIO_ENH Specifications for P0 | | | | | | | |
| SID650A | $V_{OL1_GPIO_ENH}$ | Output voltage LOW level | – | – | 0.6 | V | $I_{OL} = 6\text{ mA}$, drive_sel<1:0> = 0b0X, $2.7\text{ V} \leq V_{DDDD} \leq 5.5\text{ V}$ |
| SID650D | $V_{OL1D_GPIO_ENH}$ | Output voltage LOW level | – | – | 0.4 | V | $I_{OL} = 5\text{ mA}$, drive_sel<1:0> = 0b0X, $4.5\text{ V} \leq V_{DDDD} \leq 5.5\text{ V}$ |
| SID651A | $V_{OL2_GPIO_ENH}$ | Output voltage LOW level | – | – | 0.4 | V | $I_{OL} = 2\text{ mA}$, drive_sel<1:0> = 0b0X, $2.7\text{ V} \leq V_{DDDD} < 4.5\text{ V}$ |
| SID652A | $V_{OL3_GPIO_ENH}$ | Output voltage LOW level | – | – | 0.4 | V | $I_{OL} = 1\text{ mA}$, drive_sel<1:0> = 0b10, $2.7\text{ V} \leq V_{DDDD} < 4.5\text{ V}$ |

Table 25-6. I/O Specifications (continued)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|--|---|-------------------------|-------|------------------------|-------|---|
| SID652D | V _{OL3D_GPIO_ENH} | Output voltage LOW level | – | – | 0.4 | V | I _{OL} = 2 mA drive_sel<1:0> = 0b10, 4.5 V ≤ V _{DDD} ≤ 5.5 V |
| SID653A | V _{OL4_GPIO_ENH} | Output voltage LOW level | – | – | 0.4 | V | I _{OL} = 0.5 mA drive_sel<1:0> = 0b11, 2.7 V ≤ V _{DDD} < 4.5 V |
| SID653D | V _{OL4D_GPIO_ENH} | Output voltage LOW level | – | – | 0.4 | V | I _{OL} = 1 mA drive_sel<1:0> = 0b11, 4.5 V ≤ V _{DDD} ≤ 5.5 V |
| SID654A | V _{OH1_GPIO_ENH} | Output voltage HIGH level | V _{DDD} – 0.5 | – | – | V | I _{OH} = –2 mA drive_sel<1:0> = 0b0X, 2.7 V ≤ V _{DDD} < 4.5 V |
| SID655A | V _{OH2_GPIO_ENH} | Output voltage HIGH level | V _{DDD} – 0.5 | – | – | V | I _{OH} = –5 mA drive_sel<1:0> = 0b0X, 4.5 V ≤ V _{DDD} ≤ 5.5 V |
| SID656A | V _{OH3_GPIO_ENH} | Output voltage HIGH level | V _{DDD} – 0.5 | – | – | V | I _{OH} = –1 mA drive_sel<1:0> = 0b10, 2.7 V ≤ V _{DDD} < 4.5 V |
| SID656D | V _{OH3D_GPIO_ENH} | Output voltage HIGH level | V _{DDD} – 0.5 | – | – | V | I _{OH} = –2 mA drive_sel<1:0> = 0b10, 4.5 V ≤ V _{DDD} ≤ 5.5 V |
| SID657A | V _{OH4_GPIO_ENH} | Output voltage HIGH level | V _{DDD} – 0.5 | – | – | V | I _{OH} = –0.5 mA drive_sel<1:0> = 0b11, 2.7 V ≤ V _{DDD} < 4.5 V |
| SID657D | V _{OH4D_GPIO_ENH} | Output voltage HIGH level | V _{DDD} – 0.5 | – | – | V | I _{OH} = –1 mA drive_sel<1:0> = 0b11, 4.5 V ≤ V _{DDD} ≤ 5.5 V |
| SID658A | R _{PD_GPIO_ENH} | Pull-down resistance | 25 | 50 | 100 | kΩ | |
| SID659A | R _{PU_GPIO_ENH} | Pull-up resistance | 25 | 50 | 100 | kΩ | |
| SID660A | V _{IH_CMOS_GPIO_ENH} | Input voltage HIGH threshold in CMOS mode | 0.7 × V _{DDD} | – | – | V | |
| SID661A | V _{IH_TTL_GPIO_ENH} | Input voltage HIGH threshold in TTL mode | 2.0 | – | – | V | |
| SID662A | V _{IH_AUTO_GPIO_ENH} | Input voltage HIGH threshold in AUTO mode | 0.8 × V _{DDD} | – | – | V | |
| SID663A | V _{IL_CMOS_GPIO_ENH} | Input voltage LOW threshold in CMOS mode | – | – | 0.3 × V _{DDD} | V | |
| SID664A | V _{IL_TTL_GPIO_ENH} | Input voltage LOW threshold in TTL mode | – | – | 0.8 | V | |
| SID665A | V _{IL_AUTO_GPIO_ENH} | Input voltage LOW threshold in AUTO mode | – | – | 0.5 × V _{DDD} | V | |
| SID666A | V _{HYST_CMOS_GPIO_ENH} | Hysteresis in CMOS mode | 0.05 × V _{DDD} | – | – | V | |
| SID668A | V _{HYST_AUTO_GPIO_ENH} | Hysteresis in AUTO mode | 0.05 × V _{DDD} | – | – | V | |
| SID669A | C _{in_GPIO_ENH} | Input pin capacitance | – | – | 5 | pF | For 10 MHz and 100 MHz |
| SID670A | I _{IL_GPIO_ENH} | Input leakage current | –350 | 0.055 | 350 | nA | V _{DDD} = V _{DDA} = 5.5 V, V _{SSD} < V _I < V _{DDD} –40 °C ≤ T _A ≤ 125 °C Typ: T _A = 25 °C, V _{DDD} = V _{DDA} = 5.0 V |
| SID671A | t _R or t _F (fast) _{_20_0_GPIO_ENH} | Rise time or fall time (10% to 90% of V _{DDIO}) | 1 | – | 10 | ns | 20 pF load, drive_sel<1:0> = 0b00, slow = 0 |
| SID672A | t _R or t _F (fast) _{_50_0_GPIO_ENH} | Rise time or fall time (10% to 90% of V _{DDIO}) | 1 | – | 20 | ns | 50 pF load, drive_sel<1:0> = 0b00, slow = 0 |

Table 25-6. I/O Specifications (continued)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|--|--|--|-----------------------------|-----|------------------------------|-------|--|
| SID673A | t_R or t_F (fast)_20_1_GPIO_ENH | Rise time or fall time (10% to 90% of V_{DDIO}) | 1 | – | 20 | ns | 20-pF load, drive_sel<1:0> = 0b01, slow = 0 |
| SID674A | t_R or t_F (fast)_10_2_GPIO_ENH | Rise time or fall time (10% to 90% of V_{DDIO}) | 1 | – | 20 | ns | 10-pF load, drive_sel<1:0> = 0b10, slow = 0 |
| SID675A | t_R or t_F (fast)_6_3_GPIO_ENH | Rise time or fall time (10% to 90% of V_{DDIO}) | 1 | – | 20 | ns | 6-pF load, drive_sel<1:0> = 0b11, slow = 0 |
| SID676A | t_F I2C (slow)_GPIO_ENH | Fall time (30% to 70% of V_{DDIO}) | $20 \times (V_{DDD} / 5.5)$ | – | 250 | ns | 10-pF to 400-pF load, drive_sel<1:0> = 0b00, slow = 1, minimum $R_{PU} = 400 \Omega$ |
| SID677A | t_R or t_F (slow)_20_GPIO_ENH | Rise time or fall time (10% to 90% of V_{DDIO}) | $20 \times (V_{DDD} / 5.5)$ | – | 160 | ns | 20-pF load, drive_sel<1:0> = 0b00, slow = 1, output frequency = 1 MHz |
| SID678A | t_R or t_F (slow)_400_GPIO_ENH | Rise time or fall time (10% to 90% of V_{DDIO}) | $20 \times (V_{DDD} / 5.5)$ | – | 250 | ns | 400-pF load, drive_sel<1:0> = 0b00, slow = 1, output frequency = 400 kHz |
| SID679A | $f_{IN_GPIO_ENH}$ | Input frequency | – | – | 100 | MHz | |
| SID680A | $f_{OUT_GPIO_ENH0H}$ | Output frequency | – | – | 50 | MHz | 20 pF load, drive_sel<1:0> = 0b00, $4.5 V \leq V_{DDD} \leq 5.5 V$ |
| SID681A | $f_{OUT_GPIO_ENH0L}$ | Output frequency | – | – | 32 | MHz | 20 pF load, drive_sel<1:0> = 0b00, $2.7 V \leq V_{DDD} < 4.5 V$ |
| SID682A | $f_{OUT_GPIO_ENH1H}$ | Output frequency | – | – | 25 | MHz | 20 pF load, drive_sel<1:0> = 0b01, $4.5 V \leq V_{DDD} \leq 5.5 V$ |
| SID683A | $f_{OUT_GPIO_ENH1L}$ | Output frequency | – | – | 15 | MHz | 20 pF load, drive_sel<1:0> = 0b01, $2.7 V \leq V_{DDD} < 4.5 V$ |
| SID684A | $f_{OUT_GPIO_ENH2H}$ | Output frequency | – | – | 25 | MHz | 10 pF load, drive_sel<1:0> = 0b10, $4.5 V \leq V_{DDD} \leq 5.5 V$ |
| SID685A | $f_{OUT_GPIO_ENH2L}$ | Output frequency | – | – | 15 | MHz | 10 pF load, drive_sel<1:0> = 0b10, $2.7 V \leq V_{DDD} < 4.5 V$ |
| SID686A | $f_{OUT_GPIO_ENH3H}$ | Output frequency | – | – | 15 | MHz | 6 pF load, drive_sel<1:0> = 0b11, $4.5 V \leq V_{DDD} \leq 5.5 V$ |
| SID687A | $f_{OUT_GPIO_ENH3L}$ | Output frequency | – | – | 10 | MHz | 6 pF load, drive_sel<1:0> = 0b11, $2.7 V \leq V_{DDD} < 4.5 V$ |
| HSIO Specifications for ports P24 through P27, P33, P34 | | | | | | | |
| SID650B | V_{OL_GMII} | Output LOW voltage | – | – | 0.6 | V | $I_{OL} = 4 \text{ mA}$, drive_sel<1:0> = 0b00 |
| SID651B | $V_{OL_HB_HSSPI}$ | Output LOW voltage | – | – | 0.2 | V | $I_{OL} = 0.1 \text{ mA}$, drive_sel<1:0> = 0b00 |
| SID652B | V_{OL_eMMC} | Output LOW voltage | – | – | $0.125 \times V_{DDIO_3/4}$ | V | $I_{OL} = 0.1 \text{ mA}$, drive_sel<1:0> = 0b00 |
| SID653B | V_{OL_SD} | Output LOW voltage | – | – | $0.125 \times V_{DDIO_3/4}$ | V | $I_{OL} = 2 \text{ mA}$, drive_sel<1:0> = 0b00 |

Table 25-6. I/O Specifications (continued)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|--------------------------|--|---|-----|--------------------------------|-------|--|
| SID654B | V _{OL1} | Output LOW voltage | – | – | 0.4 | V | I _{OL} = 10 mA, drive_sel<1:0> = 0b00, V _{DDIO_3/4} = 2.7 V |
| SID655B | V _{OL2} | Output LOW voltage | – | – | 0.4 | V | I _{OL} = 2 mA, drive_sel<1:0> = 0b01, V _{DDIO_3/4} = 2.7 V |
| SID656B | V _{OL3} | Output LOW voltage | – | – | 0.4 | V | I _{OL} = 1 mA, drive_sel<1:0> = 0b10, V _{DDIO_3/4} = 2.7 V |
| SID656E | V _{OL4} | Output LOW voltage | – | – | 0.4 | V | I _{OL} = 0.5 mA, drive_sel<1:0> = 0b11, V _{DDIO_3/4} = 2.7 V |
| SID657B | V _{OH_GMII} | Output HIGH voltage | V _{DDIO_3/4} – 0.6 | – | – | V | I _{OH} = –4 mA drive_sel<1:0> = 0b00 |
| SID658B | V _{OH_HB_HSSPI} | Output HIGH voltage | V _{DDIO_3/4} – 0.2 | – | – | V | I _{OH} = –0.1 mA drive_sel<1:0> = 0b00 |
| SID659B | V _{OH_eMMC} | Output HIGH voltage | V _{DDIO_3/4} – (0.25 × V _{DDIO_3/4}) | – | – | V | I _{OH} = –0.1 mA drive_sel<1:0> = 0b00 |
| SID660B | V _{OH_SD} | Output HIGH voltage | V _{DDIO_3/4} – (0.25 × V _{DDIO_3/4}) | – | – | V | I _{OH} = –2 mA drive_sel<1:0> = 0b00 |
| SID661B | V _{OH1} | Output HIGH voltage | V _{DDIO_3/4} – 0.5 | – | – | V | I _{OH} = –10 mA drive_sel<1:0> = 0b00, V _{DDIO_3/4} = 2.7 V |
| SID662B | V _{OH2} | Output HIGH voltage | V _{DDIO_3/4} – 0.5 | – | – | V | I _{OH} = –2 mA drive_sel<1:0> = 0b01, V _{DDIO_3/4} = 2.7 V |
| SID663B | V _{OH3} | Output HIGH voltage | V _{DDIO_3/4} – 0.5 | – | – | V | I _{OH} = –1 mA drive_sel<1:0> = 0b10, V _{DDIO_3/4} = 2.7 V |
| SID663E | V _{OH3} | Output HIGH voltage | V _{DDIO_3/4} – 0.5 | – | – | V | I _{OH} = –0.5 mA drive_sel<1:0> = 0b11, V _{DDIO_3/4} = 2.7 V |
| SID664B | R _{PD} | Pull-down resistance | 25 | 50 | 100 | kΩ | |
| SID665B | R _{PU} | Pull-up resistance | 25 | 50 | 100 | kΩ | |
| SID666B | V _{IH_CMOS} | Input HIGH voltage for HyperBus and HSSPI in CMOS mode | 0.7 × V _{DDIO_3/4} | – | – | V | |
| SID667B | V _{IH_RGMII} | Input HIGH voltage for RGMII in CMOS mode | 0.8 × V _{DDIO_3/4} | – | – | V | |
| SID668E | V _{IH_TTL} | Input Voltage HIGH threshold for TTL mode | 2 | – | – | V | |
| SID668B | V _{IH_GMII} | Input HIGH voltage for GMII mode | 1.7 | – | – | V | |
| SID669B | V _{IH_SD_eMMC} | Input HIGH voltage for SD and eMMC in CMOS mode | 0.625 × V _{DDIO_3/4} | – | – | V | |
| SID669E | V _{IH_AUTO} | Input Voltage HIGH threshold in AUTO mode | 0.8 × V _{DDIO_3/4} | – | – | V | |
| SID670B | V _{IL_CMOS} | Input LOW voltage for HyperBus and HSSPI in CMOS mode | – | – | 0.3 × V _{DDIO_3/4} | V | |

Table 25-6. I/O Specifications (continued)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|----------------------------------|------------------------|--|-----------------------------|------|-----------------------------|-------|---|
| SID671B | V_{IL_RGMII} | Input LOW voltage for RGMII in CMOS mode | – | – | $0.2 \times V_{DDIO_3/4}$ | V | |
| SID672E | V_{IL_TTL} | Input Voltage LOW threshold for TTL mode | – | – | 0.8 | V | |
| SID672B | V_{IL_GMII} | Input LOW voltage for GMII mode | – | – | 0.9 | V | |
| SID673B | $V_{IL_SD_eMMC}$ | Input LOW voltage for SD and eMMC in CMOS mode | – | – | $0.25 \times V_{DDIO_3/4}$ | V | |
| SID673E | V_{IL_AUTO} | Input Voltage LOW threshold in AUTO mode | – | – | $0.5 \times V_{DDIO_3/4}$ | V | |
| SID674B | V_{HYST_CMOS} | Hysteresis in CMOS mode | $0.05 \times V_{DDIO_3/4}$ | – | – | V | |
| SID674F | V_{HYST_AUTO} | Hysteresis in AUTO mode | $0.05 \times V_{DDIO_3}$ | – | – | V | |
| SID675B | C_{IN} | Input pin capacitance | – | – | 5 | pF | For 10 MHz and 100 MHz |
| SID676B | I_{IL} | Input leakage current | –450 | 1.02 | 450 | nA | $V_{DDIO_3/4} = 3.6\text{ V}$, $V_{SSIO_3/4} < V_I < V_{DDIO_3/4}$ $-40\text{ }^\circ\text{C} \leq T_A \leq 125\text{ }^\circ\text{C}$ Typ: $T_A = 25\text{ }^\circ\text{C}$, $V_{DDIO_3/4} = 3.3\text{ V}$ |
| SID677B | f_{IN_GMII} | Input frequency | – | – | 125 | MHz | |
| SID678B | f_{IN_RGMII} | Input frequency | – | – | 125 | MHz | |
| SID679B | $f_{IN_HB_HSSPI}$ | Input frequency | – | – | 100 | MHz | |
| SID680B | f_{IN_eMMC} | Input frequency | – | – | 52 | MHz | |
| SID681B | f_{IN_SD} | Input frequency | – | – | 50 | MHz | |
| SID682B | $f_{OUT_GMII_RGMII}$ | Output frequency | – | – | 125 | MHz | |
| SID683B | $f_{OUT_HB_HSSPI}$ | Output frequency | – | – | 100 | MHz | |
| SID684B | f_{OUT_eMMC} | Output frequency | – | – | 52 | MHz | |
| SID685B | f_{OUT_SD} | Output frequency | – | – | 50 | MHz | |
| GPIO Input Specifications | | | | | | | |
| SID98 | t_{FT} | Analog glitch filter (pulse suppression width) | – | – | 50 ^[57] | ns | One filter per port |
| SID99 | t_{INT} | Minimum pulse width for GPIO interrupt | 160 | – | – | ns | |

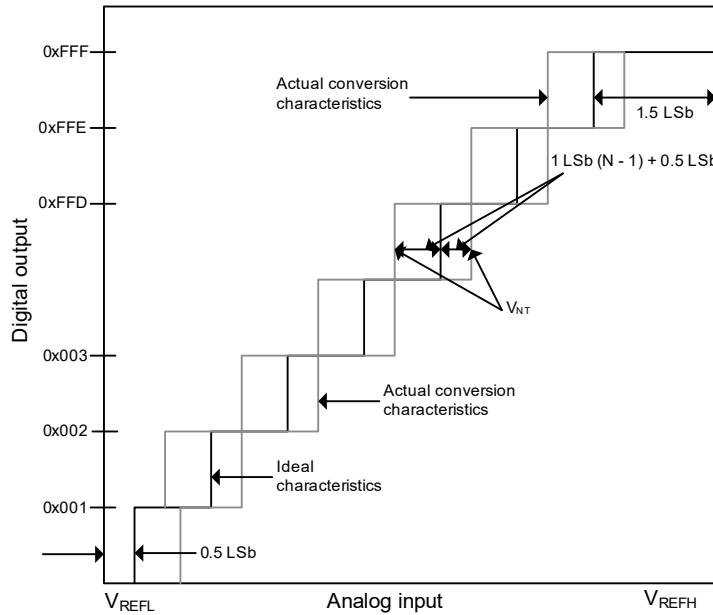
Note

57. If a longer pulse suppression width is necessary, use Smart I/O.

25.7 Analog Peripherals

25.7.1 SAR ADC

Figure 25-4.ADC Characteristics and Error Descriptions



$$\text{Total error of digital output } N = (V_{NT} \{1 \text{ LSb} \times (N - 1) + 0.5 \text{ LSb}\}) / 1 \text{ LSb} \quad [\text{LSb}]$$

$$1 \text{ LSb (Ideal value)} = (V_{REFH} - V_{REFL}) / 4096 \quad [\text{V}]$$

- N: A/D converter digital output value
- V_{ZT} (Ideal value): $V_{REFL} + 0.5 \text{ LSb}$ [V]
- V_{FST} (Ideal value): $V_{REFH} - 1.5 \text{ LSb}$ [V]
- V_{NT} : Voltage at which the digital output changes from $N - 1$ to N

Table 25-7. 12-Bit SAR ADC DC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|------------------------------------|---|-------------------|-----|-------------------|-------|--|
| SID100 | A_RES | SAR ADC resolution | – | – | 12 | bits | |
| SID101 | A_V _{INS} | Input voltage range | V _{REFL} | – | V _{REFH} | V | |
| SID102A | A_V _{DDA} ^[58] | V _{DDA} voltage range | 2.7 | – | 5.5 | V | |
| SID102 | A_V _{REFH} | V _{REFH} voltage range | 2.7 | – | V _{DDA} | V | ADC performance degrades when high reference is higher than supply (V _{DDA}) |
| SID103 | A_V _{REFL} | V _{REFL} voltage range | V _{SSA} | – | V _{SSA} | V | ADC performance degrades when low reference is lower than ground |
| SID103A | V _{band_gap} | Internal band gap reference voltage | 0.882 | 0.9 | 0.918 | V | |
| SID19A | CLAMP_COUPLING_RATIO_POS | Ratio of current collected on a pin to the positive current injected into a neighboring pin | – | – | 0.1 | % | |
| SID19B | CLAMP_COUPLING_RATIO_NEG | Ratio of current collected on a pin to the negative current injected into a neighboring pin | – | – | 1.2 | % | |
| SID19C | R _{CLAMP_INTERNAL} | Internal pin resistance to current collection point | – | – | 50 | Ω | |

25.7.2 Calculating the impact of neighboring Pins

The three ADC specifications based on SID19A, SID19B, and SID19C, can be used to calculate the pin leakage and resulting ADC offset caused by injection current using the below formula:

$$I_{LEAK} = I_{INJECTED} \times CLAMP_COUPLING_RATIO$$

$$V_{ERROR} = I_{LEAK} \times (R_{CLAMP_INTERNAL} + R_{SOURCE})$$

$$Code\ Error = V_{ERROR} \times 2^{12} / V_{REF}$$

Where:

I_{INJECTED} is the injected current in mA.

I_{LEAK} is the calculated leakage current in mA.

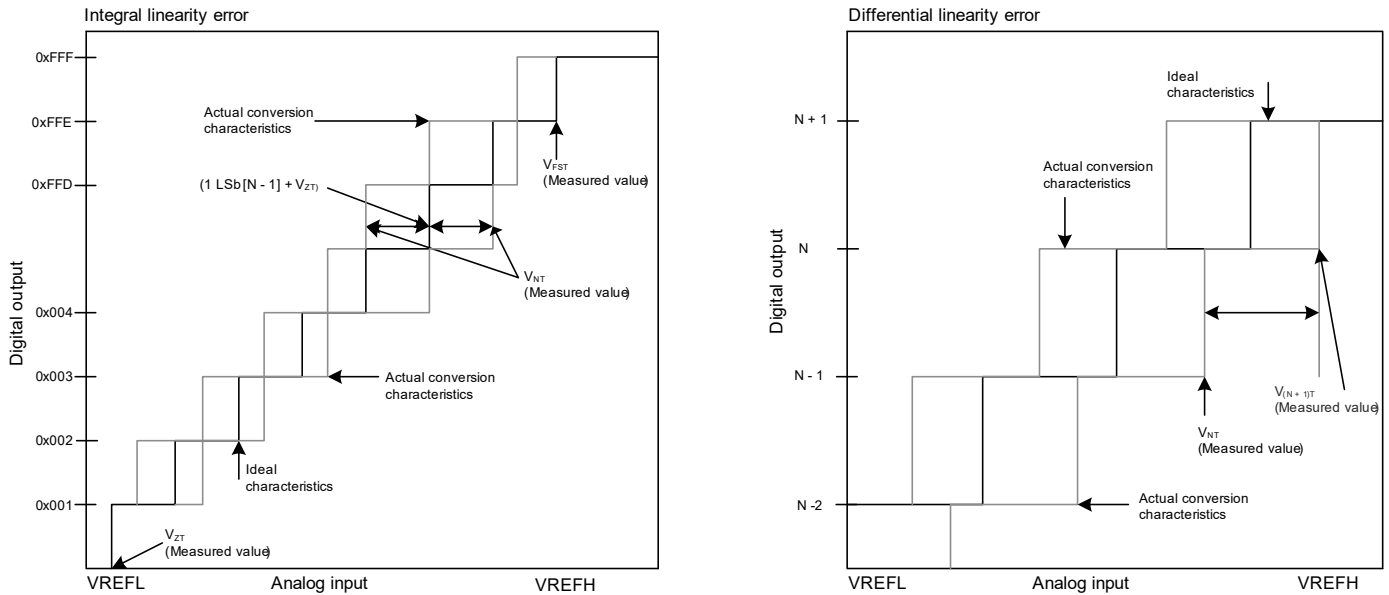
V_{ERROR} is the voltage error calculated due to leakage currents in V.

V_{REF} is the ADC reference voltage in V.

Note

58. V_{DD} must be greater than 0.8 × V_{DDA} when ADC[2] is enabled. V_{DDIO_1} must be greater than 0.8 × V_{DDA} when ADC[0] is enabled.

Figure 25-5. Integral and Differential Linearity Errors



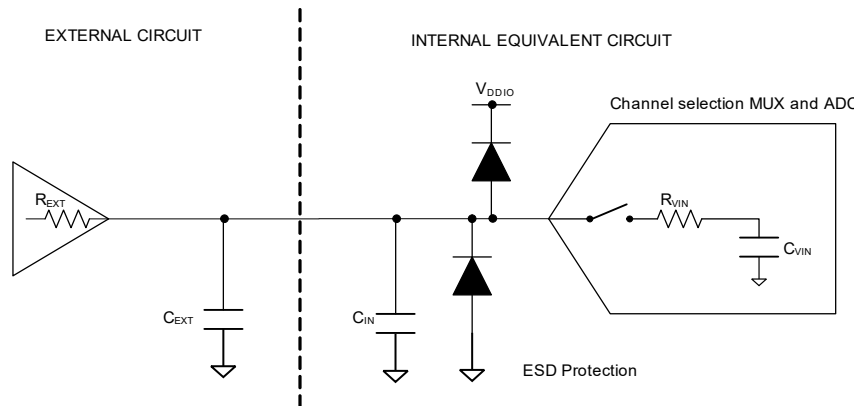
Integral linearity error of digital output N = $(V_{NT} - \{1 \text{LSb} \times (N - 1) + V_{ZT}\}) / 1 \text{LSb}$ [LSb]

Differential linearity error of digital output N = $(V_{(N+1)T} - V_{NT} - 1 \text{LSb}) / 1 \text{LSb}$ [LSb]

1 LSb = $(V_{FST} - V_{ZT}) / 4094$ [V]

V_{ZT}: Voltage for which digital output changes from 0x000 to 0x001
 V_{FST}: Voltage for which digital output changes from 0xFFE to 0xFFF.

Figure 25-6. ADC Equivalent Circuit for Analog Input



R_{EXT}: Source impedance
 C_{EXT}: On-PCB capacitance
 C_{IN}: I/O pad or Input capacitance
 R_{VIN}: ADC equivalent input resistance
 C_{VIN}: ADC equivalent input capacitance
 K: Constant for sampling accuracy $K = \ln(\text{abs}(4096/\text{LSb}_{\text{SAMPLE}}))$

Sampling Time (t_{SAMPLE}) requirement is shown in the following equation
 $t_{\text{SAMPLE}} > K \times \{C_{\text{VIN}} \times (R_{\text{VIN}} + R_{\text{EXT}}) + (C_{\text{IN}} + C_{\text{EXT}}) \times (R_{\text{EXT}})\}$ [seconds]

K = value of 9.0 is recommended to get ±0.5 LSb sampling accuracy at 12-bit (LSb_{SAMPLE} = ±0.5)

Table 25-8. SAR ADC AC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-----------------------|--|-------|-----|-------|-------|---|
| SID104 | V _{ZT} | Zero transition voltage | -20 | - | 20 | mV | V _{DDA} = 2.7 V to 5.5 V, -40 °C ≤ T _A ≤ 125 °C before offset adjustment |
| SID105 | V _{FST} | Full-scale transition voltage | -20 | - | 20 | mV | V _{DDA} = 2.7 V to 5.5 V, -40 °C ≤ T _A ≤ 125 °C before offset adjustment |
| SID114 | f _{ADC_4P5} | ADC operating frequency | 2 | - | 26.67 | MHz | 4.5 V ≤ V _{DDA} ≤ 5.5 V |
| SID114A | f _{ADC_2P7} | ADC operating frequency | 2 | - | 13.34 | MHz | 2.7 V ≤ V _{DDA} ≤ 4.5 V |
| SID113 | t _{S_4P5} | Analog input sample time (4.5 V ≤ V _{DDA}) | 412 | - | - | ns | 4.5 V ≤ V _{DDA} ≤ 5.5 V, guaranteed by design |
| SID113A | t _{S_2P7} | Analog input sample time (2.7 V ≤ V _{DDA}) | 600 | - | - | ns | 2.7 V ≤ V _{DDA} ≤ 4.5 V, guaranteed by design |
| SID113B | t _{S_DR_4P5} | Analog input sample time when input is from diagnostic reference (4.5 V ≤ V _{DDA}) | 2 | - | - | μs | 4.5 V ≤ V _{DDA} ≤ 5.5 V, guaranteed by design |
| SID113C | t _{S_DR_2P7} | Analog input sample time when input is from diagnostic reference (2.7 V ≤ V _{DDA}) | 2.5 | - | - | μs | 2.7 V ≤ V _{DDA} ≤ 4.5 V, guaranteed by design |
| SID106 | t _{ST_4P5} | Max Throughput (samples per second) | - | - | 1 | Msp/s | 4.5 V ≤ V _{DDA} ≤ 5.5 V, 80 MHz / 3 = 26.67 MHz, 11 sampling cycles, 15 conversion cycles |
| SID106A | t _{ST_2P7} | Max Throughput (samples per second) | - | - | 0.5 | Msp/s | 2.7 V ≤ V _{DDA} < 4.5 V 80 MHz / 6 = 13.3 MHz, 11 sampling cycles, 15 conversion cycles |
| SID107 | C _{VIN} | ADC input sampling capacitance | - | - | 4.8 | pF | Guaranteed by design |
| SID108 | R _{VIN1} | Input path ON resistance (4.5 V to 5.5 V) | - | - | 9.4 | kΩ | Guaranteed by design |
| SID108A | R _{VIN2} | Input path ON resistance (2.7 V to 4.5 V) | - | - | 13.9 | kΩ | Guaranteed by design |
| SID108B | R _{DREF1} | Diagnostic path ON resis- tance (4.5 V to 5.5 V) | - | - | 40 | kΩ | Guaranteed by design |
| SID108C | R _{DREF2} | Diagnostic path ON resis- tance (2.7 V to 4.5 V) | - | - | 50 | kΩ | Guaranteed by design |
| SID119 | ACC_RLAD | Diagnostic reference resistor ladder accuracy | -4 | - | 4 | % | |
| SID109 | A _{TE} | Total error | -5 | - | 5 | LSb | V _{DDA} = V _{REFH} = 2.7 V to 5.5 V, V _{REFL} = V _{SSA} -40 °C ≤ T _A ≤ 125 °C Total Error after offset and gain adjustment at 12-bit resolution mode |
| SID109A | A _{TEB} | Total error | -12 | - | 12 | LSb | V _{DDA} = V _{REFH} = 2.7 V to 5.5 V, V _{REFL} = V _{SSA} -40 °C ≤ T _A ≤ 125 °C Total error before offset and gain adjustment at 12 bit resolution mode |
| SID110 | A _{INL} | Integral nonlinearity | -2.5 | - | 2.5 | LSb | V _{DDA} = 2.7 V to 5.5 V, -40 °C ≤ T _A ≤ 125 °C |
| SID111 | A _{DNL} | Differential nonlinearity | -0.99 | - | 1.9 | LSb | V _{DDA} = 2.7 V to 5.5 V, -40 °C ≤ T _A ≤ 125 °C |

Table 25-8. SAR ADC AC Specifications (continued)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|------------------------|---|------|-----|-----|-------|--|
| SID112 | A_CE | Channel to channel variation (for channels connected to same ADC) | -1 | - | 1 | LSb | $V_{DDA} = 2.7\text{ V to } 5.5\text{ V}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ |
| SID115 | I _{AIC} | Analog input leakage current | -350 | 70 | 350 | nA | When input pad is selected for conversion |
| SID116 | I _{DIAGREF} | Diagnostic reference current | - | - | 70 | μA | |
| SID117 | I _{VDDA} | Analog power supply current while ADC is operating | - | 360 | 550 | μA | Per enabled ADC |
| SID117A | I _{VDDA_DS} | Analog power supply current while ADC is not operating | - | 1 | 21 | μA | Per enabled ADC |
| SID118 | I _{VREF} | Analog reference voltage current while ADC is operating | - | 360 | 550 | μA | Per enabled ADC |
| SID118A | I _{VREF_LEAK} | Analog reference voltage current while ADC is not operating | - | 1.8 | 5 | μA | Per enabled ADC |

25.7.3 Temperature Sensor

Table 25-9. Temperature Sensor Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-----------------------|-------------------------------|-----|-----|-----|-------|---|
| SID200 | T _{SENSACC1} | Temperature sensor accuracy 1 | -2 | - | 2 | °C | $T_J = 150^\circ\text{C}$ This spec is valid when using ADC[0] (V _{DDIO_1}), ADC[1] (V _{DDIO_2}) or ADC[2] (V _{DDD}) with the following conditions: a. $3.0\text{ V} \leq V_{DDD}$, V _{DDIO_1} or V _{DDIO_2} = V _{DDA} = V _{REFH} ≤ 3.6 V or b. $4.5\text{ V} \leq V_{DDD}$, V _{DDIO_1} or V _{DDIO_2} = V _{DDA} = V _{REFH} ≤ 5.5 V |
| SID201 | T _{SENSACC2} | Temperature sensor accuracy 2 | -5 | - | 5 | °C | $-40^\circ\text{C} \leq T_J < 150^\circ\text{C}$ This spec is valid when using ADC[0] (V _{DDIO_1}), ADC[1] (V _{DDIO_2}) or ADC[2] (V _{DDD}) with the following conditions: a. $3.0\text{ V} \leq V_{DDD}$, V _{DDIO_1} or V _{DDIO_2} = V _{DDA} = V _{REFH} ≤ 3.6 V or b. $4.5\text{ V} \leq V_{DDD}$, V _{DDIO_1} or V _{DDIO_2} = V _{DDA} = V _{REFH} ≤ 5.5 V |
| SID201A | T _{SENSACC3} | Temperature sensor accuracy 3 | -10 | - | 10 | °C | $-40^\circ\text{C} \leq T_J \leq 150^\circ\text{C}$ This spec is valid when using ADC[0] (V _{DDIO_1}) or ADC[2] (V _{DDD}) with the following condition: $2.7\text{ V} \leq V_{DDD}$ or V _{DDIO_1} ≤ 5.5 V and $2.7\text{ V} \leq V_{DDA} = V_{REFH} \leq 5.5\text{ V}$ and $0.8 \times V_{DDA} < V_{DDD}$ or V _{DDIO_1} |

25.7.4 Voltage Divider Accuracy

Table 25-10. Voltage Divider Accuracy

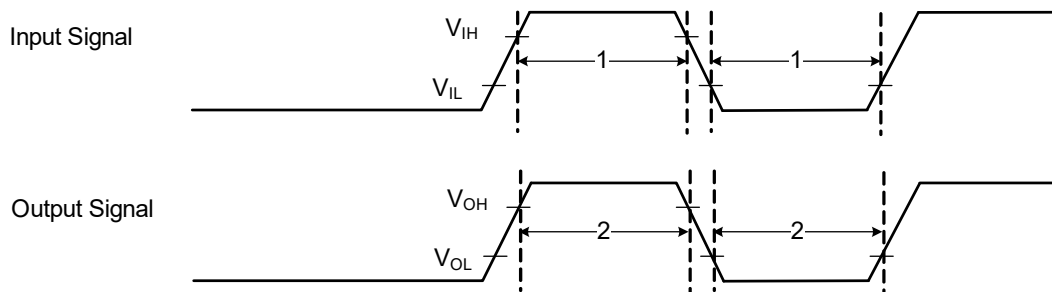
| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|---------------------|--|-----|-----|-----|-------|--|
| SID202 | V _{MONDIV} | Uncorrected monitor voltage divider accuracy (measured by ADC), compared to ideal supply/2 | -20 | 2 | 20 | % | Any HV supply pad within 2.7 V–5.5 V operating range |

25.8 Digital Peripherals
Table 25-11. Timer/Counter/PWM (TCPWM) Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|---------------|--|-----------|-----|-----|-------|--|
| SID120 | f_C | TCPWM operating frequency | – | – | 100 | MHz | f_C = peripheral clock |
| SID121 | $t_{PWMEEXT}$ | Input trigger pulse width for all trigger events | $2 / f_C$ | – | – | ns | Trigger Events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected. |
| SID122 | $t_{PWMEEXT}$ | Output trigger pulse widths | $2 / f_C$ | – | – | ns | Minimum possible width of Overflow, Underflow, and Counter = Compare (CC) value trigger outputs |
| SID123 | t_{CRES} | Resolution of counter | $1 / f_C$ | – | – | ns | Minimum time between successive counts |
| SID124 | t_{PWMRES} | PWM resolution | $1 / f_C$ | – | – | ns | Minimum pulse width of PWM output |
| SID125 | t_{QRES} | Quadrature inputs resolution | $2 / f_C$ | – | – | ns | Minimum pulse width between Quadrature phase inputs. |

Figure 25-7. TCPWM Timing Diagrams

TCPWM Timing Diagrams



1: $t_{PWMEEXT}$ t_{QRES}
 2: $t_{PWMEEXT}$

Table 25-12. Serial Communication Block (SCB) Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|-----------------------|---|------------------------------|-----|------|-------|--|
| SID129 | f _{SCB} | SCB operating frequency | – | – | 100 | MHz | |
| I²C Interface-Standard-mode | | | | | | | |
| SID130 | f _{SCL} | SCL clock frequency | – | – | 100 | kHz | |
| SID131 | t _{HD;STA} | Hold time, START condition | 4000 | – | – | ns | |
| SID132 | t _{LOW} | Low period of SCL | 4700 | – | – | ns | |
| SID133 | t _{HIGH} | High period of SCL | 4000 | – | – | ns | |
| SID134 | t _{SU;STA} | Setup time for a repeated START | 4700 | – | – | ns | |
| SID135 | t _{HD;DAT} | Data hold time, for receiver | 0 | – | – | ns | |
| SID136 | t _{SU;DAT} | Data setup time | 250 | – | – | ns | |
| SID138 | t _F | Fall time of SCL and SDA | – | – | 300 | ns | Input and output |
| SID139 | t _{SU;STO} | Setup time for STOP | 4000 | – | – | ns | |
| SID140 | t _{BUF} | Bus-free time between START and STOP | 4700 | – | – | ns | |
| SID141 | C _B | Capacitive load for each bus line | – | – | 400 | pF | |
| SID142 | t _{VD;DAT} | Time for data signal from SCL LOW to SDA output | – | – | 3450 | ns | |
| SID143 | t _{VD;ACK} | Data valid acknowledge time | – | – | 3450 | ns | |
| SID144 | V _{OL} | LOW level output voltage | 0 | – | 0.4 | V | Open-drain at 3 mA sink current |
| SID145 | I _{OL} | LOW level output current | 3 | – | – | mA | V _{OL} = 0.4 V |
| I²C Interface-Fast-mode | | | | | | | |
| SID150 | f _{SCL_F} | SCL clock frequency | – | – | 400 | kHz | |
| SID151 | t _{HD;STA_F} | Hold time, START condition | 600 | – | – | ns | |
| SID152 | t _{LOW_F} | Low period of SCL | 1300 | – | – | ns | |
| SID153 | t _{HIGH_F} | High period of SCL | 600 | – | – | ns | |
| SID154 | t _{SU;STA_F} | Setup time for a repeated START | 600 | – | – | ns | |
| SID155 | t _{HD;DAT_F} | Data hold time, for receiver | 0 | – | – | ns | |
| SID156 | t _{SU;DAT_F} | Data setup time | 100 | – | – | ns | |
| SID158 | t _{F_F} | Fall time of SCL and SDA | 20 × (V _{DD} / 5.5) | – | 300 | ns | Input and output, GPIO_ENH: slow mode, 400 pF load |
| SID158A | t _{FA_F} | Fall time of SCL and SDA | 0.35 | – | 300 | ns | Input and output GPIO_STD: drive_sel<1:0>= 0b00 MIN: 10 pF load, RPU = 35.41 kΩ Max: 400 pF load, RPU = 350 Ω |
| SID159 | t _{SU;STO_F} | Setup time for STOP | 600 | – | – | ns | Input and output |
| SID160 | t _{BUF_F} | Bus free time between START and STOP | 1300 | – | – | ns | |
| SID161 | C _{B_F} | Capacitive load for each bus line | – | – | 400 | pF | |
| SID162 | t _{VD;DAT_F} | Time for data signal from SCL LOW to SDA output | – | – | 900 | ns | |

Table 25-12. Serial Communication Block (SCB) Specifications *(continued)*

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|--|------------------------|---|------------------------------|-----|------|-------|---|
| SID163 | t _{VD;ACK_F} | Data valid acknowledge time | – | – | 900 | ns | |
| SID164 | t _{SP_F} | Pulse width of spikes that must be suppressed by the input filter | – | – | 50 | ns | |
| SID165 | V _{OL_F} | LOW level output voltage | 0 | – | 0.4 | V | Open-drain at 3 mA sink current |
| SID166 | I _{OL_F} | LOW level output current | 3 | – | – | mA | V _{OL} = 0.4 V |
| SID167 | I _{OL2_F} | LOW level output current | 6 | – | – | mA | V _{OL} = 0.6 V ^[59] |
| I²C Interface-Fast-Plus mode | | | | | | | |
| SID170 | f _{SCL_FP} | SCL clock frequency | – | – | 1 | MHz | |
| SID171 | t _{HD;STA_FP} | Hold time, START condition | 260 | – | – | ns | |
| SID172 | t _{LOW_FP} | Low period of SCL | 500 | – | – | ns | |
| SID173 | t _{HIGH_FP} | High period of SCL | 260 | – | – | ns | |
| SID174 | t _{SU;STA_FP} | Setup time for a repeated START | 260 | – | – | ns | |
| SID175 | t _{HD;DAT_FP} | Data hold time, for receiver | 0 | – | – | ns | |
| SID176 | t _{SU;DAT_FP} | Data setup time | 50 | – | – | ns | |
| SID178 | t _{F_FP} | Fall time of SCL and SDA | 20 × (V _{DD} / 5.5) | – | 160 | ns | Input and output 20-pF load GPIO_ENH: slow mode |
| SID179 | t _{SU;STO_FP} | Setup time for STOP | 260 | – | – | ns | Input and output |
| SID180 | t _{BUF_FP} | Bus free time between START and STOP | 500 | – | – | ns | |
| SID181 | C _{B_FP} | Capacitive load for each bus line | – | – | 20 | pF | |
| SID182 | t _{VD;DAT_FP} | Time for data signal from SCL LOW to SDA output | – | – | 450 | ns | |
| SID183 | t _{VD;ACK_FP} | Data valid acknowledge time | – | – | 450 | ns | |
| SID184 | t _{SP_FP} | Pulse width of spikes that must be suppressed by the input filter | – | – | 50 | ns | |
| SID186 | V _{OL_FP} | LOW level output voltage | 0 | – | 0.4 | V | Open-drain at 3 mA sink current |
| SID187 | I _{OL_FP} | LOW level output current | 3 ^[60] | – | – | mA | V _{OL} = 0.4 V ^[60] |
| SPI Interface Master (Full-clock mode: LATE_MISO_SAMPLE = 1) [Conditions: drive_sel<1:0>= 0x] | | | | | | | |
| SID190 | f _{SPI} | SPI operating frequency | – | – | 12.5 | MHz | Do not use half-clock mode: LATE_MISO_SAMPLE = 0 |
| SID191 | t _{DMO} | SPI Master: MOSI valid after SCLK driving edge | – | – | 15 | ns | |

Notes

59. In order to drive full bus load at 400 kHz, 6 mA I_{OL} is required at 0.6 V V_{OL}.

60. In order to drive full bus load at 1 MHz, 20 mA I_{OL} is required at 0.4 V V_{OL}. However, this device does not support it.

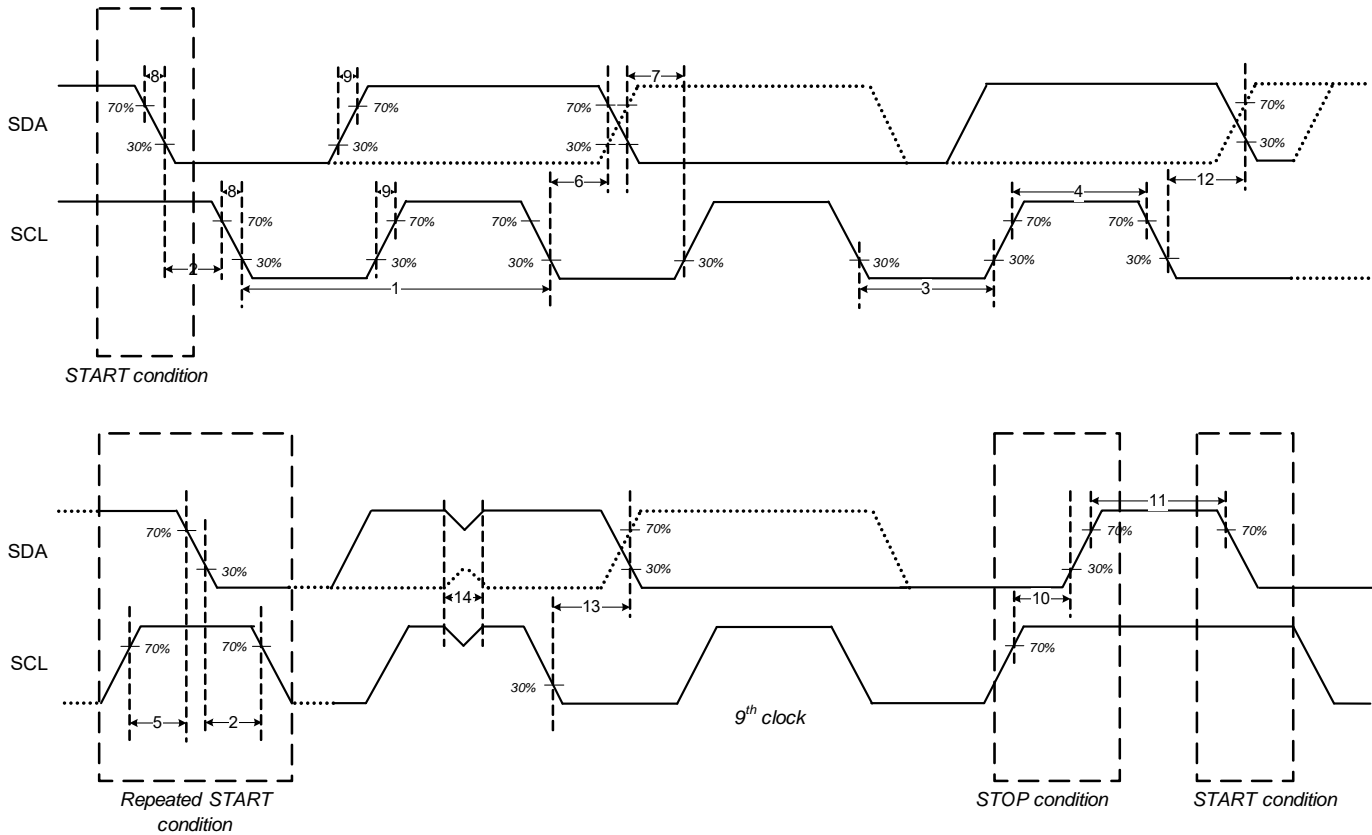
Table 25-12. Serial Communication Block (SCB) Specifications *(continued)*

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|--|---------------------------|---|--------------------------------|----------------------------------|------|-------|---|
| SID192 | t _{DSI} | SPI Master: MISO valid before SCLK capturing edge | 40 | – | – | ns | |
| SID193 | t _{HMO} | SPI Master: Previous MOSI data hold time | 0 | – | – | ns | |
| SID193A | t _{HMOA} | SPI Master: Previous MOSI data hold time | –3.5 | – | – | ns | Only for SCB4_MOSI/P0.3 and SCB4_CLK/P1.0 |
| SID194 | t _{W_SCLK_H_L} | SPI SCLK pulse width HIGH or LOW | – | 0.4 × (1 / f _{SPI}) | – | ns | |
| SID196 | t _{DHI} | SPI Master: MISO hold time after SCLK capturing edge | 0 | – | – | ns | |
| SID198 | t _{EN_SETUP} | SSEL valid, before the first SCK capturing edge | 0.5 × (1/f _{SPI}) | – | – | ns | Min is half clock period |
| SID199 | t _{EN_SHOLD} | SSEL hold, after the last SCK capturing edge | 0.5 × (1/f _{SPI}) | – | – | ns | Min is half clock period |
| SID195 | C _{SPIM_MS} | SPI capacitive load | – | – | 10 | pF | |
| SPI Interface Slave (internally clocked) [Conditions: drive_sel<1:0>= 0x] | | | | | | | |
| SID205 | f _{SPI_INT} | SPI operating frequency | – | – | 10 | MHz | |
| SID206 | t _{DMI_INT} | SPI Slave: MOSI Valid before Sclock capturing edge | 5 | – | – | ns | |
| SID207 | t _{DSO_INT} | SPI Slave: MISO Valid after Sclock driving edge, in the internal-clocked mode | – | – | 62 | ns | |
| SID208 | t _{HSP} | SPI Slave: Previous MISO data hold time | 3 | – | – | ns | |
| SID209 | t _{EN_SETUP_INT} | SPI Slave: SSEL valid to first SCK valid edge | 33 | – | – | ns | |
| SID210 | t _{EN_HOLD_INT} | SPI Slave Select active (LOW) from last SCLK hold | 33 | – | – | ns | |
| SID211 | t _{EN_SETUP_PRE} | SPI Slave: from SSEL valid, to SCK falling edge before the first data bit | 20 | – | – | ns | |
| SID212 | t _{EN_HOLD_PRE} | SPI Slave: from SCK falling edge before the first data bit, to SSEL invalid | 20 | – | – | ns | |
| SID213 | t _{EN_SETUP_CO} | SPI Slave: from SSEL valid, to SCK falling edge in the first data bit | 20 | – | – | ns | |
| SID214 | t _{EN_HOLD_CO} | SPI Slave: from SCK falling edge in the first data bit, to SSEL invalid | 20 | – | – | ns | |
| SID215 | t _{W_DIS_INT} | SPI Slave Select inactive time | 40 | – | – | ns | |
| SID216 | t _{W_SCLKH_INT} | SPI SCLK pulse width HIGH | 20 | – | – | ns | |
| SID217 | t _{W_SCLKL_INT} | SPI SCLK pulse width LOW | 20 | – | – | ns | |
| SID218 | t _{SIH_INT} | SPI MOSI hold from SCLK | 12 | – | – | ns | |
| SID219 | C _{SPIS_INT} | SPI Capacitive Load | – | – | 10 | pF | |
| SPI Interface Slave (externally clocked) [Conditions: drive_sel<1:0>= 0x] | | | | | | | |
| SID220 | f _{SPI_EXT} | SPI operating frequency | – | – | 12.5 | MHz | |
| SID221 | t _{DMI_EXT} | SPI Slave: MOSI Valid before Sclock capturing edge | 5 | – | – | ns | |

Table 25-12. Serial Communication Block (SCB) Specifications *(continued)*

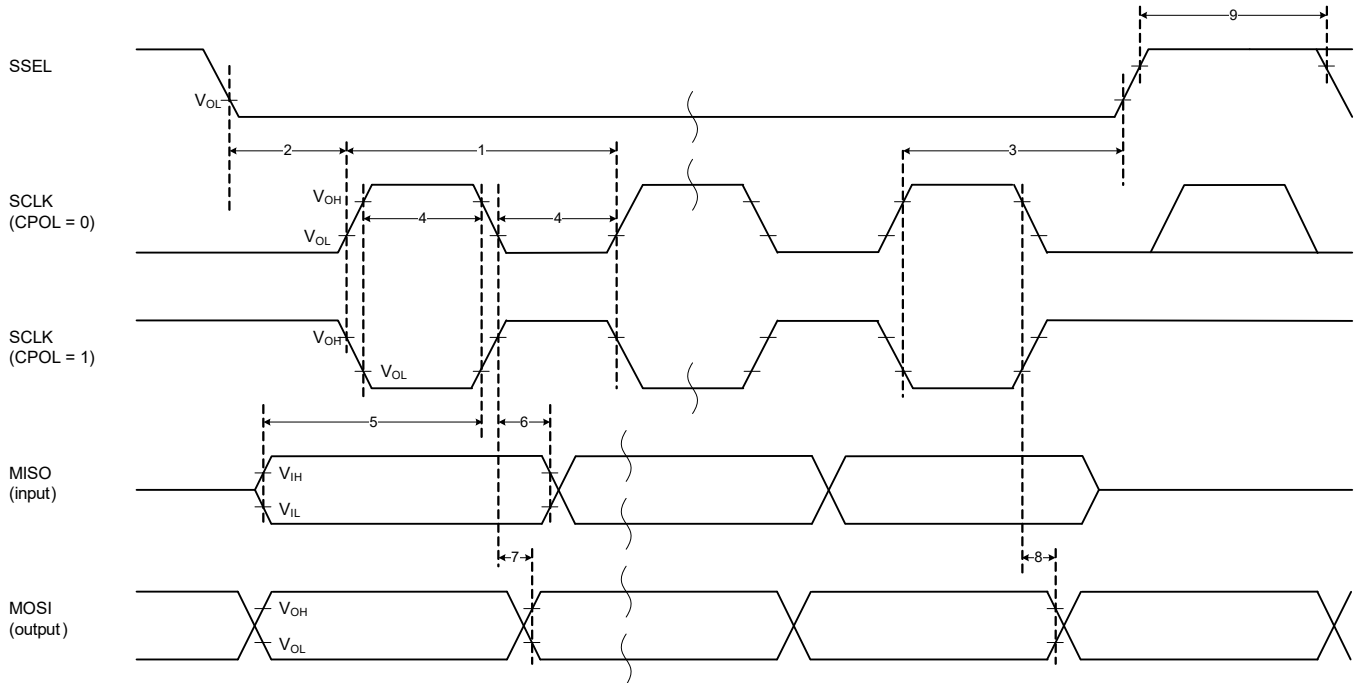
| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|-----------------------|-----------------------------|---|-----|-----|-----|-------|--------------------|
| SID222 | $t_{\text{DSO_EXT}}$ | SPI Slave: MISO Valid after Sclock driving edge, in the external-clocked mode | – | – | 32 | ns | |
| SID223 | $t_{\text{HSO_EXT}}$ | SPI Slave: Previous MISO data hold time | 3 | – | – | ns | |
| SID224 | $t_{\text{EN_SETUP_EXT}}$ | SPI Slave: SSEL valid to first SCK valid edge | 40 | – | – | ns | |
| SID225 | $t_{\text{EN_HOLD_EXT}}$ | SPI Slave Select active (LOW) from last SCLK hold | 40 | – | – | ns | |
| SID226 | $t_{\text{W_DIS_EXT}}$ | SPI Slave Select inactive time | 80 | – | – | ns | |
| SID227 | $t_{\text{W_SCLKH_EXT}}$ | SPI SCLK pulse width HIGH | 34 | – | – | ns | |
| SID228 | $t_{\text{W_SCLKL_EXT}}$ | SPI SCLK pulse width LOW | 34 | – | – | ns | |
| SID229 | $t_{\text{SIH_EXT}}$ | SPI MOSI hold from SCLK | 20 | – | – | ns | |
| SID230 | $C_{\text{SPIS_EXT}}$ | SPI Capacitive Load | – | – | 10 | pF | |
| SID231 | $t_{\text{VSS_EXT}}$ | SPI Slave: MISO valid after SSEL falling edge (CPHA = 0) | – | – | 33 | ns | |
| UART Interface | | | | | | | |
| SID240 | f_{BPS} | Data rate | – | – | 10 | Mbps | |

Figure 25-8. I²C Timing Diagrams



- 1: SCL clock period = $1/f_{SCL}$
- 2: Hold time, START condition = $t_{HD,STA}$
- 3: LOW period of SCL = t_{LOW}
- 4: HIGH period of SCL = t_{HIGH}
- 5: Setup time for a repeated START = $t_{SU,STA}$
- 6: Data hold time, for receiver = $t_{HD,DAT}$
- 7: Data setup time = $t_{SU,DAT}$
- 8: Fall time of SCL and SDA = t_F
- 9: Rise time of SCL and SDA = t_R
- 10: Setup time for STOP = $t_{SU,STO}$
- 11: Bus-free time between START and STOP = t_{BUF}
- 12: Time for data signal from SCL LOW to SDA output = $t_{VD,DAT}$
- 13: Data valid acknowledge time = $t_{VD,ACK}$
- 14: Pulse width of spikes that must be suppressed by the input filter = t_{SP}

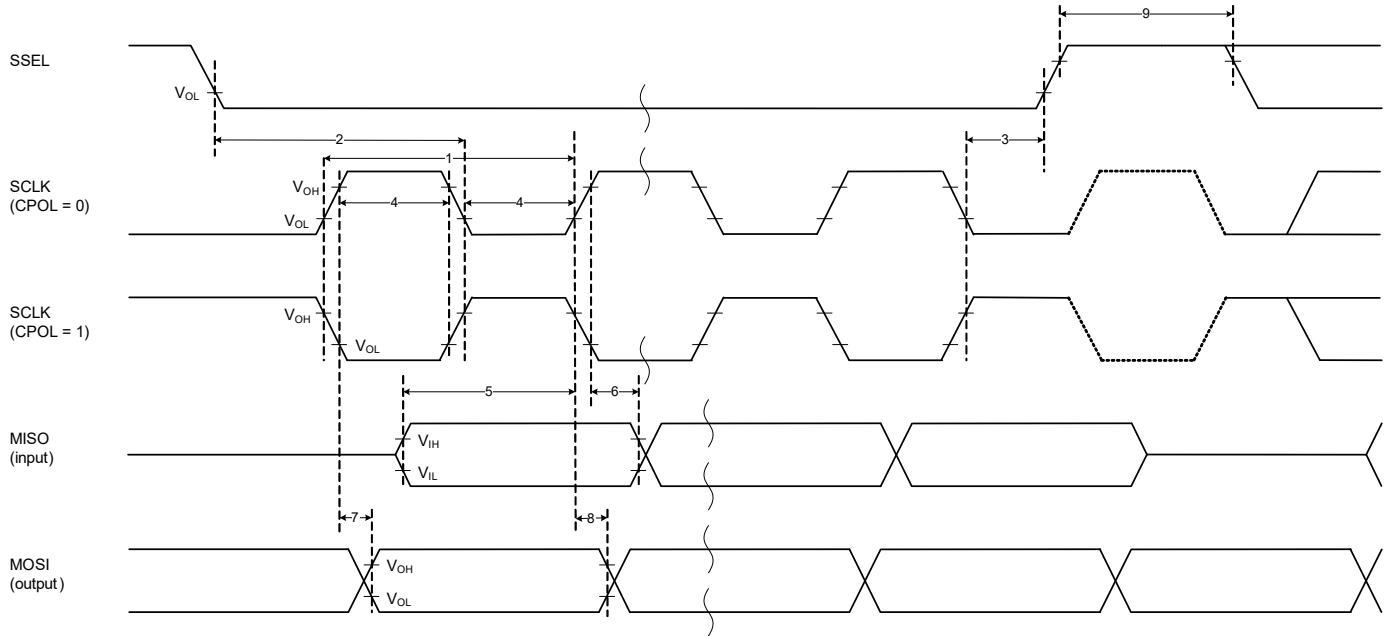
Figure 25-9.SPI Master Timing Diagrams with LOW Clock Phase

 SPI Master Timing Diagrams (LATE_MISO_SAMPLE = 1)
 CPHA = 0


- 1: SCLK period = $1 / f_{SPI}$
- 2: Enable lead time (setup) = t_{EN_SETUP} = Depends on SPI_CTRL.SSEL_SETUP_DEL (Refer to the Register TRM)
- 3: Enable trail time (hold) = t_{EN_HOLD} = Depends on SPI_CTRL.SSEL_HOLD_DEL (Refer to the Register TRM)
- 4: SCLK high or low time = $t_{W_SCLK_H_L}$
- 5: Input data setup time = t_{DSI}
- 6: Input data hold time = t_{DHI}
- 7: Output data valid after SCLK driving edge = t_{DMO}
- 8: Output data hold time = t_{HMO}
- 9: SSEL high pulse width = Depends on SPI_CTRL.SSEL_INTER_FRAME_DEL (Refer to the Register TRM)

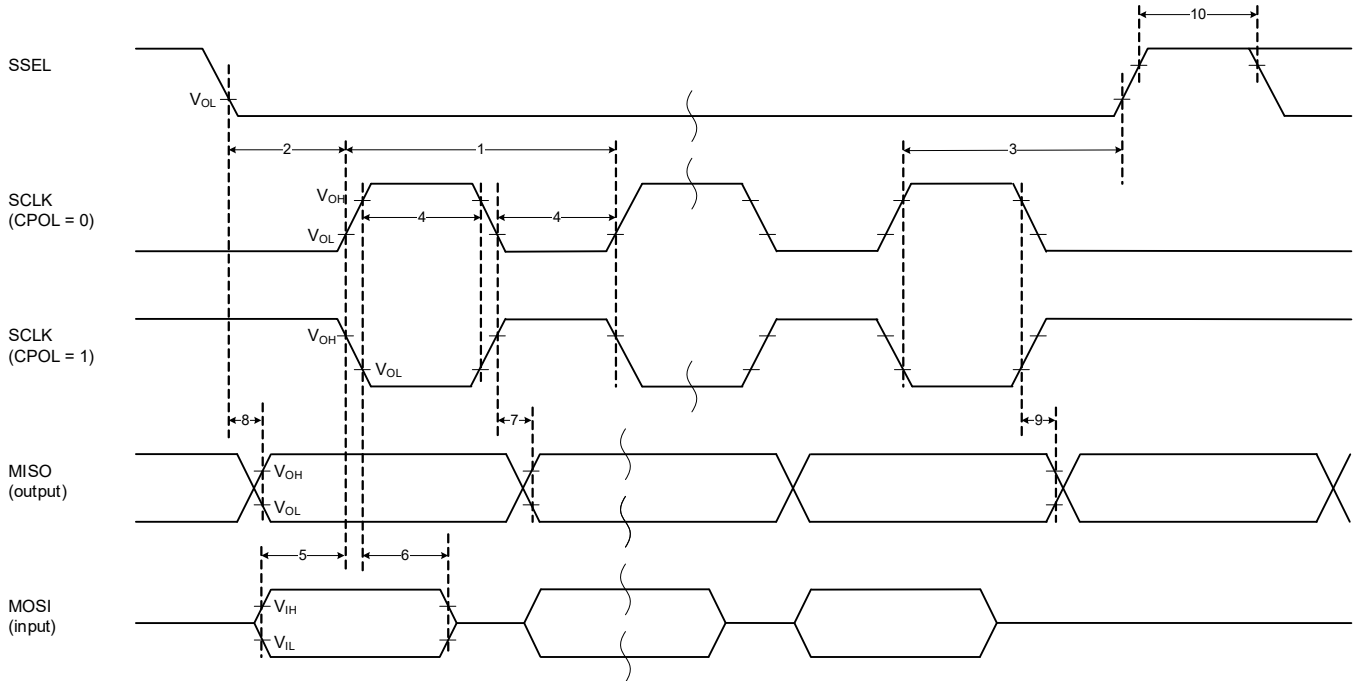
Figure 25-10.SPI Master Timing Diagrams with HIGH Clock Phase

SPI Master Timing Diagrams (LATE_MISO_SAMPLE = 1)
CPHA = 1



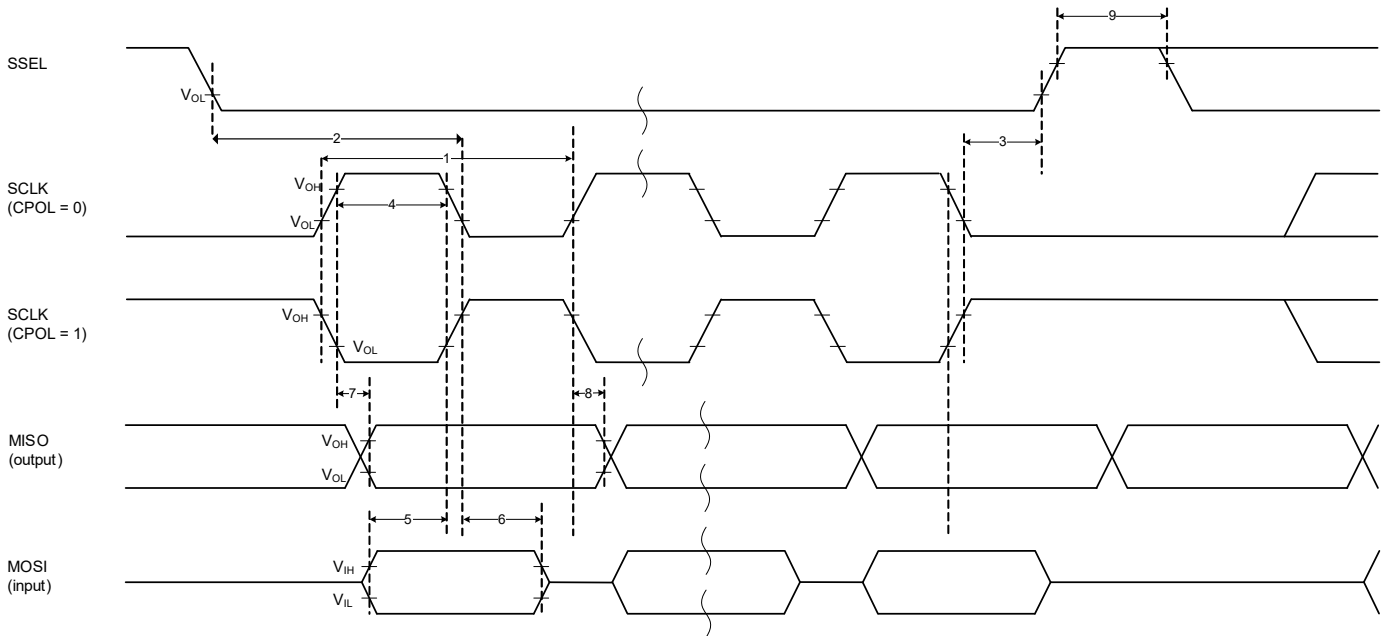
- 1: SCLK period = $1 / f_{SPI}$
- 2: Enable lead time (setup) = t_{EN_SETUP} = Depends on SPI_CTRL.SSEL_SETUP_DEL (Refer to the Register TRM)
- 3: Enable trail time (hold) = t_{EN_HOLD} = Depends on SPI_CTRL.SSEL_HOLD_DEL (Refer to the Register TRM)
- 4: SCLK high or low time = $t_{W_SCLK_H_L}$
- 5: Input data setup time = t_{DSI}
- 6: Input data hold time = t_{HDI}
- 7: Output data valid after SCLK driving edge = t_{DMO}
- 8: Output data hold time = t_{HMO}
- 9: SSEL high pulse width = Depends on SPI_CTRL.SSEL_INTER_FRAME_DEL (Refer to the Register TRM)

Figure 25-11. SPI Slave Timing Diagrams with LOW Clock Phase

 SPI Slave Timing Diagrams
 CPHA = 0


- 1: SCLK period = $1 / f_{\text{SPI_EXT}}$
- 2: enable lead time (setup) = $t_{\text{EN_SETUP_EXT}}$
- 3: enable trail time (hold) = $t_{\text{EN_HOLD_EXT}}$
- 4: SCLK high or low time = $t_{\text{w_SCLKH_EXT}} = t_{\text{w_SCLKL_EXT}}$
- 5: input data setup time = $t_{\text{DMI_EXT}}$
- 6: input data hold time = $t_{\text{SIH_EXT}}$
- 7: output data valid after SCLK driving edge = $t_{\text{DSO_EXT}}$
- 8: output data valid after SSEL falling edge (CPHA = 0) = $t_{\text{VSS_EXT}}$
- 9: output data hold time = t_{HSO}
- 10: SSEL high pulse width = $t_{\text{DIS_EXT}}$

Figure 25-12. SPI Slave Timing Diagrams with HIGH Clock Phase

 SPI slave Timing Diagrams
 CPHA = 1


- 1: SCLK period = $1 / f_{\text{SPI_EXT}}$
- 2: enable lead time (setup) = $t_{\text{EN_SETUP_EXT}}$
- 3: enable trail time (hold) = $t_{\text{EN_HOLD_EXT}}$
- 4: SCLK high or low time = $t_{\text{W_SCLKH_EXT}} = t_{\text{W_SCLKL_EXT}}$
- 5: input data setup time = $t_{\text{DMI_EXT}}$
- 6: input data hold time = $t_{\text{SIH_EXT}}$
- 7: output data valid after SCLK driving edge = $t_{\text{DSO_EXT}}$
- 8: output data hold time = t_{HSO}
- 9: SSEL high pulse width = $t_{\text{DIS_EXT}}$

Table 25-13. CAN FD Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-------------------|------------------------|-----|-----|-----|-------|--|
| SID630 | f _{HCLK} | System clock frequency | – | – | 100 | MHz | f _{CCLK} ≤ f _{HCLK} , guaranteed by design |
| SID631 | f _{CCLK} | CAN clock frequency | – | – | 100 | MHz | f _{CCLK} ≤ f _{HCLK} , guaranteed by design |

Table 25-14. LIN Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|------------------|---|-----|-----|-------|-------|----------------------|
| SID249 | f _{LIN} | Internal clock frequency to the LIN block | – | – | 100 | MHz | |
| SID250 | BR_NOM | Bit rate on the LIN bus | 1 | – | 20 | kbps | Guaranteed by design |
| SID250A | BR_REF | Bit rate on the LIN bus (not in standard LIN specification) for re-flashing in LIN slave mode | 1 | – | 115.2 | kbps | Guaranteed by design |

25.9 Memory

Table 25-15. Flash DC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-----------------|---------------------------|-----|-----|-----|-------|--------------------|
| SID260A | V _{PE} | Erase and program voltage | 2.7 | – | 5.5 | V | |

Table 25-16. Flash AC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|---------------------------|--|-----|-----|--------------|-------|--|
| SID257 | f _{FO} | Maximum flash memory operation frequency | – | – | 100 | MHz | Zero wait access to code-flash memory up to 100 MHz Zero wait access with cache hit up to 350 MHz |
| SID254 | t _{ERS_SUS} | Maximum time from erase suspend command till erase is indeed suspend | – | – | 37.5 | µs | |
| SID255 | t _{ERS_RES_SUS} | Minimum time allowed from erase resume to erase suspend | 250 | – | – | µs | Guaranteed by design |
| SID258 | t _{BC_WF} | Blank check time for N-bytes of work-flash | – | – | 10 + 0.3 × N | µs | At 100 MHz, N ≥ 4 and multiple of 4, excludes system overhead time |
| SID259 | t _{SECTORERASE1} | Sector erase time (code-flash: 32 KB) | – | 45 | 90 | ms | Includes internal preprogramming time |
| SID260 | t _{SECTORERASE2} | Sector erase time (code-flash: 8 KB) | – | 15 | 30 | ms | Includes internal preprogramming time |
| SID261 | t _{SECTORERASE3} | Sector erase time (work-flash, 2 KB) | – | 80 | 160 | ms | Includes internal preprogramming time |
| SID262 | t _{SECTORERASE4} | Sector erase time (work-flash, 128 B) | – | 5 | 15 | ms | Includes internal preprogramming time |
| SID263 | t _{WRITE1} | 64-bit write time (code-flash) | – | 30 | 60 | µs | Excludes system overhead time |
| SID264 | t _{WRITE2} | 256-bit write time (code-flash) | – | 40 | 70 | µs | Excludes system overhead time |
| SID265 | t _{WRITE3} | 4096-bit write time (code-flash) ^[61] | – | 320 | 1200 | µs | Excludes system overhead time |
| SID266 | t _{WRITE4} | 32-bit write time (work-flash) | – | 30 | 60 | µs | Excludes system overhead time |
| SID267 | t _{FRET1} | Code-flash retention. 1000 program/erase cycles | 20 | – | – | years | T _A (power on and off) ≤ 85 °C average |

Note

61. The code-flash includes a 'Write Buffer' of 4096-bit. If the application software writes this buffer multiple times, to get the overall write time multiply one sector write time with the corresponding factor (say for factor 64, example, 64 x 512 B = 32 KB [one sector])

Table 25-16. Flash AC Specifications (continued)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-----------------------|--|-----|-----|-----|-------|---|
| SID268 | t _{FRET3} | Work-flash retention. 125,000 program/erase cycles | 20 | – | – | years | T _A (power on and off) ≤ 85 °C average |
| SID269 | t _{FRET4} | Work-flash retention. 250,000 program/erase cycles | 10 | – | – | years | T _A (power on and off) ≤ 85 °C average |
| SID612 | I _{CC_ACT2} | Program operating V _{CCD} current (code or work-flash) | – | 7 | 58 | mA | Typ: T _A = 25 °C, V _{DDD} = 5.0 V, V _{CCD} = 1.15 V, process typ (TT) Max: T _A = 125 °C, V _{DDD} = 5.5 V, V _{CCD} = 1.2 V, process worst (FF) Guaranteed by design |
| SID613 | I _{CC_ACT3} | Erase operating V _{CCD} current (code- or work-flash) | – | 7 | 52 | mA | Typ: T _A = 25 °C, V _{DDD} = 5.0 V, V _{CCD} = 1.15 V, process typ (TT) Max: T _A = 125 °C, V _{DDD} = 5.5 V, V _{CCD} = 1.2 V, process worst (FF) Guaranteed by design |
| SID612A | I _{CC_ACT2A} | Program operating V _{DDD} current (code or work-flash) | – | 8 | 10 | mA | Typ: T _A = 25 °C, V _{DDD} = 5.0 V, V _{CCD} = 1.15 V, process typ (TT) Max: T _A = 125 °C, V _{DDD} = 5.5 V, V _{CCD} = 1.2 V, process worst (FF) Guaranteed by design |
| SID613A | I _{CC_ACT3A} | Erase operating V _{DDD} current (code- or work-flash) | – | 8 | 16 | mA | Typ: T _A = 25 °C, V _{DDD} = 5.0 V, V _{CCD} = 1.15 V, process typ (TT) Max: T _A = 125 °C, V _{DDD} = 5.5 V, V _{CCD} = 1.2 V, process worst (FF) Guaranteed by design |

25.10 System Resources
Table 25-17. System Resources

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|----------------------------|---|-------|-------|-------|-------|---|
| Power-On Reset Specifications | | | | | | | |
| SID270 | V _{POR_D} | V _{DDD} rising voltage to de assert POR | 1.5 | – | 2.35 | V | Guaranteed by design |
| SID276 | V _{POR_A} | V _{DDD} falling voltage to assert POR | 1.45 | – | 2.1 | V | |
| SID271 | V _{POR_H} | Level detection hysteresis | 20 | – | 300 | mV | |
| SID272 | t _{DLY_POR} | Delay between V _{DDD} rising through 2.3 V and internal deassertion of POR | – | – | 3 | µs | Guaranteed by design |
| SID273 | t _{POFF} | V _{DDD} Power off time | 100 | – | – | µs | V _{DDD} < 1.45 V |
| SID274 | POR_RR1 | V _{DDD} power ramp rate with robust BOD (BOD operation is guaranteed) | – | – | 100 | mV/µs | This ramp supports robust BOD |
| SID275 | POR_RR2 | V _{DDD} power ramp rate without robust BOD | – | – | 1000 | mV/µs | This ramp does not support robust BOD t _{POFF} must be satisfied. |
| High-voltage BOD (HV BOD) Specifications | | | | | | | |
| SID500 | V _{TR_2P7_R} | HV BOD 2.7 V rising detection point for V _{DDD} and V _{DDA} (default) | 2.474 | 2.55 | 2.627 | V | |
| SID501 | V _{TR_2P7_F} | HV BOD 2.7 V falling detection point for V _{DDD} and V _{DDA} (default) | 2.449 | 2.525 | 2.601 | V | |
| SID502 | V _{TR_3P0_R} | HV BOD 3.0 V rising detection point for V _{DDD} and V _{DDA} | 2.765 | 2.85 | 2.936 | V | |
| SID503 | V _{TR_3P0_F} | HV BOD 3.0 V falling detection point for V _{DDD} and V _{DDA} | 2.74 | 2.825 | 2.91 | V | |
| SID505 | HVBOD_RR_A | Power ramp rate: V _{DDD} and V _{DDA} (Active) | – | – | 100 | mV/µs | |
| SID506 | HVBOD_RR_DS | Power ramp rate: V _{DDD} and V _{DDA} (DeepSleep) | – | – | 10 | mV/µs | |
| SID507 | t _{DLY_ACT_HVBOD} | Active mode delay between V _{DDD} falling/rising through V _{TR_2P7_F/R} or V _{TR_3P0_F/R} and an internal HV BOD signal transitioning | – | – | 0.5 | µs | Guaranteed by design |
| SID507A | t _{DLY_ACT_HVBOD} | Active mode delay between V _{DDA} falling/rising through V _{TR_2P7_F/R} or V _{TR_3P0_F/R} and internal HV BOD signal transitioning | – | – | 1 | µs | Guaranteed by design |
| SID507B | t _{DLY_DS_HVBOD} | DeepSleep mode delay between V _{DDD} /V _{DDA} falling/rising through V _{TR_2P7_F/R} or V _{TR_3P0_F/R} and an internal HV BOD signal transitioning | – | – | 4 | µs | Guaranteed by design |
| SID508 | t _{RES_HVBOD} | Response time of HV BOD, V _{DDD} /V _{DDA} supply. (For falling-then-rising supply at max ramp rate; threshold is V _{TR_2P7_F} or V _{TR_3P0_F}) | 100 | – | – | ns | Guaranteed by design |
| Low-voltage BOD (LV BOD) Specifications | | | | | | | |
| SID510 | V _{TR_R_LVBOD} | LV BOD rising detection point for V _{CCD} | 0.917 | 0.945 | 0.973 | V | |
| SID511 | V _{TR_F_LVBOD} | LV BOD falling detection point for V _{CCD} | 0.892 | 0.920 | 0.948 | V | |
| SID515 | t _{DLY_ACT_LVBOD} | Active delay between V _{CCD} falling/rising through V _{TR_R/F_LVBOD} and an internal LV BOD signal transitioning | – | – | 1 | µs | Guaranteed by design |

Table 25-17. System Resources (continued)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---------------------------|--|----------|------|----------|-------|---------------------------------------|
| SID515A | t _{DLY_DS_LVBOD} | DeepSleep mode delay between V _{CCD} falling/rising through V _{TR_R/F_LVBOD} and an internal LV BOD signal transitioning | – | – | 12 | µs | Guaranteed by design |
| SID516 | t _{RES_LVBOD} | Response time of LV BOD (for falling-then-rising supply at max ramp rate; threshold is V _{TR_F_LVBOD}) | 100 | – | – | ns | Guaranteed by design |
| Low-voltage Detector (LVD) DC Specifications | | | | | | | |
| SID520 | V _{TR_2P8_F} | LVD 2.8 V falling detection point for V _{DDD} | Typ – 4% | 2800 | Typ + 4% | mV | |
| SID521 | V _{TR_2P9_F} | LVD 2.9 V falling detection point for V _{DDD} | Typ – 4% | 2900 | Typ + 4% | mV | |
| SID522 | V _{TR_3P0_F} | LVD 3.0 V falling detection point for V _{DDD} | Typ – 4% | 3000 | Typ + 4% | mV | |
| SID523 | V _{TR_3P1_F} | LVD 3.1 V falling detection point for V _{DDD} | Typ – 4% | 3100 | Typ + 4% | mV | |
| SID524 | V _{TR_3P2_F} | LVD 3.2 V falling detection point for V _{DDD} | Typ – 4% | 3200 | Typ + 4% | mV | |
| SID525 | V _{TR_3P3_F} | LVD 3.3 V falling detection point for V _{DDD} | Typ – 4% | 3300 | Typ + 4% | mV | |
| SID526 | V _{TR_3P4_F} | LVD 3.4 V falling detection point for V _{DDD} | Typ – 4% | 3400 | Typ + 4% | mV | |
| SID527 | V _{TR_3P5_F} | LVD 3.5 V falling detection point for V _{DDD} | Typ – 4% | 3500 | Typ + 4% | mV | |
| SID528 | V _{TR_3P6_F} | LVD 3.6 V falling detection point for V _{DDD} | Typ – 4% | 3600 | Typ + 4% | mV | |
| SID529 | V _{TR_3P7_F} | LVD 3.7 V falling detection point for V _{DDD} | Typ – 4% | 3700 | Typ + 4% | mV | |
| SID530 | V _{TR_3P8_F} | LVD 3.8 V falling detection point for V _{DDD} | Typ – 4% | 3800 | Typ + 4% | mV | |
| SID531 | V _{TR_3P9_F} | LVD 3.9 V falling detection point for V _{DDD} | Typ – 4% | 3900 | Typ + 4% | mV | |
| SID532 | V _{TR_4P0_F} | LVD 4.0 V falling detection point for V _{DDD} | Typ – 4% | 4000 | Typ + 4% | mV | |
| SID533 | V _{TR_4P1_F} | LVD 4.1 V falling detection point for V _{DDD} | Typ – 4% | 4100 | Typ + 4% | mV | |
| SID534 | V _{TR_4P2_F} | LVD 4.2 V falling detection point for V _{DDD} | Typ – 4% | 4200 | Typ + 4% | mV | |
| SID535 | V _{TR_4P3_F} | LVD 4.3 V falling detection point for V _{DDD} | Typ – 4% | 4300 | Typ + 4% | mV | |
| SID536 | V _{TR_4P4_F} | LVD 4.4 V falling detection point for V _{DDD} | Typ – 4% | 4400 | Typ + 4% | mV | |
| SID537 | V _{TR_4P5_F} | LVD 4.5 V falling detection point for V _{DDD} | Typ – 4% | 4500 | Typ + 4% | mV | |
| SID538 | V _{TR_4P6_F} | LVD 4.6 V falling detection point for V _{DDD} | Typ – 4% | 4600 | Typ + 4% | mV | |
| SID539 | V _{TR_4P7_F} | LVD 4.7 V falling detection point for V _{DDD} | Typ – 4% | 4700 | Typ + 4% | mV | |
| SID540 | V _{TR_4P8_F} | LVD 4.8 V falling detection point for V _{DDD} | Typ – 4% | 4800 | Typ + 4% | mV | |
| SID541 | V _{TR_4P9_F} | LVD 4.9 V falling detection point for V _{DDD} | Typ – 4% | 4900 | Typ + 4% | mV | |
| SID542 | V _{TR_5P0_F} | LVD 5.0 V falling detection point for V _{DDD} | Typ – 4% | 5000 | Typ + 4% | mV | |
| SID543 | V _{TR_5P1_F} | LVD 5.1 V falling detection point for V _{DDD} | Typ – 4% | 5100 | Typ + 4% | mV | |
| SID544 | V _{TR_5P2_F} | LVD 5.2 V falling detection point for V _{DDD} | Typ – 4% | 5200 | Typ + 4% | mV | |
| SID545 | V _{TR_5P3_F} | LVD 5.3 V falling detection point for V _{DDD} | Typ – 4% | 5300 | Typ + 4% | mV | |
| SID546 | V _{TR_2P8_R} | LVD 2.8 V rising detection point for V _{DDD} | Typ – 4% | 2825 | Typ + 4% | mV | Same as V _{TR_2P8_F} + 25 mV |
| SID547 | V _{TR_2P9_R} | LVD 2.9 V rising detection point for V _{DDD} | Typ – 4% | 2925 | Typ + 4% | mV | Same as V _{TR_2P9_F} + 25 mV |
| SID548 | V _{TR_3P0_R} | LVD 3.0 V rising detection point for V _{DDD} | Typ – 4% | 3025 | Typ + 4% | mV | Same as V _{TR_3P0_F} + 25 mV |
| SID549 | V _{TR_3P1_R} | LVD 3.1 V rising detection point for V _{DDD} | Typ – 4% | 3125 | Typ + 4% | mV | Same as V _{TR_3P1_F} + 25 mV |
| SID550 | V _{TR_3P2_R} | LVD 3.2 V rising detection point for V _{DDD} | Typ – 4% | 3225 | Typ + 4% | mV | Same as V _{TR_3P2_F} + 25 mV |
| SID551 | V _{TR_3P3_R} | LVD 3.3 V rising detection point for V _{DDD} | Typ – 4% | 3325 | Typ + 4% | mV | Same as V _{TR_3P3_F} + 25 mV |
| SID552 | V _{TR_3P4_R} | LVD 3.4 V rising detection point for V _{DDD} | Typ – 4% | 3425 | Typ + 4% | mV | Same as V _{TR_3P4_F} + 25 mV |

Table 25-17. System Resources (continued)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|--------------------------|--|----------|------|----------|-------|---------------------------------------|
| SID553 | V _{TR_3P5_R} | LVD 3.5 V rising detection point for V _{DDD} | Typ – 4% | 3525 | Typ + 4% | mV | Same as V _{TR_3P5_F} + 25 mV |
| SID554 | V _{TR_3P6_R} | LVD 3.6 V rising detection point for V _{DDD} | Typ – 4% | 3625 | Typ + 4% | mV | Same as V _{TR_3P6_F} + 25 mV |
| SID555 | V _{TR_3P7_R} | LVD 3.7 V rising detection point for V _{DDD} | Typ – 4% | 3725 | Typ + 4% | mV | Same as V _{TR_3P7_F} + 25 mV |
| SID556 | V _{TR_3P8_R} | LVD 3.8 V rising detection point for V _{DDD} | Typ – 4% | 3825 | Typ + 4% | mV | Same as V _{TR_3P8_F} + 25 mV |
| SID557 | V _{TR_3P9_R} | LVD 3.9 V rising detection point for V _{DDD} | Typ – 4% | 3925 | Typ + 4% | mV | Same as V _{TR_3P9_F} + 25 mV |
| SID558 | V _{TR_4P0_R} | LVD 4.0 V rising detection point for V _{DDD} | Typ – 4% | 4025 | Typ + 4% | mV | Same as V _{TR_4P0_F} + 25 mV |
| SID559 | V _{TR_4P1_R} | LVD 4.1 V rising detection point for V _{DDD} | Typ – 4% | 4125 | Typ + 4% | mV | Same as V _{TR_4P1_F} + 25 mV |
| SID560 | V _{TR_4P2_R} | LVD 4.2 V rising detection point for V _{DDD} | Typ – 4% | 4225 | Typ + 4% | mV | Same as V _{TR_4P2_F} + 25 mV |
| SID561 | V _{TR_4P3_R} | LVD 4.3 V rising detection point for V _{DDD} | Typ – 4% | 4325 | Typ + 4% | mV | Same as V _{TR_4P3_F} + 25 mV |
| SID562 | V _{TR_4P4_R} | LVD 4.4 V rising detection point for V _{DDD} | Typ – 4% | 4425 | Typ + 4% | mV | Same as V _{TR_4P4_F} + 25 mV |
| SID563 | V _{TR_4P5_R} | LVD 4.5 V rising detection point for V _{DDD} | Typ – 4% | 4525 | Typ + 4% | mV | Same as V _{TR_4P5_F} + 25 mV |
| SID564 | V _{TR_4P6_R} | LVD 4.6 V rising detection point for V _{DDD} | Typ – 4% | 4625 | Typ + 4% | mV | Same as V _{TR_4P6_F} + 25 mV |
| SID565 | V _{TR_4P7_R} | LVD 4.7 V rising detection point for V _{DDD} | Typ – 4% | 4725 | Typ + 4% | mV | Same as V _{TR_4P7_F} + 25 mV |
| SID566 | V _{TR_4P8_R} | LVD 4.8 V rising detection point for V _{DDD} | Typ – 4% | 4825 | Typ + 4% | mV | Same as V _{TR_4P8_F} + 25 mV |
| SID567 | V _{TR_4P9_R} | LVD 4.9 V rising detection point for V _{DDD} | Typ – 4% | 4925 | Typ + 4% | mV | Same as V _{TR_4P9_F} + 25 mV |
| SID568 | V _{TR_5P0_R} | LVD 5.0 V rising detection point for V _{DDD} | Typ – 4% | 5025 | Typ + 4% | mV | Same as V _{TR_5P0_F} + 25 mV |
| SID569 | V _{TR_5P1_R} | LVD 5.1 V rising detection point for V _{DDD} | Typ – 4% | 5125 | Typ + 4% | mV | Same as V _{TR_5P1_F} + 25 mV |
| SID570 | V _{TR_5P2_R} | LVD 5.2 V rising detection point for V _{DDD} | Typ – 4% | 5225 | Typ + 4% | mV | Same as V _{TR_5P2_F} + 25 mV |
| SID571 | V _{TR_5P3_R} | LVD 5.3 V rising detection point for V _{DDD} | Typ – 4% | 5325 | Typ + 4% | mV | Same as V _{TR_5P3_F} + 25 mV |
| SID573 | LVD_RR_A | Power ramp rate: V _{DDD} (Active) | – | – | 100 | mV/μs | |
| SID574 | LVD_RR_DS | Power ramp rate: V _{DDD} (DeepSleep) | – | – | 10 | mV/μs | |
| SID575 | t _{DLY_ACT_LVD} | Active mode delay between V _{DDD} falling/rising through LVD rising/falling point and an internal LVD signal transitioning | – | – | 1 | μs | Guaranteed by design |
| SID575A | t _{DLY_DS_LVD} | DeepSleep mode delay between V _{DDD} falling/rising through LVD rising/falling point and an internal LVD signal transitioning | – | – | 4 | μs | Guaranteed by design |
| SID576 | t _{RES_LVD} | Response time of LVD, V _{DDD} supply. (For falling-then-rising supply at max ramp rate; threshold is LVD falling point) | 100 | – | – | ns | Guaranteed by design |

Table 25-17. System Resources (continued)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|--|------------------------------|---|-------|-------|-------|-------|----------------------|
| High-voltage OVD Specifications | | | | | | | |
| SID580 | V _{TR_5P0_R} | HV OVD 5.0-V rising detection point for V _{DDD} and V _{DDA} | 5.049 | 5.205 | 5.361 | V | |
| SID581 | V _{TR_5P0_F} | HV OVD 5.0-V falling detection point for V _{DDD} and V _{DDA} | 5.025 | 5.18 | 5.335 | V | |
| SID582 | V _{TR_5P5_R} | HV OVD 5.5-V rising detection point for V _{DDD} and V _{DDA} (default) | 5.548 | 5.72 | 5.892 | V | |
| SID583 | V _{TR_5P5_F} | HV OVD 5.5-V falling detection point for V _{DDD} and V _{DDA} (default) | 5.524 | 5.695 | 5.866 | V | |
| SID585 | HVOVD_RR_A | Power ramp rate: V _{DDD} and V _{DDA} (Active) | – | – | 100 | mV/μs | |
| SID586 | HVOVD_RR_DS | Power ramp rate: V _{DDD} and V _{DDA} (DeepSleep) | – | – | 10 | mV/μs | |
| SID587 | t _{DLY_ACT_HVOVD} | Active mode delay between V _{DDD} falling/rising through V _{TR_5P0_F/R} or V _{TR_5P5_F/R} and an internal HV OVD signal transitioning | – | – | 1 | μs | Guaranteed by design |
| SID587A | t _{DLY_ACT_HVOVD_A} | Active mode delay between V _{DDA} falling/rising through V _{TR_5P0_F/R} or V _{TR_5P5_F/R} and an internal HV OVD signal transitioning | – | – | 1.5 | μs | Guaranteed by design |
| SID587B | t _{DLY_DS_HVOVD} | DeepSleep mode delay between V _{DDD} /V _{DDA} falling/rising through V _{TR_5P0_F/R} or V _{TR_5P5_F/R} and an internal HV OVD signal transitioning | – | – | 4 | μs | Guaranteed by design |
| SID588 | t _{RES_HVOVD} | Response time of HV OVD (for rising-then-falling supply at max ramp rate; threshold is V _{TR_5P0_R} or V _{TR_5P5_R}) | 100 | – | – | ns | Guaranteed by design |
| Low-voltage OVD Specifications | | | | | | | |
| SID590 | V _{TR_R_LVOVD} | LV OVD rising detection point for V _{CCD} | 1.261 | 1.3 | 1.339 | V | |
| SID591 | V _{TR_F_LVOVD} | LV OVD falling detection point for V _{CCD} | 1.237 | 1.275 | 1.313 | V | |
| SID595 | t _{DLY_ACT_LVOVD} | Active mode delay between V _{CCD} falling/rising through V _{TR_F/R_LVOVD} and an internal LV OVD signal transitioning | – | – | 1 | μs | Guaranteed by design |
| SID595A | t _{DLY_DS_LVOVD} | DeepSleep mode delay between V _{CCD} falling/rising through V _{TR_F/R_LVOVD} and an internal LV OVD signal transitioning | – | – | 12 | μs | Guaranteed by design |
| SID596 | t _{RES_LVOVD} | Response time of LV OVD. (For rising-then-falling supply at max ramp rate; threshold is V _{TR_R_LVOVD}) | 100 | – | – | ns | Guaranteed by design |
| Over Current Detection (OCD) Specifications | | | | | | | |
| SID598A | I _{OCD_LDO} | Over current detection range for internal Active regulator | 312 | – | 630 | mA | Guaranteed by design |
| SID598B | I _{OCD_EXT} | Over current detection range for external transistor mode | 675 | – | 825 | mA | |
| SID599 | I _{OCD_DPSP} | Over current detection range for internal DeepSleep regulator | 18 | – | 72 | mA | |

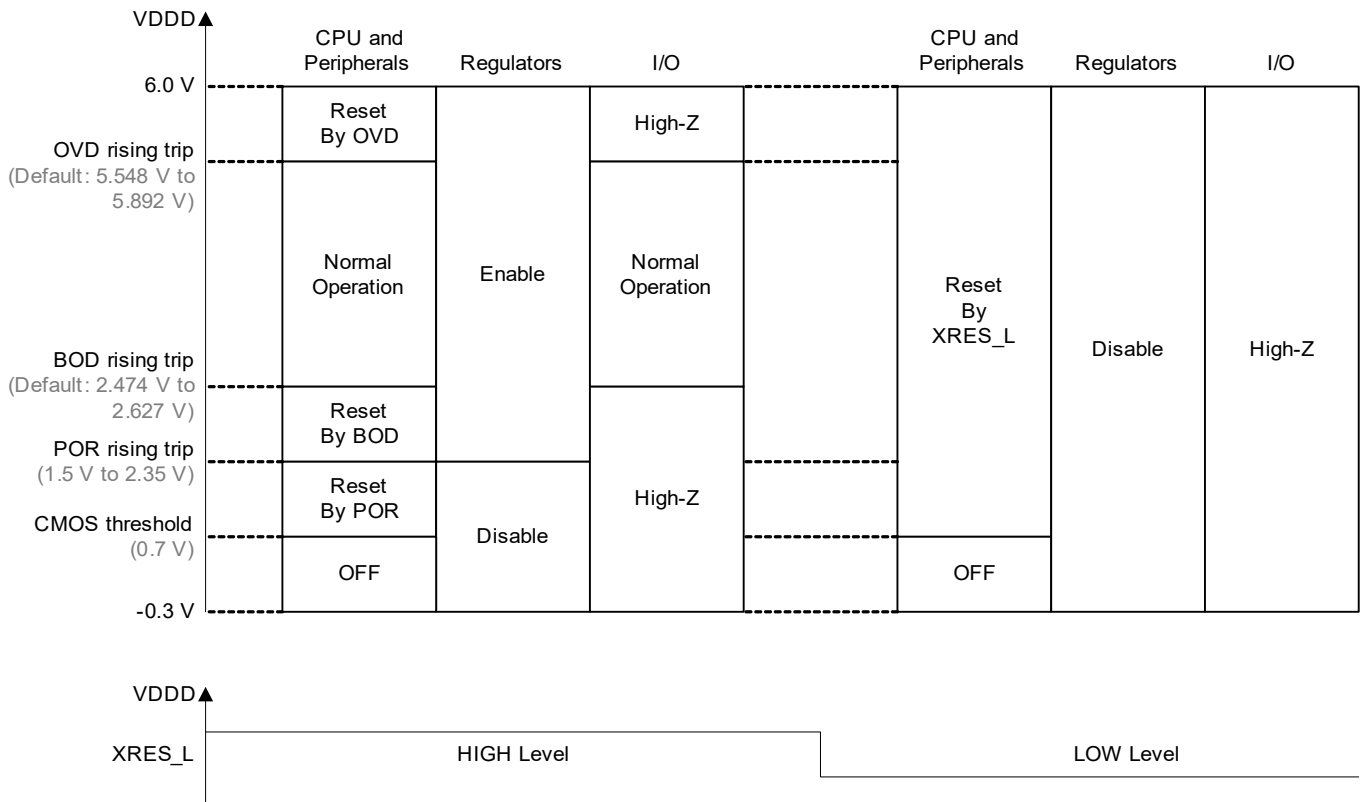
Figure 25-13. Device Operations Supply Range


Figure 25-14.POR Specifications

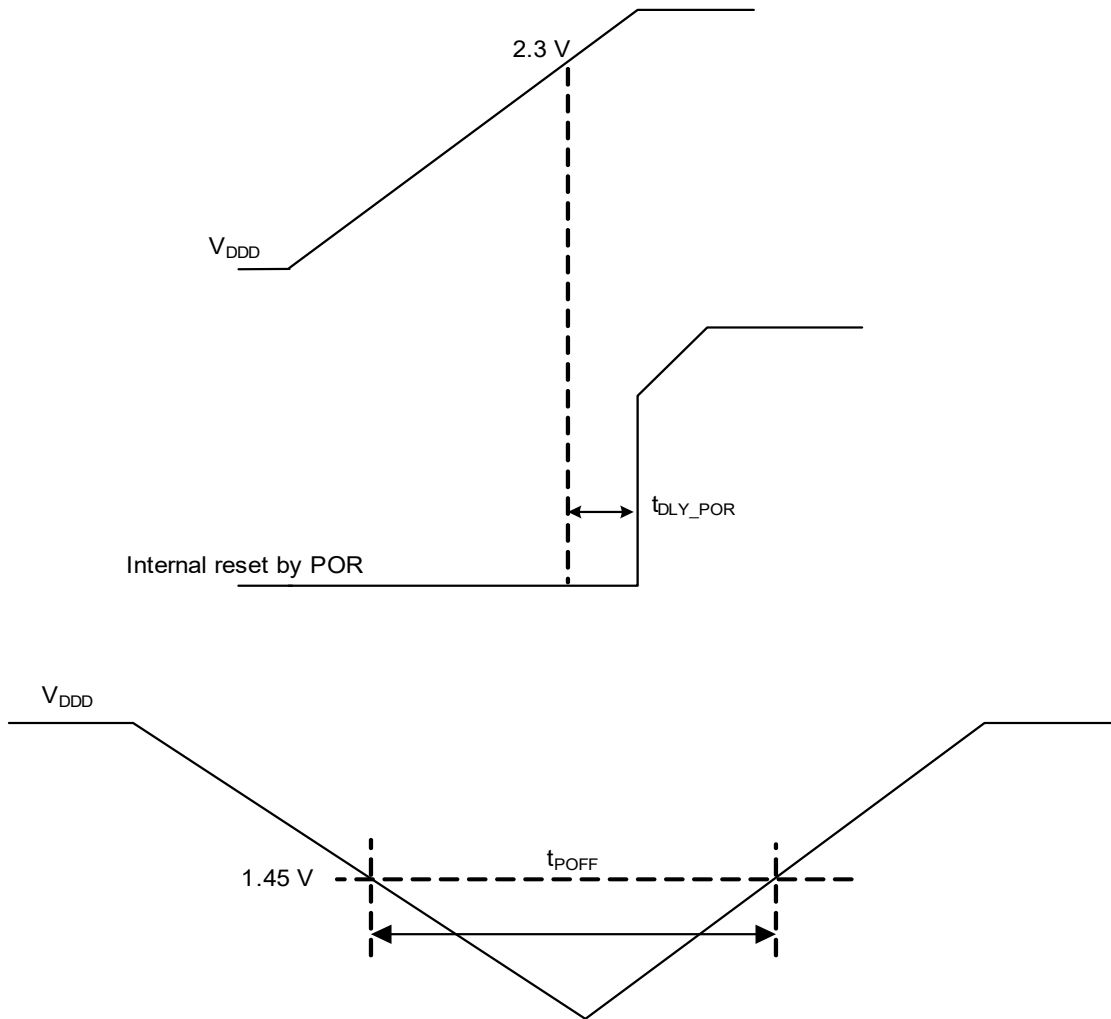


Figure 25-15. High-Voltage BOD Specifications

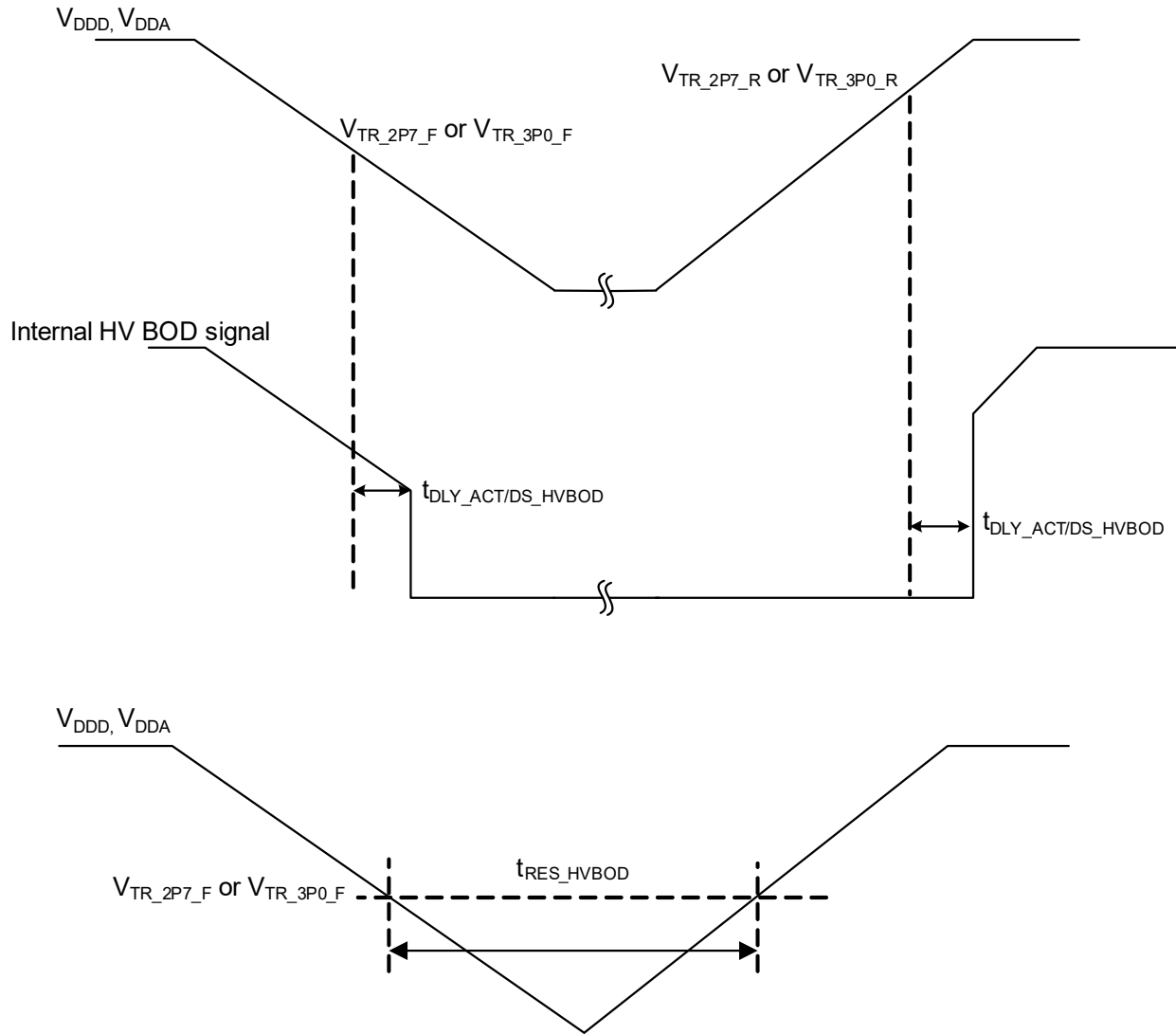


Figure 25-16. Low-Voltage BOD Specifications

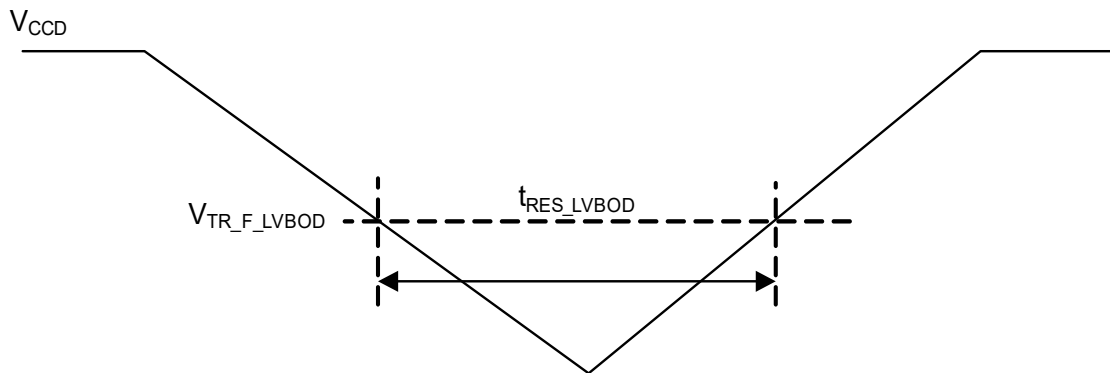
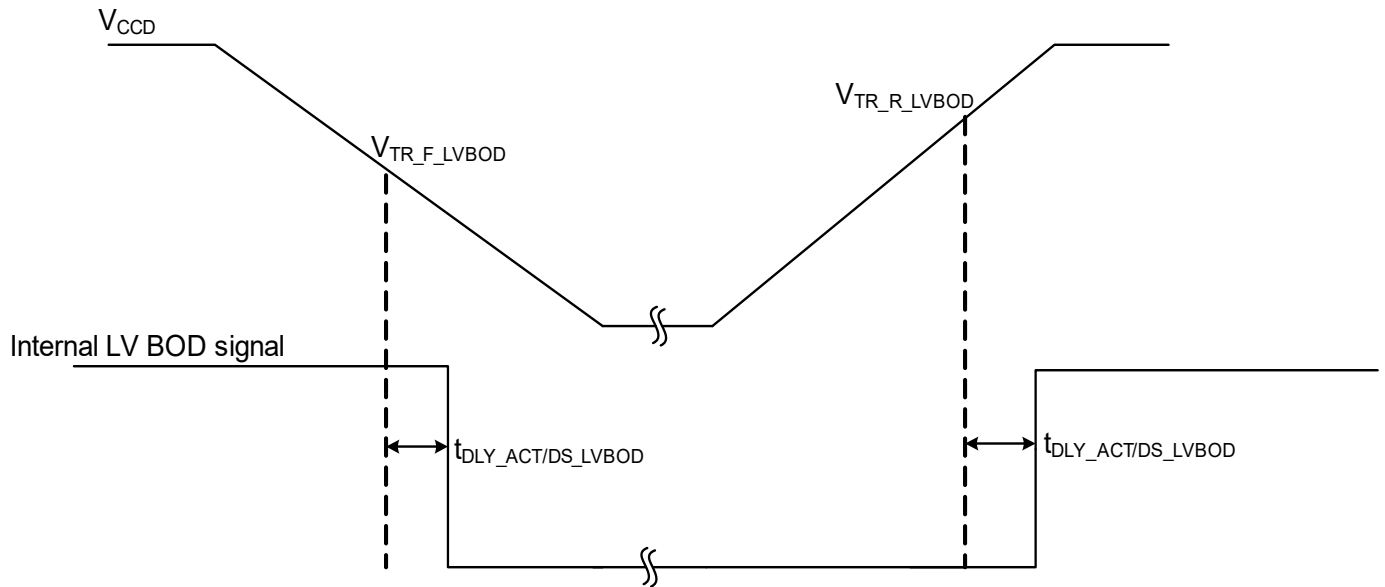


Figure 25-17. High-Voltage OVD Specifications

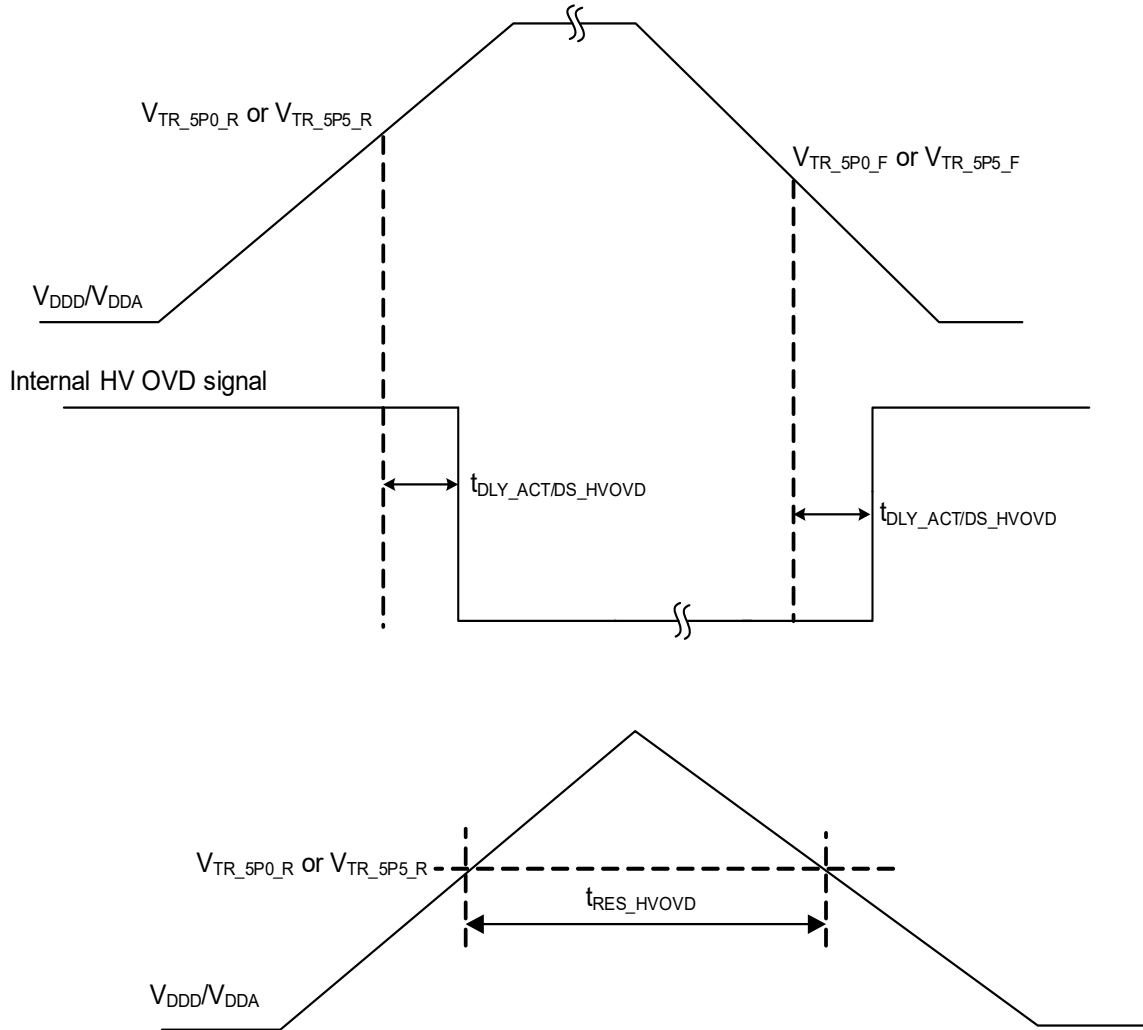


Figure 25-18. Low-Voltage OVD Specifications

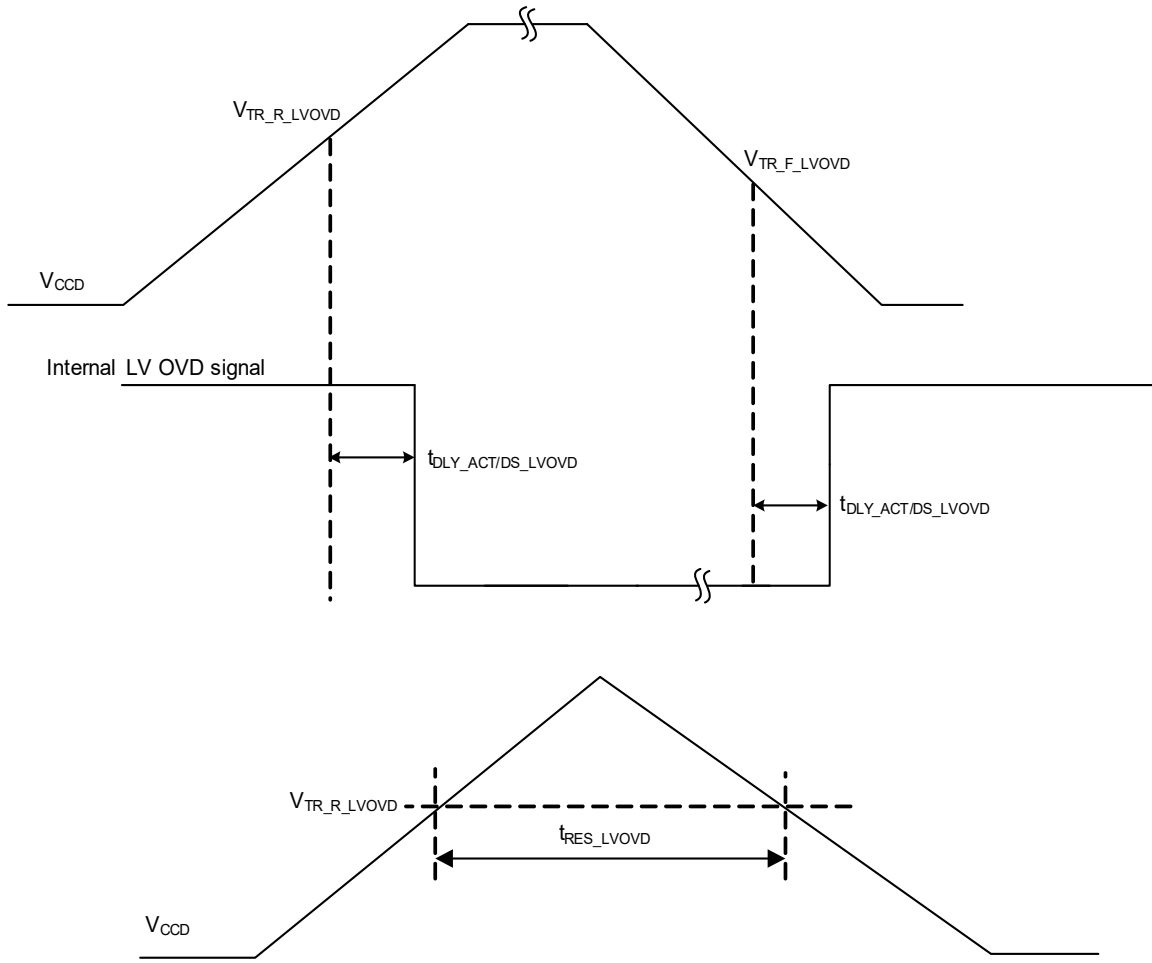
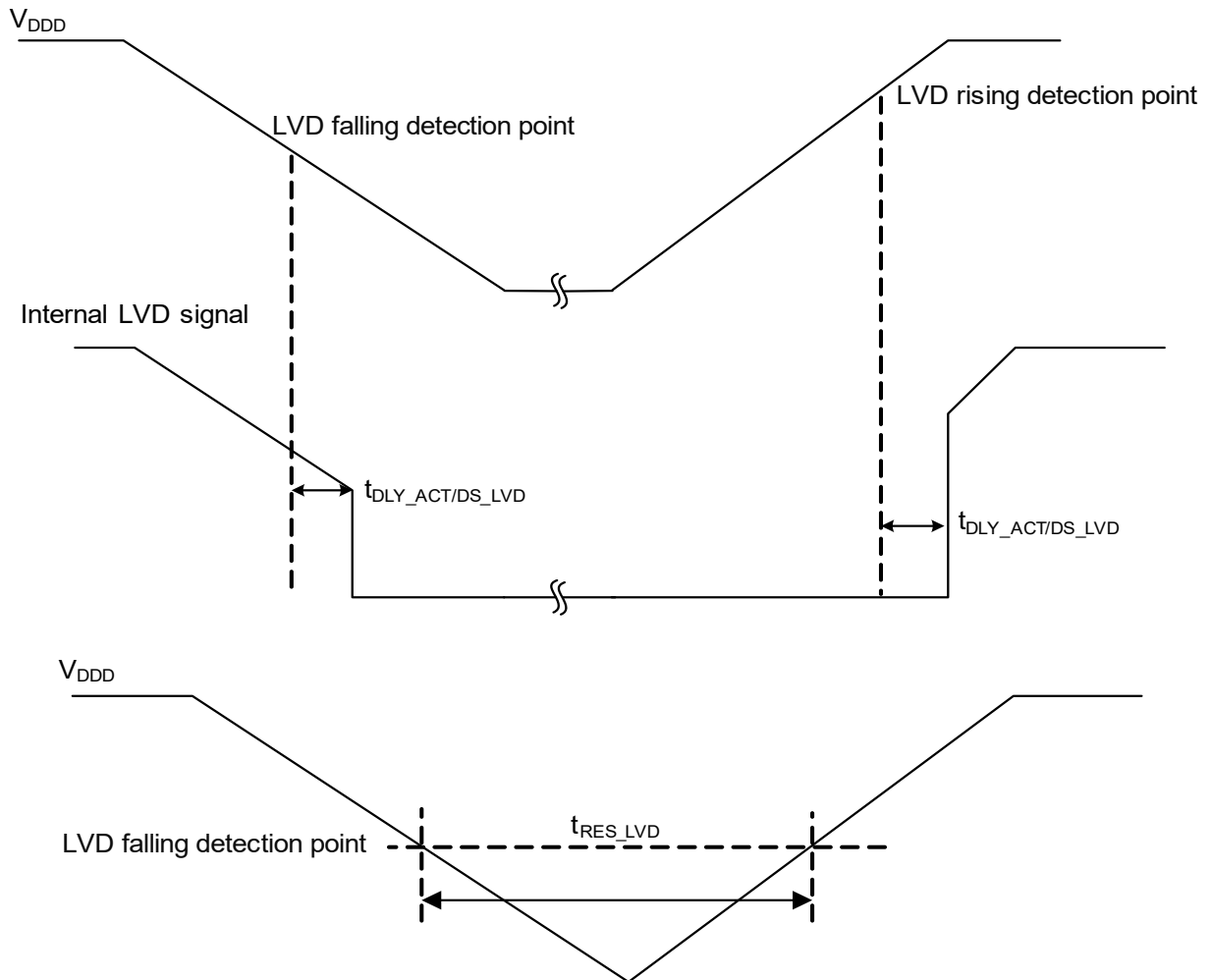


Figure 25-19.LVD Specifications



25.10.1 SWD Interface

Table 25-18. SWD Interface Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|--------------------------|---------------------------|-----------------|-----|----------------|-------|---|
| SID300 | f_{SWDCLK} | SWD clock input frequency | – | – | 10 | MHz | $2.7\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}$ |
| SID301 | $t_{\text{SWDI_SETUP}}$ | SWDI setup time | $0.25 \times T$ | – | – | ns | $T = 1 / f_{\text{SWDCLK}}$ |
| SID302 | $t_{\text{SWDI_HOLD}}$ | SWDI hold time | $0.25 \times T$ | – | – | ns | $T = 1 / f_{\text{SWDCLK}}$ |
| SID303 | $t_{\text{SWDO_VALID}}$ | SWDO valid time | – | – | $0.5 \times T$ | ns | $T = 1 / f_{\text{SWDCLK}}$ |
| SID304 | $t_{\text{SWDO_HOLD}}$ | SWDO hold time | 1 | – | – | ns | $T = 1 / f_{\text{SWDCLK}}$ |

Table 25-19. JTAG AC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-------------------|----------------------|------|-----|-----|-------|--------------------|
| SID620 | t_{JCKH} | TCK HIGH time | 30 | – | – | ns | 30-pF load |
| SID621 | t_{JCKL} | TCK LOW time | 30 | – | – | ns | 30-pF load |
| SID622 | t_{JCP} | TCK clock period | 66.7 | – | – | ns | 30-pF load |
| SID623 | t_{JSU} | TDI/TMS setup time | 12 | – | – | ns | 30-pF load |
| SID624 | t_{JH} | TDI/TMS hold time | 12 | – | – | ns | 30-pF load |
| SID625 | t_{JZX} | TDO High-Z to active | – | – | 30 | ns | 30-pF load |
| SID626 | t_{JXZ} | TDO active to High-Z | – | – | 30 | ns | 30-pF load |
| SID627 | t_{JCO} | TDO clock to output | – | – | 30 | ns | 30-pF load |

Figure 25-20. JTAG Specifications

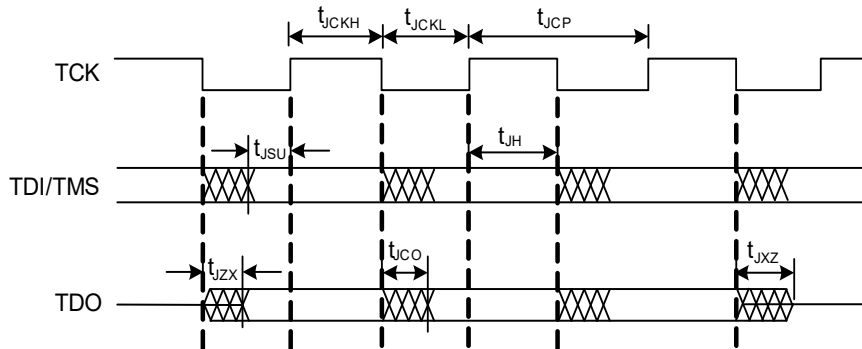


Table 25-20. Trace Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|----------|---------------------------|------------------------------|-----|-----|-----|-------|-----------------------------------|
| SID1412A | C_{TRACE} | Trace Capacitive Load | – | – | 30 | pF | |
| SID1412 | $t_{\text{TRACE_CYC}}$ | Trace clock period | 40 | – | – | ns | Trace clock cycle time for 25 MHz |
| SID1413 | $t_{\text{TRACE_CLKL}}$ | Trace clock LOW pulse width | 2 | – | – | ns | Clock low pulse width |
| SID1414 | $t_{\text{TRACE_CLKH}}$ | Trace clock HIGH pulse width | 2 | – | – | ns | Clock high pulse width |
| SID1415A | $t_{\text{TRACE_SETUP}}$ | Trace data setup time | 3 | – | – | ns | Trace data setup time |
| SID1416A | $t_{\text{TRACE_HOLD}}$ | Trace data hold time | 2 | – | – | ns | Trace data hold time |

25.11 Clock Specifications
Table 25-21. Root and Intermediate Clocks^[62]

| Clock | Max Frequency (MHz) | Source | Description |
|------------|---------------------|----------|--|
| CLK_HF0 | 200 | PLL200#0 | Root clock for CPUSS, PERI |
| CLK_HF1 | 350 | PLL400#0 | CM7 CPU Core#0, CM7 CPU Core#1 clock |
| CLK_HF2 | 100 | PLL200#1 | Peripheral clock root other than CLK_PERI |
| CLK_HF3 | 100 | PLL200#0 | Event generator, clock output on EXT_CLK pins (when used as output) |
| CLK_HF4 | 125 | PLL400#1 | Ethernet Channel#0, Ethernet Channel#1 internal clock |
| CLK_HF5 | 196.608 | PLL400#1 | I ² S channel#0, I ² S channel#1, I ² S channel#2 interface clock, Ethernet Channel#0 TSU, Ethernet Channel#1 TSU |
| CLK_HF6 | 200 | PLL200#0 | Root clock for SDHC, SMIF interface clock |
| CLK_HF7 | 8 | ILO | CSV |
| CLK_FAST_0 | 350 | NA | CM7 CPU Core#0, intermediate clock |
| CLK_FAST_1 | 350 | NA | CM7 CPU Core#1, intermediate clock |
| CLK_MEM | 200 | NA | Generated by clock gating CLK_HF0, intermediate clock for SMIF, Flash, Ethernet |
| CLK_SLOW | 100 | NA | Generated by clock gating CLK_MEM, intermediate clock for CM0+, P-DMA, M-DMA, Crypto, SMIF, SDHC |
| CLK_PERI | 100 | NA | Generated by clock gating CLK_HF0, intermediate clock for IOSS, TCPWM0, CPU trace, SMIF |

Table 25-22. Relation between CLK_HF0 and CLK_SLOW (Example)^[63]

| CLK_HF0 (MHz) | CLK_SLOW (MHz) |
|---------------|----------------|
| 200 | 100 |
| 180 | 90 |
| 160 | 80 |
| 120 | 60 |
| 100 | 100 |
| 80 | 80 |

Table 25-23. IMO AC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-----------------------|-------------------------|------|------|------|-------|---|
| SID310 | f _{IMOTOL} | IMO operating frequency | 7.92 | 8 | 8.08 | MHz | |
| SID311 | t _{STARTIMO} | IMO start-up time | – | – | 7.5 | μs | Start-up time to 90% of final frequency |
| SID312 | I _{IMO_ACT} | IMO current | – | 13.5 | 22 | μA | |

Table 25-24. ILO AC Specifications

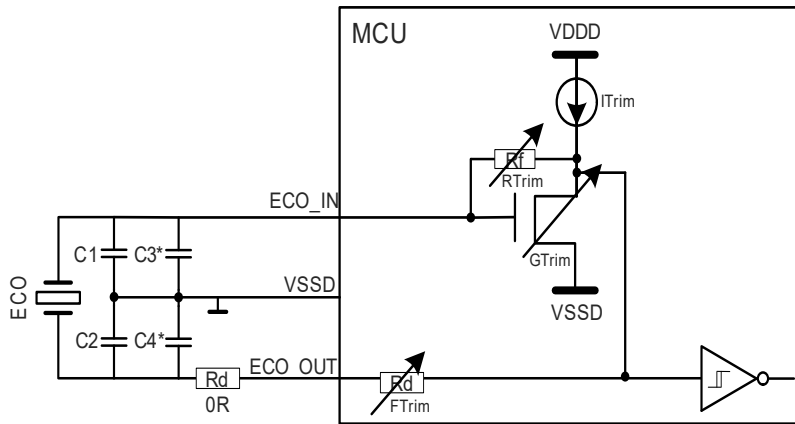
| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-----------------------|-------------------------|----------|--------|----------|-------|---|
| SID320 | f _{ILOTRIM} | ILO operating frequency | 30.47424 | 32.768 | 35.06176 | kHz | |
| SID321 | t _{STARTILO} | ILO start-up time | – | 8 | 12 | μs | Start-up time to 90% of final frequency |
| SID323 | I _{ILO} | ILO current | – | 500 | 2800 | nA | |

Notes

62. Intermediate clocks that are not listed have the same limitations as that of their parent clock.

63. CLOCK_SLOW and CLK_HF0 are related by integer frequency ratio (that is, 1:1, 1:2, 1:3, and so on).

Figure 25-21. ECO Connection Scheme^[65]



ECO_IN: External crystal oscillator input pin
 ECO_OUT: External crystal oscillator output pin
 C1, C2: Load Capacitors
 C3*, C4*: Stray Capacitance of the PCB

Table 25-25. ECO Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|------------------|--|-----|-----|-------|---------------|---|
| SID330 | f_{ECO} | Crystal frequency range | 8 | – | 33.34 | MHz | |
| SID332 | R_{FDBK} | Feedback resistor value. Min: RTRIM = 3; Max: RTRIM = 0 with 100-k Ω step size on RTRIM | 100 | – | 400 | k Ω | Guaranteed by design |
| SID333 | I_{ECO3} | ECO current at $T_J = 150\text{ }^\circ\text{C}$ | – | – | 2000 | μA | Maximum operation current with a 33-MHz crystal, 18-pF load |
| SID334 | t_{START_8M} | 8-MHz ECO start-up time ^[64] | – | – | 10 | ms | Start-up time to 90% of final frequency |
| SID335 | t_{START_33M} | 33-MHz ECO start-up time ^[64] | – | – | 1 | ms | Start-up time to 90% of final frequency |

Note

64. Mainly depends on the external crystal.

65. Refer to the family-specific Architecture TRM for more information on crystal requirements (002-24401, TRAVEO(TM) II AUTOMOTIVE BODY CONTROLLER HIGH FAMILY ARCHITECTURE TECHNICAL REFERENCE MANUAL (TRM)).

Table 25-26. PLL Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|--------------------|--|-------|------|-------|---------|--|
| PLL (without SSCG and fractional divider) Specifications for 200 MHz | | | | | | | |
| SID340 | t_{PLL200_LOCK} | Time to achieve PLL lock | – | – | 35 | μ s | Time from stable reference clock until PLL frequency is within 0.1% of final value and lock indicator is set |
| SID341 | f_{PLL_OUT} | Output frequency from PLL block | 11 | – | 200 | MHz | |
| SID342 | PLL_LJIT1 | Long term jitter | –0.25 | – | 0.25 | ns | For 125 ns Guaranteed by design f_{PLL_VCO} : 320 MHz or 400 MHz f_{PLL_OUT} : 40 MHz to 200 MHz f_{PLL_PFD} : 8 MHz f_{PLL_IN} : ECO |
| SID343 | PLL_LJIT2 | Long term jitter | –0.5 | – | 0.5 | ns | For 500 ns Guaranteed by design f_{PLL_VCO} : 320 MHz or 400 MHz f_{PLL_OUT} : 40 MHz to 200 MHz f_{PLL_PFD} : 8 MHz f_{PLL_IN} : ECO |
| SID344 | PLL_LJIT3 | Long term jitter | –0.5 | – | 0.5 | ns | For 1000 ns Guaranteed by design f_{PLL_VCO} : 320 MHz or 400 MHz f_{PLL_OUT} : 40 MHz to 200 MHz f_{PLL_PFD} : 8 MHz f_{PLL_IN} : ECO |
| SID345A1 | PLL_LJIT5 | Long term jitter | –0.75 | – | 0.75 | ns | For 10000 ns Guaranteed by design f_{PLL_VCO} : 320 MHz or 400 MHz f_{PLL_OUT} : 40 MHz to 200 MHz f_{PLL_PFD} : 8 MHz f_{PLL_IN} : ECO |
| SID346 | f_{PLL_IN} | PLL input frequency | 3.988 | – | 33.34 | MHz | |
| SID347 | I_{PLL_200M} | PLL operating current ($f_{OUT} = 200$ MHz) | – | 0.87 | 1.85 | mA | $f_{OUT} = 200$ MHz |
| SID348C | f_{PLL_VCO} | VCO frequency | 170 | – | 400 | MHz | |
| SID349C | f_{PLL_PFD} | PFD frequency | 4 | – | 8 | MHz | |
| PLL (with SSCG and fractional divider) Specifications for 400 MHz | | | | | | | |
| SID340A | t_{PLL400_LOCK} | Time to achieve PLL lock | – | – | 50 | μ s | Time from stable reference clock until PLL frequency is within 0.1% of final value and lock indicator is set |
| SID341A | f_{OUT} | Programmed output frequency from PLL Block (spreading off) | 25 | – | 350 | MHz | Spreading off |
| SID341B | f_{OUT} | Programmed output frequency from PLL Block (spreading on) | 25 | – | 340 | MHz | Spreading on |
| SID342D1 | PLL400_LJIT1 | Long term jitter | –0.25 | – | 0.25 | ns | For 125 ns Guaranteed by design f_{VCO} : 800 MHz or 700 MHz (spreading is off) f_{IN} : ECO f_{PFD} : 4 MHz f_{OUT} : 100 MHz to 350 MHz |

Table 25-26. PLL Specifications (continued)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|----------|-------------------------|---|-------|-----|-------|-------|---|
| SID343D1 | PLL400_LJIT2 | Long term jitter | -0.5 | - | 0.5 | ns | For 500 ns Guaranteed by design f_{VCO} : 800 MHz or 700 MHz (spreading is off) f_{IN} : ECO f_{PFD} : 4 MHz f_{OUT} : 100 MHz to 350 MHz |
| SID344D1 | PLL400_LJIT3 | Long term jitter | -1 | - | 1 | ns | For 1000 ns Guaranteed by design f_{VCO} : 800 MHz or 700 MHz (spreading is off) f_{IN} : ECO f_{PFD} : 4 MHz f_{OUT} : 100 MHz to 350 MHz |
| SID345E1 | PLL400_LJIT5 | Long term jitter | -1.5 | - | 1.5 | ns | For 10000 ns Guaranteed by design f_{VCO} : 800 MHz or 700 MHz (spreading is off) f_{IN} : ECO f_{PFD} : 4 MHz f_{OUT} : 100 MHz to 350 MHz |
| SID345A | f_{VCO} | VCO frequency | 400 | - | 800 | MHz | |
| SID346A | f_{IN} | PLL input frequency | 3.988 | - | 33.34 | MHz | |
| SID347A | I_{PLL_400M} | PLL operating current ($f_{OUT} = 400$ MHz) | - | 1.4 | 2.2 | mA | $f_{OUT} = 400$ MHz |
| SID348A | f_{PFD_S} | PFD Frequency (f_{IN} / Reference divider) | 4 | - | 20 | MHz | Spreading off/on |
| SID349A | f_{PFD_F} | PFD Frequency (f_{IN} / Reference divider) | 8 | - | 20 | MHz | Fractional operation |
| SID341C | $f_{OUT_400_8S1}$ | Output frequency from PLL Block (spreading on) | 93 | - | 105 | MHz | $f_{PFD} = 8$ MHz, $f_{VCO} = 400$ MHz, $f_{OUT} = 100$ MHz, Modulation frequency: $f_{PFD} / 512$, Modulation depth: -3% |
| SID342C | $t_{PLL_CJIT400_8S1}$ | Cycle to cycle jitter (spreading on) | -710 | - | 710 | ps | $f_{PFD} = 8$ MHz, $f_{VCO} = 400$ MHz, $f_{OUT} = 100$ MHz, Modulation frequency: $f_{PFD} / 512$, Modulation depth: -3% |
| SID341D | $f_{OUT_400_8S2}$ | Output frequency from PLL Block (spreading on) | 93 | - | 105 | MHz | $f_{PFD} = 8$ MHz, $f_{VCO} = 400$ MHz, $f_{OUT} = 100$ MHz, Modulation frequency: $f_{PFD} / 256$, Modulation depth: -3% |
| SID342D | $t_{PLL_CJIT400_8S2}$ | Cycle to cycle jitter (spreading on) | -710 | - | 710 | ps | $f_{PFD} = 8$ MHz, $f_{VCO} = 400$ MHz, $f_{OUT} = 100$ MHz, Modulation frequency: $f_{PFD} / 256$, Modulation depth: -3% |

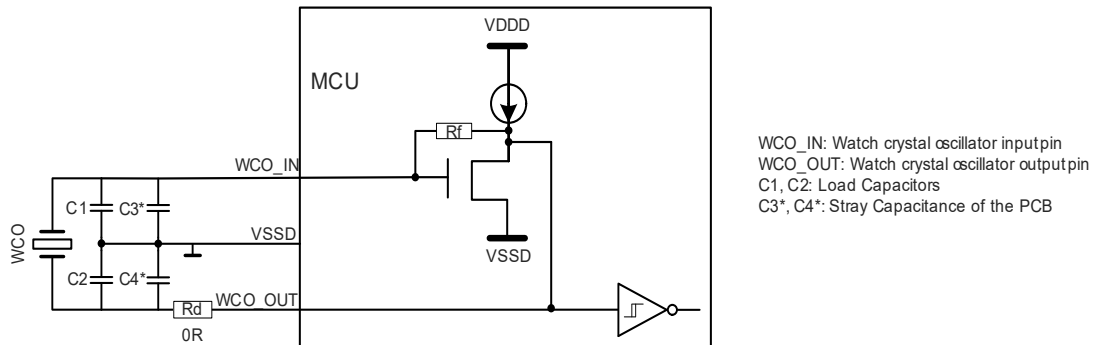
Table 25-27. FLL Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-----------------|---------------------------------|------|-----|-----|---------|--|
| SID350 | t_{FLL_WAKE} | FLL wake up time | – | – | 5 | μs | Wakeup with $< 10\text{ }^{\circ}C$ temperature change while in DeepSleep. $f_{FLL_IN} = 8\text{ MHz}$, $f_{FLL_OUT} = 100\text{ MHz}$, Time from stable reference clock until FLL frequency is within 5% of final value |
| SID351 | f_{FLL_OUT} | Output frequency from FLL block | 24 | – | 100 | MHz | Output range of FLL divided-by-2 output |
| SID352 | FLL_CJIT | FLL frequency accuracy | –1 | – | 1 | % | This is added to the error of the source |
| SID353 | f_{FLL_IN} | Input frequency | 0.25 | – | 80 | MHz | |
| SID354 | I_{FLL} | FLL operating current | – | 250 | 360 | μA | Reference clock: IMO, CCO frequency: 200 MHz, FLL frequency: 100 MHz, guaranteed by design |

Table 25-28. WCO Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-------------------|-----------------------------------|-----|--------|------|---------|----------------------------------|
| SID360 | f_{WCO} | Crystal frequency | – | 32.768 | – | kHz | Maximum drive level: 0.5 μW |
| SID361 | WCO_DC | WCO duty cycle | 10 | – | 90 | % | |
| SID362 | t_{START_WCO} | WCO start up time ^[66] | – | – | 1000 | ms | For Grade-S devices |
| SID362E | t_{START_WCOE} | WCO start-up time ^[66] | – | – | 1400 | ms | For Grade-E devices |
| SID363 | I_{WCO} | WCO current | – | 1.4 | – | μA | |

Figure 25-22.WCO Connection Scheme^[67]



WCO_IN: Watch crystal oscillator inputpin
WCO_OUT: Watch crystal oscillator outputpin
C1, C2: Load Capacitors
C3*, C4*: Stray Capacitance of the PCB

Note

66. Mainly depends on the external crystal.

67. Refer to the family-specific Architecture TRM for more information on crystal requirements (002-24401, TRAVEO(TM) II AUTOMOTIVE BODY CONTROLLER HIGH FAMILY ARCHITECTURE TECHNICAL REFERENCE MANUAL (TRM)).

Table 25-29. External Clock Input Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|------------------|--------------------------------|------|-----|-----|-------|---|
| SID366 | f _{EXT} | External clock input frequency | 0.25 | – | 80 | MHz | For EXT_CLK pin (all input level settings: CMOS, TTL, Automotive) |
| SID367 | EXT_DC | External clock duty cycle | 45 | – | 55 | % | |

Table 25-30. MCWDT Timeout Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|---------------------|-----------------------|-----|-----|------|-------|---|
| SID410 | t _{MCWDT1} | Minimum MCWDT timeout | 57 | – | – | μs | When using the ILO (32.768 kHz + 7%) and 16-bit MCWDT counter Guaranteed by design |
| SID411 | t _{MCWDT2} | Maximum MCWDT timeout | – | – | 2.15 | s | When using the ILO (32.768 kHz – 7%) and 16-bit MCWDT counter Guaranteed by design |

Table 25-31. WDT Timeout Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-------------------|---------------------|-----|-----|-------|-------|--|
| SID412 | t _{WDT1} | Minimum WDT timeout | 57 | – | – | μs | When using the ILO (32.768 kHz + 7%) and 16-bit WDT counter, guaranteed by design |
| SID413 | t _{WDT2} | Maximum WDT timeout | – | – | 39.15 | h | When using the ILO (32.768 kHz – 7%) and 16-bit WDT counter, guaranteed by design |
| SID414 | t _{WDT3} | Default WDT timeout | – | 125 | – | ms | When using the ILO and 32-bit WDT counter at 0x1000 (default value), guaranteed by design |

25.12 Clock Timing Diagrams

Figure 25-23. ECO to PLL or FLL Diagram

ECO: 8 MHz
 PLL: 160 MHz
 FLL: 100 MHz

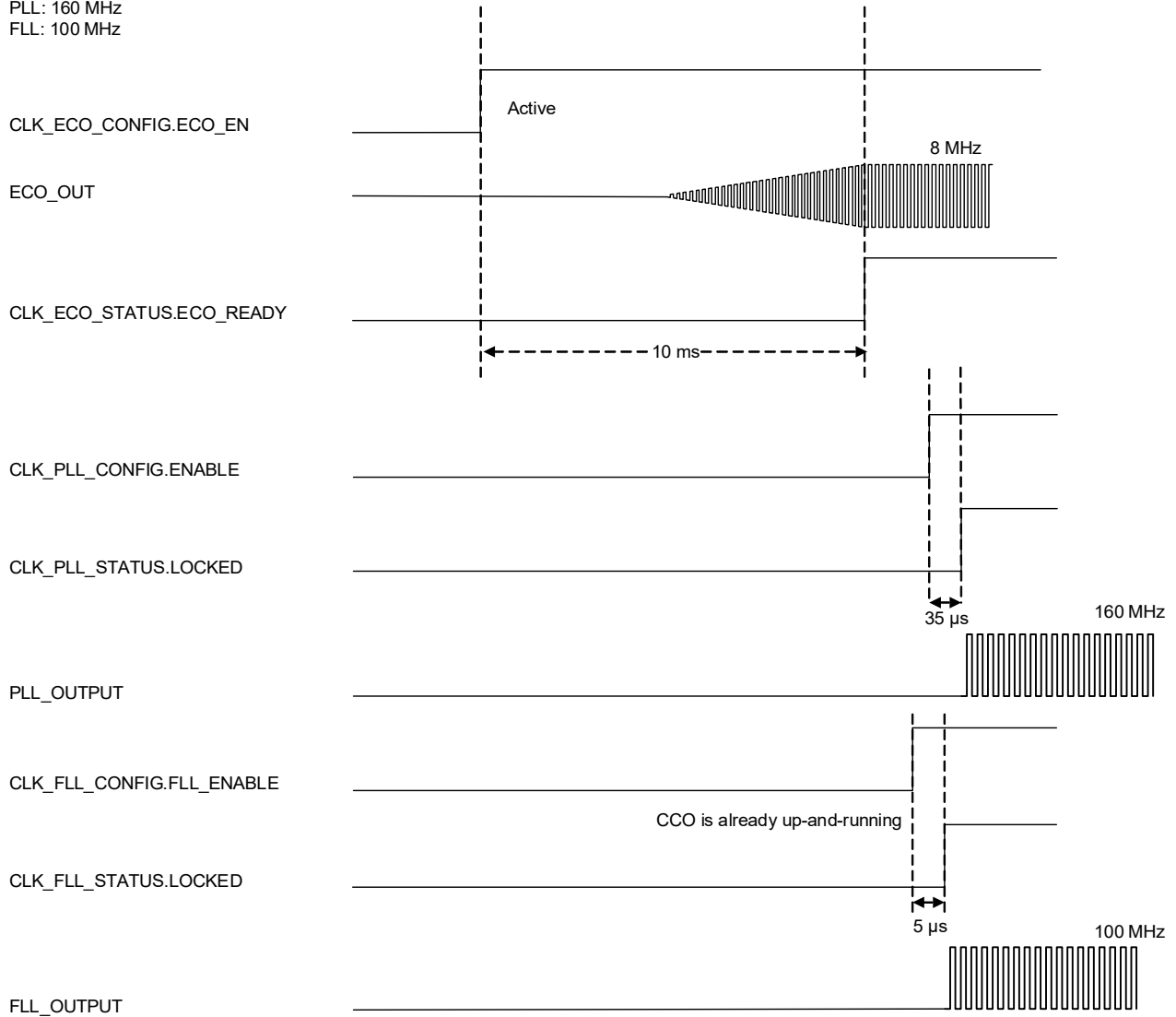
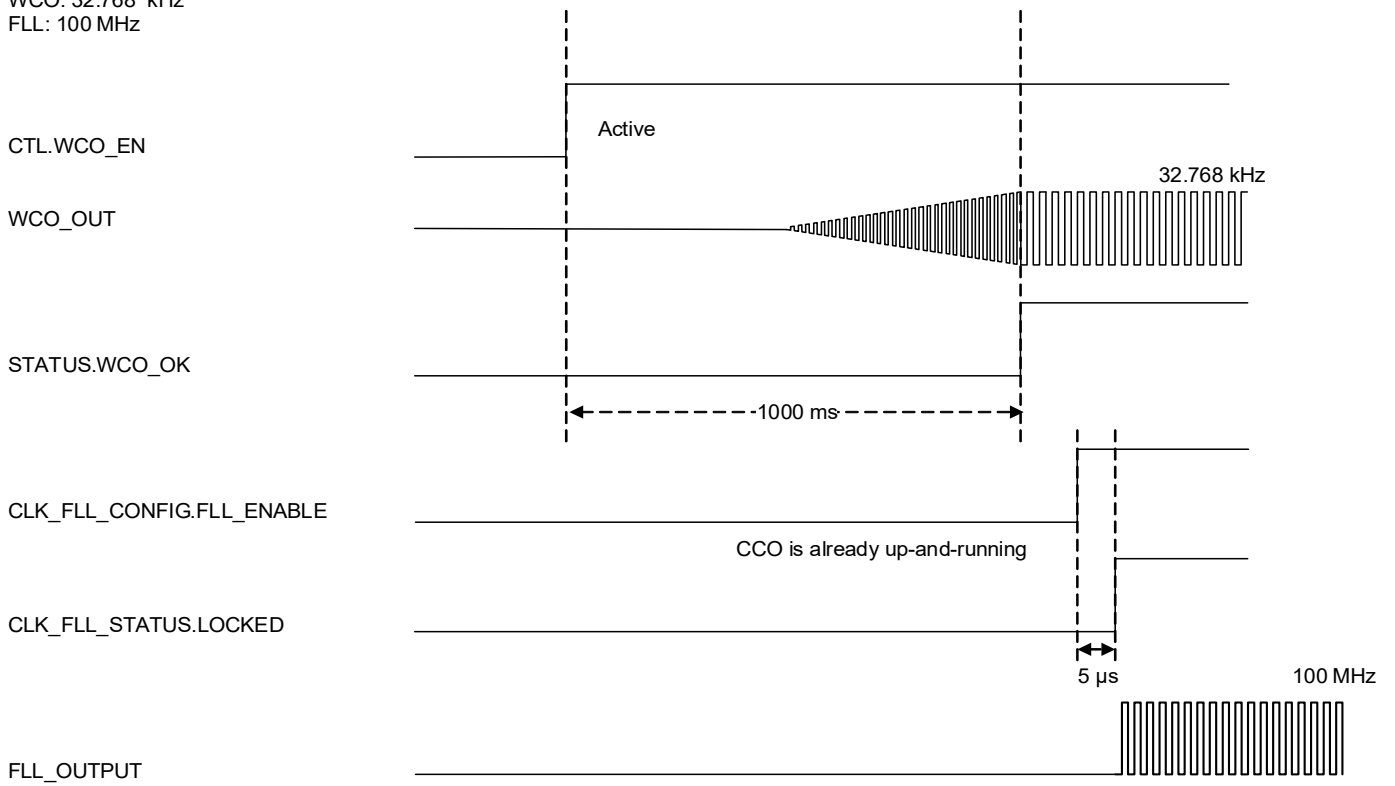


Figure 25-24.WCO to FLL Diagram

WCO: 32.768 kHz
FLL: 100 MHz



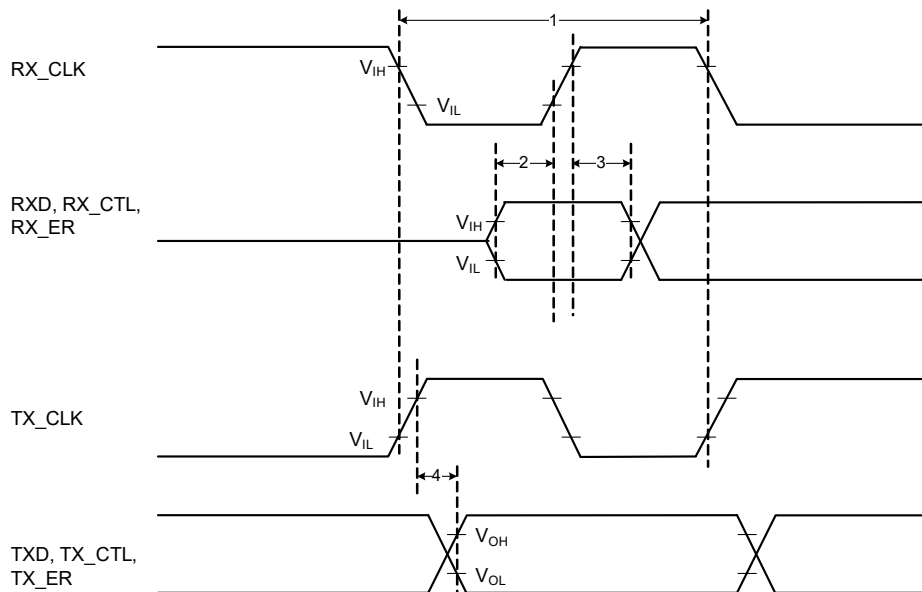
25.13 Ethernet Specifications
Table 25-32. Ethernet Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|-----------------------|---|-------|-----|-------|-------|--|
| Ethernet General Specifications | | | | | | | |
| SID368 | f _{SYS} | System clock max frequency | – | – | 100 | MHz | Guaranteed by design |
| SID369 | f _{AXI} | AXI clock max frequency | – | – | 200 | MHz | Guaranteed by design |
| SID370 | V _{ETH} | Ethernet MAC IO supply voltage | 3.0 | – | 3.6 | V | For V _{DDD} or V _{DDIO_4} |
| SID364A | C _L | Load capacitance | – | – | 10 | pF | For all signals between MAC and PHY |
| SID365B | t _{RF} | Rise / fall time | – | – | 0.99 | ns | 20% to 80%, for GMII and RGMII using HSIO_STD |
| SID365A | t _{RF} | Rise / fall time | – | – | 2 | ns | 20% to 80%, for MII and GMII using GPIO_STD and HSIO_STD |
| Ethernet MII Specifications for GPIO_STD/HSIO_STD | | | | | | | |
| SID375 | f _{TXRX_CLK} | MI I TX/RX_CLK Clock frequency | – | 25 | – | MHz | |
| SDI376 | DUTY_REF | Duty cycle of reference clock | 40 | – | 60 | % | |
| SID372 | t _{SKWEWT} | MI I Transmit data (TXD, TX_CTL, TX_ER) valid after TX_CLK | 0.5 | – | 25 | ns | |
| SID373 | t _{SUR} | MI I Receive data setup to RX_CLK rising edge | 10 | – | – | ns | |
| SID374 | t _{HOLDR} | MI I Receive data hold to RX_CLK rising edge | 10 | – | – | ns | |
| Ethernet RMII Specifications for GPIO_STD/HSIO_STD | | | | | | | |
| SID375A | f _{REF_CLK} | RMII reference Clock frequency | – | 50 | – | MHz | External clock |
| SID376A | DUTY_REF | Duty cycle of reference clock | 40 | – | 60 | % | |
| SID377 | t _{SU} | RXD[1:0], RX_CTL, RX_ER Data Setup to REF_CLK rising edge | 4 | – | – | ns | |
| SID378 | t _{HOLD} | RXD[1:0], RX_CTL, RX_ER, Data hold from REF_CLK rising edge | 2 | – | – | ns | |
| SID393 | t _{TXOUT} | TX_EN, TXD[1:0], Data output delay from REF_CLK rising edge | 2 | – | 14 | ns | |
| Ethernet GMII Specifications for HSIO_STD | | | | | | | |
| SID379 | f _{P_REFCLK} | REF_CLK clock frequency | – | 125 | – | MHz | |
| SID380 | f _{P_RXCLK} | RX_CLK clock frequency | – | 125 | – | MHz | |
| SID389 | DUTY_G | Clock Duty cycle for Gigabit | 31.25 | – | 68.75 | % | |
| SID381 | t _{SETUPT} | TXD, TX_CTL, TX_ER Setup to GTX_CLK rising edge | 2.5 | – | – | ns | |
| SID382 | t _{HOLDT} | TXD, TX_CTL, TX_ER Hold from GTX_CLK rising edge | 0.5 | – | – | ns | |
| SID383 | t _{SETUPR} | RXD, RX_CTL, RX_ER Setup to RX_CLK rising edge | 2 | – | – | ns | |
| SID384 | t _{HOLDR} | RXD, RX_CTL, RX_ER Hold from RX_CLK rising edge | 0 | – | – | ns | |
| Ethernet RGMII Specifications for HSIO_STD | | | | | | | |
| SID385 | f _{CYC} | REF_CLK, TX_CLK and RX_CLK clock frequency | – | 125 | – | MHz | |
| SID386 | DUTY_G | Duty cycle for gigabit | 45 | – | 55 | % | |

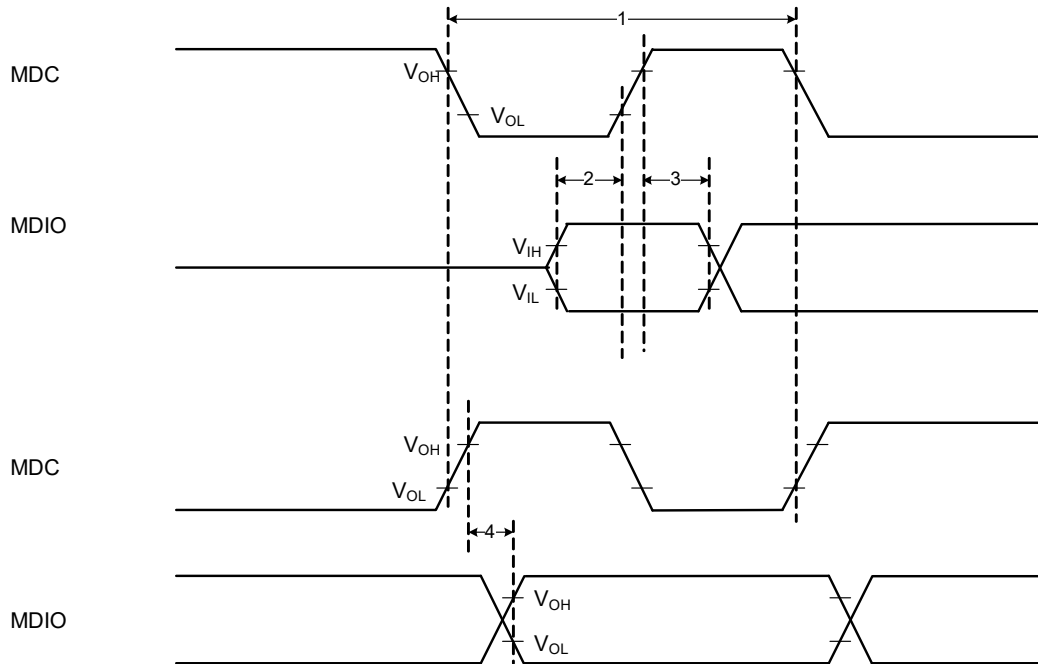
Table 25-32. Ethernet Specifications (continued)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|-------------|--|------|-----|-----|-------|--------------------|
| SID387 | t_{SKEWT} | Data to clock output skew | -0.5 | - | 0.5 | ns | |
| SID388 | t_{SKEWR} | Data to clock input skew | 1 | - | 2.6 | ns | |
| Ethernet MDIO Specifications for GPIO_STD/HSIO_STD | | | | | | | |
| SID395 | t_{MDCYC} | MDC clock cycle | 400 | - | - | ns | |
| SID396 | t_{MDIS} | MDIO input setup time to MDC rising edge | 100 | - | - | ns | |
| SID397 | t_{MDIH} | MDIO input hold time to MDC rising edge | 0 | - | - | ns | |
| SID398 | t_{MDIO} | MDIO output skew from MDC rising edge | 10 | - | 390 | ns | |

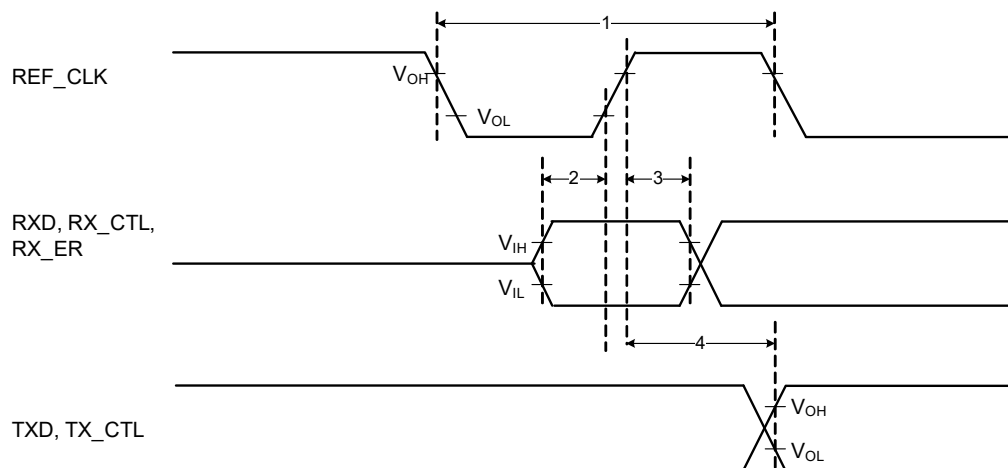
Figure 25-25.MII Timing Diagram



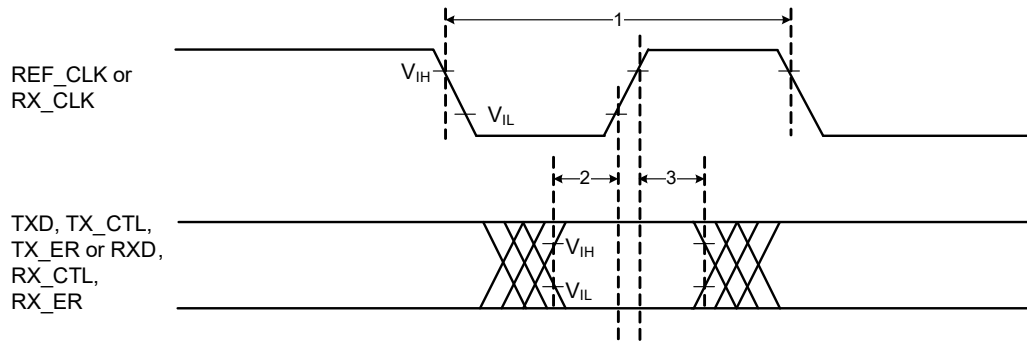
- 1: RX_CLK or TX_CLK cycle = $1/f_{TXRX_CLK}$
- 2: MII receive data setup time to RX_CLK rising edge = t_{SUR}
- 3: MII receive data hold time to RX_CLK rising edge = t_{HOLDR}
- 4: MII transmit data valid after TX_CLK rising edge = t_{SKEWT}

Figure 25-26.MDIO Timing Diagram


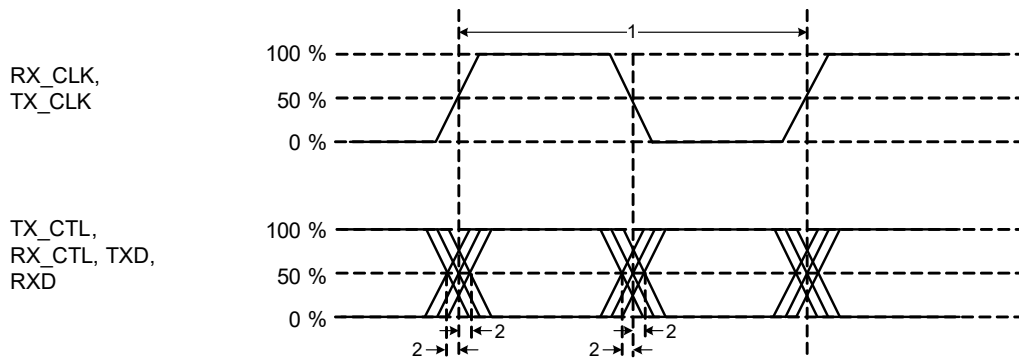
- 1: MDC clock cycle = t_{MDCCYC}
- 2: MDIO input setup time to MDC rising edge = t_{MDIS}
- 3: MDIO input hold time to MDC rising edge = t_{MDIH}
- 4: MDIO output skew from MDC rising edge = t_{MDIO}

Figure 25-27.RMII Timing Diagram


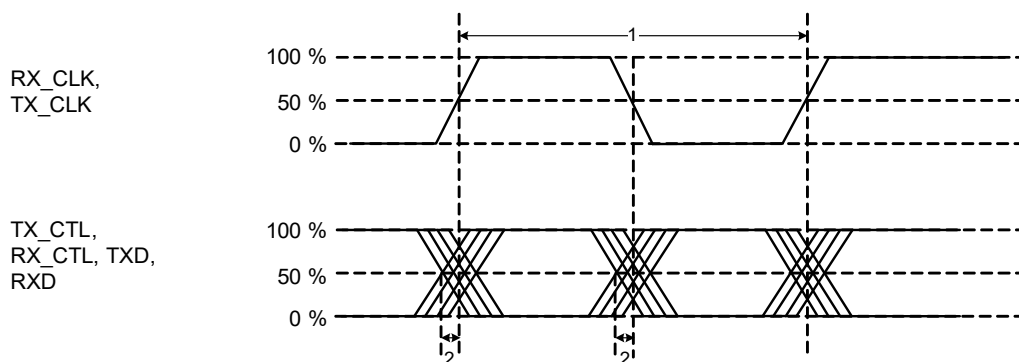
- 1: RMII reference clock cycle = $1/f_{REF_CLK}$
- 2: Data setup to REF_CLK rising edge = t_{SU}
- 3: Data hold from REF_CLK rising edge = t_{HOLD}
- 4: Data output delay from REF_CLK rising edge = t_{TXOUT}

Figure 25-28.GMII Timing Diagram


- 1: REF_CLK or RX_CLK cycle = $1/f_{P_REFCLK} = 1/f_{P_RXCLK}$
- 2: Data setup to REF_CLK or RX_CLK rising edge = t_{SETUPD} or t_{SETUPR}
- 3: Data hold from REF_CLK or RX_CLK rising edge = t_{HOLDT} or t_{HOLDR}

Figure 25-29.RGMII Tx Timing Diagram


- 1: TX_CLK and RX_CLK clock cycle = $1/f_{CYC}$
- 2: Data to clock output skew = t_{SKEWT}

Figure 25-30.RGMII Rx Timing Diagram


- 1: TX_CLK and RX_CLK clock cycle = $1/f_{CYC}$
- 2: Data to clock input skew = t_{SKEWR}

25.14 SDHC Specifications
Table 25-33. SDHC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|--|-----------------------------|---|-----|-----|-----|-------|--|
| SDHC and eMMC Specifications (The source clock must be divided by 2 or more in DDR modes) | | | | | | | |
| SID801 | V _{SDHC} | SDHC IO supply voltage | 2.7 | – | 3.6 | V | For V _{DDIO_1} or V _{DDIO_3} |
| SID802 | I _{ODS} | I/O drive select | 8 | – | 8 | mA | drive_sel<1:0>= 0b00 for all modes |
| SID803 | t _{IT} | Input transition time | 0.7 | – | 3 | ns | |
| SD: DS Timing Specifications for GPIO_STD/HSIO_STD | | | | | | | |
| SID810 | f _{LP} | Interface clock period | – | – | 25 | MHz | 40-ns period |
| SID812 | C _D | I/O loading at DATA/CMD pins | 40 | – | 40 | pF | |
| SID813 | C _C | I/O loading at CLK pins | 40 | – | 40 | pF | |
| SID814 | t _{OS} | Output setup time of CMD/DAT prior to CLK | 5.5 | – | – | ns | |
| SID815 | t _{OH} | Output hold time of CMD/DAT after CLK | 5.5 | – | – | ns | |
| SID816 | t _{IS_LP} | Input setup time of CMD/DAT prior to CLK | 24 | – | – | ns | Clock period - Output delay |
| SID818 | t _{IH} | Input hold time of CMD/DAT after CLK | 0 | – | – | ns | |
| SD: HS Timing Specifications for HSIO_STD | | | | | | | |
| SID820 | f _{LP_SD_HS} | Interface clock period | – | – | 50 | MHz | 20-ns period |
| SID822 | C _{D_SD_HS} | I/O loading at DATA/CMD pins | 40 | – | 40 | pF | |
| SID823 | C _{C_SD_HS} | I/O loading at CLK pins | 40 | – | 40 | pF | |
| SID824 | t _{OS_SD_HS} | Output setup time of CMD/DAT prior to CLK | 6.5 | – | – | ns | |
| SID825 | t _{OH_SD_HS} | Output hold time of CMD/DAT after CLK | 2.5 | – | – | ns | |
| SID826 | t _{IS_LP_SD_HS} | Input setup time of CMD/DAT prior to CLK | 4 | – | – | ns | Clock period less output delay |
| SID828 | t _{IH_SD_HS} | Input hold time of CMD/DAT after CLK | 2.5 | – | – | ns | |
| eMMC: BWC Timing Specifications for GPIO_STD/HSIO_STD | | | | | | | |
| SID870 | f _{LP_eMMC_BWC} | Interface clock period | – | – | 26 | MHz | 38.4-ns period |
| SID872 | C _{D_eMMC_BWC} | I/O loading at DATA/CMD pins | 30 | – | 30 | pF | |
| SID873 | C _{C_eMMC_BWC} | I/O loading at CLK pins | 30 | – | 30 | pF | |
| SID874 | t _{OS_eMMC_BWC} | Output setup time of CMD/DAT prior to CLK | 3.5 | – | – | ns | |
| SID875 | t _{OH_eMMC_BWC} | Output hold time of CMD/DAT after CLK | 3.5 | – | – | ns | |
| SID876 | t _{IS_LP_eMMC_BWC} | Input setup time of CMD/DAT prior to CLK | 9.7 | – | – | ns | Clock period less output delay |
| SID878 | t _{IH_eMMC_BWC} | Input hold time of CMD/DAT after CLK | 8.3 | – | – | ns | |
| eMMC: SDR Timing Specifications for HSIO_STD | | | | | | | |
| SID880 | f _{LP_eMMC_SDR} | Interface clock period | – | – | 52 | MHz | 19.2-ns period |
| SID882 | C _{D_eMMC_SDR} | I/O loading at DATA/CMD pins | 30 | – | 30 | pF | |
| SID883 | C _{C_eMMC_SDR} | I/O loading at CLK pins | 30 | – | 30 | pF | |

Table 25-33. SDHC Specifications (continued)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|-----------------------------|---|-----|-----|-----|-------|--------------------------------|
| SID884 | t _{OS_eMMC_SDR} | Output setup time of CMD/DAT prior to CLK | 3.5 | – | – | ns | |
| SID885 | t _{OH_eMMC_SDR} | Output hold time of CMD/DAT after CLK | 3.5 | – | – | ns | |
| SID886 | t _{IS_LP_eMMC_SDR} | Input setup time of CMD/DAT prior to CLK | 3.5 | – | – | ns | Clock period less output delay |
| SID888 | t _{IH_eMMC_SDR} | Input hold time of CMD/DAT after CLK | 2.5 | – | – | ns | |
| eMMC: DDR Timing Specifications for HSIO_STD | | | | | | | |
| SID890 | f _{LP_eMMC_DDR} | Interface clock period | – | – | 52 | MHz | 19.2-ns period |
| SID892 | DUTY_CLK_eMMC_DDR | Duty cycle of output CLK | 45 | – | 55 | % | |
| SID893 | C _{D_eMMC_DDR} | I/O loading at DATA/CMD pins | 20 | – | 20 | pF | |
| SID894 | C _{C_eMMC_DDR} | I/O loading at CLK pins | 20 | – | 20 | pF | |
| SID895 | t _{OS_eMMC_DDR} | Output setup time of CMD/DAT prior to CLK | 2.6 | – | – | ns | |
| SID896 | t _{OH_eMMC_DDR} | Output hold time of CMD/DAT after CLK | 2.6 | – | – | ns | |
| SID897 | t _{IS_LP_eMMC_DDR} | Input setup time of CMD/DAT prior to CLK | 2.4 | – | – | ns | Clock period less output delay |
| SID899 | t _{IH_eMMC_DDR} | Input hold time of CMD/DAT after CLK | 1.5 | – | – | ns | |

25.15 FlexRay Specifications
Table 25-34. FlexRay Specification

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|------------------------------------|---------------------------|--|----------------------------|-----|----------------------------|-------|--|
| SID465 | f _{CLK_S} | System clock (clk_sys) frequency | – | – | 80 | MHz | Guaranteed by design, Reference clock: ECO |
| SID466 | f _{CLK_P} | FlexRay clock (clk_peri) frequency | – | – | 80 | MHz | Guaranteed by design, Reference clock: ECO |
| SID470 | V _{FR} | FlexRay I/O supply voltage (V _{DDIO_2}) | 3.0 | – | 5.5 | V | drive_sel<1:0> = 0b00 |
| TxEN output characteristics | | | | | | | |
| SID450 | t _{CCTxENRISE25} | Rise time of TxEN signal at CC | – | – | 9 | ns | 20% to 80%, 25-pF load |
| SID451 | t _{CCTxENFALL25} | Fall time of TxEN signal at CC | – | – | 9 | ns | 20% to 80%, 25-pF load |
| SID452 | t _{CCTxEN01} | Sum of delay between TP1_FF and TP1_CC and delays derived from TP1_FFi, rising edge TxEN | – | – | 25 | ns | 20% to 80%, 25-pF load, guaranteed by design |
| SID453 | t _{CCTxEN10} | Sum of delay between TP1_FF and TP1_CC and delays derived from TP1_FFi, falling edge TxEN | – | – | 25 | ns | 20% to 80%, 25-pF load, guaranteed by design |
| SID468 | C _{TXEN} | I/O loading at TxEN pin | – | – | 25 | pF | |
| TxD output characteristics | | | | | | | |
| SID454 | t _{CCTxASYM} | Asymmetry of sending CC (= t _{CCTxD} 50% – 100 ns) | –2.45 | – | 2.45 | ns | 25-pF load, guaranteed by design |
| SID455 | t _{CCTxDRF25} | Sum of rise and fall time | – | – | 9 | ns | 20% to 80%, 25-pF load |
| SID455A | t _{CCTxDR15} | Rise time of TxD signal | – | – | 2.5 | ns | 30% to 70%, 15-pF load |
| SID455B | t _{CCTxDF15} | Fall time of TxD signal | – | – | 2.5 | ns | 30% to 70%, 15-pF load |
| SID456 | t _{CCTxD01} | Sum of delay between clock to Q of the last FF and the final output buffer, rising edge TxD | – | – | 25 | ns | 20% to 80%, 25-pF load, guaranteed by design |
| SID457 | t _{CCTxD10} | Sum of delay between clock to Q of the last FF and the final output buffer, falling edge TxD | – | – | 25 | ns | 20% to 80%, 25-pF load, guaranteed by design |
| SID469 | C _{TXD} | I/O loading at TxD pin | – | – | 25 | pF | |
| RxD input characteristics | | | | | | | |
| SID458 | C _{CCRxD} | Input capacitance on RxD pin | – | – | 10 | pF | |
| SID459 | V _{CCLogic_1} | Threshold for detecting logical HIGH | 0.35 × V _{DDIO_2} | – | 0.70 × V _{DDIO_2} | V | |
| SID460 | V _{CCLogic_0} | Threshold for detecting logical LOW | 0.30 × V _{DDIO_2} | – | 0.65 × V _{DDIO_2} | V | |
| SID461 | t _{CCRxD01} | Sum of delay from actual input to the D input of the first FF, rising edge RxD | – | – | 10 | ns | Guaranteed by design |
| SID462 | t _{CCRxD10} | Sum of delay from actual input to the D input of the first FF, falling edge RxD | – | – | 10 | ns | Guaranteed by design |
| Receiver asymmetry | | | | | | | |
| SID463 | t _{CCRxASYMAC15} | Acceptance of asymmetry at receiving CC with 15-pF load | –31.5 | – | 44 | ns | For all data rates including clock deviation of ±500 ppm |
| SID464 | t _{CCRxASYMAC25} | Acceptance of asymmetry at receiving CC with 25-pF load | –30.5 | – | 43 | ns | For all data rates including clock deviation of ±500 ppm |

25.16 Audio Subsystem Specifications
Table 25-35. Audio Subsystem Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|--|--------------------------|--|---------------------------|-----|---------------------------|-------|---|
| SID770 | f _{AUDIO} | Audio subsystem frequency | – | – | 200 | MHz | Guaranteed by design |
| SID772 | V _{AUDIO} | Audio Sub System I/O supply voltage | 3.0 | – | 3.6 | V | For V _{DDIO_2} |
| SID773 | V _{OL_A} | Output Voltage LOW level | – | – | 0.4 | V | drive_sel<1:0> = 0b0X, Pull-up, pull-down: off |
| SID774 | V _{OH_A} | Output Voltage HIGH level | V _{DDIO_2} – 0.5 | – | – | V | drive_sel<1:0> = 0b0X, Pull-up, pull-down: off |
| SID775 | V _{IH_CMOS_A} | Input Voltage HIGH threshold in CMOS mode | 0.7 × V _{DDIO_2} | – | – | V | |
| SID776 | V _{IL_CMOS_A} | Input Voltage LOW threshold in CMOS mode | – | – | 0.3 × V _{DDIO_2} | V | |
| I²S/TDM Word Clock Frequency | | | | | | | |
| SID796 | f _{WS_I2S} | WS Clock Rate in I ² S mode | 8 | – | 192 | kHz | Guaranteed by design |
| SID797 | f _{WS_TDM} | WS Clock Rate in TDM mode | – | – | 96 | kHz | Guaranteed by design |
| SID798 | Word | Length of I ² S Word | 8 | – | 32 | bit | Guaranteed by design |
| I²S/TDM Master Mode | | | | | | | |
| SID740 | t _{D_WS} | Delay Time of TX/RX_WS Output Transition from Falling Edge of TX/RX_SCK Output | –8 | – | 9 | ns | Except TDM 96 kHz mode, TX/RX_WS output and TX/RX_SCK output with drive_sel<1:0> = 0b 01, guaranteed by design |
| SID740A | t _{D_WS_TDM96A} | Delay Time of TX/RX_WS output Transition from Falling Edge of TX/RX_SCK output | –8 | – | 11 | ns | TDM 96 kHz mode, TX/RX_WS output with drive_sel<1:0> = 0b01 and TX/RX_SCK output with drive_sel<1:0> = 0b00, guaranteed by design |
| SID741 | t _{D_SDO} | Delay Time of TX_SDO Transition from Falling Edge of TX_SCK Output | –8 | – | 8 | ns | TX_SDO and TX_SCK output with drive_sel<1:0> = 0b01 for except TDM 96 kHz mode, guaranteed by design |
| SID741A | t _{D_SDO_TDM96} | Delay Time of TX_SDO Transition from Falling Edge of TX_SCK Output | –8 | – | 8 | ns | TX_SDO with drive_sel<1:0> = 0b01 and TX_SCK output with drive_sel<1:0> = 0b00 for TDM 96 kHz mode, guaranteed by design |

Table 25-35. Audio Subsystem Specifications (continued)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|--------------------------------------|--------------------|--|------------------------|-----|----------------------|-------|--|
| SID742 | t_{S_SDI} | RX_SDI Setup Time to the Following Rising Edge of RX_SCK Output (RX_CTL.B_CLOCK_INV = 0) | 11 | – | – | ns | RX_SCK output with drive_sel<1:0> = 0b00, guaranteed by design |
| SID743 | t_{H_SDI} | RX_SDI Hold Time to the Rising Edge of RX_SCK Output (RX_CTL.B_CLOCK_INV = 0) | $t_{MCLK_SOC} - 0.9$ | – | – | ns | RX_SCK output with drive_sel<1:0> = 0b00, guaranteed by design |
| SID744 | t_{S_SDI1} | RX_SDI Setup Time to the Following Falling Edge of RX_SCK Output (RX_CTL.B_CLOCK_INV = 1) | 11 | – | – | ns | RX_SCK output with drive_sel<1:0> = 0b00, guaranteed by design |
| SID745 | t_{H_SDI1} | RX_SDI Hold Time to the Falling Edge of RX_SCK Output (RX_CTL.B_CLOCK_INV = 1) | $t_{MCLK_SOC} - 0.9$ | – | – | ns | RX_SCK output with drive_sel<1:0> = 0b00, guaranteed by design |
| SID746 | t_{SCKCY} | TX/RX_SCK Output Bit Clock Duty Cycle | 45 | – | 55 | % | Guaranteed by design |
| SID748 | f_{MCLK_SOC} | MCLK input clock frequency | 1.024 | – | 196.608 | MHz | Internal Fractional PLL, guaranteed by design |
| SID748A | $f_{MCLK_SOC_E}$ | MCLK input clock frequency | 1.024 | – | 98.304 | MHz | External clock |
| SID749 | t_{MCLK_SOC} | MCLK input clock period | 5.086 | – | 976.563 | ns | Guaranteed by design |
| SID750 | t_{JITTER} | MCLK Input clock jitter tolerance | –200 | – | 200 | ps | Guaranteed by design |
| SID748B | f_{MCLK} | MCLK output clock frequency | 1.024 | – | 25 | MHz | MCLK output with drive_sel<1:0> = 0b00 Guaranteed by design |
| SID748C | f_{MCLK1} | MCLK output clock frequency | 1.024 | – | 15 | MHz | MCLK output with drive_sel<1:0> = 0b01 Guaranteed by design |
| SID749B | f_{MCLK_DT} | MCLK output clock duty | 45 | – | 55 | % | Guaranteed by design |
| I²S/TDM Slave Mode | | | | | | | |
| SID751 | t_{S_WS} | TX/RX_WS Input Alignment Clock Setup Time to the following Rising Edge of TX/RX_SCK Input | 5 | – | – | ns | Guaranteed by design |
| SID752 | t_{H_WS} | TX/RX_WS Input Alignment Clock Hold Time to the Rising Edge of TX/RX_SCK Input | $t_{MCLK_SOC} + 5.0$ | – | – | ns | Guaranteed by design |
| SID753 | t_{D_SDO} | Delay Time of TX_SDO Transition from Falling Edge of TX_SCK Input (TX_CTL.B_CLOCK_INV = 0) | $-t_{MCLK_SOC} + 5.0$ | – | $t_{MCLK_SOC} + 15$ | ns | TX_SDO with drive_sel<1:0> = 0b00, guaranteed by design |

Table 25-35. Audio Subsystem Specifications (continued)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|---------------|---|------------------------|-----|----------------------|-------|--|
| SID754 | t_{D_SDO1} | Delay Time of TX_SDO Transition from Rising Edge of TX_SCK Input (TX_CTL.B_CLOCK_INV = 1) | $-t_{MCLK_SOC} + 5.0$ | – | $t_{MCLK_SOC} + 15$ | ns | TX_SDO with drive_sel<1:0>= 0b00, guaranteed by design |
| SID755 | t_{S_SDI} | RX_SDI Setup Time to the Following Rising Edge of RX_SCK Input | 5 | – | – | ns | Guaranteed by design |
| SID756 | t_{H_SDI} | RX_SDI Hold Time to the Rising Edge of RX_SCK Input | $t_{MCLK_SOC} + 5.0$ | – | – | ns | Guaranteed by design |
| SID757 | t_{SCKCY} | TX/RX_SCK Input Bit Clock Duty Cycle | 45 | – | 55 | % | Guaranteed by design |

25.17 Serial Memory Interface Specifications
Table 25-36. SMIF Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|-------------------------------|---|------------------------------|-----|------|-------|--|
| SMIF DC Specification | | | | | | | |
| SID785 | V _{SMIF} | SMIF I/O supply voltage | 2.7 | – | 3.6 | V | For V _{DDIO_1} or V _{DDIO_3} |
| SMIF HSSPI(SDR) Specification for HSIO_STD | | | | | | | |
| SID760 | C _{L_SDR_HSIO} | Load capacitance | – | – | 30 | pF | |
| SID761 | SR _{_SDR_HSIO} | Input rise and fall slew rates | 1.5 | – | – | V/ns | Guaranteed by design |
| SID762 | f _{CK_SDR_HSIO} | Clock frequency | – | – | 100 | MHz | |
| SID763 | t _{CK_SDR_HSIO} | Clock period | 1 / f _{CK_SDR_HSIO} | – | – | ns | |
| SID764 | DCK _{_SDR_HSIO} | Clock duty | 45 | – | 55 | % | |
| SID765 | CSR _{_SDR_HSIO} | Clock rise and fall slew rates | 1.5 | – | – | V/ns | |
| SID766 | t _{CS_SDR_HSIO} | Chip select HIGH time | 10 | – | – | ns | |
| SID767 | t _{CSS_SDR_HSIO} | Chip select active setup time | 3 | – | – | ns | |
| SID768 | t _{CSH_SDR_HSIO} | Chip select active hold time | 5 | – | – | ns | |
| SID769 | t _{SU_SDR_HSIO} | Data setup time | 1.5 | – | – | ns | |
| SID780 | t _{HD_SDR_HSIO} | Data hold time | 2 | – | – | ns | |
| SID781 | t _{V_SDR_HSIO} | Clock LOW output valid | 1.5 | – | 7.65 | ns | |
| SID782 | t _{HO_SDR_HSIO} | Input hold time | 2 | – | – | ns | |
| SID783 | t _{DIS_SDR_HSIO} | Input disable time | 0 | – | 7.5 | ns | Guaranteed by design |
| SID784 | t _{IO_SKEW_SDR_HSIO} | Data skew (first data bit to last data bit) | – | – | 0.6 | ns | Guaranteed by design |
| SMIF HSSPI(SDR) Specification for GPIO_STD | | | | | | | |
| SID760A | C _{L_SDR_GPIO} | Load capacitance | – | – | 30 | pF | |
| SID761A | SR _{_SDR_GPIO} | Input rise and fall slew rates | 1 | – | – | V/ns | Guaranteed by design |
| SID762A | f _{CK_SDR_GPIO} | Clock frequency | – | – | 32 | MHz | |
| SID763A | t _{CK_SDR_GPIO} | Clock period | 1 / f _{CK_SDR_GPIO} | – | – | ns | |
| SID764A | DCK _{_SDR_GPIO} | Clock duty | 45 | – | 55 | % | |
| SID765A | CSR _{_SDR_GPIO} | Clock rise and fall slew rates | 1 | – | – | V/ns | |
| SID766A | t _{CS_SDR_GPIO} | Chip select HIGH time | 30 | – | – | ns | |
| SID767A | t _{CSS_SDR_GPIO} | Chip select active setup time | 9 | – | – | ns | |
| SID768A | t _{CSH_SDR_GPIO} | Chip select active hold time | 15 | – | – | ns | |
| SID769A | t _{SU_SDR_GPIO} | Data setup time | 4.5 | – | – | ns | |
| SID780A | t _{HD_SDR_GPIO} | Data hold time | 6 | – | – | ns | |
| SID781A | t _{V_SDR_GPIO} | Clock LOW output valid | 4.5 | – | 9 | ns | |
| SID782A | t _{HO_SDR_GPIO} | Input hold time | 2 | – | – | ns | |
| SID783A | t _{DIS_SDR_GPIO} | Input disable time | 0 | – | 22.5 | ns | Guaranteed by design |
| SID784A | t _{IO_SKEW_SDR_GPIO} | Data skew (first data bit to last data bit) | – | – | 1.8 | ns | Guaranteed by design |
| SMIF HSSPI(DDR) Specification for HSIO_STD | | | | | | | |
| SID760B | C _{L_DDR_HSIO} | Load capacitance | – | – | 15 | pF | |
| SID761B | SR _{_DDR_HSIO} | Input rise and fall slew rates | 1.5 | – | – | V/ns | Guaranteed by design |
| SID762B2 | f _{CK_DDR_HSIO} | Clock frequency | – | – | 90 | MHz | |

Table 25-36. SMIF Specifications (continued)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---------------------------|---|-------------------------|-----|------|-------|---------------------------------------|
| SID763B | $t_{CK_DDR_HSIO}$ | Clock period | 1 / $f_{CK_DDR_HSIO}$ | – | – | ns | |
| SID764B | DCK_DDR_HSIO | Clock duty | 45 | – | 55 | % | |
| SID765B | CSR_DDR_HSIO | Clock rise and fall slew rates | 1.5 | – | – | V/ns | |
| SID766B | $t_{CS_DDR_HSIO}$ | Chip select HIGH time | 10 | – | – | ns | |
| SID767B | $t_{CSS_DDR_HSIO}$ | Chip select active setup time | 4 | – | – | ns | |
| SID768B | $t_{CSH_DDR_HSIO}$ | Chip select active hold time | 4 | – | – | ns | |
| SID769B | $t_{SU_DDR_HSIO}$ | Data setup time | 2 | – | – | ns | |
| SID780B | $t_{HD_DDR_HSIO}$ | Data hold time | 1.2 | – | – | ns | |
| SID781B | $t_{V_DDR_HSIO}$ | Clock LOW output valid | 0 | – | 6.5 | ns | |
| SID782B | $t_{HO_DDR_HSIO}$ | Input hold time | 1 | – | – | ns | |
| SID783B | $t_{DIS_DDR_HSIO}$ | Input disable time | – | – | 7.5 | ns | Guaranteed by design |
| SID784B | $t_{IO_SKEW_DDR_HSIO}$ | Data skew (first data bit to last data bit) | – | – | 0.6 | ns | Guaranteed by design |
| SMIF HSSPI(DDR) Specification for GPIO_STD | | | | | | | |
| SID760C | $C_L_DDR_GPIO$ | Load capacitance | – | – | 15 | pF | |
| SID761C | SR_DDR_GPIO | Input rise and fall slew rates | 1 | – | – | V/ns | Guaranteed by design |
| SID762C | $f_{CK_DDR_GPIO}$ | Clock frequency | – | – | 32 | MHz | |
| SID763C | $t_{CK_DDR_GPIO}$ | Clock period | 1 / $f_{CK_DDR_GPIO}$ | – | – | ns | |
| SID764C | DCK_DDR_GPIO | Clock duty | 45 | – | 55 | % | |
| SID765C | CSR_DDR_GPIO | Clock rise and fall slew rates | 1 | – | – | V/ns | |
| SID766C | $t_{CS_DDR_GPIO}$ | Chip select HIGH time | 30 | – | – | ns | |
| SID767C | $t_{CSS_DDR_GPIO}$ | Chip select active setup time | 5 | – | – | ns | |
| SID768C | $t_{CSH_DDR_GPIO}$ | Chip select active hold time | 4 | – | – | ns | |
| SID769C | $t_{SU_DDR_GPIO}$ | Data setup time | 5 | – | – | ns | |
| SID780C | $t_{HD_DDR_GPIO}$ | Data hold time | 4.5 | – | – | ns | |
| SID781C | $t_{V_DDR_GPIO}$ | Clock LOW output valid | 0 | – | 9 | ns | |
| SID782C | $t_{HO_DDR_GPIO}$ | Input hold time | 3 | – | – | ns | |
| SID783C | $t_{DIS_DDR_GPIO}$ | Input disable time | – | – | 22.5 | ns | Guaranteed by design |
| SID784C | $t_{IO_SKEW_DDR_GPIO}$ | Data skew (first data bit to last data bit) | – | – | 1.8 | ns | Guaranteed by design |
| SMIF HyperBus Specification for HSIO_STD | | | | | | | |
| SID788 | $C_L_HB_HSIO$ | Load capacitance | – | – | 20 | pF | |
| SID786 | SRI_HB_HSIO | Input rise and fall slew rates | 1 | – | – | V/ns | For all signals, guaranteed by design |
| SID787 | SRO_HB_HSIO | Output rise and fall slew rates | 1 | – | – | V/ns | For all signals |
| Clock characteristics | | | | | | | |
| SID700 | $f_{CK_HB_HSIO}$ | Clock frequency | – | – | 100 | MHz | |
| SID701 | $t_{CK_HB_HSIO}$ | Clock period | 1 / $f_{CK_HB_HSIO}$ | – | – | ns | |
| SID702 | DCK_HB_HSIO | Clock duty | 45 | – | 55 | % | |
| AC Parameters | | | | | | | |
| SID706 | $t_{CSHI_HB_HSIO}$ | Chip select HIGH between transactions | 10 | – | – | ns | Guaranteed by design |

Table 25-36. SMIF Specifications (continued)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|----------------------|--|------------------------|-----|------|-------|---------------------------------------|
| SID708 | $t_{CSS_HB_HSIO}$ | Chip select setup to next CK rising edge | 3 | – | – | ns | |
| SID709 | $t_{DSV_HB_HSIO}$ | Data strobe valid | – | – | 12 | ns | |
| SID710 | $t_{OSU_HB_HSIO}$ | DQ output setup | 1 | – | – | ns | |
| SID711 | $t_{OH_HB_HSIO}$ | DQ output hold | 1 | – | – | ns | |
| SID715 | $t_{CKD_HB_HSIO}$ | CK transition to DQ valid | 1 | – | 5.5 | ns | |
| SID718 | $t_{CKDS_HB_HSIO}$ | CK transition to RWDS valid | 1 | – | 5.5 | ns | |
| SID719 | $t_{DSS_HB_HSIO}$ | RWDS transition to DQ valid | –0.8 | – | 0.8 | ns | |
| SID720 | $t_{DSH_HB_HSIO}$ | RWDS transition to DQ invalid | –0.8 | – | 0.8 | ns | |
| SID721 | $t_{CSH_HB_HSIO}$ | Chip select hold after CK falling edge | 0 | – | – | ns | |
| SMIF HyperBus Specification for GPIO_STD | | | | | | | |
| SID785A | $C_L_HB_GPIO$ | Load capacitance | – | – | 20 | pF | |
| SID786A | SRI_HB_GPIO | Input rise and fall slew rates | 0.45 | – | – | V/ns | For all signals, guaranteed by design |
| SID787A | SRO_HB_GPIO | Output rise and fall slew rates | 0.45 | – | – | V/ns | For all signals |
| Clock characteristics | | | | | | | |
| SID700A | $f_{CK_HB_GPIO}$ | Clock frequency | – | – | 32 | MHz | |
| SID701A | $t_{CK_HB_GPIO}$ | Clock period | $1 / f_{CK_HB_GPIO}$ | – | – | ns | |
| SID702A | DCK_HB_GPIO | Clock duty | 45 | – | 55 | % | |
| AC Parameters | | | | | | | |
| SID706A | $t_{CSHI_HB_GPIO}$ | Chip select HIGH between transactions | 30 | – | – | ns | Guaranteed by design |
| SID708A | $t_{CSS_HB_GPIO}$ | Chip select setup to next CK rising edge | 9 | – | – | ns | |
| SID709A | $t_{DSV_HB_GPIO}$ | Data strobe valid | – | – | 36 | ns | Guaranteed by design |
| SID710A | $t_{OSU_HB_GPIO}$ | DQ output setup | 3 | – | – | ns | |
| SID711A | $t_{OH_HB_GPIO}$ | DQ output hold | 3 | – | – | ns | |
| SID715A | $t_{CKD_HB_GPIO}$ | CK transition to DQ valid | 3 | – | 16.5 | ns | |
| SID718A | $t_{CKDS_HB_GPIO}$ | CK transition to RWDS valid | 3 | – | 16.5 | ns | |
| SID719A | $t_{DSS_HB_GPIO}$ | RWDS transition to DQ valid | –2.4 | – | 2.4 | ns | |
| SID720A | $t_{DSH_HB_GPIO}$ | RWDS transition to DQ invalid | –2.4 | – | 2.4 | ns | |
| SID721A | $t_{CSH_HB_GPIO}$ | Chip select hold after CK falling edge | 0 | – | – | ns | |

Figure 25-31.SDR Write Timing Reference Level

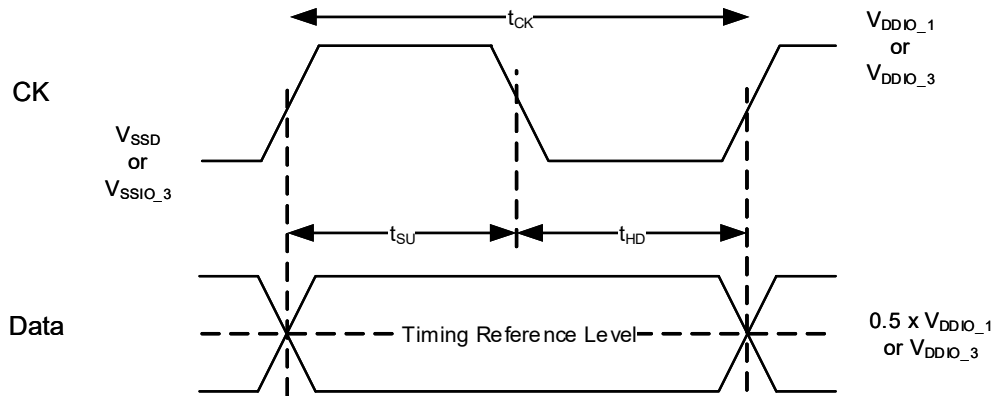


Figure 25-32.SDR Read Timing Reference Level

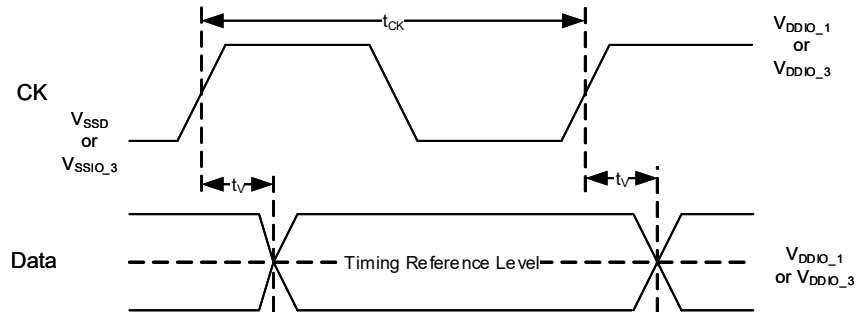


Figure 25-33.DDR Write Timing Reference Level

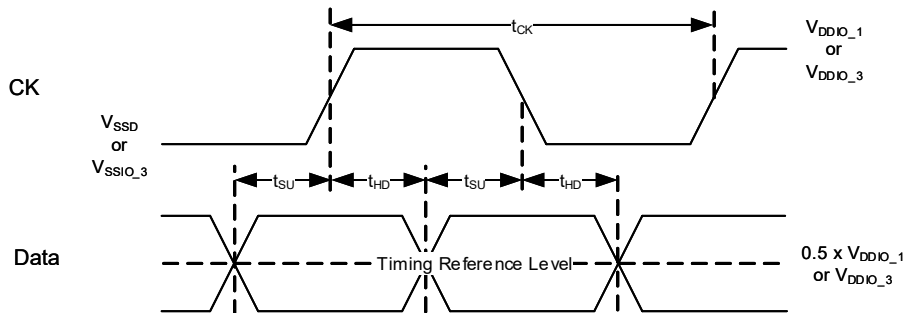


Figure 25-34.DDR Read Timing Reference Level

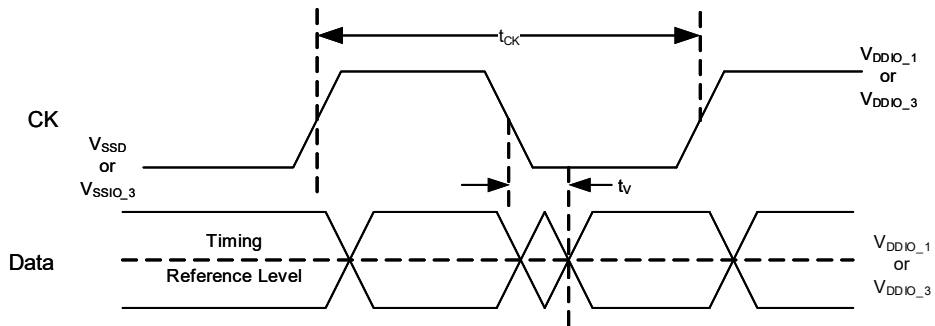
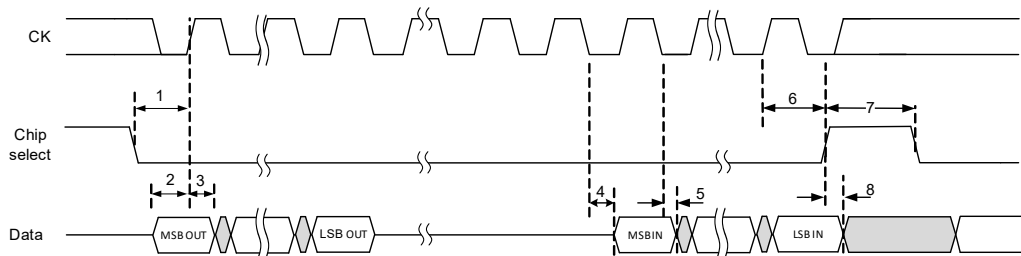
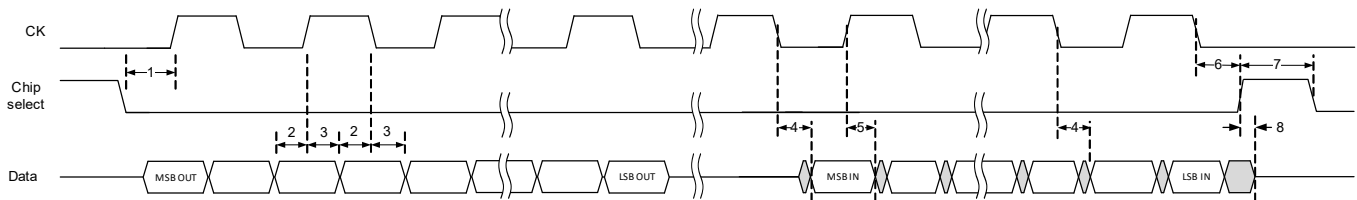


Figure 25-35.SDR Write and Read Timing Diagram



- 1: Chip select active setup time = t_{CSS}
- 2: Data setup time = t_{SU}
- 3: Data hold time = t_{HD}
- 4: Clock LOW output valid = t_V
- 5: Input data hold time = t_{HO}
- 6: Chip select active hold time = t_{CSH}
- 7: Chip select HIGH time = t_{CS}
- 8: Input disable time = t_{DIS}

Figure 25-36.DDR Write and Read Timing Diagram



- 1: Chip select active setup time = t_{CSS}
- 2: Data setup time = t_{SU}
- 3: Data hold time = t_{HD}
- 4: Clock LOW output valid = t_V
- 5: Input data hold time = t_{HO}
- 6: Chip select active hold time = t_{CSH}
- 7: Chip select HIGH time = t_{CS}
- 8: Input disable time = t_{DIS}

Figure 25-37. HyperBus Timing Reference Level

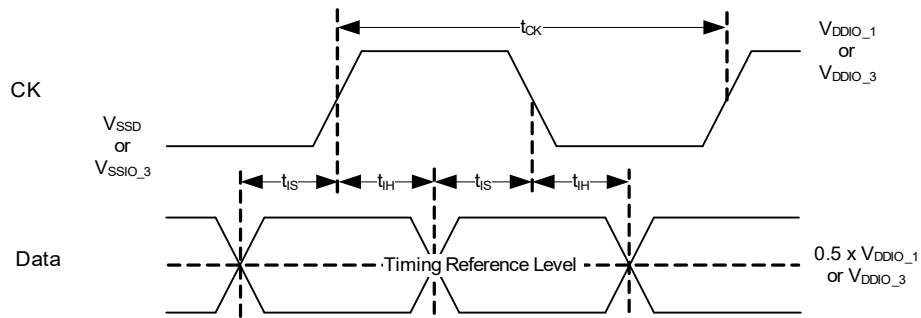
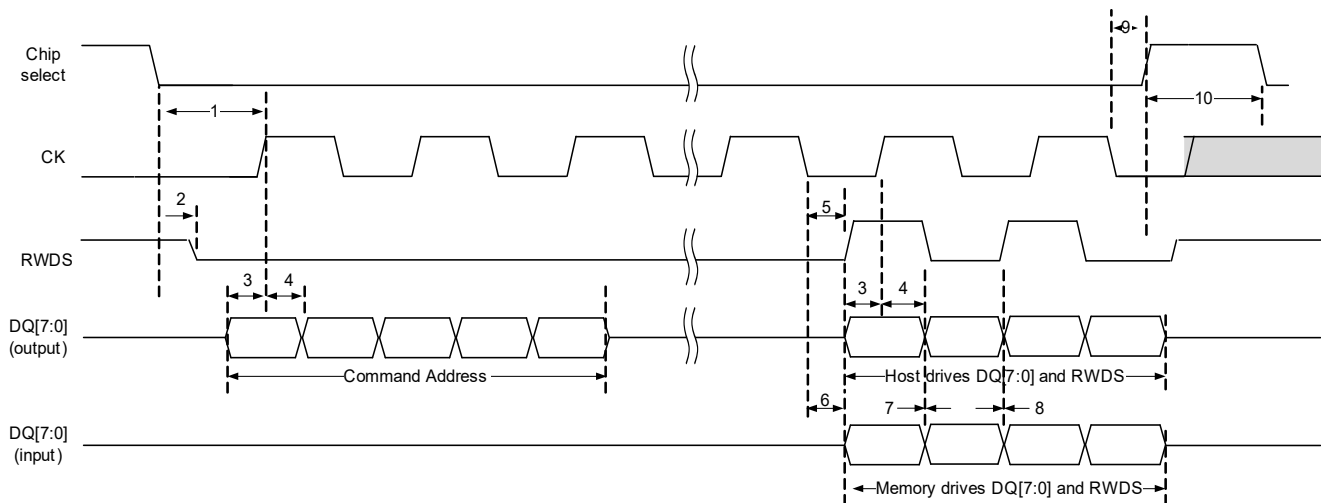


Figure 25-38. HyperBus Timing Diagram



- 1: Chip select setup to next CK rising edge = t_{CSS}
- 2: Data strobe valid = t_{DSV}
- 3: DQ output setup = t_{OSU}
- 4: DQ output hold = t_{OH}
- 5: CK transition to RWDS valid = t_{CKDS}
- 6: CK transition to DQ valid = t_{CKD}
- 7: RWDS transition to DQ valid = t_{DSS}
- 8: RWDS transition to DQ invalid = t_{DSH}
- 9: Chip select hold after CK falling edge = t_{CSH}
- 10: Chip select HIGH between transactions = t_{CSHI}

26. Ordering Information

The CYT4BF microcontroller part numbers and features are listed in [Table 26-1](#). The Arm TAP JTAG ID is 0x6BA0 0477.

Table 26-1. CYT4BF Ordering Information

| Device Code | Ordering Code ^[68] | Package | CM7 Cores | Code-flash (KB) | Work-flash (KB) | RAM (KB) | ADC Channels | SCB Channels | LIN Channels | Ethernet Channels | FlexRay | SD/eMMC | Temperature Grade | JTAG ID Code |
|----------------------------|-------------------------------|-----------|-----------|----------------------|---------------------|----------|--------------|--------------|--------------|-------------------|-------------------|---------|-------------------|----------------------------|
| CYT4BF8CES | CYT4BF8CEDQ0AESGS | 176-TEQFP | 2 | 8384 ^[69] | 256 ^[70] | 1024 | 81 | 10 | 17 | 1 | 0 | 1 | S ^[71] | 0x2E5D3069 ^[75] |
| CYT4BF8CEE | CYT4BF8CEDQ0AEEGS | 176-TEQFP | 2 | 8384 | 256 | 1024 | 81 | 10 | 17 | 1 | 0 | 1 | E ^[72] | 0x2E5D3069 |
| CYT4BF8CDS | CYT4BF8CDDQ0AESGS | 176-TEQFP | 2 | 8384 | 256 | 1024 | 81 | 10 | 17 | 1 | 1 ^[74] | 1 | S | 0x2E5D7069 |
| CYT4BF8CDE ^[73] | CYT4BF8CDDQ0AEEGS | 176-TEQFP | 2 | 8384 | 256 | 1024 | 81 | 10 | 17 | 1 | 1 | 1 | E | 0x2E5D7069 |
| CYT4BFBCJS | CYT4BFBCJDQ0BZSGS | 272-BGA | 2 | 8384 | 256 | 1024 | 96 | 11 | 20 | 2 | 0 | 1 | S | 0x2E5EB069 |
| CYT4BFBCJE | CYT4BFBCJDQ0BZEGS | 272-BGA | 2 | 8384 | 256 | 1024 | 96 | 11 | 20 | 2 | 0 | 1 | E | 0x2E5EB069 |
| CYT4BFBCJS | CYT4BFBCJDQ0BZSGS | 272-BGA | 2 | 8384 | 256 | 1024 | 96 | 11 | 20 | 2 | 1 | 1 | S | 0x2E5EF069 |
| CYT4BFBCHE ^[73] | CYT4BFBCJDQ0BZEGS | 272-BGA | 2 | 8384 | 256 | 1024 | 96 | 11 | 20 | 2 | 1 | 1 | E | 0x2E5EF069 |
| CYT4BFCCJS | CYT4BFCCJDQ0BZSGS | 320-BGA | 2 | 8384 | 256 | 1024 | 96 | 11 | 20 | 2 | 0 | 1 | S | 0x2E5FB069 |
| CYT4BFCCJE | CYT4BFCCJDQ0BZEGS | 320-BGA | 2 | 8384 | 256 | 1024 | 96 | 11 | 20 | 2 | 0 | 1 | E | 0x2E5FB069 |
| CYT4BFCCJS | CYT4BFCCJDQ0BZSGS | 320-BGA | 2 | 8384 | 256 | 1024 | 96 | 11 | 20 | 2 | 1 | 1 | S | 0x2E5FF069 |
| CYT4BFCCHE ^[73] | CYT4BFCCJDQ0BZEGS | 320-BGA | 2 | 8384 | 256 | 1024 | 96 | 11 | 20 | 2 | 1 | 1 | E | 0x2E5FF069 |

Notes

68. Supported shipment types are "Tray" (default) and "Tape and Reel". Add the character 'T' at the end to get the ordering code for "Tape and Reel" shipment type.

69. Code-flash size 8384 KB = 32 KB × 254 (Large Sectors) + 8 KB × 32 (Small Sectors)

70. Work-flash size 256 KB = 2 KB × 96 (Large Sectors) + 128 B × 512 (Small Sectors)

71. S-grade Temperature (−40 °C to 105 °C).

72. E-grade Temperature (−40 °C to 125 °C).

73. These parts are available as engineering samples.

74. One interface of FlexRay supports two channels (ch A and ch B).

75. JTAG ID CODE bits 12 through 27, represents the Silicon ID of the device.

26.1 Part Number Nomenclature

Table 26-2. Device Code Nomenclature

| Field | Description | Value | Meaning |
|-------|-------------------------------------|-------|--|
| CY | Cypress Prefix | CY | |
| T | Category | T | Traveo |
| 2 | Family Name | 4 | Traveo II (Core M7 dual) |
| B | Application | B | Body |
| D | Code-flash/Work-flash/SRAM quantity | F | 8384 KB / 256 KB / 1024 KB |
| P | Packages | 8 | 176-TEQFP |
| | | B | 272-BGA |
| | | C | 320-BGA |
| H | Hardware Option | C | eSHE – on, HSM – on |
| I | Marketing Option | E | Ethernet - 1 ch, FlexRay - 0, eMMC - 1 |
| | | D | Ethernet - 1 ch, FlexRay - 2, eMMC - 1 |
| | | J | Ethernet - 2 ch, FlexRay - 0, eMMC - 1 |
| | | H | Ethernet - 2 ch, FlexRay - 2, eMMC - 1 |
| C | Temperature Grade | S | S-grade (–40 °C to 105 °C) |
| | | E | E-grade (–40 °C to 125 °C) |

Table 26-3. Ordering Code Nomenclature

| Field | Description | Value | Meaning |
|-------|-------------------------------------|-------|--|
| CY | Cypress Prefix | CY | |
| T | Category | T | Traveo |
| 2 | Family Name | 4 | Traveo II (Core M7 dual) |
| B | Application | B | Body |
| D | Code-flash/Work-flash/SRAM quantity | F | 8384 KB / 256 KB / 1024 KB |
| P | Packages | 8 | 176-TEQFP |
| | | B | 272-BGA |
| | | C | 320-BGA |
| H | Hardware Option | C | eSHE – on, HSM – on |
| I | Marketing Option | E | Ethernet - 1 ch, FlexRay - 0, eMMC - 1 |
| | | D | Ethernet - 1 ch, FlexRay - 2, eMMC - 1 |
| | | J | Ethernet - 2 ch, FlexRay - 0, eMMC - 1 |
| | | H | Ethernet - 2 ch, FlexRay - 2, eMMC - 1 |
| R | Revision | A | First revision |
| | | B | Second revision |
| | | C | Third revision |
| | | D | Fourth revision |
| F | Fab Location | Q | UMC (Fab 12i) Singapore |
| X | Reserved | 0 | Reserved |
| K | Package Code | AE | TEQFP |
| | | BZ | BGA |
| C | Temperature Grade | S | S-grade (-40 °C to 105 °C) |
| | | E | E-grade (-40 °C to 125 °C) |
| Q | Quality Grade | ES | Engineering samples |
| | | GS | Standard grade of automotive |
| S | Shipment Type | Blank | Tray shipment |
| | | T | Tape and Reel shipment |

27. Packaging

CYT4BF microcontroller is offered in the packages listed in the [Table 27-1](#).

Table 27-1. Package Information

| Package | Dimensions ^[76] | Contact/Lead Pitch | Coefficient of Thermal Expansion | I/O Pins |
|-----------|----------------------------|--------------------|--|----------|
| 176-TEQFP | 24 × 24 × 1.70 mm (max) | 0.5-mm | a1 ^[77] = 8.4 ppm/°C, a2 ^[78] = 29.4 ppm/°C | 148 |
| 272-BGA | 16 × 16 × 1.70 mm (max) | 0.8-mm | a1 ^[77] = 11.9 ppm/°C, a2 ^[78] = 34.3 ppm/°C | 220 |
| 320-BGA | 17 × 17 × 1.70 mm (max) | 0.8-mm | a1 ^[77] = 11.9 ppm/°C, a2 ^[78] = 34.5 ppm/°C | 240 |

Table 27-2. Package Characteristics

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|------------------|---|------------|-----|-----|-------|-------|
| T _A | Operating ambient temperature | S-grade | -40 | - | 105 | °C |
| T _A | Operating ambient temperature | E-grade | -40 | - | 125 | °C |
| T _J | Operating junction temperature | - | - | - | 150 | °C |
| R _{θJA} | Package thermal resistance, junction to ambient θ _{JA} ^[79, 80] | 176-TEQFP | - | - | 16.4 | °C/W |
| | | 272-BGA | - | - | 22.4 | °C/W |
| | | 320-BGA | - | - | 21.8 | °C/W |
| R _{θJB} | Package θ _{JB} | 176-TEQFP | - | - | 11.96 | °C/W |
| | | 272-BGA | - | - | 13.5 | °C/W |
| | | 320-BGA | - | - | 13.6 | °C/W |
| R _{θJC} | Package thermal resistance, junction to case θ _{JC} | 176-TEQFP | - | - | 7.5 | °C/W |
| | | 272-BGA | - | - | 8.9 | °C/W |
| | | 320-BGA | - | - | 6.5 | °C/W |

Table 27-3. Solder Reflow Peak Temperature, Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

| Package | Maximum Peak Temperature (°C) | Maximum Time at Peak Temperature (seconds) | MSL |
|-----------|-------------------------------|--|-----|
| 176-TEQFP | 260 | 30 | 3 |
| 272-BGA | 260 | 30 | 3 |
| 320-BGA | 260 | 30 | 3 |

Notes

76. The dimensions (column 2) are valid for room temperature.

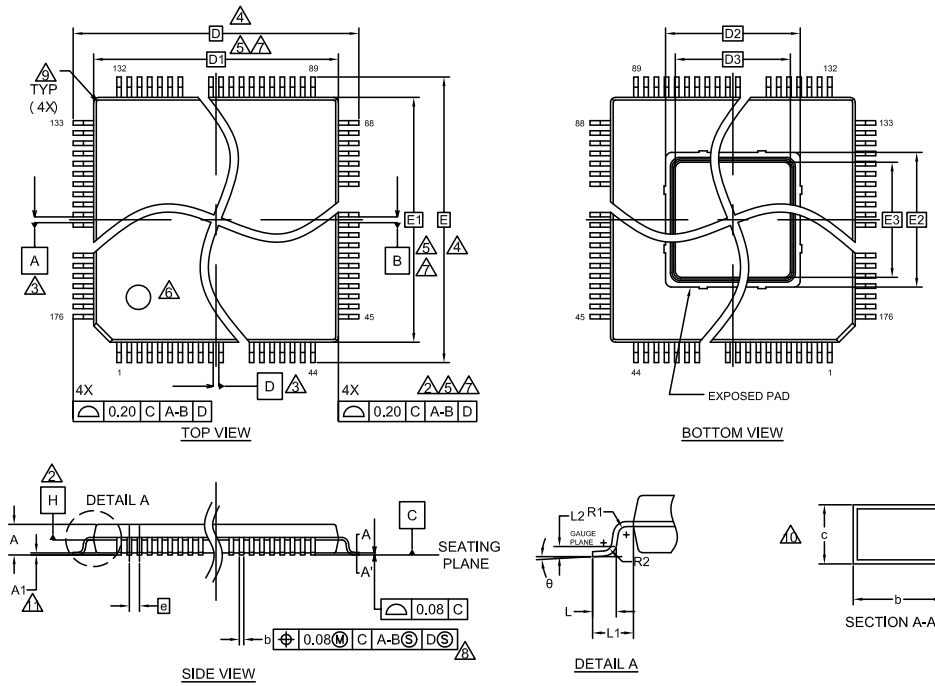
77. a1 = CTE (Coefficient of Thermal Expansion) value below T_g (ppm/°C) (T_g is glass transition temperature which is 131°C).

78. a2 = CTE value above T_g (ppm/°C).

79. Maximum value °C/Watt shown is for T_A = 125 °C.

80. Board condition complies to JESD51-7(4 Layers).

Figure 27-1.Package Outline – 176-TEQFP



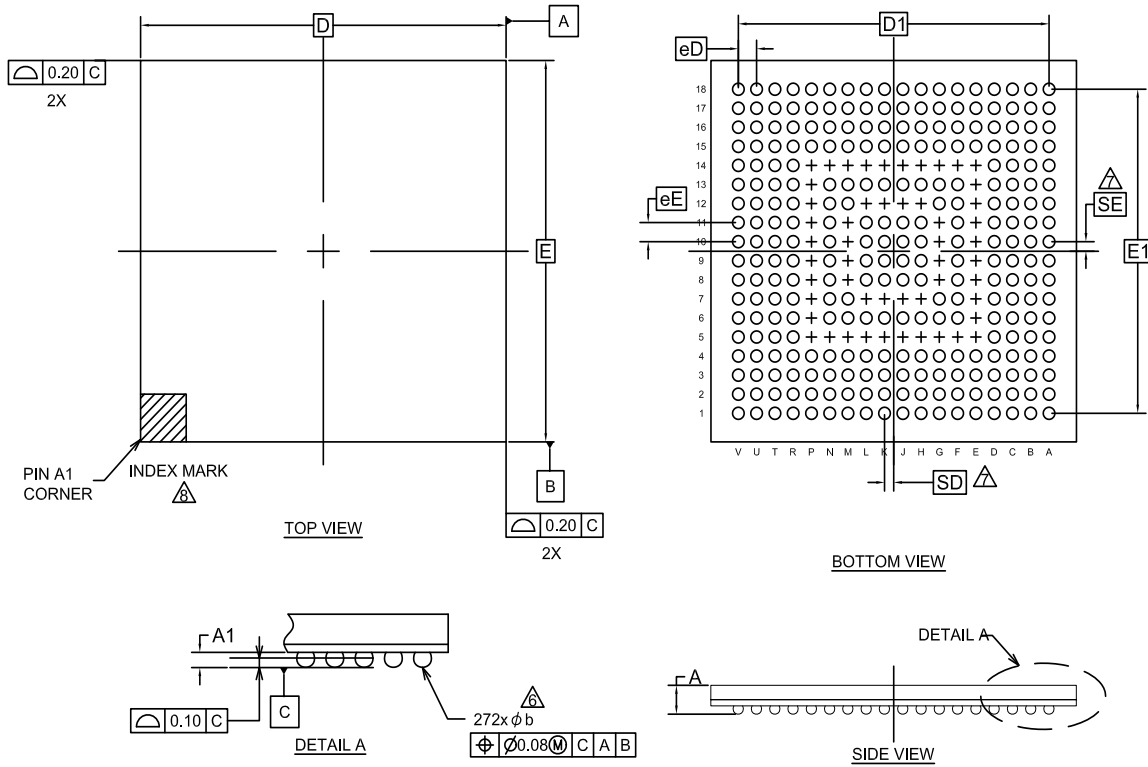
| SYMBOL | DIMENSION | | |
|--------|-----------|------|------|
| | MIN. | NOM. | MAX. |
| A | — | — | 1.70 |
| A1 | 0.05 | — | 0.15 |
| D | 26.00 BSC | | |
| D1 | 24.00 BSC | | |
| D2 | 6.60 REF | | |
| D3 | 5.40 REF | | |
| E | 26.00 BSC | | |
| E1 | 24.00 BSC | | |
| E2 | 6.60 REF | | |
| E3 | 5.40 REF | | |
| R1 | 0.08 | — | 0.20 |
| R2 | 0.08 | — | — |
| θ | 0° | 2° | 8° |
| c | 0.09 | — | 0.20 |
| b | 0.17 | 0.22 | 0.27 |
| L | 0.45 | 0.60 | 0.75 |
| L 1 | 1.00 REF | | |
| L 2 | 0.25 | | |
| e | 0.50 BSC | | |

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
1. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
2. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
3. TO BE DETERMINED AT SEATING PLANE C.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE.
5. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBER PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
10. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
11. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-25324 **

Figure 27-2.Package Outline – 272-BGA



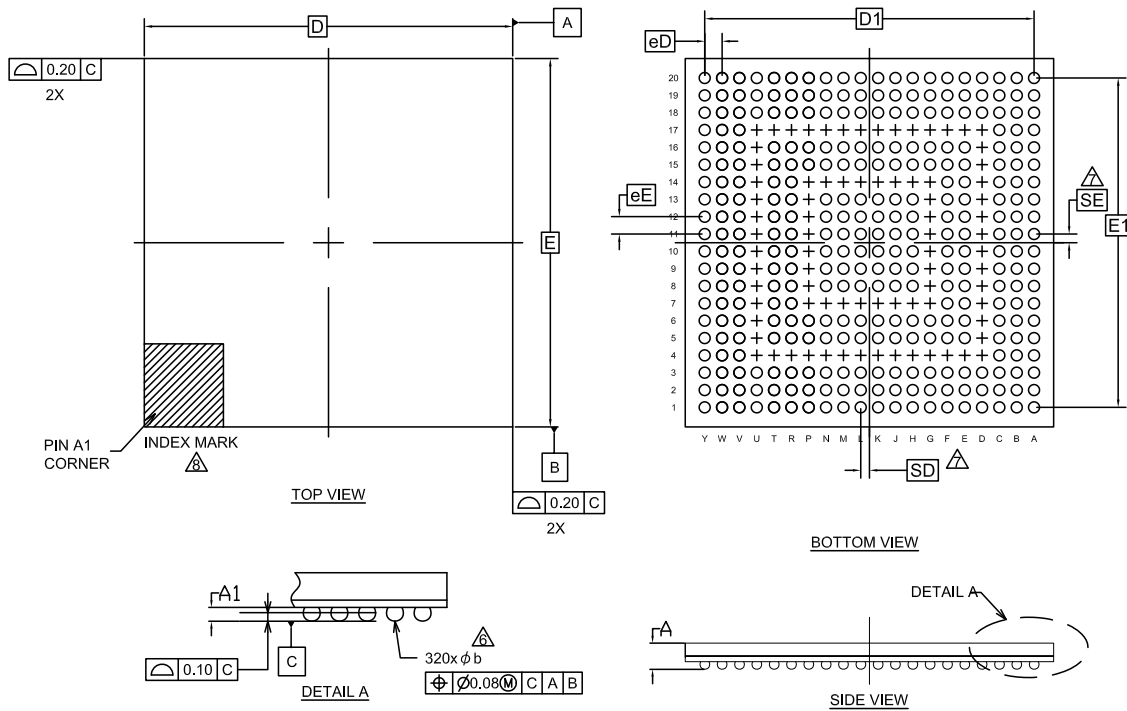
| SYMBOL | DIMENSIONS | | |
|---------|------------|------|------|
| | MIN. | NOM. | MAX. |
| A | — | — | 1.70 |
| A1 | 0.30 | 0.35 | 0.40 |
| D | 16.00 BSC | | |
| E | 16.00 BSC | | |
| D1 | 13.60 BSC | | |
| E1 | 13.60 BSC | | |
| MD | 18 | | |
| ME | 18 | | |
| n | 272 | | |
| Φb | 0.40 | 0.45 | 0.50 |
| eD | 0.80 BSC | | |
| eE | 0.80 BSC | | |
| SD / SE | 0.40 BSC | | |

NOTES

- ALL DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS AND TOLERANCES METHODS PER ASME Y14.5-2009. THIS OUTLINE CONFORMS TO JEP95, SECTION 4.5.
- BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-010.
- "e" REPRESENTS THE SOLDER BALL GRID PITCH.
- SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION. n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
- DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
- "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
- A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK. METALLIZED MARK INDENTATION OR OTHER MEANS.
- "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

002-24865 *A

Figure 27-3.Package Outline – 320-BGA



| SYMBOL | DIMENSIONS | | |
|---------|------------|------|------|
| | MIN. | NOM. | MAX. |
| A | — | — | 1.70 |
| A1 | 0.30 | 0.35 | 0.40 |
| D | 17.00 BSC | | |
| E | 17.00 BSC | | |
| D1 | 15.20 BSC | | |
| E1 | 15.20 BSC | | |
| MD | 20 | | |
| ME | 20 | | |
| n | 320 | | |
| Φb | 0.40 | 0.45 | 0.50 |
| eD | 0.80 BSC | | |
| eE | 0.80 BSC | | |
| SD / SE | 0.40 BSC | | |

NOTES

- ALL DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS AND TOLERANCES METHODS PER ASME Y14.5-2009. THIS OUTLINE CONFORMS TO JEP95, SECTION 4.5.
- BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-010.
- "e" REPRESENTS THE SOLDER BALL GRID PITCH.
- SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION. n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
- DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
- "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
- A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK. METALLIZED MARK INDENTATION OR OTHER MEANS.
- "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

002-23091 *A

28. Appendix

28.1 Bootloading or End-of-line Programming

- Triggered at device startup, if a trigger condition is applied
- Either CAN or LIN communication may be used
- Bootloader polls for the communication on CAN or LIN at the separate time frames, until the overall 300-second timeout is reached
- If a bootloader command is received on either communication interface, the polling stops and bootloader starts using this interface

Figure 28-1.Bootloading Sequence

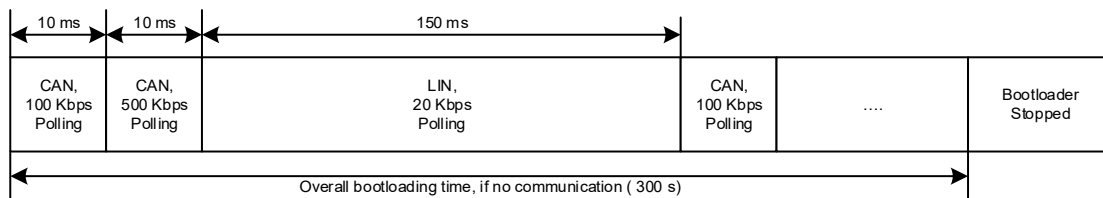


Table 28-1. CAN Interface Details

| SI. No. | CAN Interface | Configuration |
|---------|---------------------------------|-----------------------------|
| 1 | CAN Mode | Classic CAN |
| 2 | CAN Instance | CAN0, Channel#1 |
| 3 | CAN TX | P0.2 / CAN0_1_TX |
| 4 | CAN RX | P0.3 / CAN0_1_RX |
| 5 | CAN Transceiver NSTB / EN (Low) | P23.3 (optional) |
| 6 | CAN Transceiver EN / EN (High) | P2.1 (optional) |
| 7 | CAN RX Message ID | 0x1A1 |
| 8 | CAN TX Message ID | 0x1B1 |
| 9 | Baud | 100 or 500 kbps alternating |

Figure 28-2.MCU to CAN Transceiver Connections

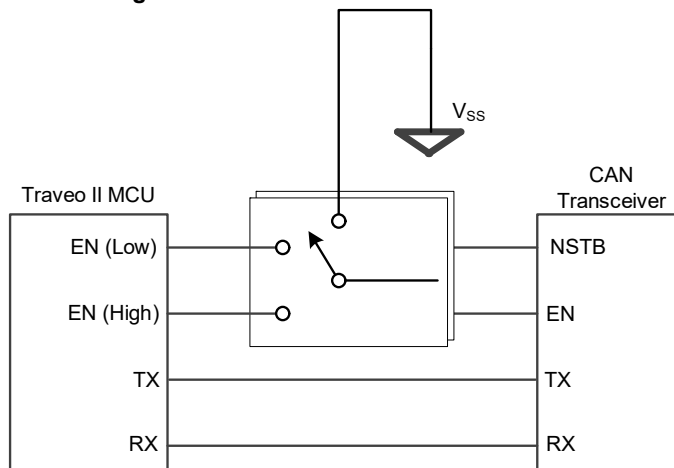
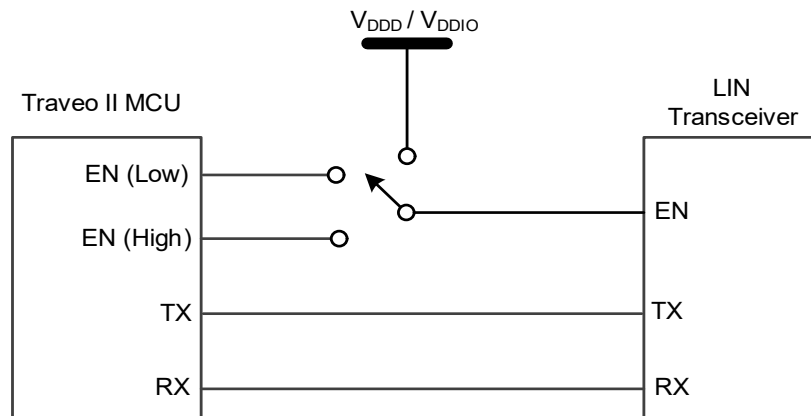


Table 28-2. LIN Interface Details

| SI. No. | LIN Interface | Configuration |
|---------|------------------------|------------------|
| 1 | LIN Type | LIN0, Channel#1 |
| 2 | LIN Mode | Slave |
| 3 | LIN Checksum Type | Classic |
| 4 | LIN TX | P0.1 / LIN1_TX |
| 5 | LIN RX | P0.0 / LIN1_RX |
| 6 | LIN EN / EN (High) | P2.1 (optional) |
| 7 | LIN EN (Low) | P23.3 (optional) |
| 8 | LIN TX PID | 0x46 |
| 9 | LIN RX PID | 0x45 |
| 10 | Baud | 20 or 115.2 kbps |
| 11 | Break Field Length | 11 |
| 12 | Break Delimiter Length | 1 bit |

Figure 28-3. MCU to LIN Transceiver Connections



28.2 External IP Revisions

Table 28-3. IP Revisions

| Module | IP | Revision | Vendor |
|----------------|----------------|---|----------|
| FlexRay | mxflexray | Release - Revision 1.0.3, CREL - 103 9 02 06, E-Ray Spec - v1.2.7, Protocol Spec - v2.1 | Bosch |
| SDHC | mxsdhc | version 1.70a | Synopsys |
| CANFD | mxttcanfd | M_TTCAN IP revision: Rev.3.2.3 | Bosch |
| Arm Cortex-M0+ | armcm0p | Cortex-M0+ AT590-r0p1-00rel0 | Arm |
| Arm Cortex-M7 | armcm7 | CORTEX-M7-r1p1-00rel0 | Arm |
| Arm Coresight | armcoresighttk | CoreSight-SoC-TM100-r3p2-00rel0 | Arm |
| Ethernet | mxeth | GEM_GXL r1p09 | Cadence |

29. Acronyms

Table 29-1. Acronyms used in the document

| Acronym | Description | Acronym | Description |
|------------------|--|---------|--|
| A/D | Analog to Digital | PLL | Phase Locked Loop |
| ABS | Absolute | POR | Power-on reset |
| ADC | Analog to Digital converter | PPU | Peripheral protection unit |
| AES | Advanced encryption standard | PRNG | Pseudorandom number generator |
| AHB | AMBA (advanced microcontroller bus architecture) high-performance bus, Arm data transfer bus | PSoC | Programmable system on chip |
| Arm | Advanced RISC machine, a CPU architecture | PWM | Pulse-width modulation |
| ASIL | Automotive safety integrity level | MCU | Microcontroller Unit |
| BOD | Brown-out detection | MCWDT | Multi-counter watchdog timer |
| CAN FD | Controller Area Network with Flexible Data rate | M-DMA | Memory-Direct Memory Access |
| CMOS | Complementary metal-oxide-semiconductor | MISO | Master-in slave-out |
| CPU | Central Processing Unit | MMIO | Memory mapped I/O |
| CRC | Cyclic redundancy check, an error-checking protocol | MOSI | Master-out slave-in |
| CSV | Clock supervisor | MPU | Memory protection unit |
| CTI | Cross Trigger Interface | NVIC | Nested vectored interrupt controller |
| DES | Data encryption standard | RAM | Random access memory |
| ECC | Error correcting code | RISC | Reduced-instruction-set computing |
| ECO | External crystal oscillator | ROM | Read only memory |
| ETM | Embedded Trace Macrocell | RTC | Real-time clock |
| FLL | Frequency Locked Loop | SAR | Successive approximation register |
| FPU | Floating point unit | SCB | Serial communication block |
| GHS | Green hills tool chain with IDE | SCL | I ² C serial clock |
| GPIO | General purpose input/output | SDA | I ² C serial data |
| HSM | Hardware security module | SHA | Secure hash algorithm |
| I/O | Input/output | SHE | Secure hardware extension |
| I ² C | Inter-Integrated Circuit, a communications protocol | SMPU | Shared memory protection unit |
| I ² S | Inter-Integrated Circuit Sound | SPI | Serial peripheral interface, a communications protocol |
| ILO | Internal low-speed oscillator | SRAM | Static random access memory |
| IMO | Internal main oscillator | SWD | Single wire debug |
| IPC | Inter-processor communication | TCM | Tightly Coupled Memory |
| IrDA | Infrared interface | TCPWM | Timer/Counter Pulse-width modulator |
| IRQ | Interrupt request | TTL | Transistor-transistor logic |
| JTAG | Joint test action group | TRNG | True random number generator |
| LIN | Local Interconnect Network, a communications protocol | UART | Universal Asynchronous Transmitter Receiver, a communications protocol |
| LVD | Low voltage detection | WCO | Watch crystal oscillator |
| OTA | Over-the-air programming | WDT | Watchdog timer reset |
| OTP | One-time programmable | XIP | eXecute In Place |
| OVD | Over voltage detection | XTAL | Crystal |
| PASS | Programmable Analog Subsystem | | |
| P-DMA | Peripheral-Direct Memory Access | | |

30. Errata

This section describes the errata for the CYT4BF product family. Details include trigger conditions, scope of impact, available workaround, and silicon revision applicability. Contact your local Cypress Sales Representative if you have further questions.

Part Numbers Affected

| Part Numbers |
|------------------|
| All CYT4BF parts |

CYT4BF Qualification Status

Production samples

CYT4BF Errata Summary

The following table defines the errata applicability to available CYT4BF family devices.

| Items | Errata ID | CYT4BF | Silicon Rev. | Fix Status |
|---|-----------|--|--------------|--|
| [1] CAN FD RX FIFO top pointer feature does not function as expected | 96 | CYT4BF8CEDQ0AESGS CYT4BF8CEDQ0AEEGS | D | No silicon fix planned. Use workaround. |
| [2] CAN FD debug message handling state machine is not reset to Idle state when CANFD_CH_CCCR.INIT is set | 97 | CYT4BF8CDDQ0AESGS CYT4BF8CDDQ0AEEGS CYT4BFBCJDQ0BZSGS CYT4BFBCJDQ0BZEGS | | No silicon fix planned. Use workaround. |
| [3] Limitation of the memory hole in SCB register space | 124 | CYT4BFBCJDQ0BZSGS CYT4BFBCJDQ0BZEGS | | No silicon fix planned. Use workaround. |
| [4] Limitation of the memory hole in Ethernet (ETH) register space | 128 | CYT4BFCCJDQ0BZSGS CYT4BFCCJDQ0BZEGS CYT4BFCCJDQ0BZSGS CYT4BFCCJDQ0BZEGS | | No silicon fix planned. Use workaround. |

| 1. CAN FD RX FIFO top pointer feature does not function as expected | |
|---|---|
| Problem Definition | RX FIFO top pointer function calculates the address for received messages in Message RAM by hardware. This address should restart back from the start address after reading all messages of RX FIFO n size (n: 0 or 1). However, the address does not restart back from the start address when RX FIFO n size is set to 1(CANFD_CH_RXFnC.FnS = 0x01). This results in CPU/DMA reading messages from the wrong address in Message RAM. |
| Parameters Affected | NA |
| Trigger Condition(s) | The RX FIFO top pointer function is used when RX FIFO n size is set to 1 element (CANFD_CH_RXFnC.FnS = 0x01). |
| Scope of Impact | Received message cannot be correctly read by using the RX FIFO top pointer function, when RX FIFO n size is set to 1 element. |
| Workaround | Any of the following can be used as a workaround: 1) Set RX FIFO n size to 2 or more when using RX FIFO top pointer function. 2) Do not use the RX FIFO top pointer function when RX FIFO n size is set to 1 element. Instead of RX FIFO top pointer, read received messages from the Message RAM directly. |
| Fix Status | No silicon fix planned. Use workaround. |

| 2. CAN FD debug message handling state machine is not reset to Idle state when CANFD_CH_CCCR.INIT is set | |
|---|--|
| Problem Definition | If either of the CANFD_CH_CCCR.INIT bits is set by the Host or when the M_TTCAN module enters BusOff state, the debug message handling state machine stays in its current state instead of being reset to Idle state. Configuring the bit CANFD_CH_CCCR.CCE does not change CANFD_CH_RXF1S.DMS. |
| Parameters Affected | NA |
| Trigger Condition(s) | Either of the CANFD_CH_CCCR.INIT bits is set by the Host or when the M_TTCAN module enters BusOff state. |
| Scope of Impact | The errata is limited to the use case when the debug on CAN functionality is active. Normal operation of the CAN module is not affected, in which case the debug message handling state machine always remains in Idle state. In the described use case, the debug message handling state machine is stopped and remains in the current state signaled by the CANFD_CH_RXF1S.DMS bit. In case CANFD_CH_RXF1S.DMS is set to 0b11, the DMA request remains active. Bosch classifies this as a non-critical error with low severity, there is no fix for the IP. Bosch recommends the workaround listed here. |
| Workaround | In case the debug message handling state machine has stopped while CANFD_CH_RXF1S.DMS is 0b01 or 0b10, it can be reset to Idle state by hardware reset or by reception of debug messages after CANFD_CH_CCCR.INIT is reset to zero. |
| Fix Status | No silicon fix planned. Use workaround. |

| 3. Limitation of the memory hole in SCB register space | |
|---|---|
| Problem Definition | The memory hole [offset address: 0x1000 to 0xFFFF] inside SCB register space is not aligned to the below defined spec. The offset address bits [15:12] are ignored and treated as 4'b0000, so write/read access to offset address [0x1000 to 0xFFFF], will actually happen to [0x0000 to 0x0FFF]. - Access to address gaps in memory mapped space: writes are ignored and any read returns a zero. |
| Parameters Affected | NA |
| Trigger Condition(s) | Access to the memory hole [offset address: 0x1000 to 0xFFFF] in SCB register space. |
| Scope of Impact | The memory hole [offset address: 0x1000 to 0xFFFF] in SCB register space is not aligned to other IP registers. |
| Workaround | Do not access to the memory hole [offset address: 0x1000 to 0xFFFF] in SCB register space. |
| Fix Status | No silicon fix planned. |

| 4. Limitation of the memory hole in Ethernet (ETH) register space | |
|--|---|
| Problem Definition | The memory hole [offset address: 0x2000 to 0xFFFF] in ETH register space has the below mentioned original spec. However, when accessing to address gaps within [0x1000 to 0x1FFF], the offset address bits [15:13] are ignored and treated as 3'b000, so write/read access to offset address [0x3000 to 0x3FFF, 0x5000 to 0x5FFF, 0x7000 to 0x7FFF, 0x9000 to 0x9FFF, 0xB000 to 0xBFFF, 0xD000 to 0xDFFF, 0xF000 to 0xFFFF], will actually happen to [0x1000 to 0x1FFF]. - Access to address gaps within [0x0000 to 0x0FFF]: writes are ignored and any read returns a zero. - Access to address gaps within [0x1000 to 0x1FFF]: returns AHB ERROR. |
| Parameters Affected | NA |
| Trigger Condition(s) | Access to the memory hole [offset address: 0x3000 to 0x3FFF, 0x5000 to 0x5FFF, 0x7000 to 0x7FFF, 0x9000 to 0x9FFF, 0xB000 to 0xBFFF, 0xD000 to 0xDFFF, 0xF000 to 0xFFFF] in ETH register space. |

| | |
|------------------------|---|
| Scope of Impact | Write/read access to offset address [0x3000 to 0x3FFF, 0x5000 to 0x5FFF, 0x7000 to 0x7FFF, 0x9000 to 0x9FFF, 0xB000 to 0xBFFF, 0xD000 to 0xDFFF, 0xF000 to 0xFFFF], will actually happen to [0x1000 to 0x1FFF]. |
| Workaround | Do not access to the memory hole [offset address: 0x3000 to 0x3FFF, 0x5000 to 0x5FFF, 0x7000 to 0x7FFF, 0x9000 to 0x9FFF, 0xB000 to 0xBFFF, 0xD000 to 0xDFFF, 0xF000 to 0xFFFF] in ETH register space. |
| Fix Status | No silicon fix planned. |

Document History Page

| Document Title: CYT4BF Datasheet 32-bit Arm® Cortex®-M7 Microcontroller Traveo™ II Family | | | |
|---|---------|-----------------|---|
| Document Number: 002-21617 | | | |
| Revision | ECN | Submission Date | Description of Change |
| ** | 6079640 | 02/23/2018 | New datasheet |
| *A | 6165837 | 05/04/2018 | Updated Features and Features List . Updated Blocks and Functionality . Updated Functional Description . Updated CYT4BF Address Map , Flash Base Address Map , and Peripheral I/O Map . Added CYT4BF Clock Diagram . Added Pin Assignment Updated Electrical Specifications . Added the following timing diagrams in Electrical Specifications : Reset, TCPWM, SCB (I ² C, SPI), Crystal Connection Scheme, SAR ADC, System Resources, and JTAG. Added Interrupts and Wake-up Assignments , Peripheral Clock Assignments , Trigger Multiplexer , Triggers Group Inputs , Triggers Group Outputs , Triggers One-to-one , and Faults . Added Peripheral I/O Map Added Packaging . |
| *B | 6264766 | 07/27/2018 | Updated Features and Features List . Updated Blocks and Functionality . Updated Pin Assignment . Updated Electrical Specifications . Added Timing Diagrams for Ethernet, SMIF Updated SCB Diagrams Added Ordering Information . |
| *C | 6325196 | 09/28/2018 | Updated Features List and Peripheral I/O Map . Updated Functional Description . Updated Pin Assignment and Package Pin List and Alternate Functions . Updated Trigger Multiplexer , Core Interrupt Types , and Peripheral Clock Assignments . Added General P-DMA descriptions and Clock Dividers. Updated CYT4BF Clock Diagram . Updated Electrical Specifications . Updated Design Review. |
| *D | 6436980 | 01/16/2019 | Updated Features List and Peripheral I/O Map . Updated Functional Description . Updated Pin Assignment for 176-TEQFP package Updated Electrical Specifications . Updated Design and Expert Reviews. |
| *E | 6589926 | 06/06/2019 | Updated Features List , CYT4BF Address Map , Peripheral I/O Map . Updated Pin Assignment , Alternate Function Pin Assignments . Updated Trigger Group tables . Updated Peripheral Clocks and Peripheral Protection Unit Fixed Structure Pairs . Updated Bus Masters and Miscellaneous Configuration . Updated Electrical Specifications . Updated Reset Sequence and SPI Diagrams . Updated Table 25-21 . Updated Ordering Information and Packaging . Updated Appendix . |

| Document Title: CYT4BF Datasheet 32-bit Arm® Cortex®-M7 Microcontroller Traveo™ II Family Document Number: 002-21617 | | | |
|---|---------|------------|---|
| *F | 6732264 | 11/15/2019 | Updated TCPWM Channels and Programmable Analog in Features . Updated Ethernet MAC, TCPWM, SAR ADC, Audio I2S, and Debug Trace in Features List . Updated TCPWM channels in Architecture Block Diagram . Updated DeepSleep, PLL and FLL, TCPWM, and External Memory Interface sections in Functional Description . Updated SRAM details in CYT4BF Address Map . Added eFUSE and updated PERI Programmable PPU in Peripheral I/O Map . Added VSSD_2 in Power Pin Assignments . Updated PASS interrupts in Interrupts and Wake-up Assignments . Added Note 40 in Peripheral Protection Unit Fixed Structure Pairs . Changed MiniProg3 to MiniProg4 in Development Support . Updated Reset Sequence , ADC Calculation of impact of neighboring pins, Clock Specifications, and SMIF Diagrams in Electrical Specifications . Updated Ordering Information and Packaging . |
| *G | 6746816 | 05/04/2020 | Updated Functional Description . Updated Power Pin Assignments . Updated Pin Function Description . Updated Fault Assignments . Updated ECO spec from 3.988 MHz to 8 MHz. Updated Electrical Specifications . Updated Ordering Information . Added Errata . |
| *H | 6970754 | 09/23/2020 | Updated Features . Updated Features List . Updated Regulators . Updated Clock System . Updated Peripheral I/O Map . Updated Power Pin Assignments . Updated Pin Function Description . Updated Smoothing Capacitor Recommendations . Updated Ethernet Specifications . Updated Packaging . Updated Appendix . Updated Electrical Specifications . Please refer to Table 1-1 for the detailed list of changes for this revision. |

Revision History Change Log

| Section | Change Description | Current Spec | New Spec | Reason for change |
|------------------|--|--|---|-------------------|
| Features | Updated Package size | 176-TEQFP, 26 × 26 × 1.7 mm (max), 0.5-mm lead pitch | 176-TEQFP, 24 × 24 × 1.7 mm (max), 0.5-mm lead pitch | Correction |
| 1. Features List | Updated CAN in Table 1-1 | CAN: 10 ch | CAN0: 5 ch CAN1: 5 ch | Clarified |
| 1. Features List | Updated SCB in Table 1-1 | SCB: 176-TEQFP: 10 ch 272-BGA: 11 ch 320-BGA: 11 ch | SCB (UART / I2C / SPI): 176-TEQFP: (10 ch / 10 ch / 10 ch) 272-BGA: (11 ch / 11 ch / 11 ch) 320-BGA: (11 ch / 11 ch / 11 ch) | Clarified |
| 1. Features List | Renamed Features in Table 1-1 | LIN | LIN0 | Updated |
| 1. Features List | Updated Internal low-speed oscillator in Table 1-1 | 32 kHz (nominal) | 32.768 kHz (nominal) | Correction |
| 1. Features List | Added 1.1 Communication Peripheral Instance List and Table 1-2 | (none) | Added 1.1 Communication Peripheral Instance List and Table 1-2 Peripheral Instance List | New addition |

Revision History Change Log *(continued)*

| Section | Change Description | Current Spec | New Spec | Reason for change |
|--|---|---|---|-------------------|
| 3.2.2 Regulators | Updated Figure 3-2 | DRV_VOUT is used for PMIC feedback in Figure 3-2 | VCCD is used for PMIC feedback in Figure 3-2 | Updated |
| 3.2.3 Clock System | Updated ILO Clock Source description | nominally 32 kHz | nominally 32.768 kHz | Correction |
| 6. Peripheral I/O Map | Updated Table 6-1 | Section / Description/ Instances: PERI_MS / PERI Programmable PPU / 6 | Section / Description/ Instances: PERI_MS / PERI Programmable PPU / 10 | Updated |
| 6. Peripheral I/O Map | Updated Note 15 | These six Programmable PPUs are... | These Programmable PPUs are... | Updated |
| 11.1 Power Pin Assignments | Updated VSSD_2 (320-BGA) assignment in Table 11-2 | VSSD_2 (320-BGA): L18, P18 | VSSD_2 (320-BGA): L20, P20 | Correction |
| 12.1 Pin Function Description | Renamed Title in Table 12-2 | Table 12-2. Alternate Function Pin MUX Description | Table 12-2. Pin Function Description | Updated |
| 12.1 Pin Function Description | Added Section 12.1 | (none) | 12.1 Pin Function Description | New addition |
| 25.3 Smoothing Capacitor Recommendations | Added 25.3 and Table 25-3. | (none) | Added 25.3 and Table 25-3. | New addition |
| 25.13 Ethernet Specifications | Updated Figure 25-30 | "2" of right side presents in Figure 25-30. | Removed "2" of right side in Figure 25-30. | Correction |
| 27. Packaging | Updated Dimensions in Table 27-1 | 176-TEQFP: 26 x 26 x 1.70 mm (max) | 176-TEQFP: 24 x 24 x 1.70 mm (max) | Correction |
| 27. Packaging | Added note in Table 27-2 | (none) | 78. Maximum value °C/Watt shown is for TA = 125 °C. | New addition |
| 27. Packaging | Updated RθJC value for 176-TEQFP | 14.5 °C/W | 7.5 °C/W | Correction |
| 28. Appendix | Updated Table 28-1 | CAN Instance: CANFD0_CH1 CAN TX: P0.2 CAN RX: P0.3 CAN Transceiver NSTB: P23.3 CAN Transceiver EN: P2.1 | CAN Instance: CAN0, Channel#1 CAN TX: P0.2 / CAN0_1_TX CAN RX: P0.3 / CAN0_1_RX CAN Transceiver NSTB / EN (Low): P23.3 (optional) CAN Transceiver EN / EN (High): P2.1 (optional) | Updated |
| 28. Appendix | Updated Table 28-2 | LIN Type: LIN0_CH1 LIN TX: P0.1 LIN RX: P0.0 LIN EN: P2.1 | LIN Type: LIN0, Channel#1 LIN TX: P0.1 / LIN1_TX LIN RX: P0.0 / LIN1_RX LIN EN / EN (High): P2.1 (optional) LIN EN (Low): P23.3 (optional) | Updated |
| 28. Appendix | Updated Figure 28-3 | EN (LOW) and VDDIO line do not present. | Added EN (LOW) and VDDIO line | Updated |
| 28. Appendix | Added 28.2 External IP Revisions and Table 28-3. | (none) | Added 28.2 External IP Revisions and Table 28-3. | New addition |

Rev *H Electrical Specification Updates

| Spec ID | Description | Changed Item | Current Spec | New Spec | Reason for Change |
|---------|--|-----------------------------------|---|--|---------------------|
| SID17F | Output voltage | Details/Conditions | For EXT_PS_CTL1/2 in external PMIC mode, DRV_VOUT in external PMIC/transistor mode | For EXT_PS_CTL1/2 in external PMIC mode and DRV_VOUT in external transistor mode | Updated condition |
| SID23A | Sink maximum current | Description Details/Conditions | Description: LOW-level maximum output current Details/Conditions: For EXT_PS_CTL1/2 at external PMIC mode | Description: Sink maximum current Details/Conditions: For pin EXT_PS_CTL1 in external PMIC mode and internal regulator mode and pin EXT_PS_CTL2 in external PMIC mode | Updated description |
| SID23B | Sink average current | Description Details/Conditions | Description: LOW-level average output current Details/Conditions: For EXT_PS_CTL1/2 at external PMIC mode | Description: Sink average current Details/Conditions: For pin EXT_PS_CTL1 in external PMIC mode and internal regulator mode and pin EXT_PS_CTL2 in external PMIC mode | Updated description |
| SID23C | Sink maximum current | All | (None) | Sink maximum current for pin DRV_VOUT in external transistor mode | Added spec |
| SID30A | Source maximum current | Description Details/Conditions | Description: HIGH-level maximum output current Details/Conditions: For EXT_PS_CTL1/2, DRV_VOUT at external PMIC mode | Description: Source maximum current Details/Conditions: For pin EXT_PS_CTL1 in external PMIC mode and internal regulator mode and pin EXT_PS_CTL2 in external PMIC mode | Updated description |
| SID30B | Source maximum current | Description Details/Conditions | Description: HIGH-level maximum output current Details/Conditions: For DRV_VOUT in external transistor mode. | Description: Source maximum current Details/Conditions: For pin DRV_VOUT in external transistor mode | Updated description |
| SID30C | Source average current | Description Details/Conditions | Description: HIGH-level average output current Details/Conditions: For EXT_PS_CTL1/2, DRV_VOUT at external PMIC mode | Description: Source average current Details/Conditions: For pin EXT_PS_CTL1 in external PMIC mode and internal regulator mode and pin EXT_PS_CTL2 in external PMIC mode | Updated description |
| SID30D | Source average current | Description Details/Conditions | Description: HIGH-level average output current Details/Conditions: For DRV_VOUT in external transistor mode. | Description: Source average current Details/Conditions: For pin DRV_VOUT in external transistor mode | Updated description |
| SID39C | The maximum pin current the device can tolerate before triggering a latch-up | Description | Pin current for latch-up | The maximum pin current the device can tolerate before triggering a latch-up | Updated description |

Rev *H Electrical Specification Updates (continued)

| Spec ID | Description | Changed Item | Current Spec | New Spec | Reason for Change |
|---------|--|--------------------|--|--|---------------------|
| SID40 | Power supply voltage | Note | VDDD, VDDIO_1, VDDIO_2, VDDIO_3, VDDIO_4, and VDDA do not have any sequencing limitation and can establish in any order. These supplies (except VDDA and VDDIO_2) are independent in voltage level. For example, VDDIO_1 = 2.7 V, VDDD = 5.0 V, and VDDA = VDDIO_2 = 4.0 V are supported, as is any other combination of voltages between 2.7 V and 5.5 V inclusive. And, VDDIO_3 = 3.3 V, and VDDIO_4 = 2.7 V are supported, as is any other combination of voltages between 2.7 V and 3.6 V inclusive. The presence of VDDA without VDDD can cause some leakage from VDDA. However, the device does not drive any analog (SAR ADC) or digital outputs. | VDDD, VDDIO_1, VDDIO_2, VDDIO_3, VDDIO_4, and VDDA do not have any sequencing limitation and can establish in any order. These supplies (except VDDA and VDDIO_2) are independent in voltage level. See 12-Bit SAR ADC DC Specifications when using ADC units. | Updated description |
| SID49E1 | VCCD current in external PMIC/transistor mode, Active mode (CM7_0 at 350 MHz, CM0+ at 100 MHz, all peripherals are enabled) | Typ | 137 mA | 155 mA | Updated spec |
| SID50A1 | VCCD current in external PMIC/transistor mode, Active mode (CM7 CPUs at 350 MHz, CM0+ at 100 MHz, all peripherals are enabled) | Typ | 196 mA | 209 mA | Updated spec |
| SID53A | VDDD current in internal regulator mode CM7_1=OFF, Other CPUs in Sleep | Description | VDDD current in internal regulator mode All CPUs in Sleep mode | VDDD current in internal regulator mode CM7_1=OFF, Other CPUs in Sleep | Updated description |
| SID64A | 64-KB SRAM retention, ILO0 operation in DeepSleep mode | Details/Conditions | DeepSleep Mode (RTC, WDT, and event generator operating, all other peripherals: only retention registers are retained), ... | DeepSleep Mode (RTC, WDT, and event generator operating, all other peripherals are off except for retention registers), ... | Updated condition |
| SID64C | 64-KB SRAM retention, ILO0 operation in DeepSleep mode | Details/Conditions | DeepSleep Mode steady state at TA = 125 °C (RTC, WDT, and event generator operating, all other peripherals: only retention registers are retained), ... | DeepSleep Mode steady state at TA = 125 °C (RTC, WDT, and event generator operating, all other peripherals are off except for retention registers), ... | Updated condition |

Rev *H Electrical Specification Updates (continued)

| Spec ID | Description | Changed Item | Current Spec | New Spec | Reason for Change |
|---------|--|----------------------------------|---|--|-------------------|
| SID80A | ROM boot startup time or wakeup time from hibernate in NORMAL protection state | Details/Conditions | Guaranteed by Design, FAST_BOOT=1, CM0+ clocked at 100 MHz | Guaranteed by Design, CM0+ clocked at 100 MHz | Updated condition |
| SID80B | ROM boot startup time or wakeup time from hibernate in SECURE protection state | Details/Conditions | Guaranteed by Design, FAST_BOOT=1, TOC2_FLAGS=0x2CF, CM0+ clocked at 100 MHz | Guaranteed by Design, TOC2_FLAGS=0x2CF, CM0+ clocked at 100 MHz | Updated condition |
| SID81A | Flash boot startup time or wakeup time from hibernate in NORMAL/SECURE protection state | Details/Conditions | Guaranteed by Design, FAST_BOOT=1, TOC2_FLAGS=0x2CF, CM0+ clocked at 100 MHz, Listen window = 0 ms | Guaranteed by Design, TOC2_FLAGS=0x2CF, CM0+ clocked at 100 MHz, Listen window = 0 ms | Updated condition |
| SID81B | Flash boot with app authentication time in NORMAL/SECURE protection state | Details/Conditions | Guaranteed by Design, FAST_BOOT=1, TOC2_FLAGS=0x2CF, CM0+ clocked at 100 MHz, Listen window = 0 ms, App size is 64 KB with the last 256 bytes being a digital signature in RSASSA-PKCS1-v1.5 | Guaranteed by Design, TOC2_FLAGS=0x2CF, CM0+ clocked at 100 MHz, Listen window = 0 ms, App size is 64 KB with the last 256 bytes being a digital signature in RSASSA-PKCS1-v1.5 | Updated condition |
| SID606A | Output Voltage HIGH level for external PMIC enable output (EXT_PS_CTL1) | Details/Conditions | IOH = 1mA | IOH = - 1mA | Correction |
| SID609 | DRV_VOUT output resistance to VCCD at external PMIC mode with through mode setting (REGHC_PMIC_DRV_VOUT=2'b11) | All | DRV_VOUT output resistance to VCCD at external PMIC mode with through mode setting (REGHC_PMIC_DRV_VOUT=2'b11) | (none) | Removed spec |
| SID73 | IDD when XRES_L asserted | Details/Conditions | (none) | MAX: TA = 125 °C, VDDD = 5.5 V, VCCD = 1.15 V, process worst (FF) | Added condition |
| SID670 | Input leakage current | Min Max Details/Conditions | Min: -1000 nA Max: 1000 nA Details/Conditions: VDDIO_1 =VDDIO_2 = VDDD = VDDA = 5.5 V, VSSD < VI < VDDD, VDDIO_1, VDDIO_2, -40 °C ≤ TA ≤ 125 °C This is valid for the Port which do not have ADC input functionality. TYP: TA = 25 °C, VDDIO_1 =VDDIO_2 = VDDD = VDDA = 5.0 V. | Min: -250 nA Max: 250 nA Details/Conditions: For GPIO_STD except P21.0, P21.1, P21.2, P21.3, P21.4, P22.1, P22.2, P22.3, P23.3, P23.4 VDDIO_1 =VDDIO_2 = VDDD = VDDA = 5.5 V, VSSD < VI < VDDD, VDDIO_1, VDDIO_2, -40 °C ≤ TA ≤ 125 °C TYP: TA = 25 °C, VDDIO_1 =VDDIO_2 = VDDD = VDDA = 5.0 V. | Updated spec |

Rev *H Electrical Specification Updates (continued)

| Spec ID | Description | Changed Item | Current Spec | New Spec | Reason for Change |
|--------------------------------------|-------------------------------------|--------------------|---|--|---|
| SID670C | Input leakage current | All | (none) | Input leakage current for P21.0, P21.1, P21.2, P21.3, P21.4, P22.1, P22.2, P22.3, P23.3, P23.4 | Added spec for P21.0, P21.1, P21.2, P21.3, P21.4, P22.1, P22.2, P22.3, P23.3, P23.4 |
| SID654A to SID657A, SID656D, SID657D | Output voltage HIGH level | Details/Conditions | IOL | IOH | Correction |
| SID670A | Input leakage current | Min Max | Min: -1000 nA Max: 1000 nA Details/Conditions: VDDD = VDDA = 5.5 V, VSSD < VI < VDDD, -40 °C ≤ TA ≤ 125 °C This is valid for the Port which do not have ADC input functionality. TYP: TA = 25 °C, VDDD = VDDA = 5.0 V. | Min: -350 nA Max: 350 nA Details/Conditions: VDDD = VDDA = 5.5 V, VSSD < VI < VDDD, -40 °C ≤ TA ≤ 125 °C TYP: TA = 25 °C, VDDD = VDDA = 5.0 V. | Updated spec |
| SID657B to SID663B, SID663E | Output HIGH voltage | Details/Conditions | IOL | IOH | Correction |
| SID676B | Input leakage current | Min Max | Min: -1000 nA Max: 1000 nA | Min: -450 nA Max: 450 nA | Updated spec |
| SID102A | VDDA voltage range | All | (none) | VDDA voltage range | Added spec |
| SID103A | Internal band gap reference voltage | All | (none) | Internal band gap reference voltage | Added spec |
| SID115 | Analog Input leakage current | Typ | - | 70 nA | Updated spec |
| SID115A | Analog Input leakage current | All | Analog Input leakage current | (none) | Removed spec (SID670 can be used) |
| SID200 | Temperature Sensor accuracy 1 | All | (none) | Temperature Sensor accuracy 1 | Added spec |
| SID201 | Temperature Sensor accuracy 2 | All | (none) | Temperature Sensor accuracy 2 | Added spec |
| SID201A | Temperature Sensor accuracy 3 | All | (none) | Temperature Sensor accuracy 3 | Added spec |

Rev *H Electrical Specification Updates (continued)

| Spec ID | Description | Changed Item | Current Spec | New Spec | Reason for Change |
|--------------|--|----------------------------------|---|--|----------------------------------|
| SID219 | SPI Capacitive Load for SPI Interface Slave (internally clocked) | Parameter | CSPIM_INT | CSPIS_INT | Fixed parameter name |
| SID223 | SPI Slave: Previous MISO data hold time for SPI Interface Slave (externally clocked) | Parameter | tHSP | tHSO_EXT | Fixed parameter name |
| SID230 | SPI Capacitive Load for SPI Interface Slave (externally clocked) | Parameter | CSPIM_EXT | CSPIS_EXT | Fixed parameter name |
| SID320 | ILO operating frequency | Min Max | Min: 31.1296 kHz Max: 34.4064 kHz | Min: 30.47424 kHz Max: 35.06176 kHz | Updated spec |
| SID332 | Feedback resistor vaule | All | (None) | Feedback resistor vaule | Added spec |
| SID334 | 8 MHz ECO startup time | Parameter Description Note | Parameter: tSTART_4M Description: 4 MHz ECO startup time Note: (none) | Parameter: tSTART_8M Description: 8 MHz ECO startup time Note: [64] Mainly depends on the external crystal. | Updated spec |
| SID335 | 33 MHz ECO startup time | Note | (none) | Note: [64] Mainly depends on the external crystal. | Added note |
| SID336 | ECO amplifier operating point | All | ECO amplifier operating point | (none) | Removed spec |
| SID342D 1 | Long term jitter | Parameter Details/Conditions | Parameter: PLL_LJIT1 Details/Conditions: For 125 ns fVCO: 800 MHz (spreading is off) fIN: ECO fPPD: 4 MHz fOUT: 100 MHz | Parameter: PLL400_LJIT1 Details/Conditions: For 125 ns Guaranteed by Design fVCO: 800 MHz or 700 MHz (spreading is off) fIN: ECO fPPD: 4 MHz fOUT: 100 MHz to 350 MHz | Updated parameter and conditions |
| SID343D 1 | Long term jitter | Details/Conditions | Parameter: PLL_LJIT2 Details/Conditions: For 500 ns fVCO: 800 MHz (spreading is off) fIN: ECO fPPD: 4 MHz fOUT: 100 MHz | Parameter: PLL400_LJIT2 Details/Conditions: For 500 ns Guaranteed by Design fVCO: 800 MHz or 700 MHz (spreading is off) fIN: ECO fPPD: 4 MHz fOUT: 100 MHz to 350 MHz | Updated parameter and conditions |

Rev *H Electrical Specification Updates (continued)

| Spec ID | Description | Changed Item | Current Spec | New Spec | Reason for Change |
|--------------|-------------------------------|----------------------------|---|--|----------------------------------|
| SID344D 1 | Long term jitter | Details/Conditions | Parameter: PLL_LJIT3 Details/Conditions: For 1000 ns fVCO: 800 MHz (spreading is off) fIN: ECO fPPD: 4 MHz fOUT: 100 MHz | Parameter: PLL400_LJIT3 Details/Conditions: For 1000 ns Guaranteed by Design fVCO: 800 MHz or 700 MHz (spreading is off) fIN: ECO fPPD: 4 MHz fOUT: 100 MHz to 350 MHz | Updated parameter and conditions |
| SID345E 1 | Long term jitter | Details/Conditions | Parameter: PLL_LJIT5 Details/Conditions: For 10000 ns fVCO: 800 MHz (spreading is off) fIN: ECO fPPD: 4 MHz fOUT: 100 MHz | Parameter: PLL400_LJIT5 Details/Conditions: For 10000 ns Guaranteed by Design fVCO: 800 MHz or 700 MHz (spreading is off) fIN: ECO fPPD: 4 MHz fOUT: 100 MHz to 350 MHz | Updated parameter and conditions |
| SID362 | WCO start up time | Note Details/Conditions | (none) | Note: [66] Mainly depends on the external crystal. Details/Conditions: For Grade-S devices | Added note and condition |
| SID362E | WCO start up time | All | (none) | WCO start up time for Grade-E devices | Added spec for Grade-E devices |
| SID363 | WCO current | Min Typ Max | Min: 1 uA Typ: 4 uA Max: 8 uA | Min: - Typ: 1.4 uA Max: - | Updated spec |
| SID364 | WCO amplifier operating point | All | WCO amplifier operating point | (none) | Removed spec |
| SID410 | Minimum MCWDT timeout | Min Details/Conditions | Min: 58.12 us Details/Conditions: 'When using the ILO (32 kHz + 5 %) and 16-bit MCWDT counter. Guaranteed by Design. | Min: 57 us Details/Conditions: When using the ILO (32.768 kHz + 7 %) and 16-bit MCWDT counter. Guaranteed by Design. | Updated condition |
| SID411 | Maximum MCWDT timeout | Max Details/Conditions | Max: 2.11 s Details/Conditions: When using the ILO (32 kHz - 5 %) and 16-bit MCWDT counter. Guaranteed by Design. | Max: 2.15 s Details/Conditions: When using the ILO (32.768 kHz - 7 %) and 16-bit MCWDT counter. Guaranteed by Design. | Updated condition |
| SID412 | Minimum WDT timeout | Min Details/Conditions | Min: 58.12 us Details/Conditions: When using the ILO (32 kHz + 5 %) and 32-bit WDT counter. Guaranteed by Design. | Min: 57 us Details/Conditions: When using the ILO (32.768 kHz + 7 %) and 32-bit WDT counter. Guaranteed by Design. | Updated condition |
| SID413 | Maximum WDT timeout | Max Details/Conditions | Max: 38.33 h Details/Conditions: When using the ILO (32 kHz - 5 %) and 32-bit WDT counter. Guaranteed by Design. | Max: 39.15 h Details/Conditions: When using the ILO (32.768 kHz - 7 %) and 32-bit WDT counter. Guaranteed by Design. | Updated condition |

Rev *H Electrical Specification Updates (continued)

| Spec ID | Description | Changed Item | Current Spec | New Spec | Reason for Change |
|---------|---|--------------|------------------------------|------------------|-------------------|
| SID375 | MII TX/RX_CLK Clock frequency | Min Max | Min: -50 ppm Max: +50 ppm | Min: - Max: - | Updated spec |
| SID390 | Short term jitter | All | Short term jitter | (none) | Removed spec |
| SID391 | Long term jitter | All | Long term jitter | (none) | Removed spec |
| SID375A | RMI reference Clock frequency | Min Max | Min: -50 ppm Max: +50 ppm | Min: - Max: - | Updated spec |
| SID390A | Short term jitter | All | Short term jitter | (none) | Removed spec |
| SID391A | Long term jitter | All | Long term jitter | (none) | Removed spec |
| SID379 | REF_CLK clock frequency | Min Max | Min: -50 ppm Max: +50 ppm | Min: - Max: - | Updated spec |
| SID380 | RX_CLK clock frequency | Min Max | Min: -50 ppm Max: +50 ppm | Min: - Max: - | Updated spec |
| SID392 | Clock jitter | All | Clock jitter | (none) | Removed spec |
| SID385 | REF_CLK, TX_CLK and RX_CLK clock frequency | Min Max | Min: -50 ppm Max: +50 ppm | Min: - Max: - | Updated spec |
| SID392A | Clock jitter | All | Clock jitter | (none) | Removed spec |

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