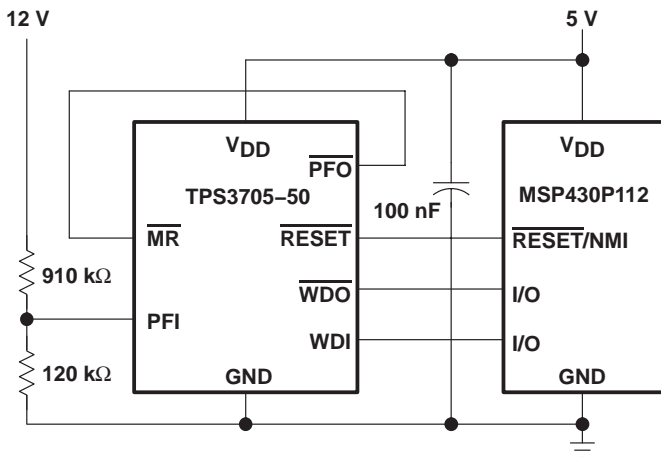


**features**

- Power-On Reset Generator with Fixed Delay Time of 200 ms, no External Capacitor Needed
- Precision Supply Voltage Monitor 2.5 V, 3 V, 3.3 V, and 5 V
- Pin-For-Pin Compatible with the MAX705 through MAX708 Series
- Integrated Watchdog Timer (TPS3705 only)
- Voltage Monitor for Power-Fail or Low-Battery Warning
- Maximum Supply Current of 50  $\mu$ A
- MSOP-8 and SO-8 Packages
- Temperature Range . . .  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$

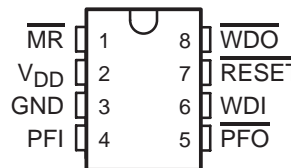
**typical applications**

- Designs Using DSPs, Microcontrollers or Microprocessors
- Industrial Equipment
- Programmable Controls
- Automotive Systems
- Portable/Battery Powered Equipment
- Intelligent Instruments
- Wireless Communication Systems
- Notebook/Desktop Computers

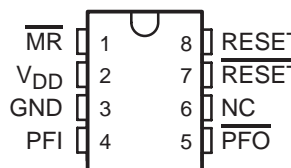


**Figure 1. Typical MSP430 Application**

**TPS3705 . . . D PACKAGE (TOP VIEW)**

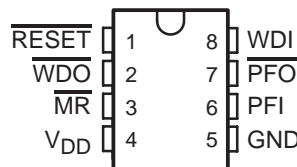


**TPS3707 . . . D PACKAGE (TOP VIEW)**

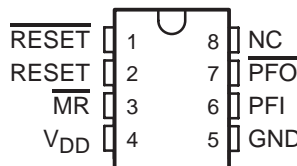


NC – No internal connection

**TPS3705 . . . DGN PACKAGE (TOP VIEW)**



**TPS3707 . . . DGN PACKAGE (TOP VIEW)**



NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



**TPS3705-xx**  
**TPS3707-xx**  
**PROCESSOR SUPERVISORY CIRCUITS WITH POWER-FAIL**

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**description**

The TPS3705, TPS3707 family of microprocessor supply-voltage supervisors provide circuit initialization and timing supervision, primarily for DSP and processor-based systems.

During power-on,  $\overline{\text{RESET}}$  is asserted when the supply voltage  $V_{DD}$  becomes higher than 1.1 V. Thereafter, the supply voltage supervisor monitors  $V_{DD}$  and keeps  $\overline{\text{RESET}}$  active as long as  $V_{DD}$  remains below the threshold voltage  $V_{IT+}$ . An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time,  $t_{d\text{typ}} = 200$  ms, starts after  $V_{DD}$  has risen above the threshold voltage  $V_{IT+}$ . When the supply voltage drops below the threshold voltage  $V_{IT-}$ , the output becomes active (low) again. No external components are required. All the devices of this family have a fixed-sense threshold voltage  $V_{IT-}$  set by an internal voltage divider.

The TPS3705-xx and TPS3707-xx devices incorporate a manual reset input,  $\overline{\text{MR}}$ . A low level at  $\overline{\text{MR}}$  causes  $\overline{\text{RESET}}$  to become active.

The TPS370x-xx families integrate a power-fail comparator which can be used for low-battery detection, power-fail warning, or for monitoring a power supply other than the main supply.

The TPS3705-xx devices have a watchdog timer that is periodically triggered by a positive or negative transition at WDI. When the supervising system fails to retrigger the watchdog circuit within the time-out interval,  $t_{t(\text{out})} = 1.6$  s,  $\overline{\text{WDO}}$  becomes active. This event also reinitializes the watchdog timer. Leaving WDI unconnected disables the watchdog.

The TPS3707-xx devices do not have the Watchdog function, but include a high-level output RESET.

The product spectrum is designed for supply voltages of 2.5 V, 3 V, 3.3 V, and 5 V. The circuits are available in either 8-pin MSOP or standard SOIC packages. The TPS3705, TPS3707 devices are characterized for operation over a temperature range of  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

**AVAILABLE OPTIONS**

$T_A$	THRESHOLD VOLTAGE	PACKAGED DEVICES		MARKING DGN PACKAGE	CHIP FORM (Y)
		SMALL OUTLINE (D)	POWER-PAD™ μ-SMALL OUTLINE (DGN)		
$-40^{\circ}\text{C}$ to $85^{\circ}\text{C}$	2.63 V	TPS3705-30D	TPS3705-30DGN	TIAAT	TPS3705-30Y
	2.93 V	TPS3705-33D	TPS3705-33DGN	TIAAU	TPS3705-33Y
	4.55 V	TPS3705-50D	TPS3705-50DGN	TIAAV	TPS3705-50Y
	2.25 V	TPS3707-25D	TPS3707-25DGN	TIAAW	TPS3707-25Y
	2.63 V	TPS3707-30D	TPS3707-30DGN	TIAAX	TPS3707-30Y
	2.93 V	TPS3707-33D	TPS3707-33DGN	TIAAY	TPS3707-33Y
	4.55 V	TPS3707-50D	TPS3707-50DGN	TIAAZ	TPS3707-50Y



**PROCESSOR SUPERVISORY CIRCUITS WITH POWER-FAIL**

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**Function Tables**

TRUTH TABLE, TPS3705

$\overline{\text{MR}}$	$V_{\text{DD}} > V_{\text{IT}}$	$\overline{\text{RESET}}$	TYPICAL DELAY
H→L	1	H→L	30 ns
L→H	1	L→H	200 ms
H	1→0	H→L	3 μs
H	0→1	L→H	200 ms

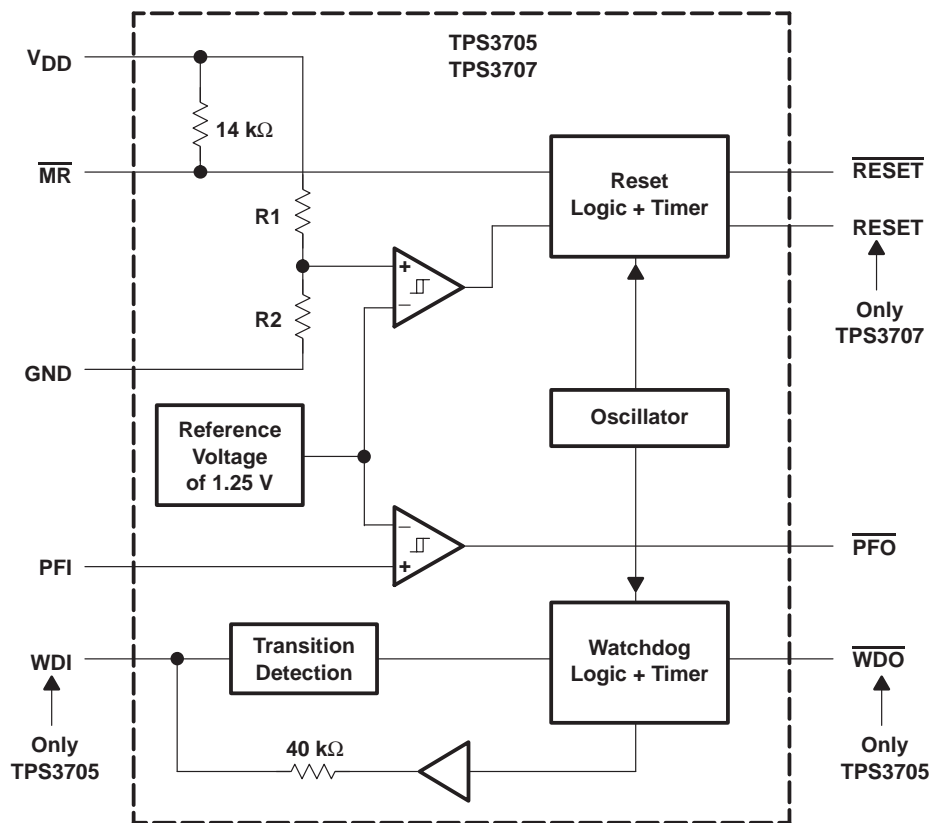
TRUTH TABLE, TPS3707

$\overline{\text{MR}}$	$V_{\text{DD}} > V_{\text{IT}}$	$\overline{\text{RESET}}$	RESET	TYPICAL DELAY
H→L	1	H→L	L→H	30 ns
L→H	1	L→H	H→L	200 ms
H	1→0	H→L	L→H	3 μs
H	0→1	L→H	H→L	200 ms

TRUTH TABLE, TPS370x

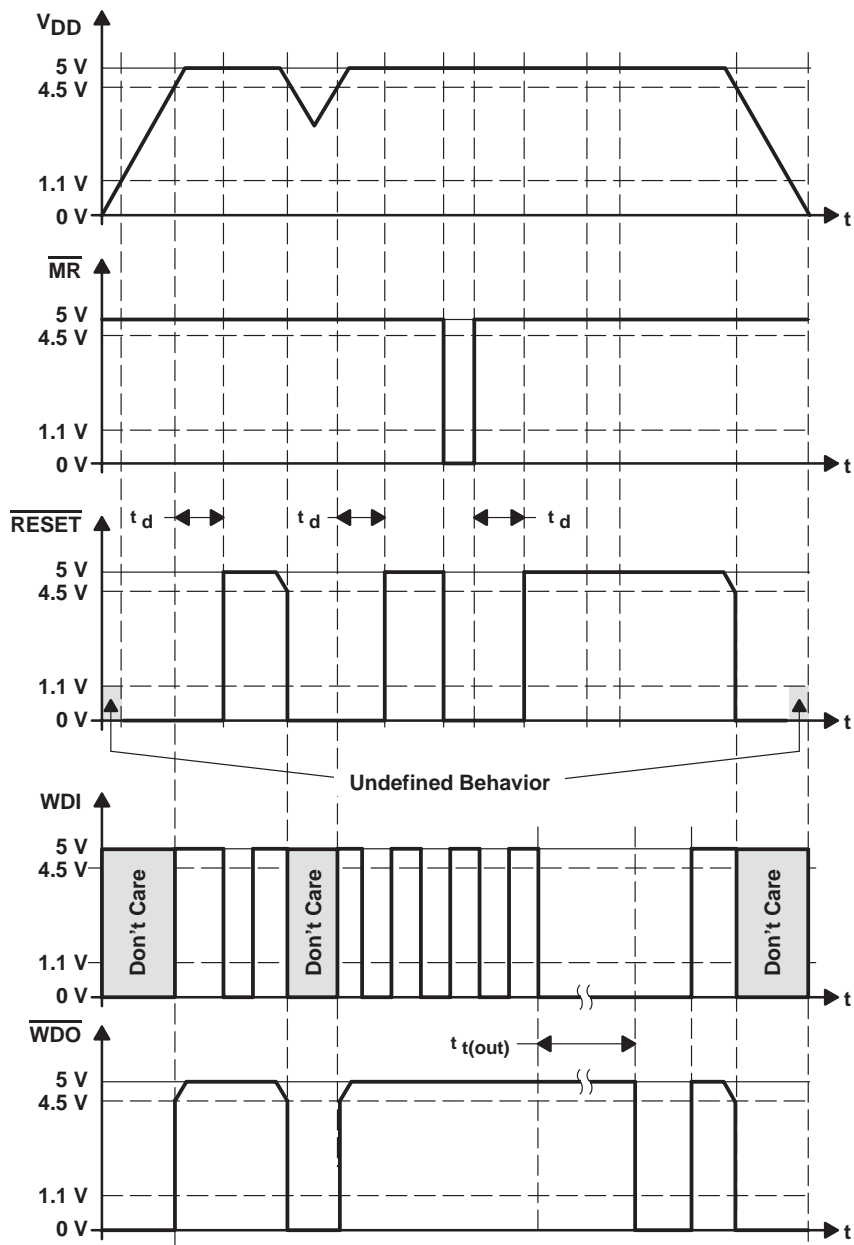
$\text{PFI} > V_{\text{IT}}$	$\overline{\text{PFO}}$	TYPICAL DELAY
0→1	L→H	0.5 μs
1→0	H→L	0.5 μs

**functional block diagram**



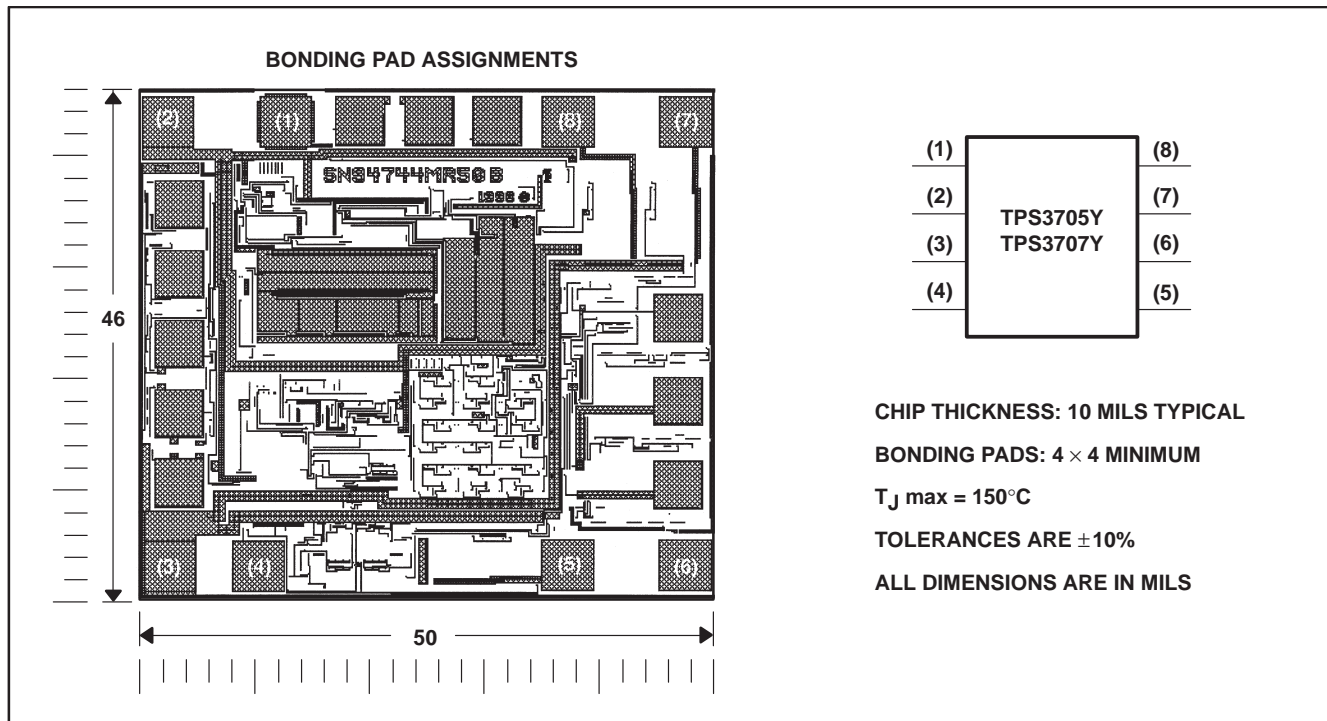
TPS3705-xx  
 TPS3707-xx  
**PROCESSOR SUPERVISORY CIRCUITS WITH POWER-FAIL**  
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timing diagrams



**TPS370xY chip information**

These chips, when properly assembled, display characteristics similar to those of the TPS370x. Thermal compression or ultrasonic bonding may be caused on the doped-aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.



**Terminal Functions**

TERMINAL NAME		NO.	I/O	DESCRIPTION
$\overline{\text{MR}}$		1	I	Manual reset
VDD		2		Supply voltage
GND		3		Ground
PFI		4	I	Power-fail comparator input
$\overline{\text{PFO}}$		5	O	Power-fail comparator output
WDI	TPS3705	6	I	Watchdog timer input
NC	TPS3707			No internal connection
$\overline{\text{RESET}}$		7	O	Active-low reset output
$\overline{\text{WDO}}$	TPS3705	8	O	Watchdog timer output
RESET	TPS3707			Active-high reset output

**PROCESSOR SUPERVISORY CIRCUITS WITH POWER-FAIL**

**absolute maximum ratings over operating free-air temperature (unless otherwise noted)†**

Supply voltage, $V_{DD}$ (see Note1)	7 V
PFI voltage range, $V_{PFI}$	-0.3 V to $V_{DD} + 0.3$ V
All other pins (see Note 1)	-0.3 V to 7 V
Maximum low output current, $I_{OL}$	5 mA
Maximum high output current, $I_{OH}$	-5 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{DD}$ )	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{DD}$ )	$\pm 20$ mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, $T_A$	-40°C to 85°C
Storage temperature range, $T_{stg}$	-65°C to 150°C
Soldering temperature	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND. For reliable operation the device must not be operated at 7 V for more than  $t = 1000h$  continuously.

**DISSIPATION RATING TABLE**

PACKAGE	$T_A < 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
DGN	2.14 W	17.1 mW/°C	1.37 W	1.11 W
D	725 mW	5.8 mW/°C	464 mW	377 mW

**recommended operating conditions at specified temperature range**

	MIN	MAX	UNIT
Supply voltage, $V_{DD}$	2	6	V
Input voltage, $V_I$	0	$V_{DD} + 0.3$	V
High-level input voltage, $V_{IH}$	$0.7 \times V_{DD}$		V
Low-level input voltage, $V_{IL}$	$0.3 \times V_{DD}$		V
Input transition rise and fall rate at $\overline{MR}$ or $WDI$ , $\Delta t/\Delta V$	100		ns/V
Operating free-air temperature range, $T_A$	-40	85	°C

**TPS3705-xx**  
**TPS3707-xx**

## PROCESSOR SUPERVISORY CIRCUITS WITH POWER-FAIL

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT		
V <sub>OH</sub>	High-level output voltage	TPS370x-xx	V <sub>DD</sub> = 1.1 V, I <sub>OH</sub> = -4 μA	0.8			V		
		TPS3707-25	V <sub>DD</sub> = V <sub>IT+</sub> + 0.2 V, I <sub>OH</sub> = -500 μA	0.7×V <sub>DD</sub>					
		TPS370x-30							
		TPS370x-33							
		TPS370x-50	V <sub>DD</sub> = V <sub>IT+</sub> + 0.2 V, I <sub>OH</sub> = -800 μA	V <sub>DD</sub> - 1.5 V					
TPS370x-xx	V <sub>DD</sub> = 6 V, I <sub>OH</sub> = -800 μA								
V <sub>OL</sub>	Low-level output voltage	TPS3707-25	V <sub>DD</sub> = V <sub>IT+</sub> + 0.2 V, I <sub>OL</sub> = 1 mA				0.3		
		TPS370x-30							
		TPS370x-33							
		TPS370x-50	V <sub>DD</sub> = V <sub>IT+</sub> + 0.2 V, I <sub>OL</sub> = 2.5 mA				0.4		
		TPS370x-xx	V <sub>DD</sub> = 6 V, I <sub>OL</sub> = 3 mA						
Power-up reset voltage (see Note 2)			V <sub>DD</sub> ≥ 1.1 V, I <sub>OL</sub> = 50 μA				0.3		
V <sub>IT-</sub>	Negative-going input threshold voltage (see Note 3)	TPS3707-25	T <sub>A</sub> = 0°C to 85°C	2.20	2.25	2.30	V		
		TPS370x-30		2.57	2.63	2.68			
		TPS370x-33		2.87	2.93	2.98			
		TPS370x-50		4.45	4.55	4.63			
		TPS3707-25	T <sub>A</sub> = -40°C to 85°C	2.20	2.25	2.32	V		
		TPS370x-30		2.57	2.63	2.70			
		TPS370x-33		2.87	2.93	3.0			
		TPS370x-50		4.45	4.55	4.65			
	PFI	TPS370x-xx	V <sub>DD</sub> ≥ 2 V, T <sub>A</sub> = -40°C to 85°C	1.20	1.25	1.30	V		
	V <sub>hys</sub>	Hysteresis	V <sub>DD</sub>	TPS3707-25	40			mV	
TPS370x-30				50					
TPS370x-33				50					
TPS370x-50				70					
PFI			TPS370x-xx	10					
I <sub>IH(AV)</sub>	Average high-level input current	WDI		WDI = V <sub>DD</sub> = 6 V, Time average (dc = 88%)		100	150	μA	
I <sub>IL(AV)</sub>	Average low-level input current			WDI = 0 V, V <sub>DD</sub> = 6 V, Time average (dc = 12%)		-15	-20	μA	
I <sub>IH</sub>	High-level input current	WDI		WDI = V <sub>DD</sub> = 6 V		120	170	μA	
		MR		MR = 0.7×V <sub>DD</sub> , V <sub>DD</sub> = 6 V		-130	-180		
I <sub>IL</sub>	Low-level input current	WDI		WDI = 0 V, V <sub>DD</sub> = 6 V		-120	-170	μA	
		MR		MR = 0 V, V <sub>DD</sub> = 6 V		-430	-600		
I <sub>I</sub>	Input current	PFI		V <sub>DD</sub> = 6 V, 0 V ≤ V <sub>I</sub> ≤ V <sub>DD</sub>		-1	0	1	μA
I <sub>DD</sub>	Supply current	TPS3707-xx		V <sub>DD</sub> = 2 V to 6 V, MR = V <sub>DD</sub> , MR, WDI and outputs unconnected		20	50	μA	
		TPS3705-xx		V <sub>DD</sub> = 2 V to 6 V, MR = V <sub>DD</sub> , MR, WDI and outputs unconnected		30	50	μA	
C <sub>i</sub>	Input capacitance			V <sub>I</sub> = 0 V to V <sub>DD</sub>		5		pF	

NOTES: 2. The lowest supply voltage at which RESET becomes active. t<sub>r</sub>V<sub>DD</sub> ≥ 15 μs/V  
3. To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 μF) should be placed near to the supply terminals.



## PROCESSOR SUPERVISORY CIRCUITS WITH POWER-FAIL

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timing requirements at  $R_L = 1\text{ M}\Omega$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$ 

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_w$	Pulse width					
	at $V_{DD}$	$V_{DD} = V_{IT+} + 0.2\text{ V}$ , $V_{DD} = V_{IT-} - 0.2\text{ V}$	6			$\mu\text{s}$
	at $\overline{\text{MR}}$	$V_{DD} \geq V_{IT+} + 0.2\text{ V}$ , $V_{IL} = 0.3 \times V_{DD}$ , $V_{IH} = 0.7 \times V_{DD}$	100			ns
	at $\text{WDI}$	$V_{DD} \geq V_{IT+} + 0.2\text{ V}$ , $V_{IL} = 0.3 \times V_{DD}$ , $V_{IH} = 0.7 \times V_{DD}$	100			ns

switching characteristics at  $R_L = 1\text{ M}\Omega$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$ 

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{t(\text{out})}$	Watchdog time out	$V_{DD} \geq V_{IT+} + 0.2\text{ V}$ , See timing diagram	1.1	1.6	2.3	s
$t_d$	Delay time	$V_{DD} > V_{IT+} + 0.2\text{ V}$ , See timing diagram	140	200	280	ms
$t_{\text{PHL}}$	Propagation (delay) time, high-to-low-level output	$\overline{\text{MR}}$ to $\overline{\text{RESET}}$ delay		50	250	ns
$t_{\text{PLH}}$	Propagation (delay) time, low-to-high-level output	$\overline{\text{MR}}$ to $\overline{\text{RESET}}$ delay (TPS3707-xx only)		50	250	
$t_{\text{PHL}}$	Propagation (delay) time, high-to-low-level output	$V_{DD}$ to $\overline{\text{RESET}}$ delay		3	5	$\mu\text{s}$
$t_{\text{PLH}}$	Propagation (delay) time, low-to-high-level output	$V_{DD}$ to $\overline{\text{RESET}}$ delay (TPS3707-xx only)		3	5	
$t_{\text{PHL}}$	Propagation (delay) time, high-to-low-level output	$\text{PFI}$ to $\overline{\text{PFO}}$ delay	$V_{DD} = 2\text{ V to }6\text{ V}$	0.5	1	$\mu\text{s}$
$t_{\text{PLH}}$	Propagation (delay) time, low-to-high-level output			0.5	1	



TYPICAL CHARACTERISTICS

NORMALIZED INPUT THRESHOLD VOLTAGE  
vs  
FREE-AIR TEMPERATURE AT  $V_{DD}$

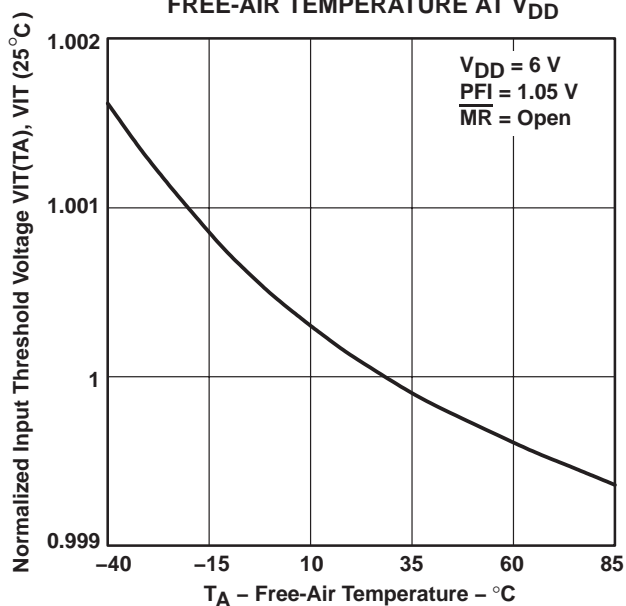


Figure 2

SUPPLY CURRENT  
vs  
SUPPLY VOLTAGE

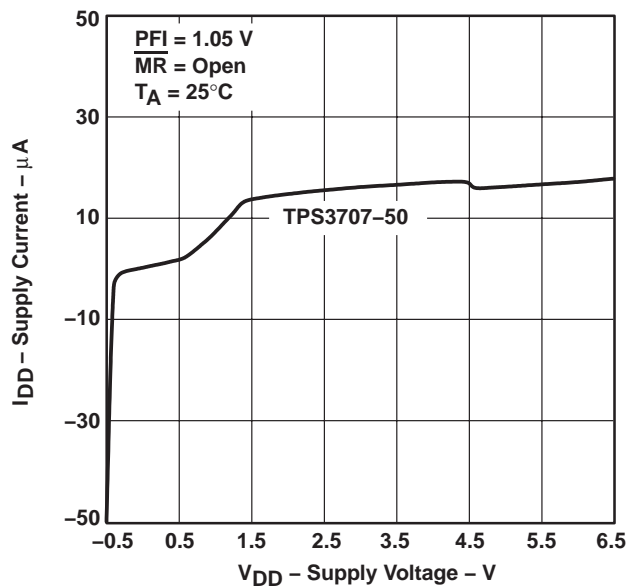


Figure 3

INPUT CURRENT  
vs  
INPUT VOLTAGE AT  $\overline{MR}$

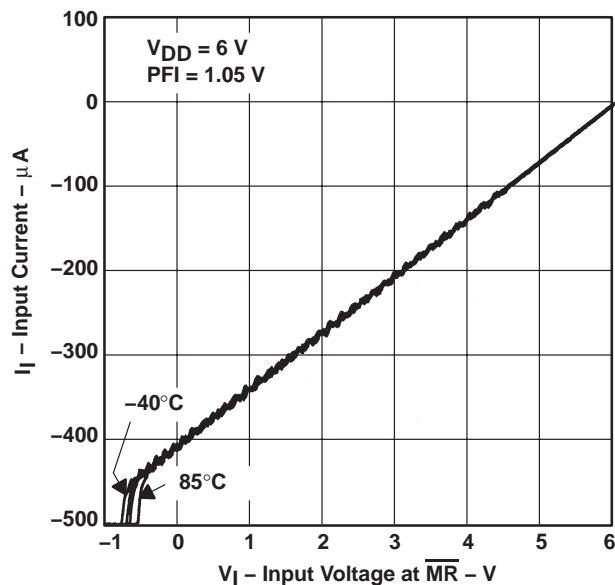


Figure 4

TYPICAL CHARACTERISTICS

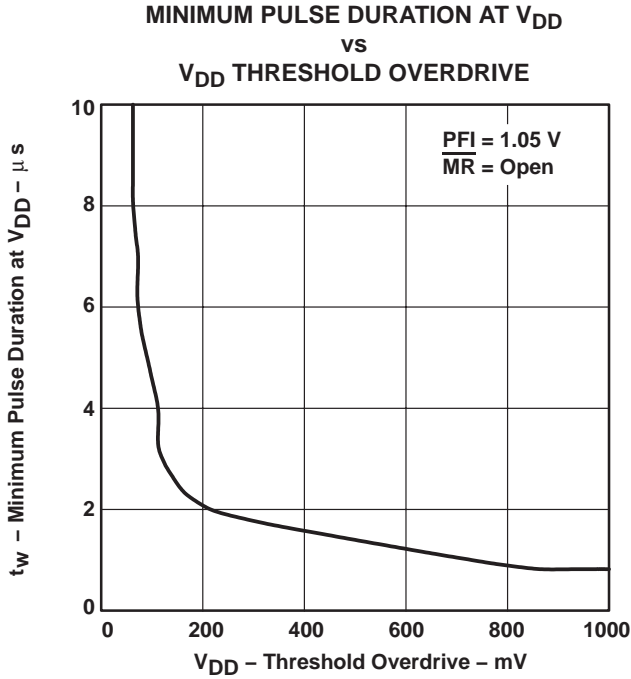


Figure 5

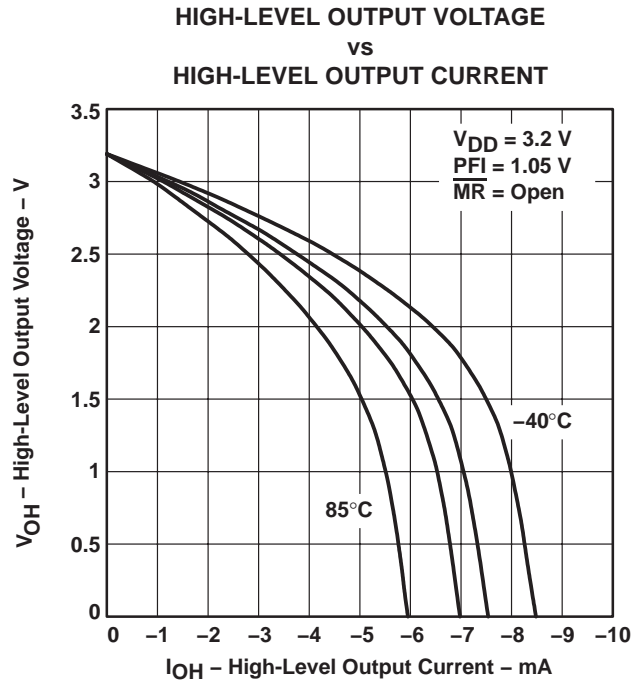


Figure 6

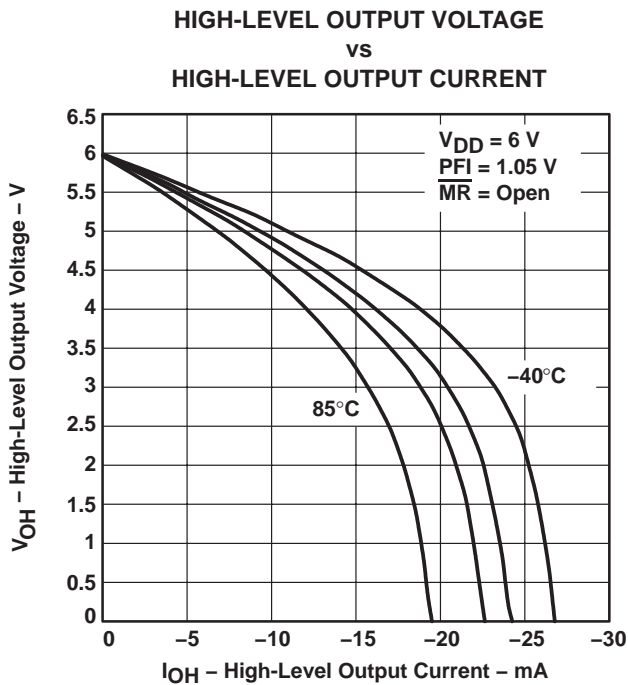


Figure 7

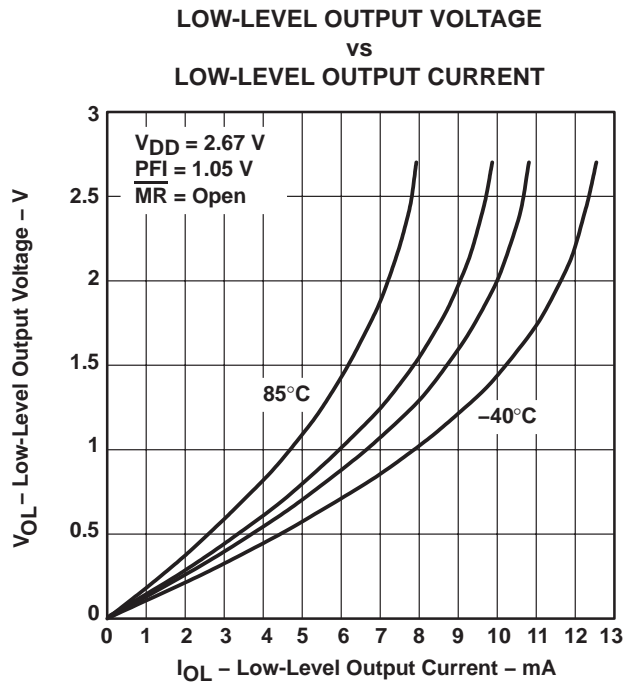


Figure 8

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3705-30D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	70530	<a href="#">Samples</a>
TPS3705-30DGN	ACTIVE	MSOP- PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAT	<a href="#">Samples</a>
TPS3705-30DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	70530	<a href="#">Samples</a>
TPS3705-30DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	70530	<a href="#">Samples</a>
TPS3705-33D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	70533	<a href="#">Samples</a>
TPS3705-33DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	70533	<a href="#">Samples</a>
TPS3705-33DGN	ACTIVE	MSOP- PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAU	<a href="#">Samples</a>
TPS3705-33DGN4	ACTIVE	MSOP- PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAU	<a href="#">Samples</a>
TPS3705-33DGNR	ACTIVE	MSOP- PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAU	<a href="#">Samples</a>
TPS3705-33DGNRG4	ACTIVE	MSOP- PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAU	<a href="#">Samples</a>
TPS3705-33DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	70533	<a href="#">Samples</a>
TPS3705-33DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	70533	<a href="#">Samples</a>
TPS3705-50D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	70550	<a href="#">Samples</a>
TPS3705-50DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	70550	<a href="#">Samples</a>
TPS3705-50DGN	ACTIVE	MSOP- PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAV	<a href="#">Samples</a>
TPS3705-50DGN4	ACTIVE	MSOP- PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAV	<a href="#">Samples</a>
TPS3705-50DGNR	ACTIVE	MSOP- PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAV	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3705-50DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	70550	<a href="#">Samples</a>
TPS3705-50DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	70550	<a href="#">Samples</a>
TPS3707-25D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	70725	<a href="#">Samples</a>
TPS3707-25DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	70725	<a href="#">Samples</a>
TPS3707-25DGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAW	<a href="#">Samples</a>
TPS3707-25DGNG4	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAW	<a href="#">Samples</a>
TPS3707-25DGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAW	<a href="#">Samples</a>
TPS3707-25DGNRG4	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAW	<a href="#">Samples</a>
TPS3707-25DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	70725	<a href="#">Samples</a>
TPS3707-30D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	70730	<a href="#">Samples</a>
TPS3707-30DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	70730	<a href="#">Samples</a>
TPS3707-30DGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAX	<a href="#">Samples</a>
TPS3707-30DGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAX	<a href="#">Samples</a>
TPS3707-30DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	70730	<a href="#">Samples</a>
TPS3707-33D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	70733	<a href="#">Samples</a>
TPS3707-33DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	70733	<a href="#">Samples</a>
TPS3707-33DGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAY	<a href="#">Samples</a>
TPS3707-33DGNG4	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAY	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3707-33DGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAY	<a href="#">Samples</a>
TPS3707-33DGNRG4	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAY	<a href="#">Samples</a>
TPS3707-33DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	70733	<a href="#">Samples</a>
TPS3707-33DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	70733	<a href="#">Samples</a>
TPS3707-50D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	70750	<a href="#">Samples</a>
TPS3707-50DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	70750	<a href="#">Samples</a>
TPS3707-50DGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAZ	<a href="#">Samples</a>
TPS3707-50DGNG4	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAZ	<a href="#">Samples</a>
TPS3707-50DGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAZ	<a href="#">Samples</a>
TPS3707-50DGNRG4	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAZ	<a href="#">Samples</a>
TPS3707-50DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	70750	<a href="#">Samples</a>
TPS3707-50DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	70750	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

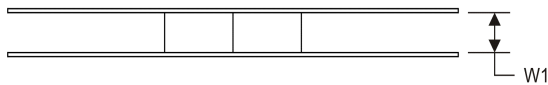
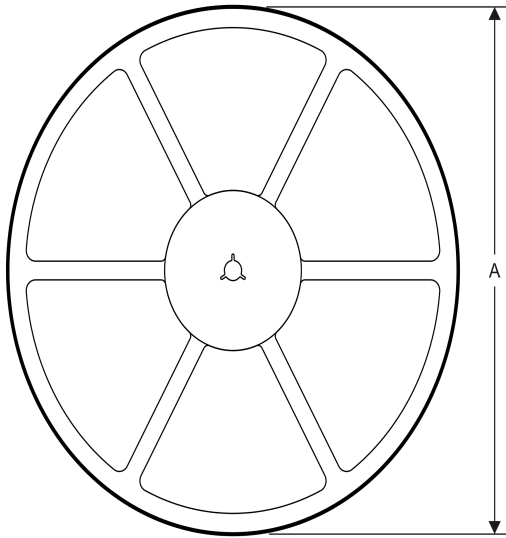
<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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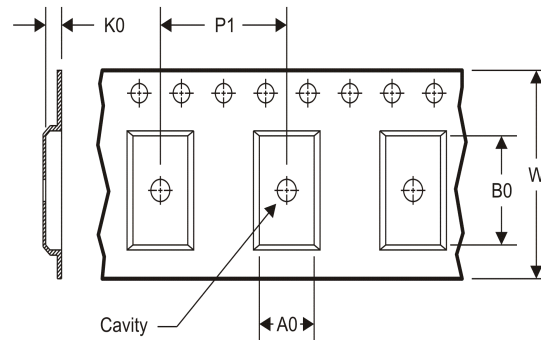
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**TAPE AND REEL INFORMATION**

**REEL DIMENSIONS**



**TAPE DIMENSIONS**



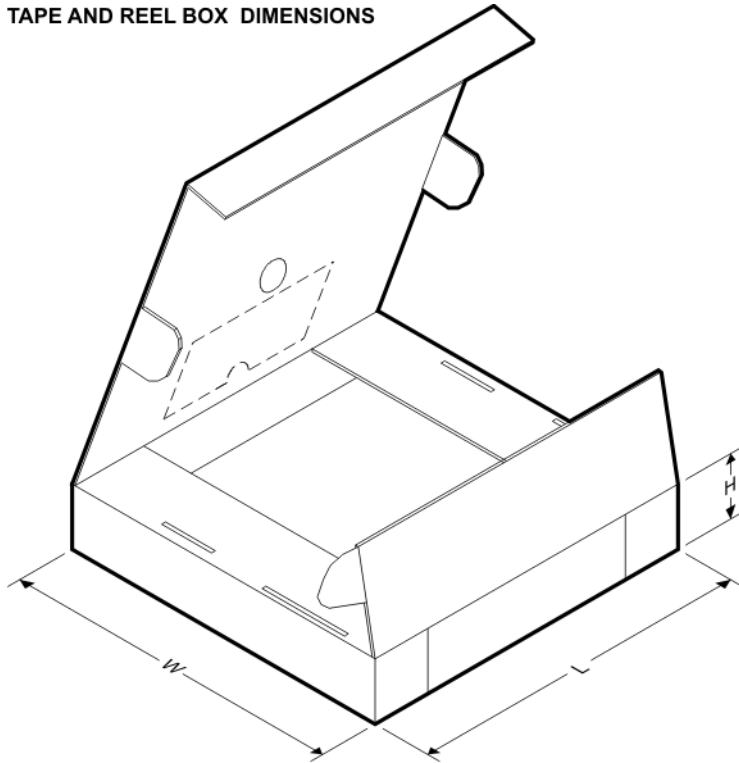
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3705-30DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS3705-33DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS3705-33DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS3705-50DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS3705-50DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS3707-25DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS3707-25DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS3707-30DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS3707-30DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS3707-30DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS3707-33DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3707-33DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS3707-50DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS3707-50DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3705-30DR	SOIC	D	8	2500	367.0	367.0	35.0
TPS3705-33DGNR	MSOP-PowerPAD	DGN	8	2500	358.0	335.0	35.0
TPS3705-33DR	SOIC	D	8	2500	367.0	367.0	35.0
TPS3705-50DGNR	MSOP-PowerPAD	DGN	8	2500	358.0	335.0	35.0
TPS3705-50DR	SOIC	D	8	2500	367.0	367.0	35.0
TPS3707-25DGNR	MSOP-PowerPAD	DGN	8	2500	358.0	335.0	35.0
TPS3707-25DR	SOIC	D	8	2500	367.0	367.0	35.0
TPS3707-30DGNR	MSOP-PowerPAD	DGN	8	2500	358.0	335.0	35.0
TPS3707-30DR	SOIC	D	8	2500	367.0	367.0	35.0
TPS3707-30DR	SOIC	D	8	2500	367.0	367.0	35.0
TPS3707-33DGNR	MSOP-PowerPAD	DGN	8	2500	358.0	335.0	35.0
TPS3707-33DR	SOIC	D	8	2500	367.0	367.0	35.0

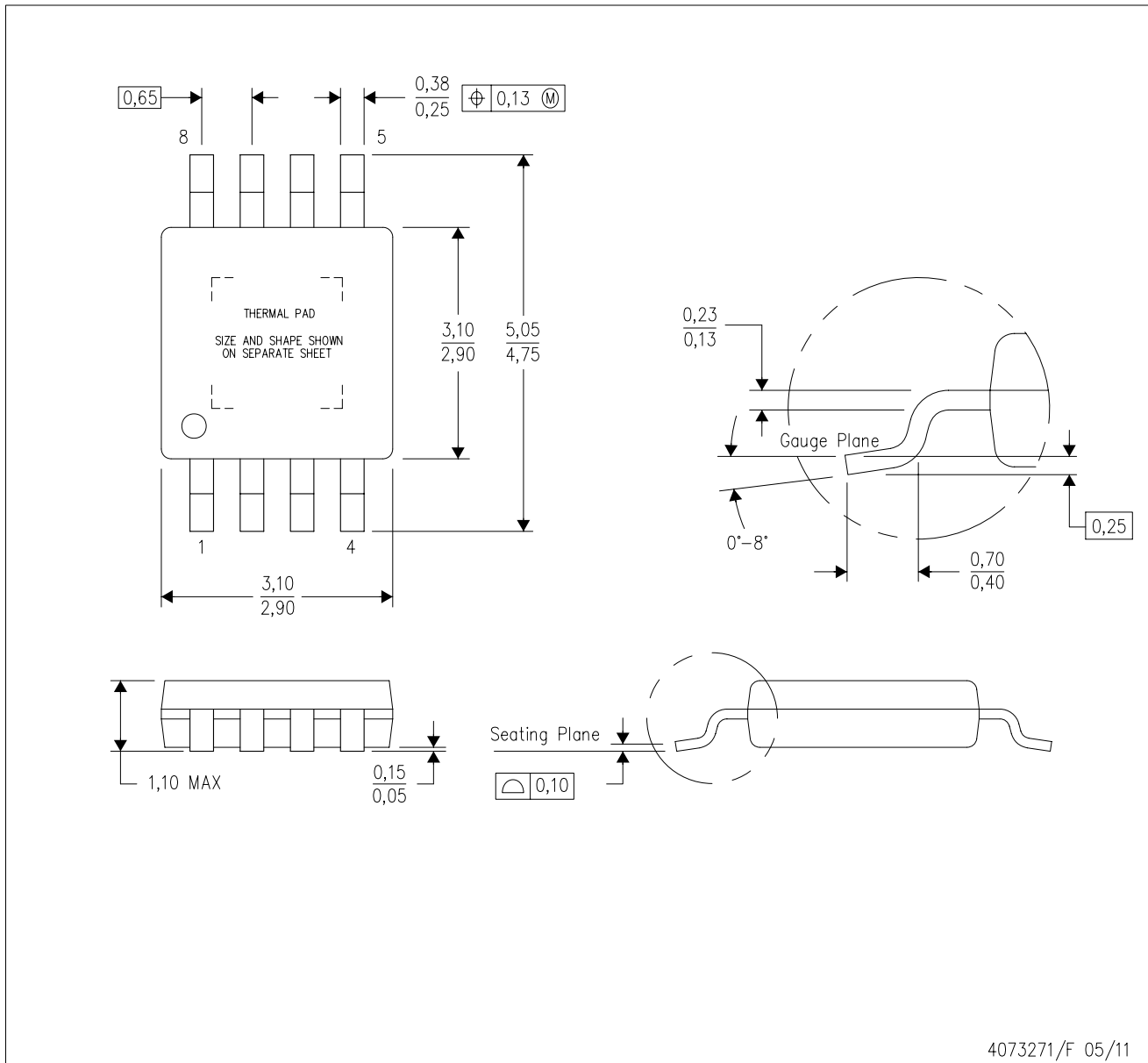


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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3707-50DGNR	MSOP-PowerPAD	DGN	8	2500	358.0	335.0	35.0
TPS3707-50DR	SOIC	D	8	2500	367.0	367.0	35.0

DGN (S-PDSO-G8)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Falls within JEDEC MO-187 variation AA-T

PowerPAD is a trademark of Texas Instruments.

DGN (S-PDSO-G8)

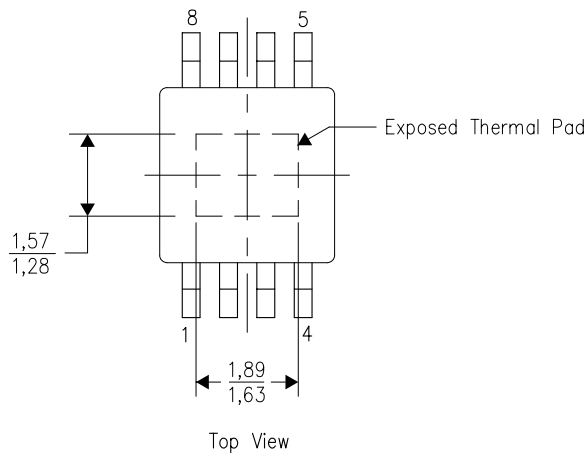
PowerPAD™ PLASTIC SMALL OUTLINE

## THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.

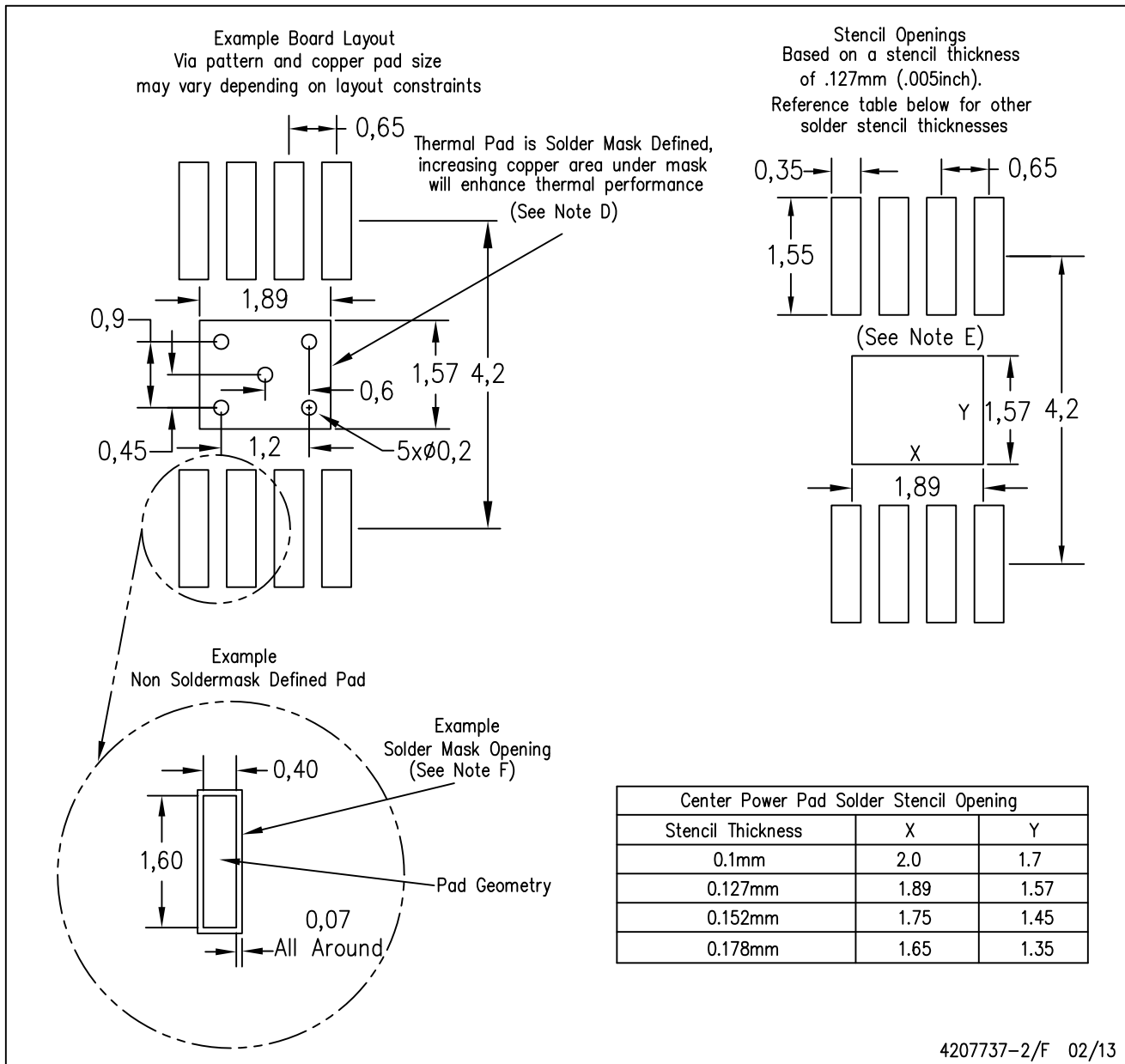


Exposed Thermal Pad Dimensions

4206323-2/1 12/11

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

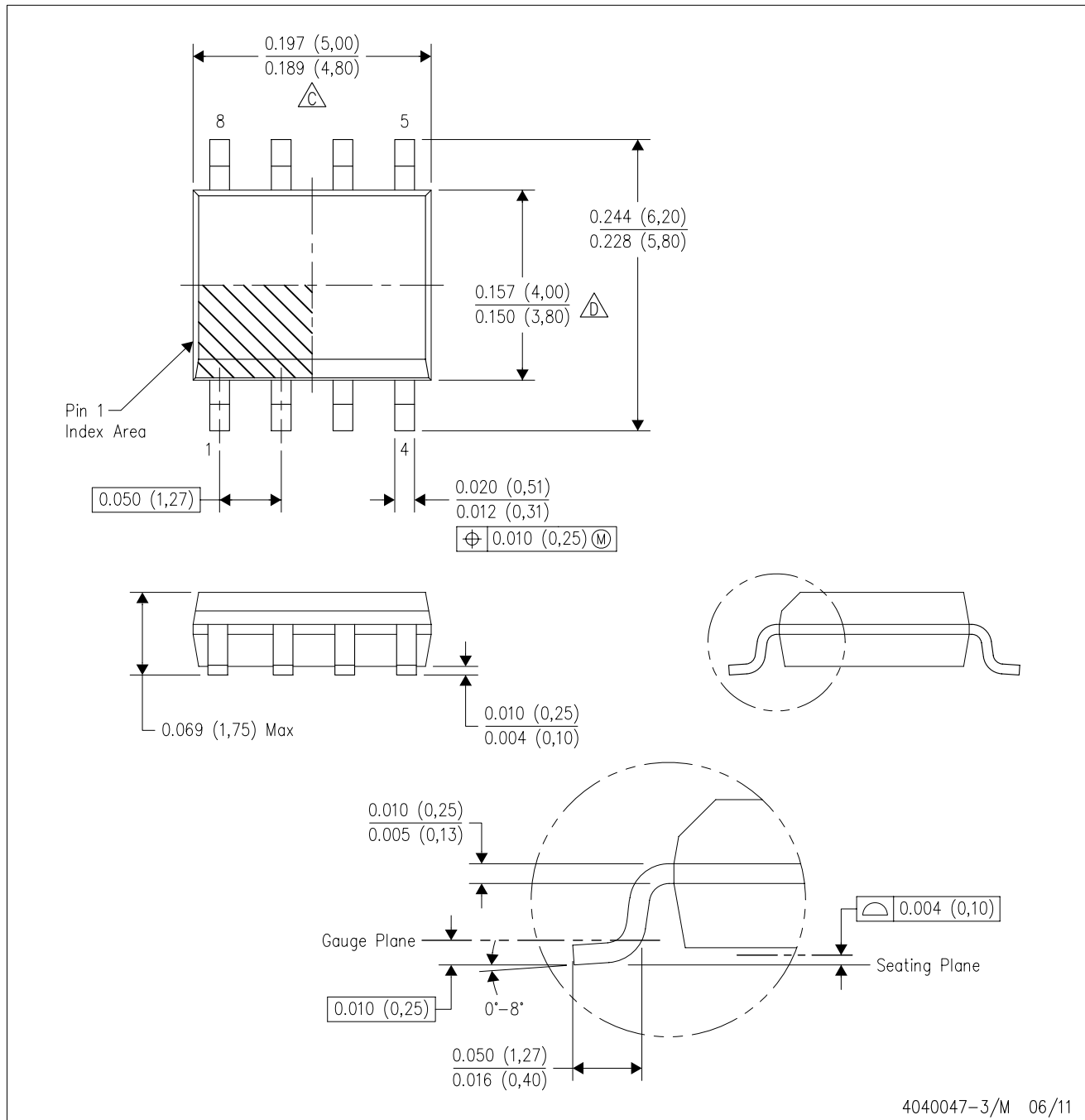


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
  - F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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D (R-PDSO-G8)

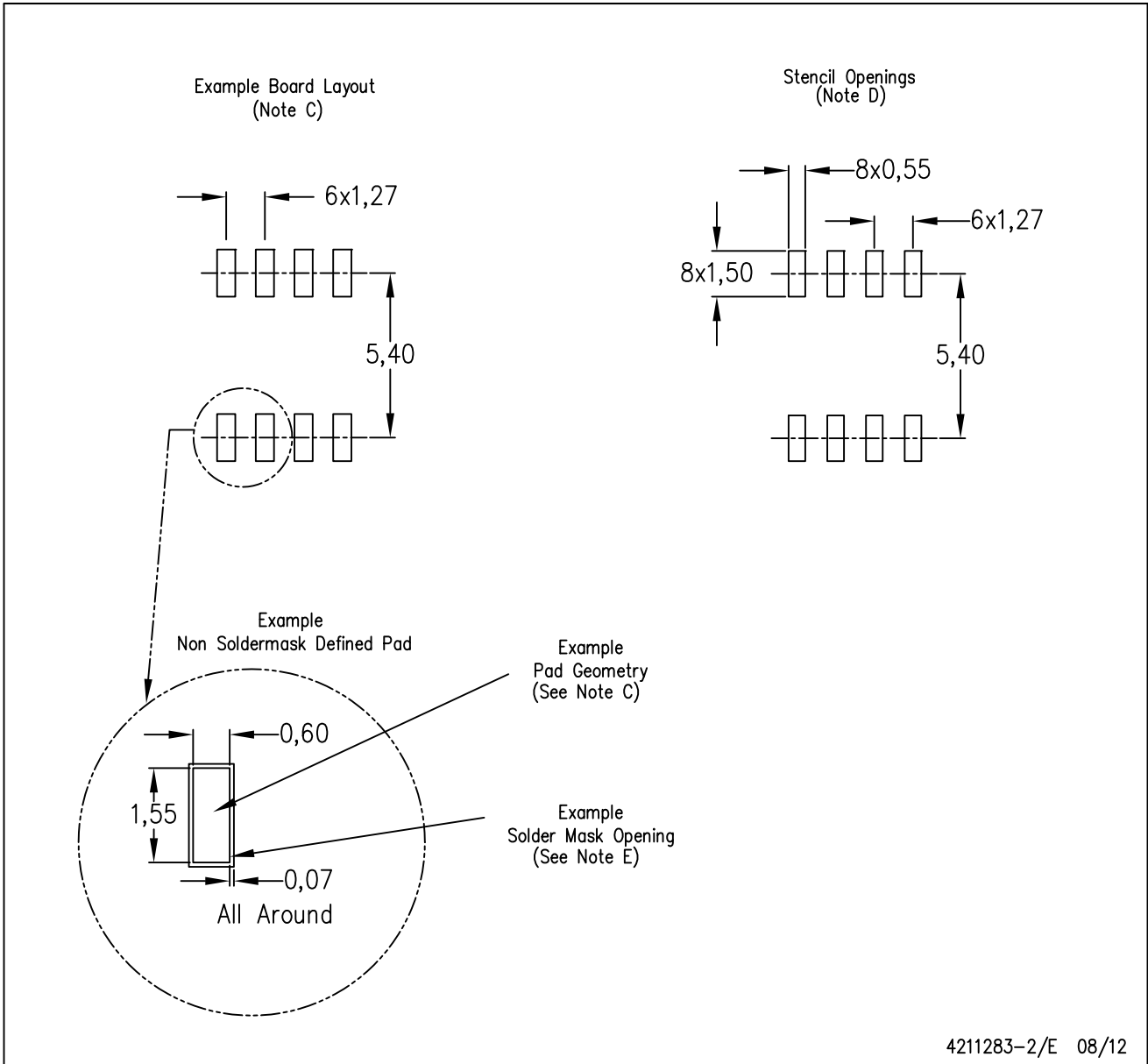
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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