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Freedom FRDM-KV31F Development Platform User's Guide

1. Introduction

The Freedom development platform is a set of software and hardware tools for evaluation and development. It is ideal for rapid prototyping of microcontroller-based applications. The Freedom KV31 hardware, FRDM-KV31F, is a simple, yet sophisticated design featuring a Kinetis V series microcontroller, built on the ARM® Cortex®-M4 core, is a high-performance solution for BLDC, PMSM and ACIM motor control applications.

FRDM-KV31F can be used to evaluate the KV3x Kinetis V series devices. The KV3x device family features the MKV31F512VLL12 microcontroller, which is part of the KV3x device family. This family runs at 100/120 MHz with DSP and floating point unit, and it features dual 16-bit analog-to-digital converters (ADCs) sampling at up to 1.2 mega samples per second (MSPS), multiple motor control timers, 64 KB to 512 KB of flash memory, and a comprehensive enablement suite from NXP and its third-party resources including reference designs, software libraries, and motor configuration tools. The FRDM-KV31F hardware is form-factor compatible with the Arduino® R3 pin layout, providing a broad range of expansion board options. The onboard interface includes a six-axis digital accelerometer & magnetometer, and a RGB LED. The FRDM-KV31F platform features OpenSDA, and an open-source hardware embedded serial and debug adapter running an open-source bootloader. This circuit offers several options for serial communication, flash programming, and run-control debugging. OpenSDA is an mbed HDK-

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compatible debug interface preloaded with the open-source CMSIS-DAP Interface firmware (mbed interface) for rapid prototyping and product development.

2. FRDM-KV31F Hardware Overview

The features of the FRDM-KV31F hardware are as follows:

- MKV31F512VLL12 MCU (120 MHz with DSP instructions, 512 KB flash memory and 96 KB RAM, motor control timers, and 100 LQFP)
- On-board debug circuit: K20DX128VFM5 (OpenSDA) with virtual serial port.RGB LED
- FXOS8700CQ Accelerometer and magnetometer
- Two user push buttons
- Flexible power supply option OpenSDA USB, and external sources
- Easy access to MCU input/output through Arduino R3-compatible I/O connectors
- Programmable OpenSDA debug circuit supporting the P&E Micro Interface software that provides:
 - Mass storage device (MSD) flash programming interface
 - Debug interface providing run-control debugging and compatibility with IDE tools or virtual serial port interface

The primary components and their placement on the hardware assembly are explained in the below figure.

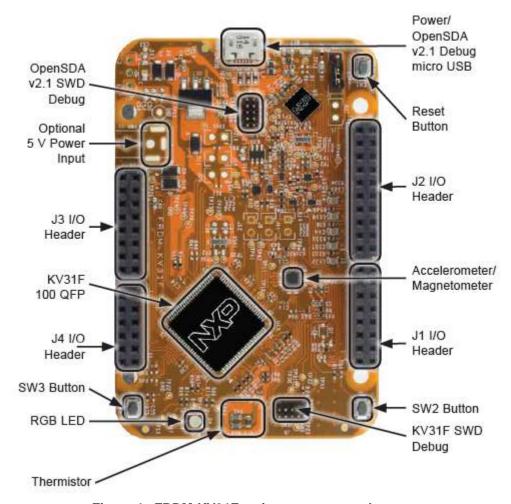


Figure 1. FRDM-KV31F main components placement

3. FRDM-KV31F Hardware Description

3.1. Power supply

There are multiple power supply options on the FRDM-KV31F. It can be powered from either of the USB connectors, the $V_{\rm IN}$ pin on the I/O header, DC Jack (not populated), or an off-board 1.71 V -3.6 V supply from the 3.3 V pin on the I/O header. The USB, DC jack, and $V_{\rm IN}$ supplies are regulated onboard using a 3.3 V linear regulator to produce the main power supply. A DC-to-DC linear regulator is not available in 3.3 V on the J20 Header. However, a direct supply to KV31 microcontroller is available. The table below provides the operational details and requirements for the power supplies.

Supply source	Valid range	OpenSDAv2 operational?	Regulated onboard?
OpenSDAv2 USB	5 V	Yes	Yes
VIN Pin	5 – 9 V	No	Yes
3.3 V Header (J20)	1.71 V – 3.6 V	No	No
DC Jack (not populated)	5 – 9 V	No	Yes

Table 1. FRDM-KV31F Power supply requirements

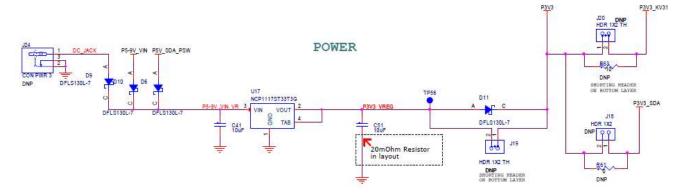


Figure 2. Power supply schematic

3.2. Serial and debug adapter (OpenSDAv2.1)

An on-board K20DX128VFM5-based OpenSDA circuit provides a SWD debug interface to the KV31F512VLL12. A standard USB A male to micro-B male cable (provided) can be used for debugging via the USB connector (J21).

The OpenSDA interface also provides a USB to serial bridge. Drivers for the OpenSDA interface are provided in the P&E Micro OpenSDA Tower Toolkit. These drivers and more utilities can be found online at www.pemicro.com/opensda.

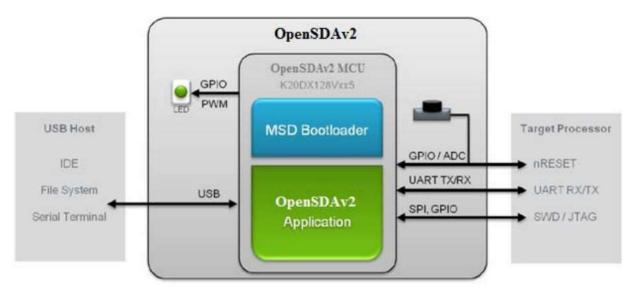


Figure 3. OpenSDA high-level block diagram

3.2.1. **Debug interface**

Signals with SPI and GPIO capability are used to connect directly to the SWD of the KV31. These signals are also brought out to a standard 10-pin (0.05") Cortex debug connector (J9). It is possible to isolate the KV31 MCU from the OpenSDA circuit and use J9 to connect to an off-board MCU. To accomplish this, cut the trace on the bottom side of the PCB that connects J11 pin 2 to the J9 pin 4. This disconnects the SWD_CLK pin to the KV31 so that it does not interfere with the communications to an off-board MCU connected to J11.

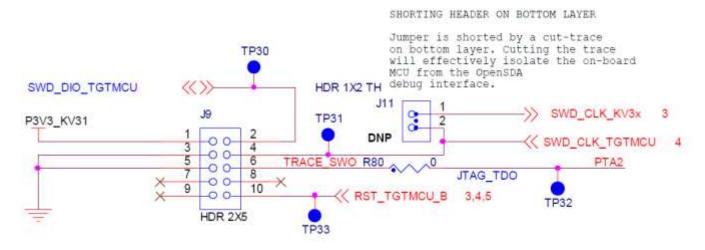


Figure 4. SWD debug connector

J9 is populated by default. A mating cable, such as a Samtec FFSD IDC cable, can then be used to connect from the OpenSDA of the FRDM-KV31F to an off-board SWD connector.

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3.2.2. Virtual serial port

A serial port connection is available between the OpenSDA MCU and pins PTA1 and PTA2 of the KV31 MCU.

4. Microcontroller

The FRDM-KV31F features the MKV31F512VLL12 MCU. The KV31 MCU family is a highly scalable member of the Kinetis V series and provides a high-performance, cost-competitive motor control solution. Built on the ARM Cortex-M4 core running at 120 MHz, combined with floating point and DSP capability, this is implemented in the 100-pin LQFP package. The following table describes some of the features of the MKV31F512VLL12 MCU.

Table 2. Features of MKV31F512VLL12

Feature	Description
Performance	120 MHz ARM Cortex-M4 core with DSP instructions delivering 1.25 Dhrystone MIPS per MHz.
	Dual 16-bit ADCs sampling at up to 1.2 MS/s in 12-bit mode.
	20 channels of highly flexible motor control timers (PWMs) across 4 independent time bases.
	Large RAM block enabling local execution of fast control loops at full clock speed.
Memories and memory interfaces	512 KB of embedded flash and 96 KB of RAM.
	FlexBus external bus interface.
	Serial programming interface (EzPort).
	Preprogrammed Kinetis flashloader for one-time, in-system factory programming.
System peripherals	Flexible low-power modes, multiple wake-up sources.
	16-channel DMA controller.
	Independent external and software watchdog monitor.
Clocks	One crystal oscillator with two ranges: 32-40 kHz or 3-32 MHz.
	Three internal oscillators: 32 kHz, 4 MHz, and 48 MHz.
	Multipurpose clock generator with PLL and FLL.
Security and integrity modules	Hardware CRC module.
	128-bit unique identification (ID) number per chip.
	Hardware random-number generator.
	Flash access control to protect proprietary software.
Analog modules	Two 16-bit SAR ADCs (1.2 MS/s in 12-bit mode).
	Two 12-bit DACs.

	 Two analog comparators (CMP) with a 6-bit DAC. Accurate internal voltage reference/
Timers	 Two 8-ch motor-control/general purpose/PWM timers. Two 2-ch motor-control/general purpose timers with quadrature decoder functionality.
	 Periodic interrupt timers. 16-bit low-power timer. Programmable delay block.
Communication interfaces	 Two SPI modules. Three UART modules and one low-power UART. Two I2C: Support for up to 1 Mbit/s operation

5. Clock source

An 8 MHz external crystal is used for the external clock source of the KV31 MCU.

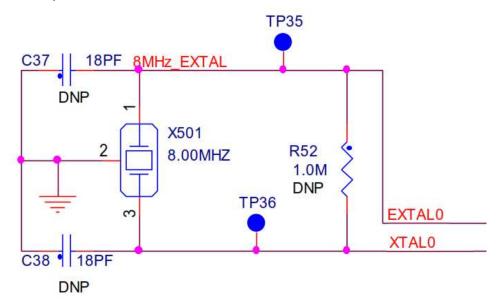


Figure 5. Clock source

6. Accelerometer and magnetometer

An FXOS8700CQ low-power, 6-axis Xtrinsic sensor is interfaced through an I2C bus and two GPIO signals, as shown in the following table. By default, the I2C address is 0x1D (SA0 pull-up and SA1 pull-down).

 Table 3.
 Accelerometer and magnetometer signals connections

FXOS8700CQ	KV31 Connection
SCL	PTD2/LLWU_P13/SPI0_SOUT/UART2_RX/FTM3_CH2/FBA_AD4/LPUART0_RX/I2C0_SCL
SDA	PTD3/SPI0_SIN/UART2_TX/FTM3_CH3/FBA_AD3/LPUART0_TX/I2C0_SDA
NT1	PTD0/LLWU_P12/SPI0_PCS0/UART2_RTS/FTM3_CH0/FBA_ALE/FBA_CS1/FBA_TS/LPUART0_RTS
INT2	PTC18/LPUART0_RTS/FBA_TBST/FBA_CS2/FBA_BE15_8_BLS23_16

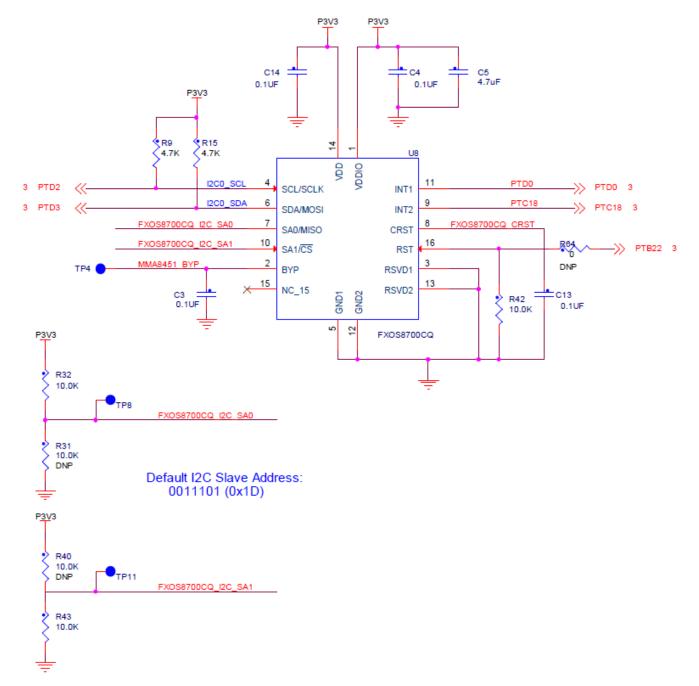


Figure 6. Accelerometer and magnetometer

7. Thermistor

There is a thermistors RT1 provided on the platform that can be used as single-ended or differential analog inputs to the KV31 MCU.

In addition to the thermistor, there is a resistor between the thermistor and 3.3 V system power supply and another resistor between the thermistor and ground. The thermistor is a 10 K ohm part, but the

associated divider chain uses different resistors. This makes the voltage across the thermistor larger or smaller, and provides the ability to try the different gain settings on the analog channels. The thermistor circuit is designed to provide useable differential inputs over the temperature range of 90° C to -20° C.

In addition to the thermistor voltage divider chain, the thermistor has a 0.1 uF capacitor in parallel.

Each analog input to the KV31 has a 100-ohm series resistor and a 2200 pF capacitor as a low-pass filter. This helps protect the KV31 from electrostatic discharge, and lowers the impedance of the analog signal so that it can be sampled with less noise.

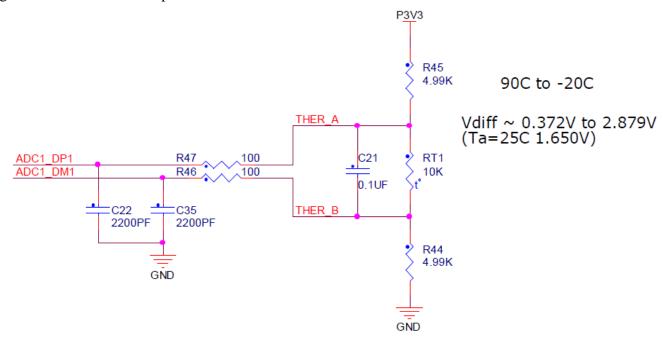


Figure 7. Thermistor

8. RGB LED

RGB LED is connected through GPIO, and signal connections are shown in the following table.

RGB LED	SB LED KV31	
RED	PTD1/ADC0_SE5B/SPI0_SCK/UART2_CTS/FTM3_CH1/FBA_CS0/LPUART0_CTS	
BLUE	PTE25/ADC0_SE18/FTM0_CH1/I2C0_SDA/EWM_IN	
GREEN	PTD7/UART0_TX/FTM0_CH7/FTM0_FLT1/SPI1_SIN	

Table 4. **LED Signal connection**

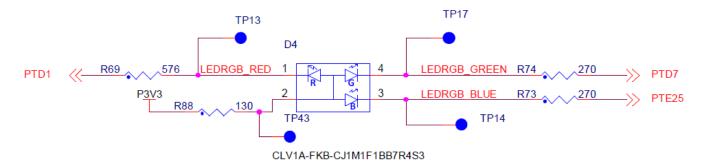


Figure 8. RGB LED

9. Serial Port

The primary serial port interface signals are PTB16 UART0_RX and PTB17 UART0_TX. These signals are connected to the OpenSDA circuit.

10. Reset

The reset signal on the K20 is connected externally to a push button, SW1, and also to the OpenSDAv2 circuit. The reset button can be used to force an external reset event on the target MCU. The reset button can also be used to force the OpenSDA circuit into bootloader mode. For more details, see Section 3.2, "Serial and debug adapter (OpenSDAv2)".

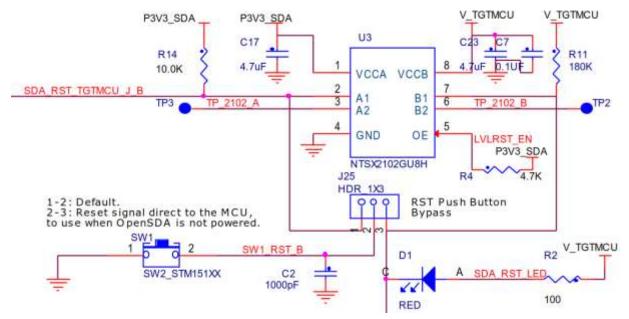


Figure 9. Reset circuit

11. Push Button Switches

Two push buttons, SW2 and SW3, are available on the FRDM-KV31F board, where SW2 is connected to

PTC6, and SW3 is connected to PTA4. Besides the general purpose input/output functions, SW2 and SW3 can be a low-power wake up signal. Also, only SW3 can be a non-maskable interrupt.

Switch	GPIO Function		
SW2	PTA4/LLWU_P3/FTM0_CH1/FTM0_FLT3/NMI/EZP_CS		
SW3	PTE4/LLWU_P2/SPI1_PCS0/LPUART0_TX		

Table 5. Push button GPIO function

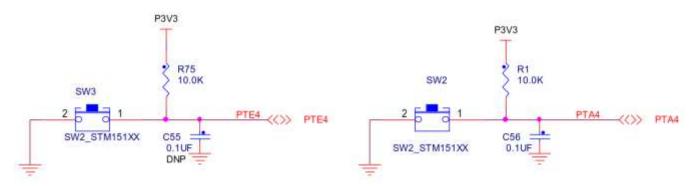


Figure 10. Push button switches

12. Input/output connectors

The MKV31F512VLL12 microcontroller is packaged in a 100-pin LQFP. Some pins are utilized in onboard circuitry, but some are directly connected to one of the four I/O headers.

The pins on the KV31 microcontroller are named for their general purpose input/output port pin function. For example, the first pin on Port A is referred as PTA1. The name assigned to the I/O connector pin is same as of the KV31 pin connected to it, if applicable.

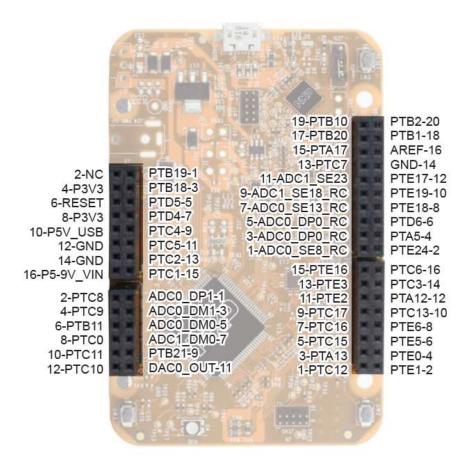


Figure 11. FRDM-KV31F I/O header pinout

13. Arduino Compatibility

The I/O headers on the FRDM-KV31F platform are arranged to enable compatibility with peripheral boards (known as shields) that connect to Arduino and Arduino-compatible microcontroller boards. The outer rows of pins (even numbered pins) on the headers, share the same mechanical spacing and placement with the I/O headers on the Arduino Revision 3 (R3) standard.

14. References

The following references are available on <u>www.nxp.com</u>:

- FRDMKV31FQRC, FRDM-KV31F Quick Reference Card
- FRDM-KV31F Schematic
- FRDM-KV31 Design Package

15. Revision History

Table 6. Revision history

Revision number	Date	Substantive changes
0	02/2016	Initial release

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