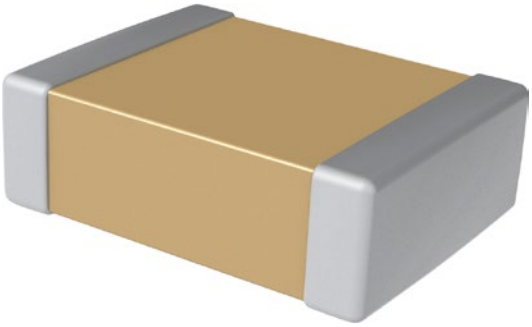
Multilayer Capacitors, SMD

Multilayer Ceramic Capacitors, 0603, X5R



SPECIFICATION:

Construction form	0603
Ceramic type	X5R
Dimensions L x H x W	1.6 x 0.6 x 0.6 mm
Temperature range	-55...+85 °C
Height	0.6 mm
Length	1.6 mm
Width	0.6 mm

PRODUCT RANGE:

Art. Nr.	Capacitance	Rated voltage	Capacitance tolerance
RND 150-0603X105K063NT	1.0 µF	6.3 VDC	±10%
RND 150-0603X105K100NT	1.0 µF	10 VDC	±10%
RND 150-0603X105K160NT	1.0 µF	16 VDC	±10%
RND 150-0603X105K250NT	1.0 µF	25 VDC	±10%
RND 150-0603X105M063NT	1.0 µF	6.3 VDC	±20%
RND 150-0603X106M063NT	10 µF	6.3 VDC	±20%
RND 150-0603X224K160NT	220 nF	16 VDC	±10%
RND 150-0603X224K250NT	220 nF	25 VDC	±10%
RND 150-0603X225K063NT	2.2 µF	6.3 VDC	±10%
RND 150-0603X225K100NT	2.2 µF	10 VDC	±10%
RND 150-0603X334K100NT	330 nF	10 VDC	±10%
RND 150-0603X334K160NT	330 nF	16 VDC	±10%
RND 150-0603X474K100NT	470 nF	10 VDC	±10%
RND 150-0603X474K160NT	470 nF	16 VDC	±10%
RND 150-0603X475K063NT	4.7 µF	6.3 VDC	±10%
RND 150-0603X475K100NT	4.7 µF	10 VDC	±10%
RND 150-0603X684K100NT	680 nF	10 VDC	±10%
RND 150-0603X684K160NT	680 nF	16 VDC	±10%

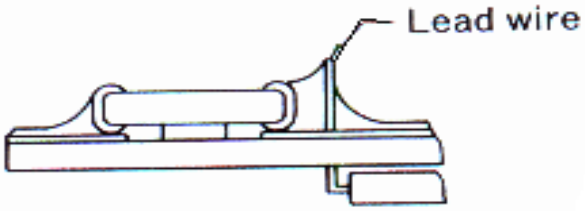
PCB design

Chip components are susceptible to board stress since the component itself is mounted directly on the board. They are also sensitive to mechanical and thermal stress when solder, which may cause chip cracked.
Please take solder form and component layout into consideration to eliminate stress.

Pattern form

(1) Placing of chip components and component.

incorrect



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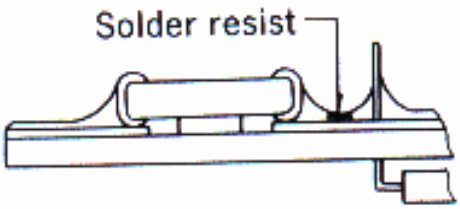
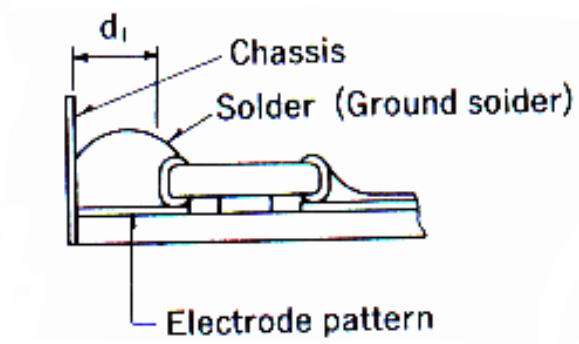


(2) Placing close to chassis.

incorrect



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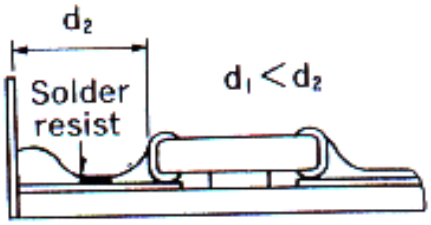
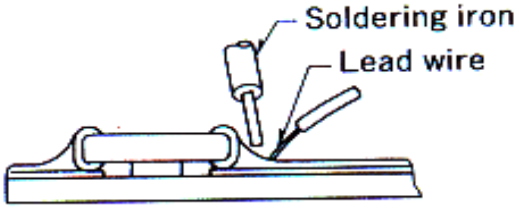


(3) Placing leaded components after chip component.

incorrect



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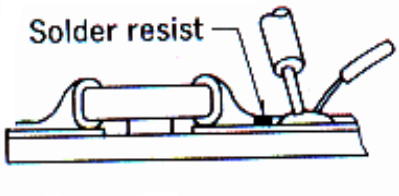
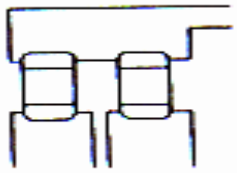


(4) Lateral mounting

incorrect



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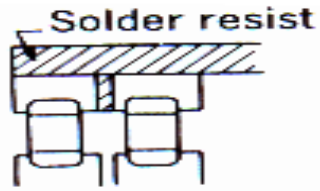
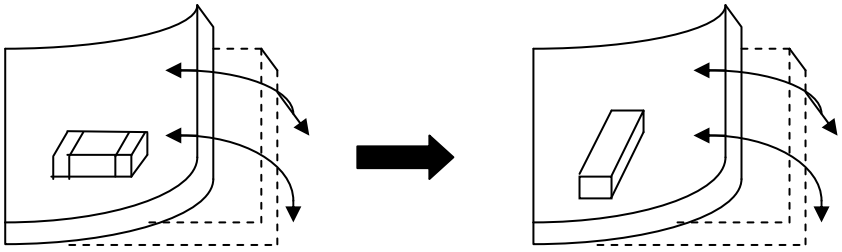


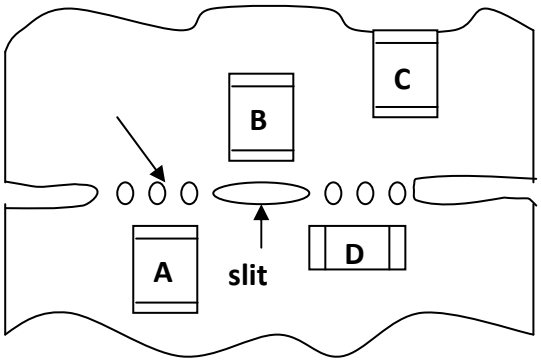
Component direction

To design a mounting position that minimizes the stress imposed on the chip during flexing or bending of the board.

(1) put the component lateral to the direction in which stress acts.



(2) Component layout close to board separation point.
Susceptibility to stress in the order: A＞C＞B＝D



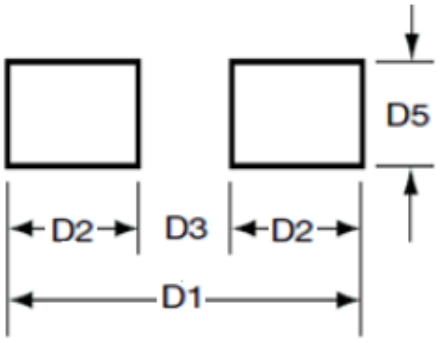
12.3. Land Pattern

When capacitors are mounted on P.C. board, the amount of solder directly affect the performance of capacitors. Therefore, the following items should be carefully considered in the design of solder land pattern.

(1) The greater the amount of solder, the higher the stress on the chip capacitors, and lead to cracking and breaking likely. It is necessary the appropriate size and configuration of the solder pads should be designed to have proper amount of solder on the termination.

(2) When two or more capacitors are soldered together onto the same land or pad, the pad must be designed so that each capacitor's soldering point is separated by solder-resist.

The following diagram and table for recommended pad dimensions.



Dimensions in millimeters

Type	0201	0402	0603	0805	1206	1210	1808	1812	1825	2220	2225
D1	0.65	1.50	2.30	2.80	4.00	4.00	5.40	5.30	5.30	7.00	7.00
D2	0.21	0.50	0.80	0.90	0.90	0.90	1.05	0.90	0.90	1.35	1.35
D3	0.23	0.50	0.70	1.00	2.20	2.20	3.30	3.50	3.50	4.30	4.30
D5	0.30	0.50	0.80	1.30	1.60	2.50	2.30	3.80	6.50	5.00	6.50

Unit: mm